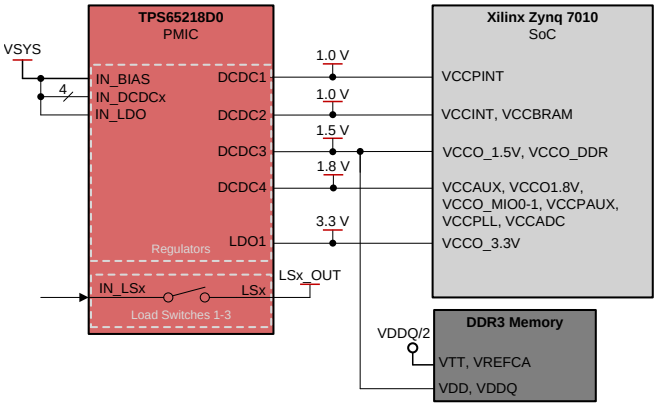
Test Report: TIDA-00478

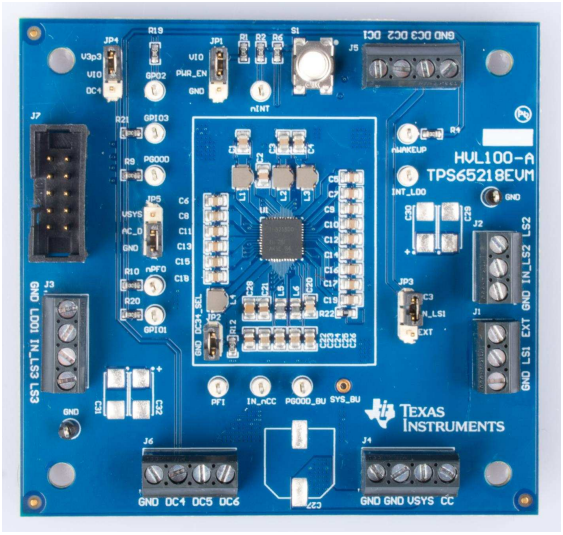
Powering the Xilinx® Zynq® 7000 Series of FPGAs With Power Management IC Reference Design

Description

This TPS65218D0-based reference design is a compact, integrated power solution for Xilinx® Zynq® 7010 SoC/FPGAs (out of the Zynq® 7000 series family of products). This design showcases TPS65218D0 as an all-in-one PMIC used to supply the five rails needed for powering the Zynq® 7010 SoC/FPGAs. The total board area needed for TPS65218D0, including passive components, to supply the five power rails to the Zynq® 7010 is just 1.594 in^2.

The TPS65218D0 has the flexibility to support either DDR3L or DDR3 memory. This power management IC can be run from a single 5-V supply or from a single cell Li-Ion battery. This design is ensured to operate across an industrial temperature range (-40°C to +105°C).





1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	VOLTAGE (V)	CURRENT (A)	TPS65218D0 PIN OR RAIL NAME
V_{IN}	3.3 – 5	—	IN_BIAS, IN_DCDCx, IN_LDO1
VCCPINT	1.0	1.041	DCDC1
VCCINT	1.0	1.521	DCDC2
VCCBRAM	1.0	0.042	
VCCO_DDR	1.5	0.131	DCDC3
VCCO_1.5V	1.5	0.284	
VCCAUX	1.8	0.518	DCDC4
VCCPAUX	1.8	0.023	
VCCPLL	1.8	0.01	
VCCADC	1.8	0.03	
VCCO_1.8V	1.8	Scalable	
VCCO_MIO0/1	1.8	Scalable	
VCCO_3.3V	3.3	Scalable	LDO1

1.2 Required Equipment

- TPS65218EVM-100 evaluation module
- IPG-UI software
- TPS65218D0 sample IC
- BOOSTXL-TPS65218 socketed EVM (optional)

1.3 Design Considerations

The TPS65218D0 operates over a range of input voltages from 2.7 V to 5.5 V, such that the system can be powered from a 5-V, line-powered supply or from a nominal 3.6-V battery supply. Figure 1 shows the block diagram of the system wired for a 5-V supply, which allows LDO1 of the TPS65218D0 to generate 3.6 V for the VCCO_3.3V rail of the Zynq device. The sequence order of each rail is circled in the diagram.

Figure 1. 5-V Supply Diagram

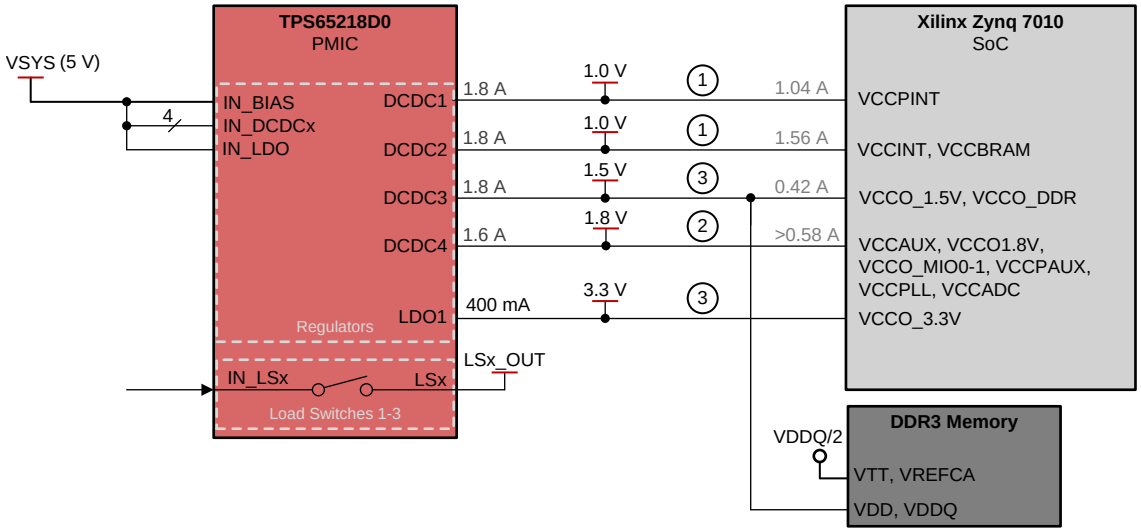


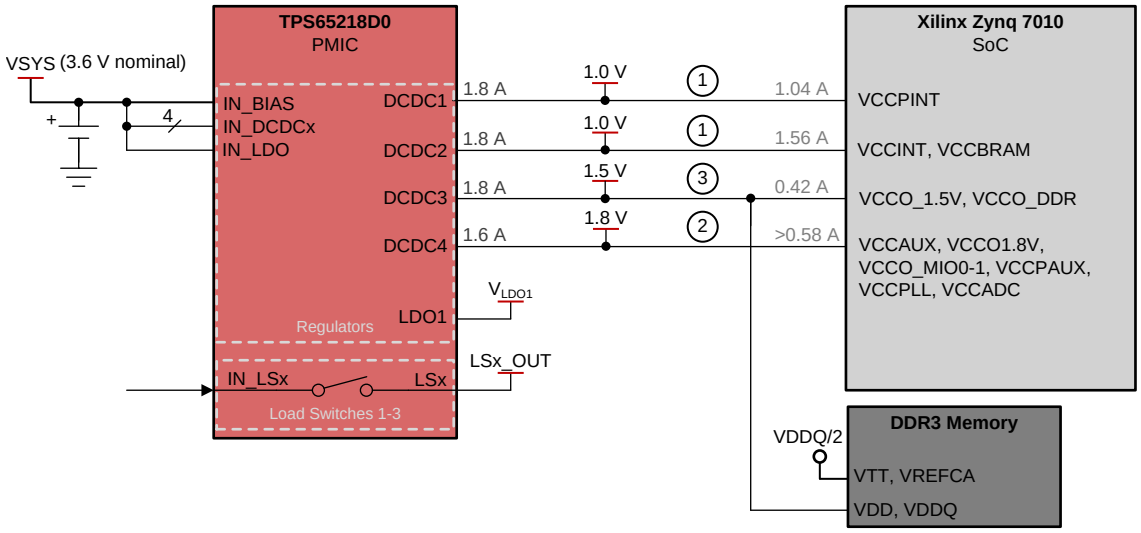
Table 2 lists the voltage settings required for the TPS65218D0 to power the Xilinx Zynq 7010 properly.

Table 2. Voltage Settings

Xilinx Rail	TPS65218D0 Regulator	Voltage (V)	Register Address (Name)	Register Value
VCCPINT	DCDC1	1.0	0x16 (DCDC1)	0x8F
VCCINT, VCCBRAM	DCDC2	1.0	0x17 (DCDC2)	0x8F
VCCO_DDR, VCCO_1.5V	DCDC3	1.5	0x18 (DCDC3)	0x98
VCCAUX, VCCPAUX, VCCO_1.8V	DCDC4	1.8	0x19 (DCDC4)	0x94
VCCO_3.3V	LDO1	3.3	0x1B (LDO1)	0x3D

Figure 2 shows the block diagram of the system wired for a nominal 3.6-V battery supply. The battery voltage can drop below 3.3 V, and as a result, LDO1 should not be used to generate 3.3 V for the VCCO_3.3V rail of the Zynq device. The sequence order of each rail is circled in the diagram.

Figure 2. 3.6-V Battery Supply Diagram



1.3.1 Xilinx® Zynq® 7010 Recommended Power Up/Down Sequencing

For reference, the sequencing requirements from the Xilinx Znyq 7010 data sheet are described in the following sections. The PS (processor system) domain is for the applications processor in the Xilinx Zynq SoC and the PL (programmable logic) domain is for the FPGA.

1.3.1.1 PS Domain Power-On/Off Sequencing

The recommended power-on sequence is VCCPINT, VCCPAUX, and VCCPLL together, then the PS VCCO supplies (VCCO_MIO0, VCCO_MIO1, and VCCO_DDR) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCPAUX, VCCPLL, and the PS VCCO supplies (VCCO_MIO0, VCCO_MIO1, and VCCO_DDR) have the same recommended voltages, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering VCCPLL with the same supply as VCCPAUX, with an optional ferrite bead filter.

For VCCO_MIO0 and VCCO_MIO1 voltages of 3.3 V:

- The voltage difference between VCCO_MIO0 /VCCO_MIO1 and VCCPAUX must not exceed 2.625 V for longer than TVCCO2VCCAUX for each power-on/off cycle to maintain device reliability levels.
- The TVCCO2VCCAUX time can be allocated in any percentage between the power-on and power-off ramps.

1.3.1.2 PL Domain Power-On/Off Sequencing

The recommended power-on sequence for the PL is VCCINT, VCCBRAM, VCCAUX, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT and VCCBRAM have the same recommended voltages then both can be powered by the same supply and ramped simultaneously.

The recommended power-on sequence for the PL is VCCINT, VCCBRAM, VCCAUX, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT and VCCBRAM have the same recommended voltages then both can be powered by the same supply and ramped simultaneously.

If VCCAUX and VCCO have the same recommended voltages then both can be powered by the same supply and ramped simultaneously.

For VCCO voltages of 3.3 V in HR I/O banks and configuration bank 0:

- The voltage difference between VCCO and VCCAUX must not exceed 2.625 V for longer than TVCCO2VCCAUX for each power-on/off cycle to maintain device reliability levels.
- The TVCCO2VCCAUX time can be allocated in any percentage between the power-on and power-off ramps.

1.3.2 TPS65218D0 Wake-up and Power Sequencing

The TPS65218D0 has a pre-defined power-up / power-down sequence which may need to be adjusted for each different SoCs, processors, or FPGAs. Re-programming the nonvolatile EEPROM memory of the TPS65218D0 device with I^2C control allows the user to change the sequence order and timing to match the target SoC, processor, or FPGA.

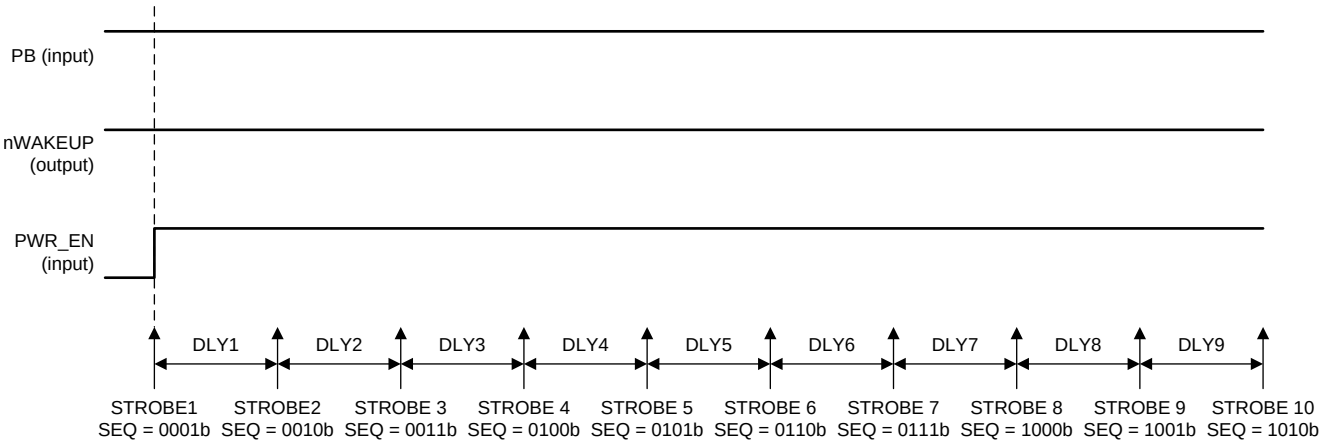
The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled. A rail can be assigned to only one strobe, but multiple rails can be assigned to the same strobe. The delay times in-between strobes are selectable between 2 ms and 5 ms.

1.3.2.1 General Power-Up Sequencing

When the power-up sequence initiates, STROBE1 occurs, and any rail assigned to this strobe is enabled.

After a delay time of DLY1, STROBE2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes occur and all DLYx times execute. Strobe assignments and delay times are defined in the SEQx registers, and are changed under I^2C control. Figure 3 shows a timing diagram detailing the power sequence when PWN_EN is the power-up event leaving the SUSPEND state. For further information on power up/down sequence, please consult the TPS65218D0 data sheet. Power-down sequencing follows the reverse order of power-up sequencing.

Figure 3. TPS65218D0 Power-Up from SUSPEND State (PWR_EN Set High)



1.3.2.2 TPS65218D0 Adjusted Sequencing for Xilinx® Zynq® 7010

Table 3 lists the strobe assignments required for the TPS65218D0 to power the Xilinx Zynq 7010 properly. The delay (DLY1-9) between each strobe can also be adjusted in registers 0x20 (SEQ1) and 0x21 (SEQ2, bit 0) and multiplied by a factor of 1 or 10 (SEQ2, bit 7). Each bit in SEQ1 and bit 0 of SEQ2 can be set to 0b for a delay of 2 ms or set to 1b for a delay of 5 ms. Bit 7 of SEQ2 can be set to 0b for a factor of 1x or set to 1b for a factor of 10x. For this design, all delays will be kept at the defaults of 2 ms with a delay factor of 1x. As a result, the data in both registers, 0x20 and 0x21, will be 0x00.

Table 3. Strobe Assignments

Xilinx Rail	TPS65218D0 Regulator	Strobe #	Register Address (Name)	Register Value
VCCPINT	DCDC1	3	0x22 (SEQ3)	0x33
VCCINT, VCCBRAM	DCDC2	3		
VCCO_DDR, VCCO_1.5V	DCDC3	7	0x23 (SEQ4)	0x57
VCCAUX, VCCPAUX, VCCO_1.8V	DCDC4	5		
VCCO_3.3V	LDO1	7	0x25 (SEQ6)	0xA7

2 Testing and Results

2.1 Efficiency Graphs

Figure 4 shows the efficiency curve for DCDC1, set to output a voltage of 1.0 V for the VCCPINT rail.

Figure 5 shows the efficiency curve for DCDC2, set to output a voltage of 1.0 V for the VCCINT and VCCBRAM rails.

Figure 4. DCDC1 Efficiency vs Load Current, T_A = 25 °C

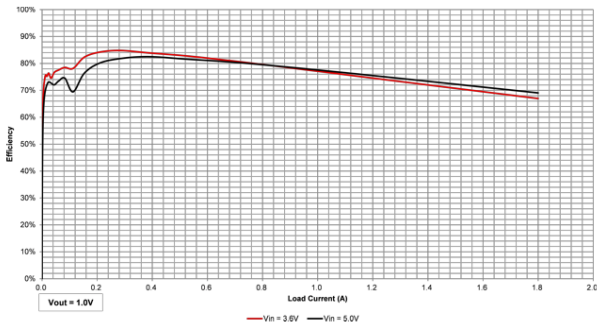


Figure 5. DCDC2 Efficiency vs Load Current, T_A = 25 °C

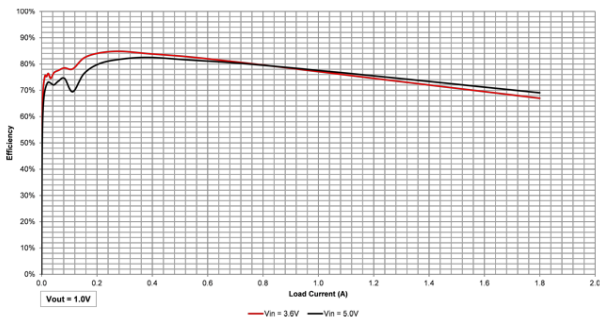


Figure 6 shows the efficiency curve for DCDC3, set to output a voltage of 1.5 V for the VCCO_DDR (DDR Memory) and VCCO_1.5V rails.

Figure 7 shows the efficiency curve for DCDC4, set to output a voltage of 1.8 V for the VCCAUX, VCCO_1.8V, VCCPAUX, VCCPLL, VCCO_MIO0/1, and VCCADC rails.

Figure 6. DCDC3 Efficiency vs Load Current, T_A = 25 °C

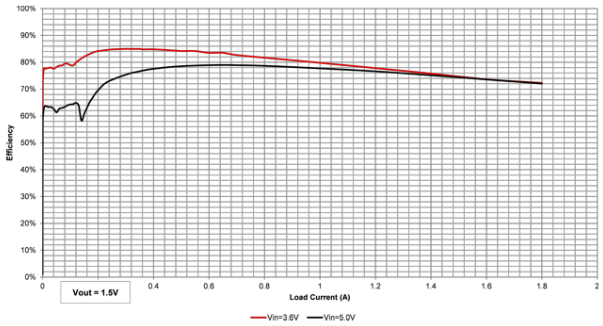
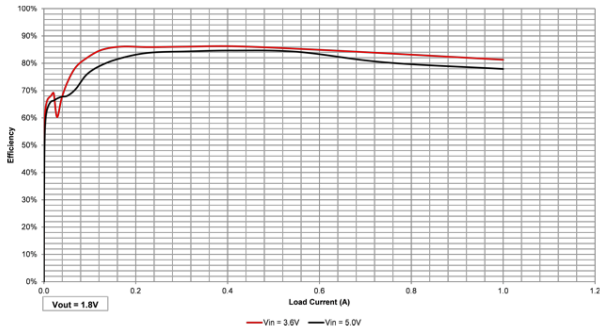


Figure 7. DCDC4 Efficiency vs Load Current, T_A = 25 °C



2.2 Load Regulation

Figure 8 shows the load regulation plot for DCDC1.

Figure 9 shows the load regulation plot for DCDC2.

Figure 8. DCDC1 Load Regulation, T_A = 25 °C

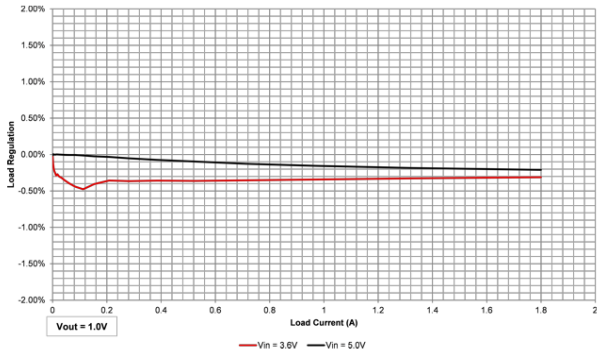


Figure 9. DCDC2 Load Regulation, T_A = 25 °C

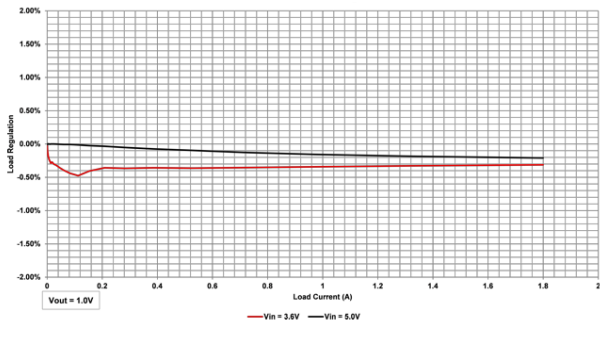


Figure 10 shows the load regulation plot for DCDC3.

Figure 11 shows the load regulation plot for DCDC4.

Figure 10. DCDC3 Load Regulation, T_A = 25 °C

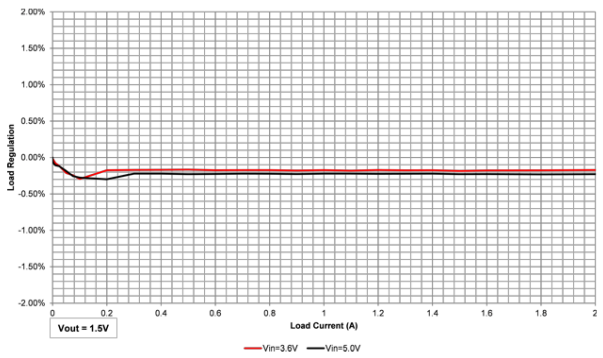
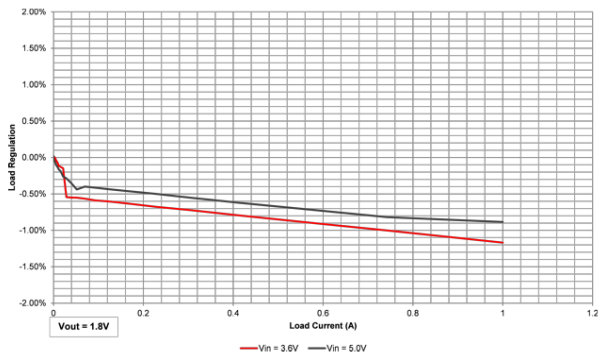


Figure 11. DCDC4 Load Regulation, T_A = 25 °C

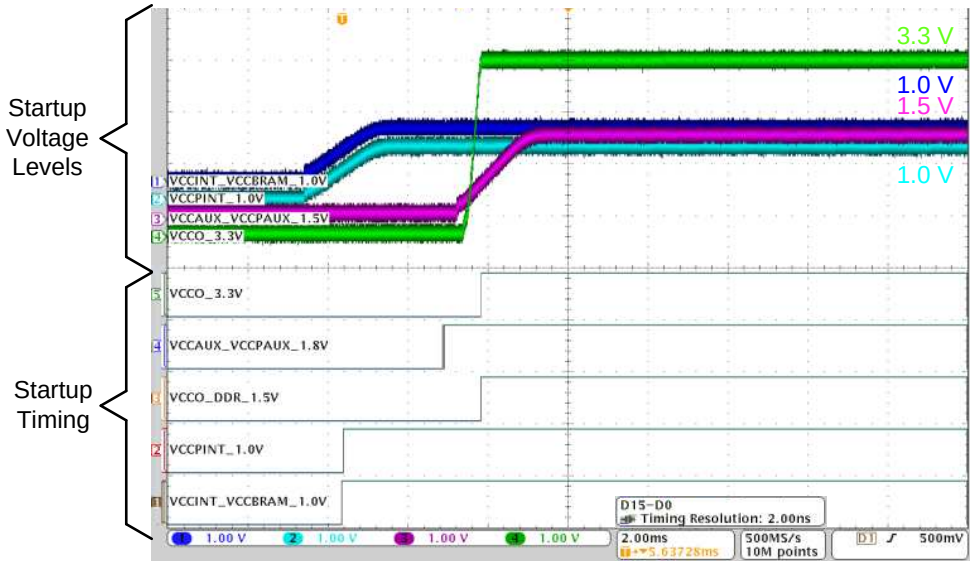


3 Waveforms

3.1 Start-up Sequence

Figure 12 shows the start-up (or power-up) sequence of the TPS65218D0 rails programmed for the Zynq 7010 with no load applied. Timing waveforms for all five rails are shown above; however, due to instrument limitations, only 4 voltage waveforms are displayed (VCCAUX_VCCPAUX_1.8V omitted).

Figure 12. Power-Up Sequence (No Load) Voltage and Timing Waveforms



3.2 Output Voltage Ripple

Figure 13 shows the measured output voltage ripple for DCDC1 at the maximum typical load of the VCCPINT rail.

Figure 14 shows the measured output voltage ripple for DCDC2 at the maximum typical load of the VCCINT and VCCBRAM rails.

Figure 13. DCDC1 Output Voltage Ripple

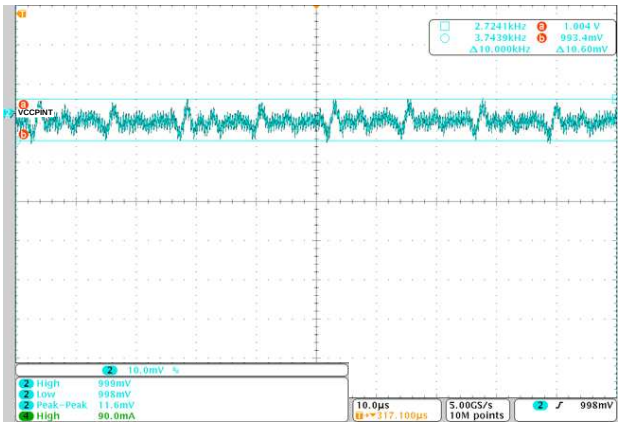


Figure 14. DCDC2 Output Voltage Ripple

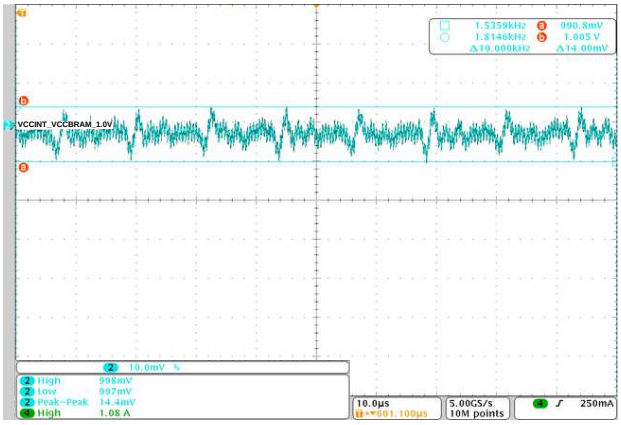


Figure 15 shows the measured output voltage ripple for DCDC3 at the maximum typical load of the VCCO_DDR (DDR Memory) and VCCO_1.5V rails.

Figure 16 shows the measured output voltage ripple for DCDC4 at the maximum typical load of the VCCAUX, VCCO_1.8V, VCCPAUX, VCCPLL, VCCO_MIO0/1, and VCCADC rails.

Figure 15. DCDC3 Output Voltage Ripple

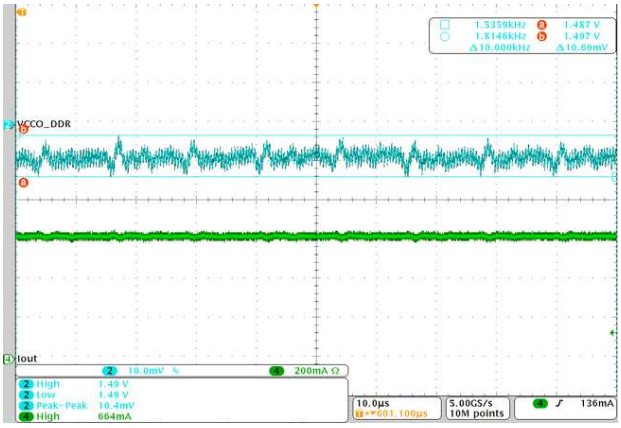
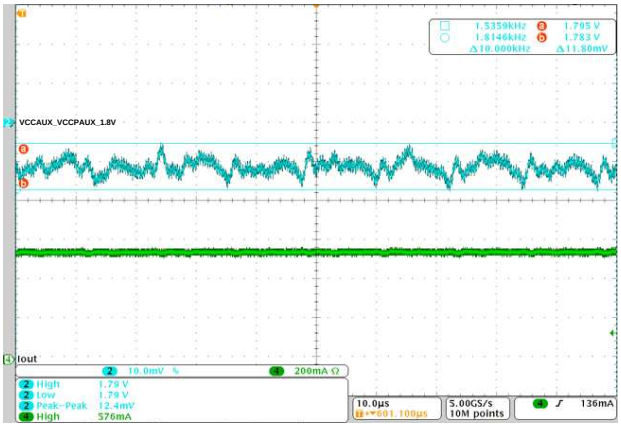


Figure 16. DCDC4 Output Voltage Ripple



3.3 Load Transients

Figure 17 shows the measured load transient response for DCDC1 for a step from 50 mA to 500 mA.

Figure 18 shows the measured load transient response for DCDC2 for a step from 50 mA to 800 mA.

Figure 17. DCDC1 Load Transient Response (50 mA to 500 mA)

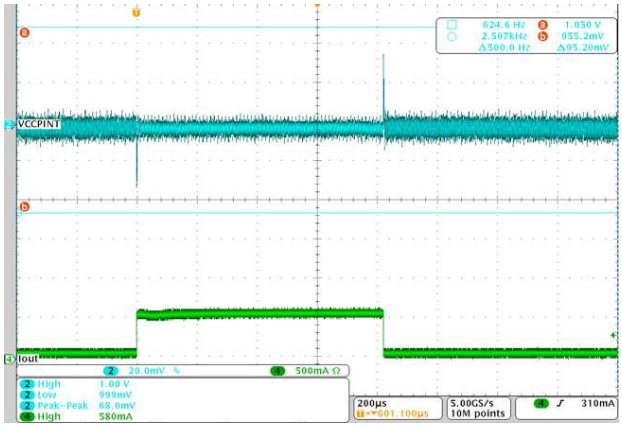


Figure 18. DCDC2 Load Transient Response (50 mA to 800 mA)

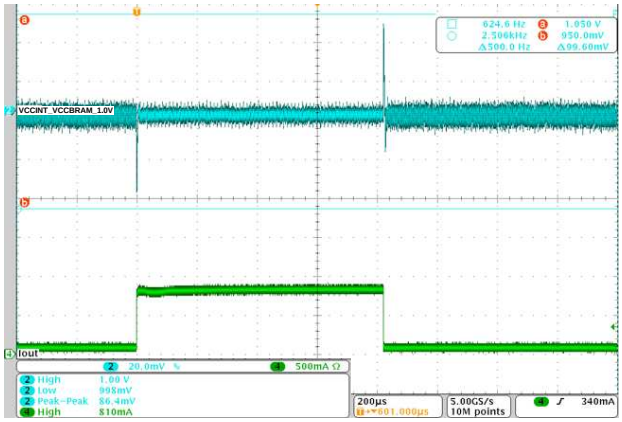


Figure 19 shows the measured load transient response for DCDC3 for a step from 50 mA to 624 mA.

Figure 20 shows the measured load transient response for DCDC4 for a step from 50 mA to 300 mA.

Figure 19. DCDC3 Load Transient Response (50 mA to 624 mA)

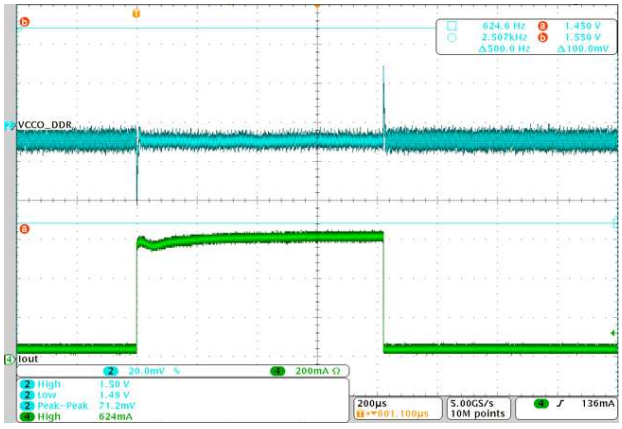
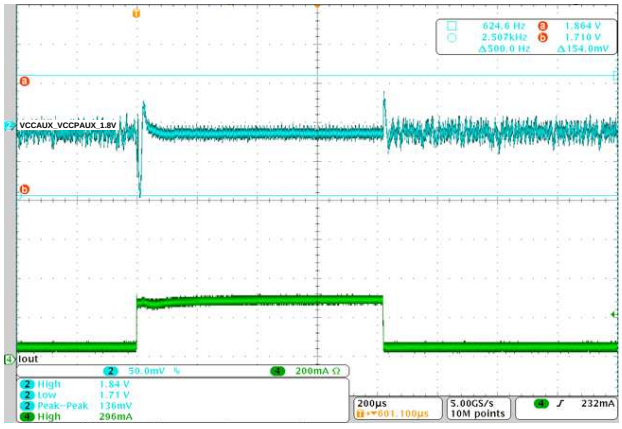


Figure 20. DCDC4 Load Transient Response (50 mA to 300 mA)



4 Next Steps

After reviewing this test report, the next steps towards building a design using the TPS65218D0 PMIC for a Xilinx Zynq SoC are simple. The EEPROM of TPS65218D0 samples can be re-programmed using a socketed BOOSTXL-TPS65218 BoosterPack EVM and an MSP430F5529 LaunchPad. The output voltage settings and sequencing outlined in this document are modified and re-programmed into the TPS65218D0 nonvolatile memory using the IPG-UI software.

The re-programmed TPS65218D0 sample is then soldered down onto the TPS65218EVM-100 board to evaluate the performance and obtain the same results captured in this documentation. If this documentation is sufficient to prove the TPS65218D0 PMIC will work in the final application, the re-programmed TPS65218D0 sample can be soldered directly into a prototype board and evaluated for use in the final application.

Although the scope of this document is limited to powering the Xilinx Zynq 7010 SoC, the TPS65218D0 device can be used to power a wide variety of SoCs, processors, and FPGAs using this same workflow.

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