Test Data
For PMP10571
12/18/2014

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1. Design Specifications

Vin Minimum	**18VDC**
Vin Maximum	**30VDC**
Vout	**+5VDC @ 3A**
Nominal Switching Frequency	**≈ 200KHz**

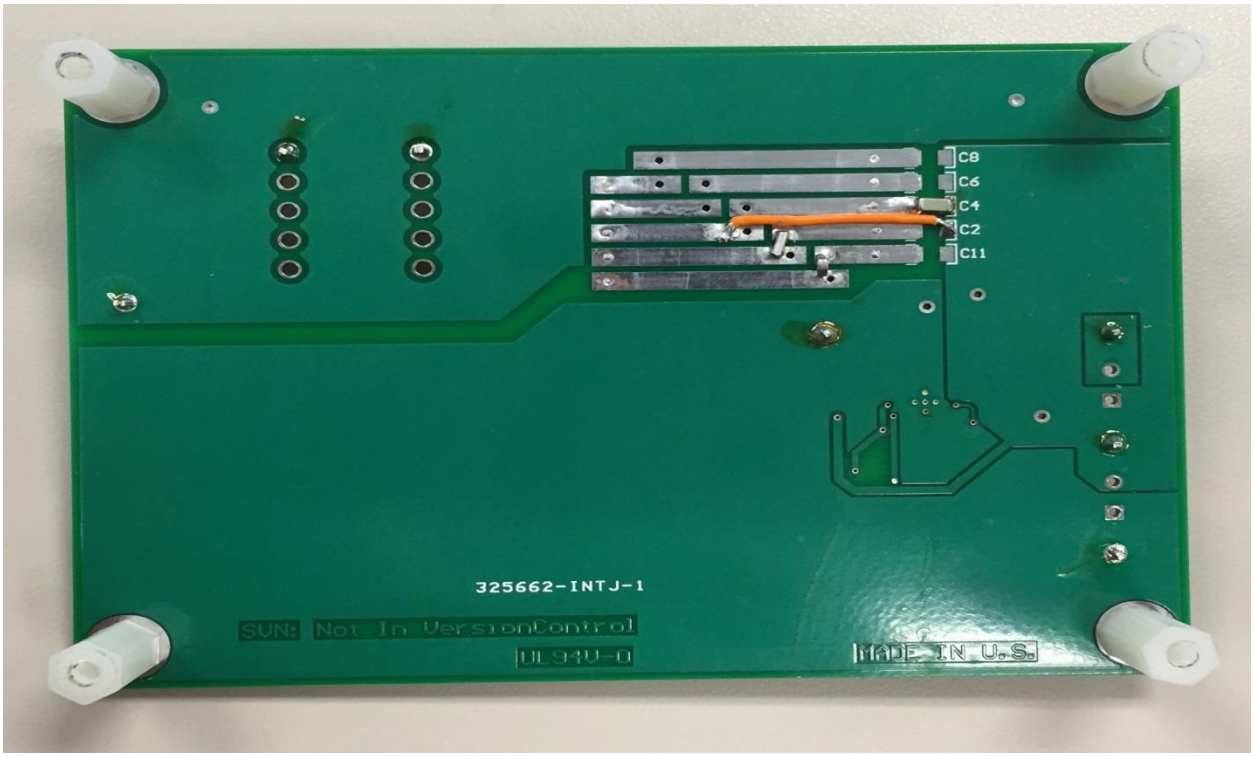
2. Circuit Description

PMP10571 is an Isolated Flyback Converter with the primary configured as a buck-boost inverter, using the LM5160 regulator IC. The design accepts an input voltage of 18Vin to 30Vin and provides one isolated outputs of +5Vout, capable of supplying 3A current. The nominal switching frequency of the design is 200KHz. The board is a 2-layer PCB with 1oz copper on both the top and bottom layer. All tests for oscilloscope waveform captures were performed on Vout at 18Vin and 30Vin. Efficiency testing was performed at 18Vin, 24Vin, and 30Vin. The design uses an easily available off-the-shelf transformer, making it a more cost effective design solution. 3 identical windings in series forms the primary, and other 3 identical windings in parallel forms the secondary winding, making the transformer of a 3:1 turns ratio. The selected transformer is capable of 500V isolation. The board is assembled on PMP10564 breakout board.

3. PMP10571 Board Photos

Board Dimensions: 79mm x 107mm

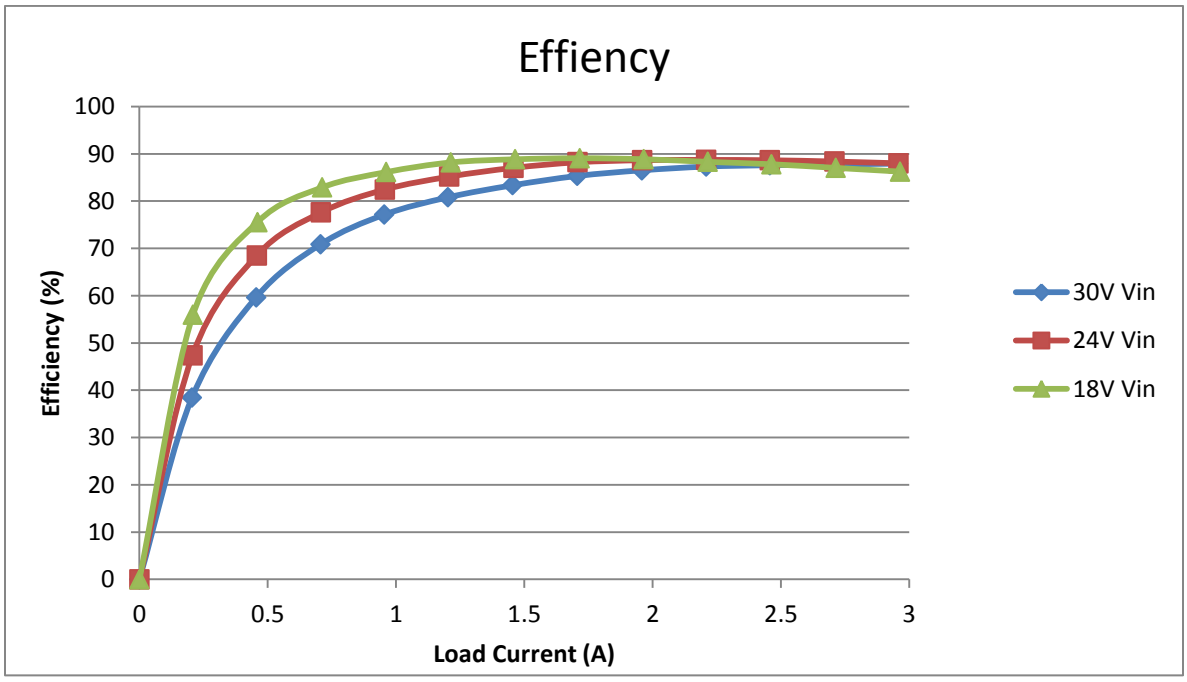
Board Photo (Top)



Board Photo (Bottom)

4. Efficiency

4.1 Efficiency Chart



4.2 Efficiency Data

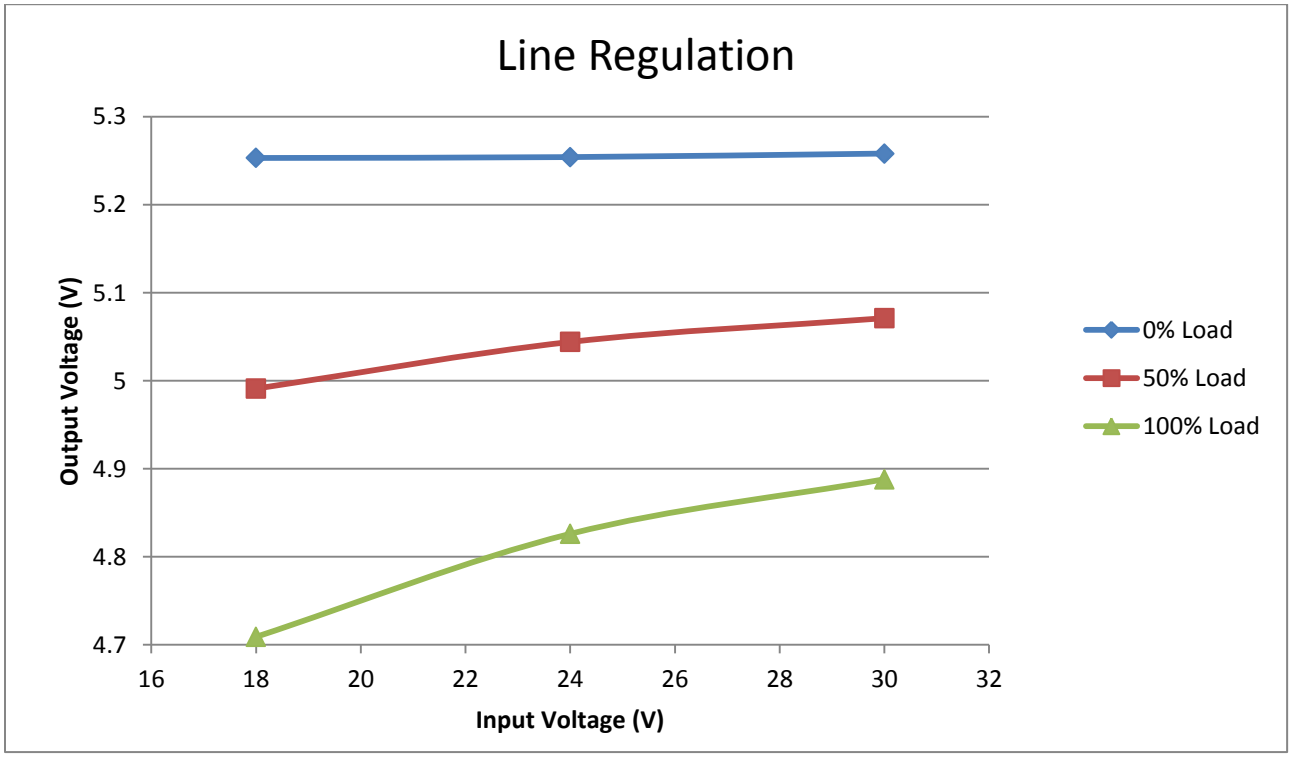
18Vin				
Vin	Iin	Vout	Iout	Eff
18.011	0.053	5.253	0	0
18.011	0.108	5.206	0.209	55.936
18.011	0.174	5.146	0.46	75.534
18.011	0.244	5.116	0.712	82.886
18.011	0.315	5.079	0.962	86.12
18.01	0.385	5.036	1.214	88.172
18.01	0.457	4.991	1.465	88.837
18.01	0.529	4.945	1.716	89.066
18.01	0.602	4.9	1.966	88.852
18.01	0.676	4.853	2.215	88.292
18.01	0.749	4.806	2.464	87.787
18.01	0.824	4.758	2.714	87.015
18.01	0.899	4.709	2.965	86.234

24Vin				
Vin	Iin	Vout	Iout	Eff
24.009	0.054	5.254	0	0
24.008	0.095	5.219	0.207	47.367
24.008	0.144	5.171	0.458	68.505
24.008	0.195	5.131	0.708	77.597
24.008	0.247	5.109	0.957	82.451
24.008	0.3	5.078	1.208	85.169
24.008	0.352	5.044	1.458	87.023
24.008	0.404	5.009	1.708	88.207
24.008	0.458	4.973	1.96	88.645
24.008	0.512	4.936	2.209	88.704
24.008	0.566	4.9	2.458	88.635
24.008	0.621	4.863	2.709	88.362
24.008	0.676	4.826	2.959	87.989

30Vin				
Vin	Iin	Vout	Iout	Eff
30.011	0.061	5.258	0	0
30.011	0.093	5.23	0.205	38.414
30.011	0.132	5.192	0.455	59.634
30.011	0.171	5.15	0.706	70.849
30.011	0.211	5.119	0.954	77.121
30.011	0.253	5.099	1.203	80.789
30.011	0.295	5.071	1.455	83.34
30.011	0.336	5.042	1.706	85.303
30.011	0.378	5.012	1.958	86.507
30.011	0.42	4.981	2.209	87.294
30.011	0.463	4.951	2.458	87.582
30.011	0.506	4.919	2.709	87.752
30.011	0.548	4.888	2.958	87.916

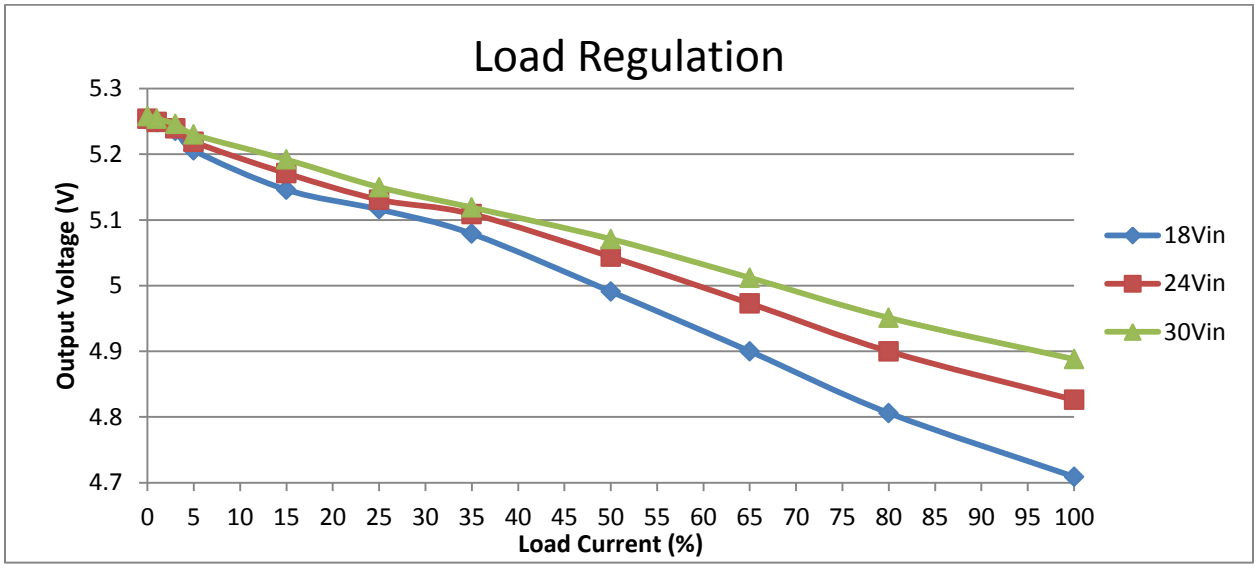
5 Output Voltage Regulation

5.1 Line Regulation



Line Regulation at 0% Load			Line Regulation at 50% Load			Line Regulation at 100% Load		
Vin	Vsec		Vin	Vsec		Vin	Vsec	
18	5.253		18	4.991		18	4.709	
24	5.254		24	5.044		24	4.826	
30	5.258		30	5.071		30	4.888	

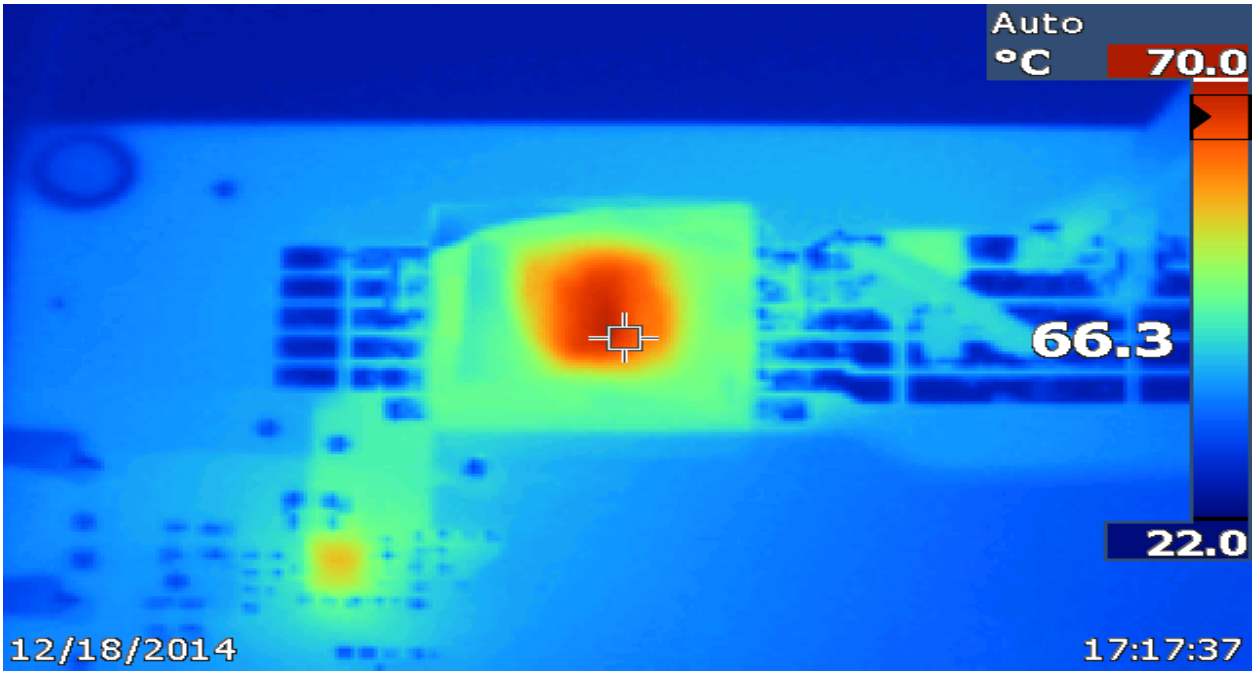
5.2 Load Regulation



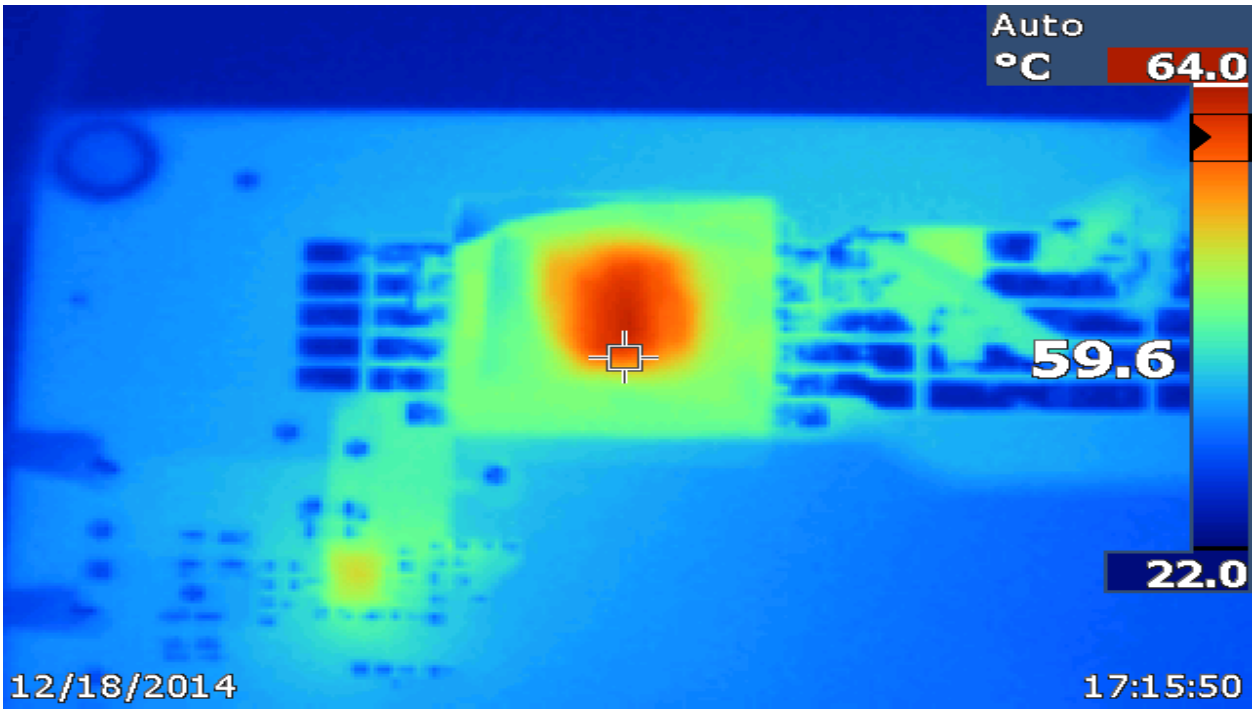
% of Load	18Vin	24Vin	30Vin
0	5.253	5.254	5.258
1	5.2485	5.2492	5.2539
3	5.2356	5.2397	5.2461
5	5.206	5.219	5.23
15	5.146	5.171	5.192
25	5.116	5.131	5.15
35	5.079	5.109	5.119
50	4.991	5.044	5.071
65	4.9	4.973	5.012
80	4.806	4.9	4.951
100	4.709	4.826	4.888

6 Thermal Images

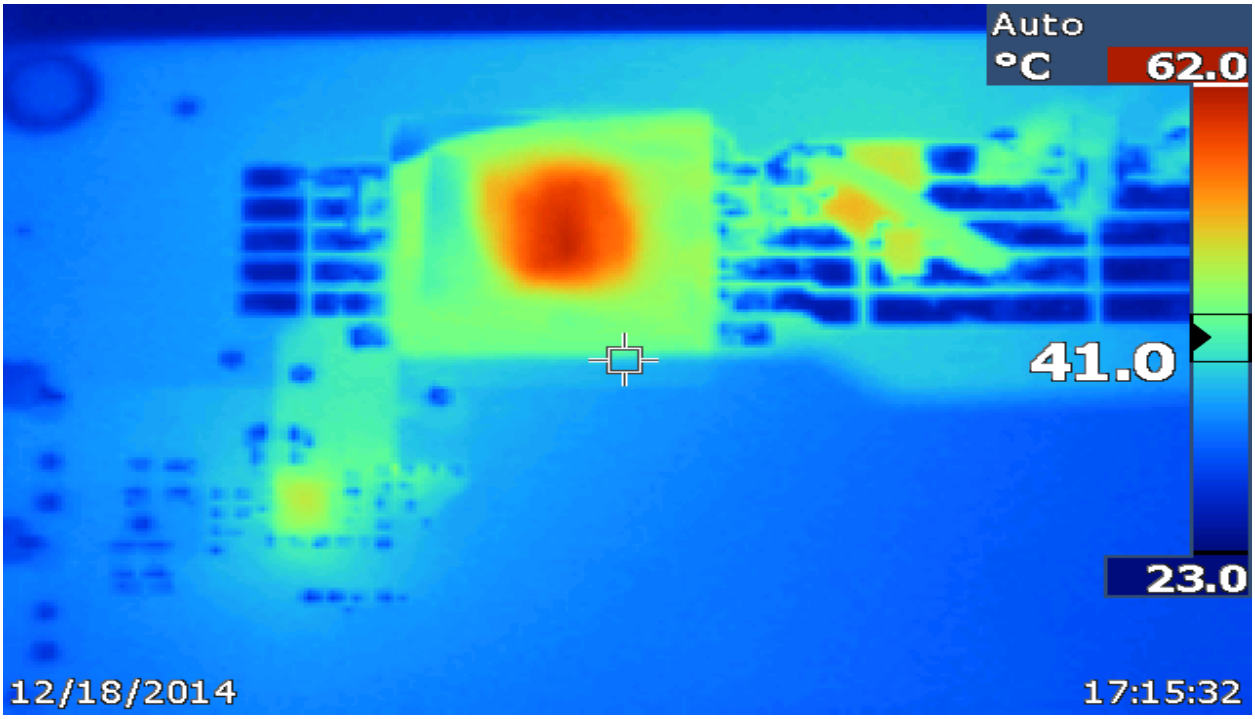
Note: The clamping zener diode is mostly conducting at 30V input, where the voltage spikes on the gate is the highest, creating another heat source. Power dissipation could be improved with a 4-layer board and thicker copper.



IR Thermal Image Taken at Steady State at 18Vin and Output at Full Load (Vout Primary Unloaded)



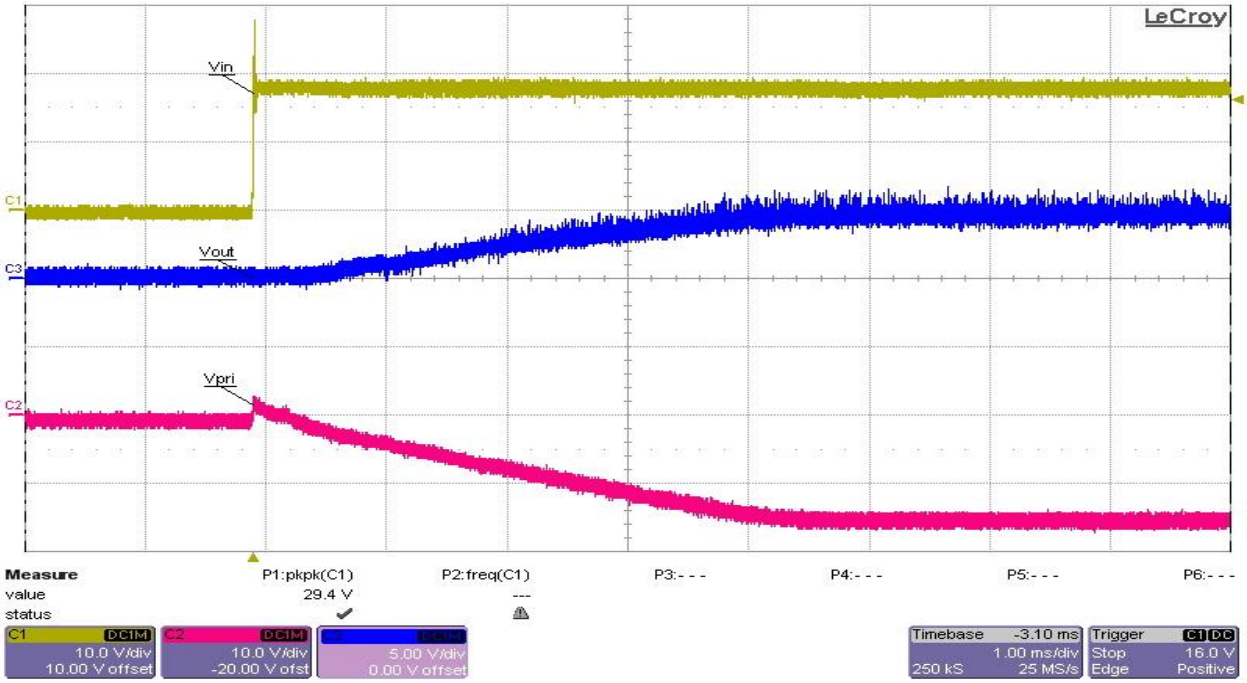
IR Thermal Image Taken at Steady State at 24Vin and Output at Full Load (Vout Primary Unloaded)



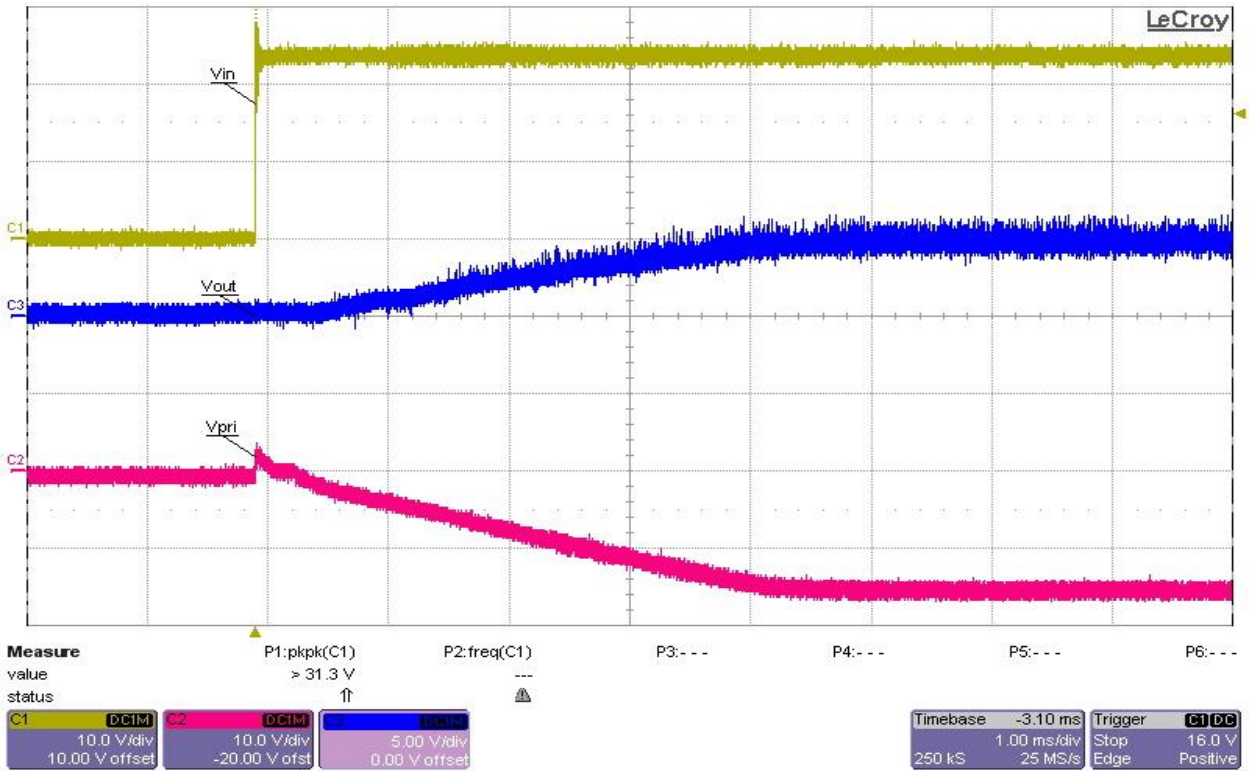
IR Thermal Image Taken at Steady State at 30Vin and Output at Full Load (Vout Primary Unloaded)

7 Waveform

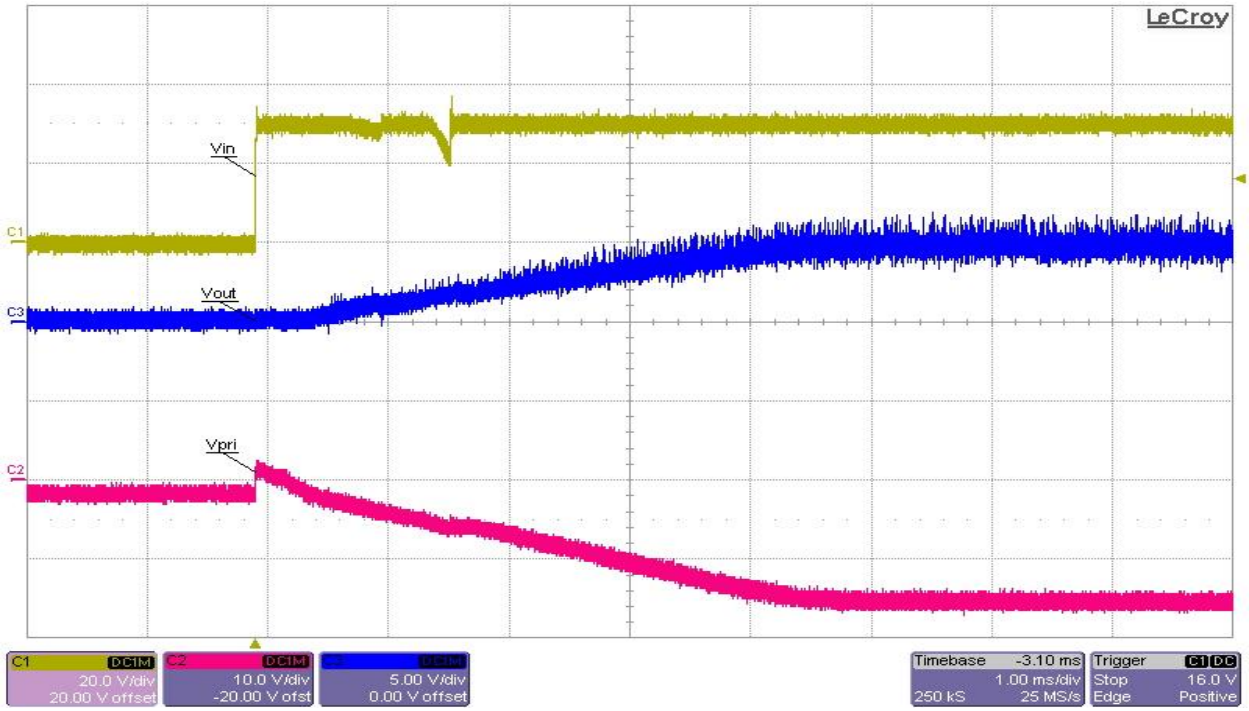
7.1 Start-Up



Startup into Full Load at 18Vin, Ch1 input, Ch2 Vpri, Ch3 Vout.

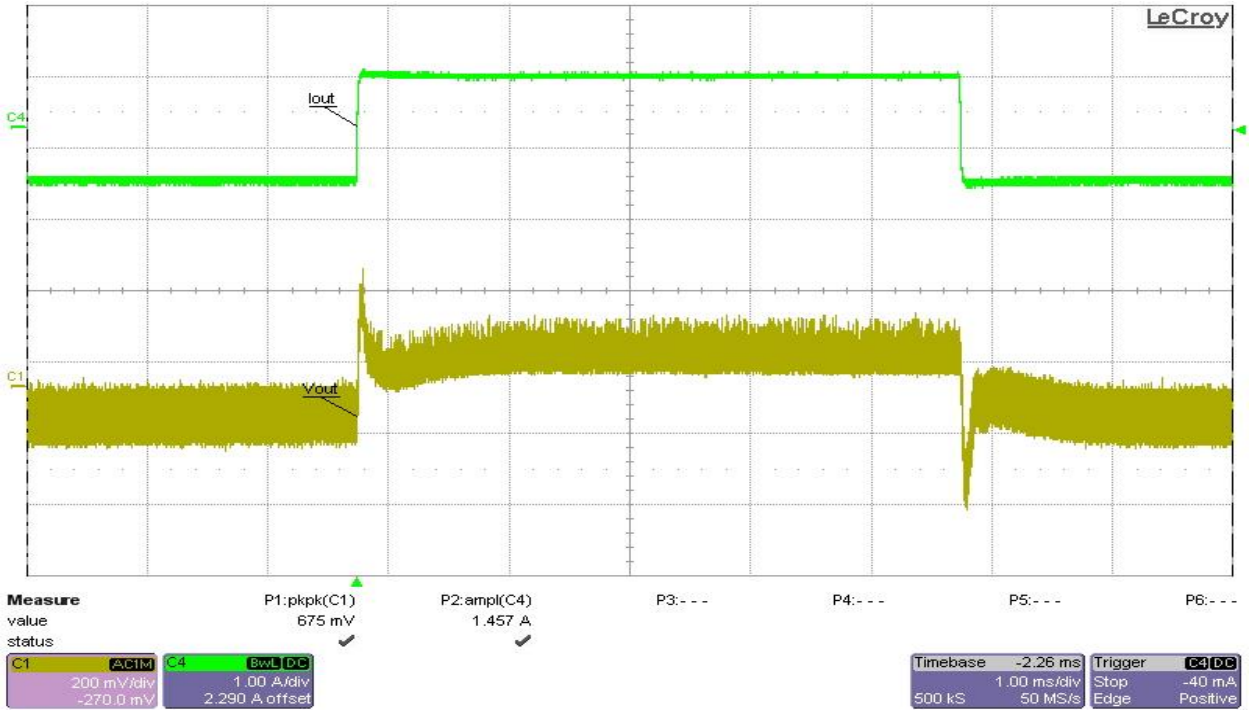


Startup into Full Load at 24Vin, Ch1 input, Ch2 Vpri, Ch3 Vout.

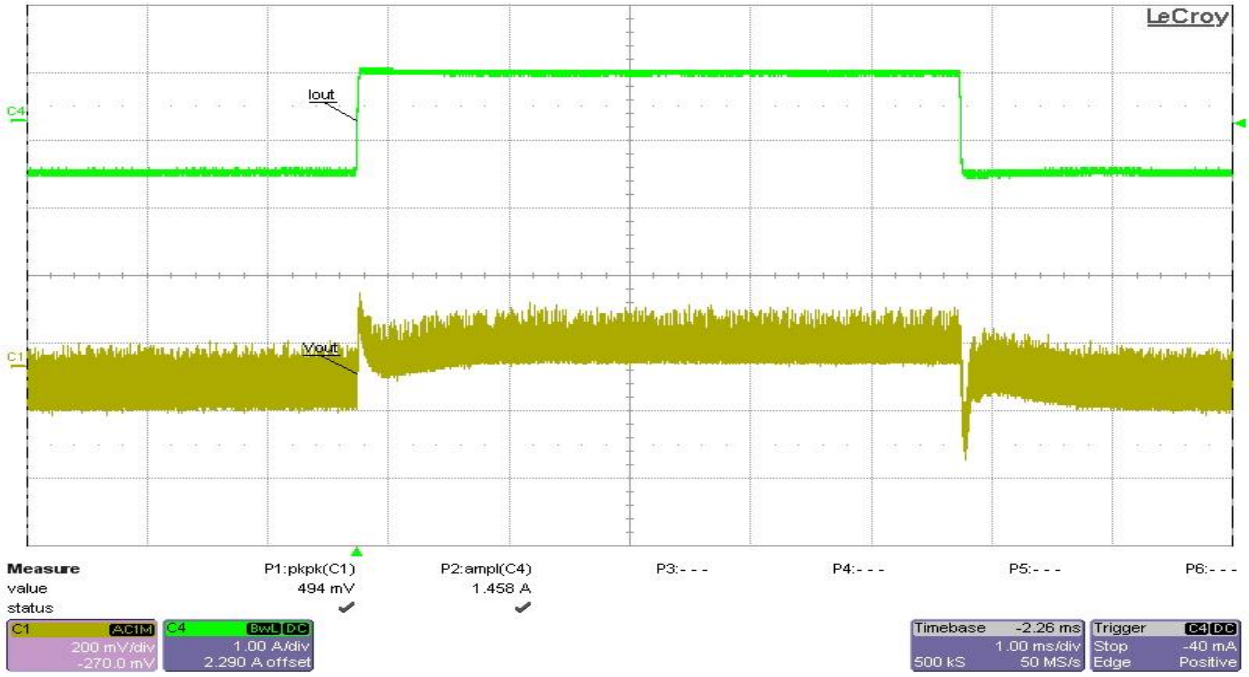


Startup into Full Load at 30Vin, Ch1 input, Ch2 Vpri, Ch3 Vout.

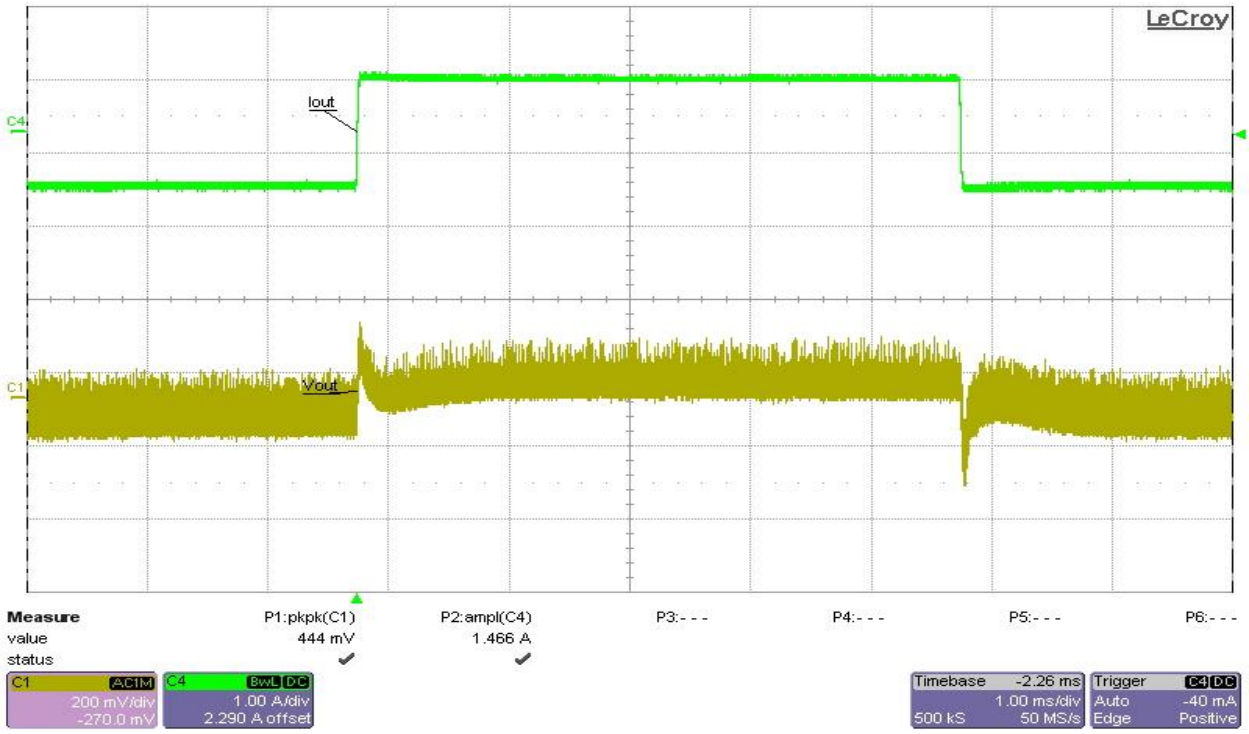
7.2 Load-Transient



Load Transient Response of Vout Rail Undergoing 50% to 100% Load Step at 18Vin. Ch4 is load current, Ch1 is Vout AC coupled.

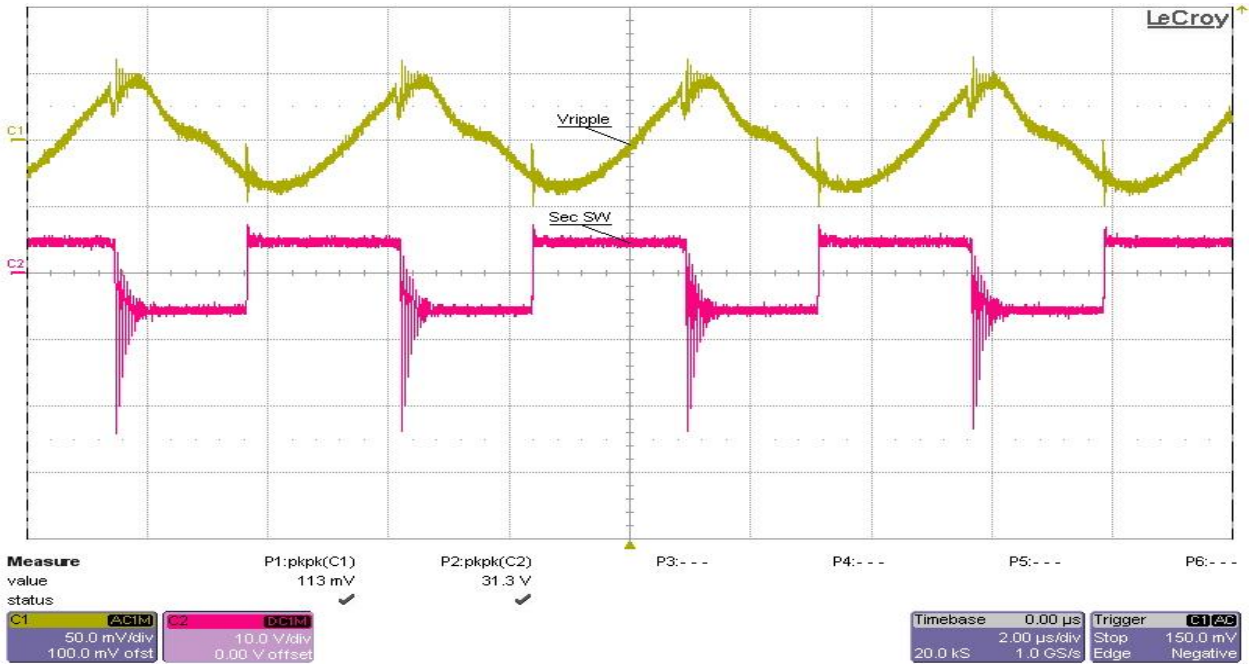


Load Transient Response of Vout Rail Undergoing 50% to 100% Load Step at 24Vin. Ch4 is load current, Ch1 is Vout AC coupled.

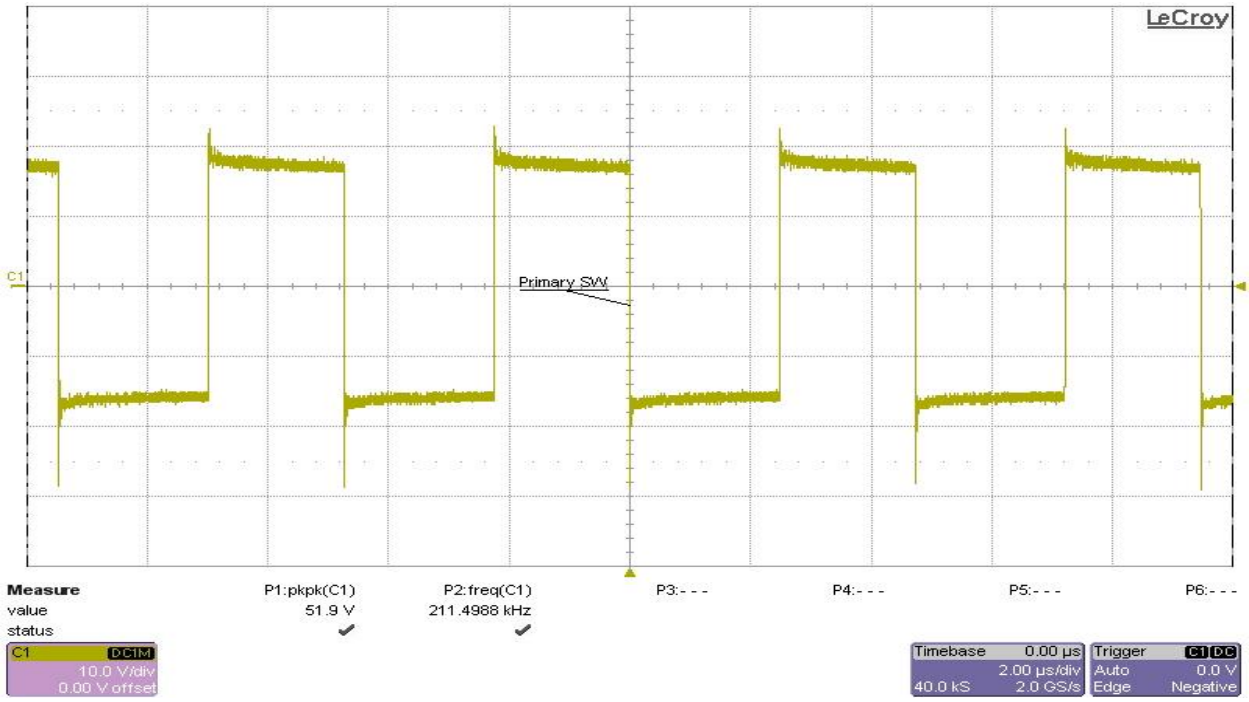


Load Transient Response of Vout Rail Undergoing 50% to 100% Load Step at 30Vin. Ch4 is load current, Ch1 is Vout AC coupled.

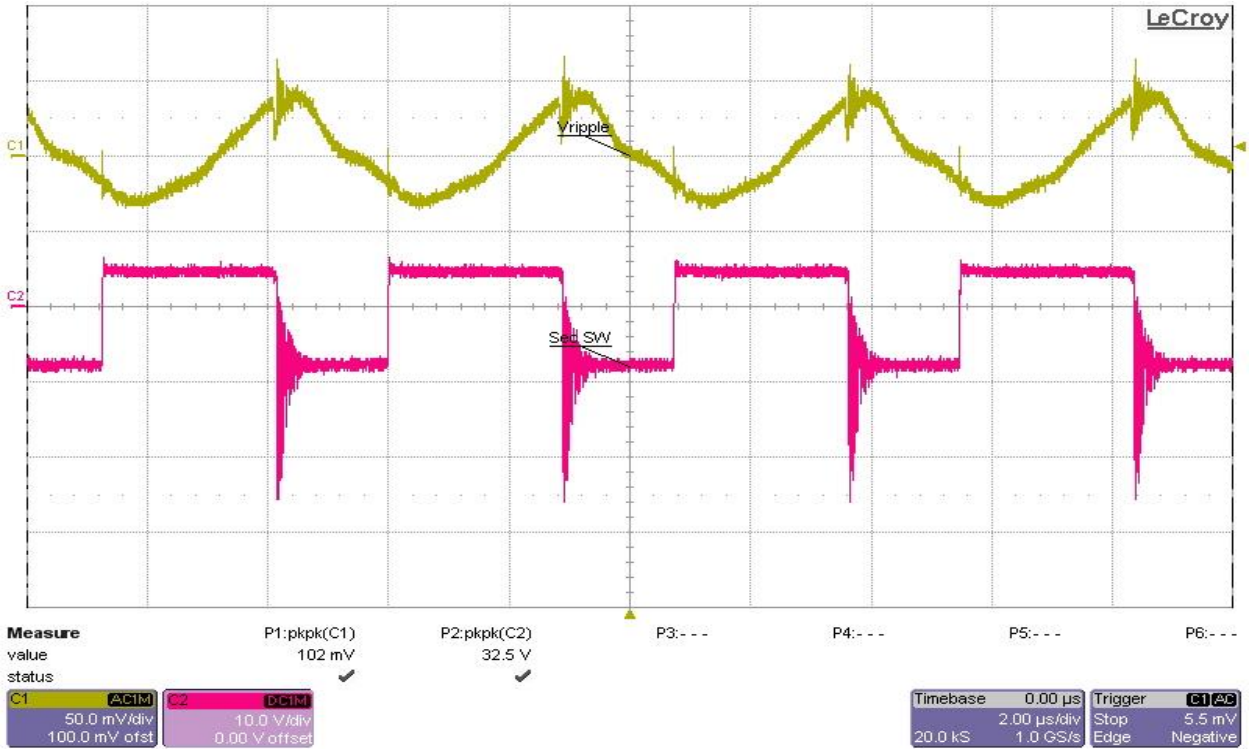
7.3 Switching Waveform and Output Ripple



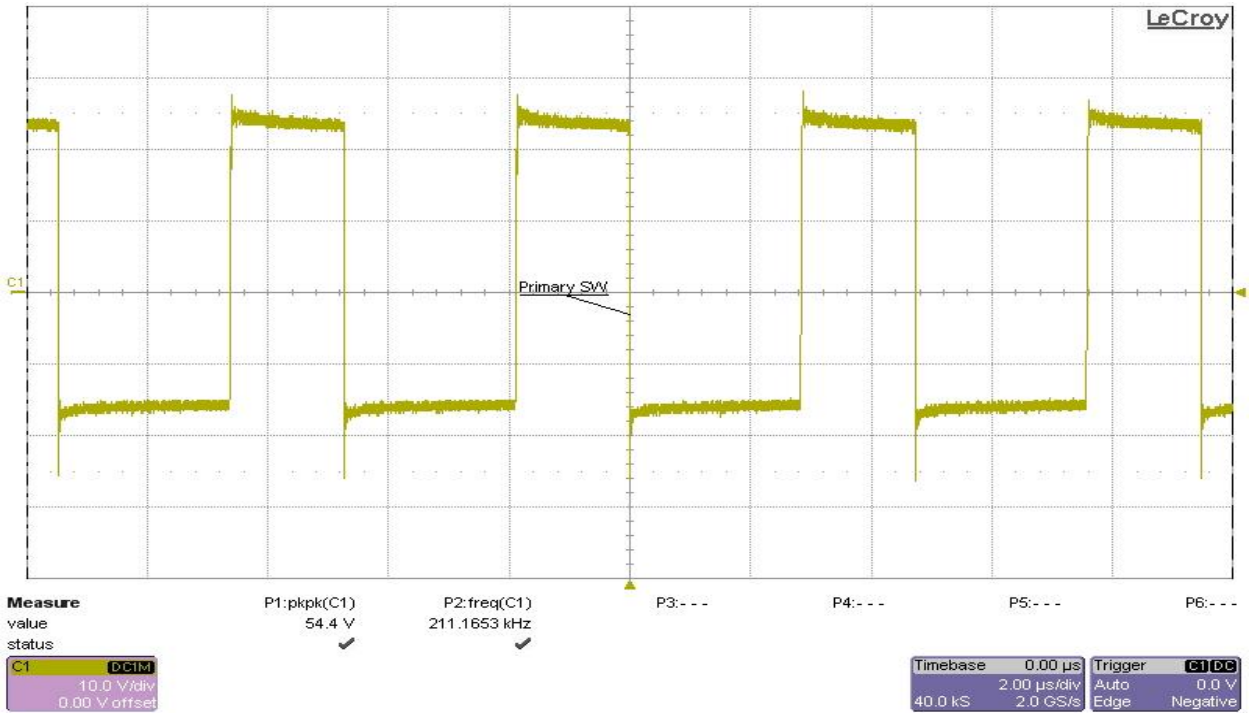
18Vin, 100% load. Ch2 measures secondary switching waveform (source voltage), Ch1 is AC coupled to measure ripple across Cout.



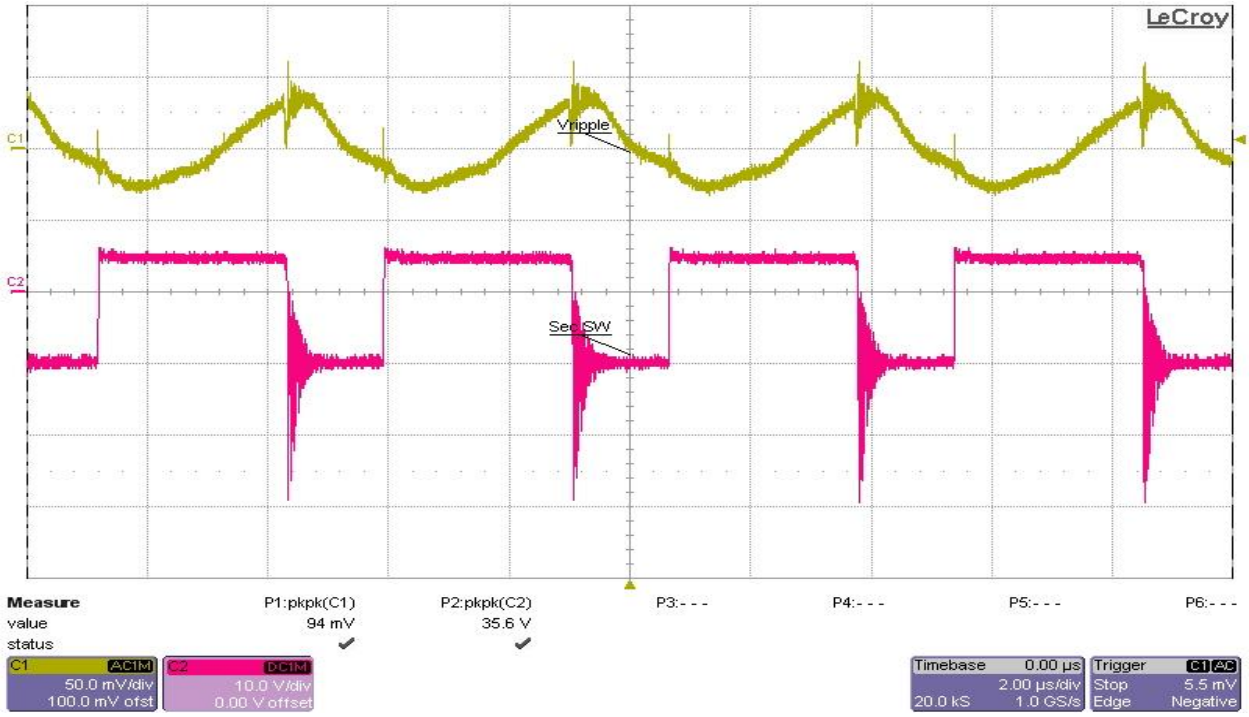
18Vin, 100% load. Ch1 measures primary switching waveform.



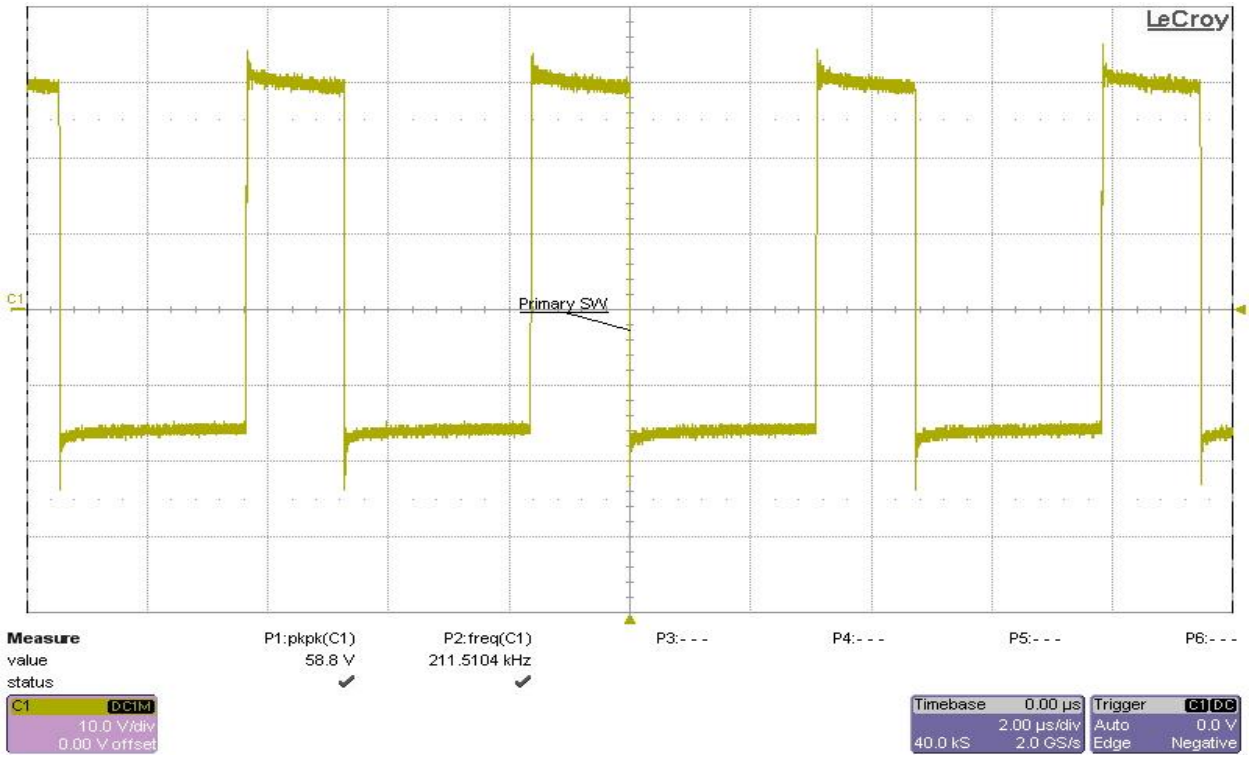
24Vin, 100% load. Ch1 measures secondary switching waveform (source voltage), Ch2 is AC coupled to measure ripple across Cout.



24Vin, 100% load. Ch1 measures primary switching waveform.

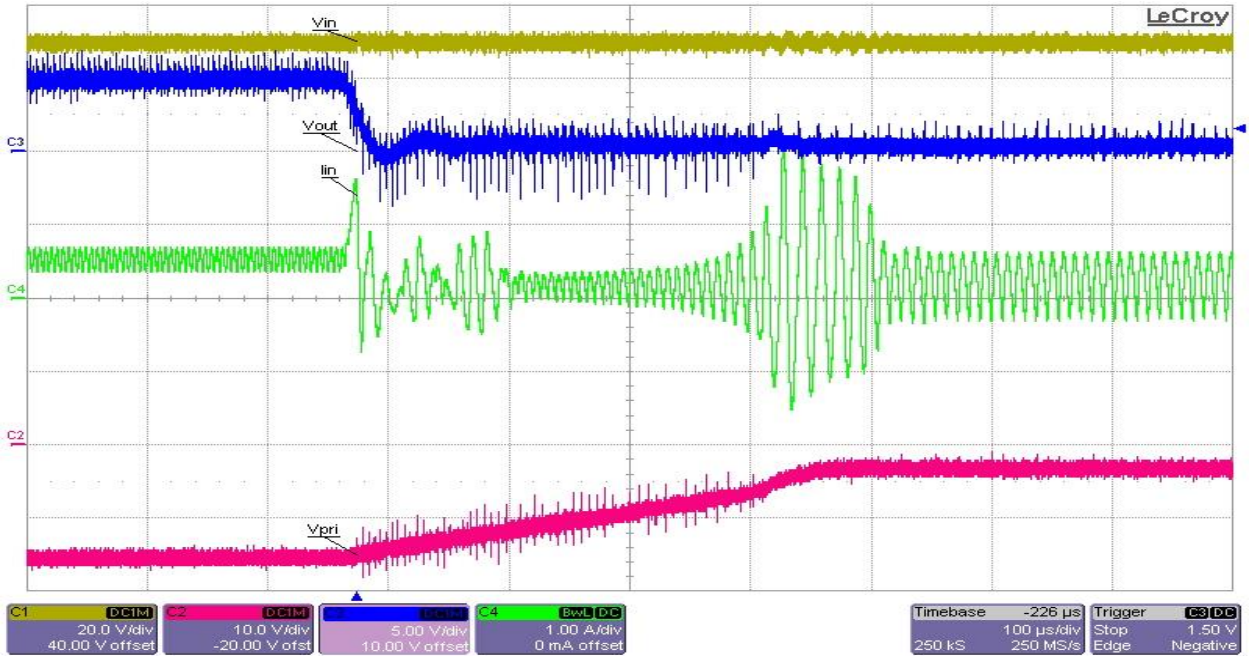


30Vin, 100% load. Ch2 measures secondary switching waveform (source voltage), Ch1 is AC coupled to measure ripple across Cout.



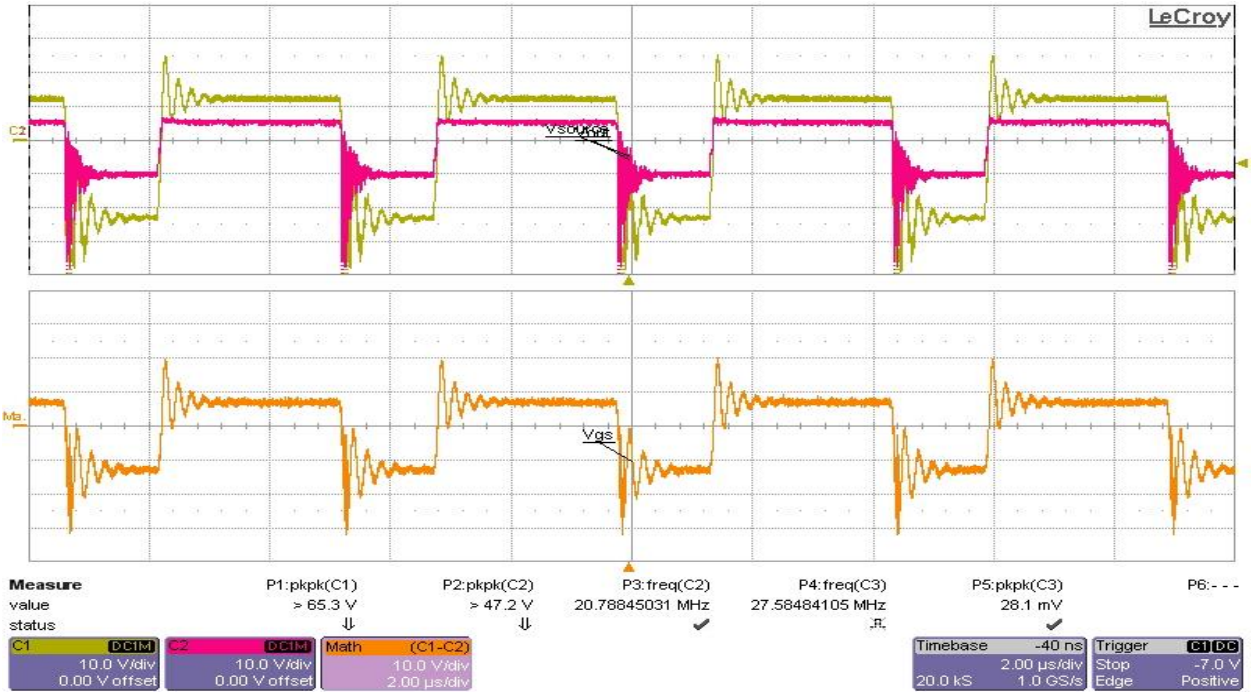
30Vin, 100% load. Ch1 measures primary switching waveform.

7.4 Short Circuit Protection

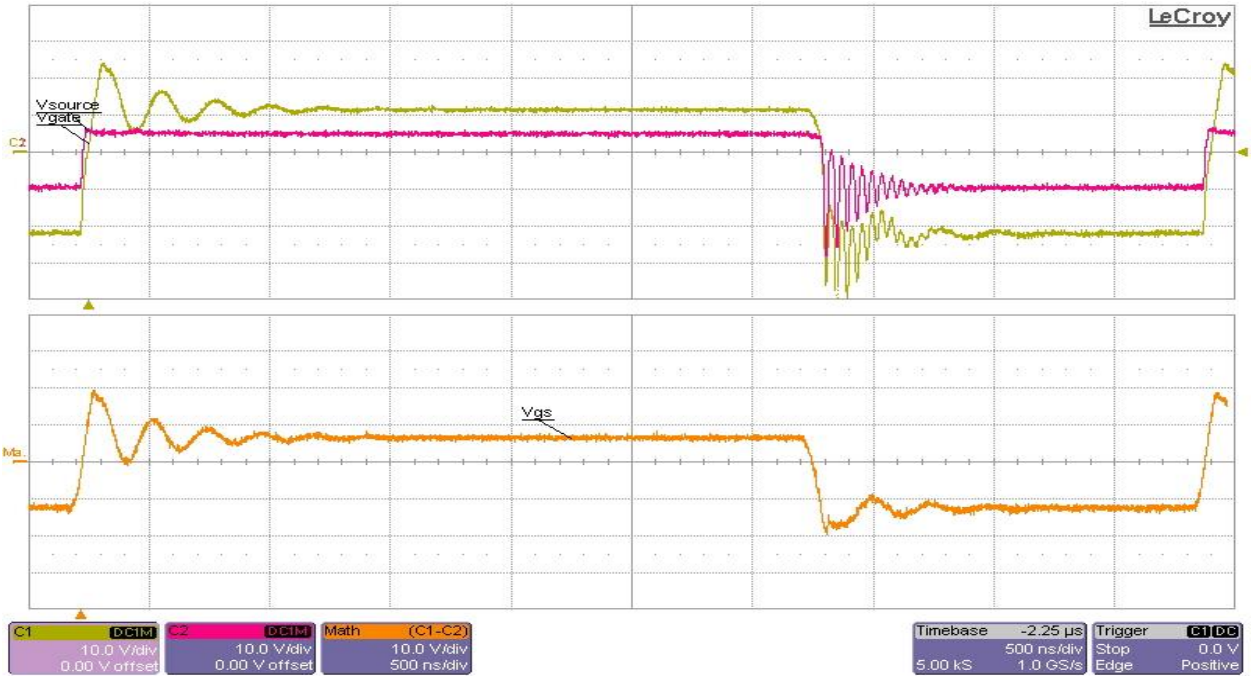


30Vin, Ch4 measures input current; Ch1 measures input voltage; Ch2 measures primary voltage; Ch4 measures output voltage. Short circuit is performed when the output is fully loaded.

7.5 Synchronous Rectifier Gate Drive



30Vin, Ch1 measures gate voltage; Ch2 measures source voltage; Orange plot measures the difference between ch1 and ch2. No zener diode is added to clamp Vgs.



30Vin, Ch1 measures gate voltage; Ch2 measures source voltage; Orange plot measures the difference between ch1 and ch2. Zener diode is added to clamp Vgs.

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