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Low Noise Power Management Reference Design for Automotive CMOS Imager Sensor and Data Serializer

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Design Resources

TIDA-00535	Design Folder
LP5907-Q1	Product Folder
LP5907	Product Folder
LM43602-Q1	Product Folder
DS90UB913A-Q1	Product Folder

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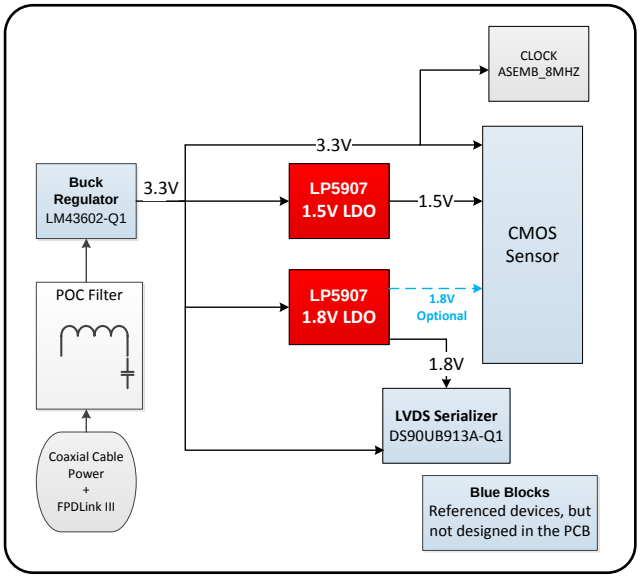
Block Diagram



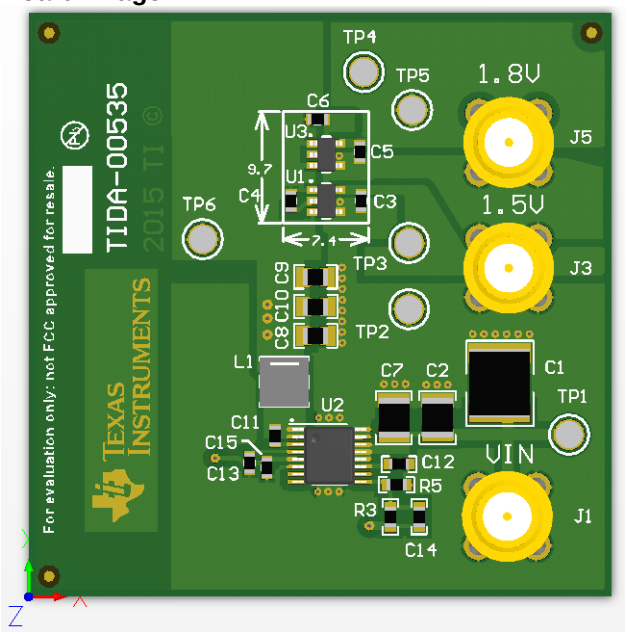
Design Features

- Space optimized power management solution for CMOS sensor and Serializer
- Cost optimize solution
- Test data and design recommendations for power management section of the system
- Components in this design are available in Automotive AEC Q100 Qualified Grade 1.
- Input voltage nominal 12 V, range from V_{IN}+0.3 V to 36 V
- Output voltage rails:3.3V, 1.8V and 1.5V

Featured Applications

- Automotive imaging applications (when Q1 grade devices are used)
  - Side camera
  - Rear camera
  - Front camera
- Non-Automotive applications
  - Webcam
  - Security Surveillance
  - Machine Vision
  - Medical Camera

Board Image



1 Key System Specifications

Table 1 Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Data Serializer for automotive camera system	Power supply recommendations for FPD-Link III SERIALIZER	See Section 4.2
CMOS image sensor	Power supply recommendations for OV10635 OmniVision HDR CMOS sensor	See Section 4.3
Design implementation	Design implementation guidelines	See Section 5

2 System Description

The TIDA-00535 reference design provides a power management solution for automotive imaging system using the voltage regulators LP5907-Q1, LP5907 and LM43602-Q1 to provide the appropriate voltage levels to power a CMOS high dynamic range camera, DS90UB913A-Q1 FPD-Link Serializer chipset and clock oscillator.

The TIDA-00535 is mainly focused in the power management section and provides test data, schematic, and Gerber files. This power management design can be used as a reference for automotive imaging applications as driver assistance including camera enabled systems for park assist rearview, side lane blind spot view, surrounding view and even forward facing vision. For ADAS applications it is recommended to use the Q100 certified version of the devices mentioned in this design.

The highlights for this design are:

- High system noise immunity over critical frequency range
- Cost optimized total power management solution
- Small foot print solution

Note: Advanced Driver Assistance Systems (ADAS) need to comply with the reliability and safety regulations and ASIL requirements (ISO-26262). For ADAS applications it is recommended to use Q100 certified discrete semiconductors and AEC-200 qualified passive components.

3 Device Selection Considerations

The highlighted design considerations for the device selection are low noise, cost, and size:

Low noise

The possible signal noise produced by the voltage regulators was taken into account at the time of selecting the components. Voltage regulators must have a switching frequency outside of the AM band (540 KHz to 1700 KHz) as well as low noise density and high power ripple rejection over critical frequency range for higher performance.

Cost:

Cost optimized integrated circuits (ICs) with few external components to keep a low bill of material (BOM) cost.

Table 2 Estimated Cost for Low noise LDOs

PART NUMBER	APPROXIMATED PRICE (USD)
LP5907 (1.5V)	$0.14 @ 1K cost
LP5907-Q1 (1.8V)	$0.16 @ 1K cost
2 Input capacitor	~$0.03
2 optional[1] output capacitor	~$0.03
Total	**~$0.36**

Table 3 Estimated Cost for pre-LDO Buck Regulator

PART NUMBER	APPROXIMATED PRICE (USD)
LM43602-Q1 (3.3V)	$2.07 @ 1K cost
11[2] external components	~$0.98
Total	**~$3.05**

AEC Q100 Qualified Grade 1:

AEC Q100 Qualified stands for qualified in accordance with AEC-Q100 industry standard.
Texas Instruments Q1 graded devices are developed to meet the requirements of reliability stress test defined by Automotive Electronics Council.
All the components in the system might have to comply with AEC-Q100 standard depending on the location and application. The LP5907-Q1 is available with fixed output voltages from 1.2 V to 4.5 V in 25 mV steps. Contact Texas Instruments Sales for specific voltage option needs.

Component Footprint:

The imaging sensors in automobiles are usually confine in small areas like bumpers, rear mirrors casing, side mirrors casing, etc. For this reason the total solution must be discrete in size for placement flexibility. The voltage regulators used in this design have small packages. The LP5907 comes in a DSBGA (0.675 mm x 0.675 mm) package, but depending on the location and application it might be necessary to use the LP5907-Q1 with the SOT-23 package which is AEC-Q100 certified.

Table 4 Power Management Components Footprint

PART NUMBER	PACKAGE	IC SIZE (NOMMINAL)
LP5907-Q1 (1.5V)	SOT-23	2.90 mm x 1.60 mm
LP5907 (1.8V)	SOT-23	2.90 mm x 1.60 mm
LM43602-Q1 (3.3)	HTSSOP (16)	5.1 mm x 6.6 mm

1 There is no strict requirement about location of the output cap, a cap <10cm away, at the input of the supplied part will be sufficient.
2 Based on the fundamental parts for operation, additional caps might be required to optimize transient behavior and regulation.

4 Block Diagram

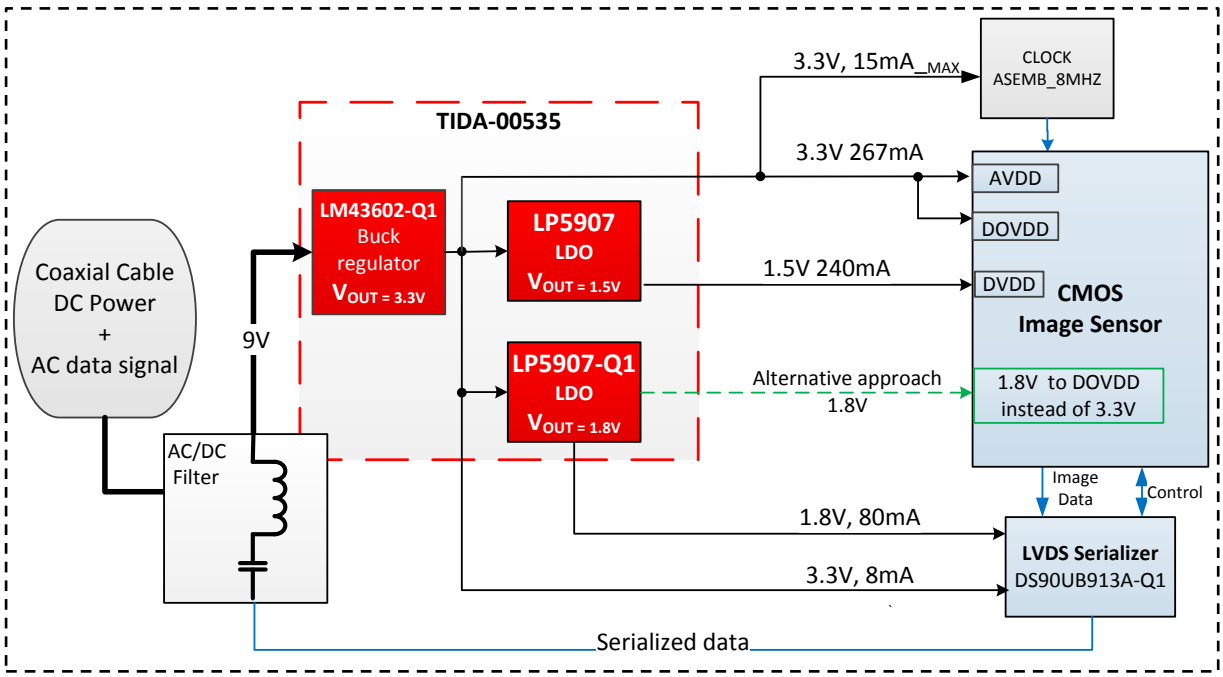


Figure 1 Comprehensive Block Diagram

As mentioned in previous section the main focus of this document is to provide test data and design parameters for the 1.5 V and 1.8 V regulated output voltage rails. These rails power the critical systems in the CMOS image sensor and data Serializer.

Figure 1 gives a high level block diagram of the complete system. The red block represents the focus component of this document.
The blue blocks represent other TI components and grey block are non TI components. Blue and grey components are mentioned in this document and their power requirements are explained and taken into consideration to define the system power requirements; however those components were not design into the TIDA-00535 evaluation board and some of their application specific requirements are not mentioned, it is recommended to review their datasheet for additional application implementation requirements.
The green dotted line connecting DOVDD of the CMOS imager to a 1.8V voltage supply rail represents an alternative power configuration.

4.1 Highlighted TI Products

TIDA-00535 features the following Texas Instruments (TI) low noise voltage regulator and high efficiency synchronous regulator. These devices were chosen taking into account the power requirements of typical CMOS sensor and data Serializer components.

LP5907-Q1: 250mA, Ultra-Low Noise Low-Dropout Regulator
LM43602-Q1: SIMPLE SWITCHER® 3.5V to 36V, 500mA Synchronous Step-Down Voltage Converter

4.1.1 LP5907-Q1

The LP5907-Q1 is a linear regulator capable of supplying 250-mA output current. Designed to meet the requirements of RF and analog circuits, the LP5907-Q1 device provides low noise, high PSRR, low quiescent current and low line or load transient response. Using new innovative design techniques, the LP5907-Q1 offers class-leading noise performance without a noise bypass capacitor and the ability for remote output capacitor placement, the remote capacitor feature can save board space by using the capacitor of the supplied part.

The device is designed to work with a 1-µF input and a 1-µF output ceramic capacitor (no separate noise bypass capacitor is required).

Two of these low noise regulators were used to step down the 3.3 V output voltage of the DC/DC converter to 1.5 V and 1.8 V.

Alternative linear regulators:
LP5907: Same functionality as LP5907-Q1 but smaller package and not Q1 graded for non-automotive camera applications.
LP3990: V_{OUT} = 1.2 V, 1.8 V, 2.8 V; smaller package but lower output current of 150 mA.
LP3892: V_{OUT} = 1.2 V, 1.8 V, 2.8. Higher maximum output current of 1.5 A, but requires a V_{BIAS} of 5V
LP3990Q: V_{OUT} = 2.8, I_{OUT}=150; some data serializers can be powered with 2.8V input voltage.

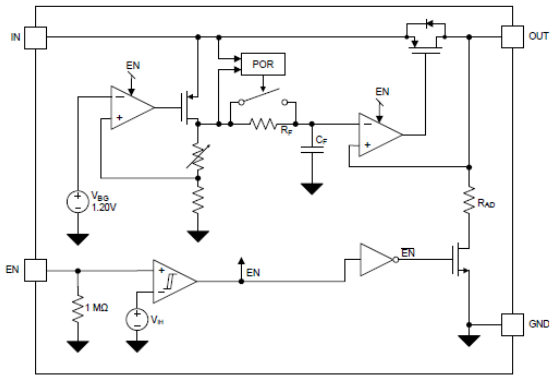


Figure 2 LP5907-Q1 Functional Block Diagram

4.1.2 LM43602-Q1

The LM43602-Q1 SIMPLE SWITCHER® regulator is an easy-to-use synchronous step-down DC-DC converter capable of driving up to 2 A of load current from an input voltage ranging from 3.5 V to 36 V (42 V abs max). The LM43602-Q1 provides exceptional efficiency, output accuracy and dropout voltage in a very small solution size. An extended family is available in 0.5 A, 1 A, and 3 A load current options in pin-to-pin compatible packages. Peak current mode control is employed to achieve simple control loop compensation and cycle-by-cycle current limiting. Optional features such as programmable switching frequency, synchronization, and power-good flag, precision enable, internal soft-start, extendable soft-start, and tracking provide a flexible and easy to use platform for a wide range of applications. Discontinuous conduction and automatic frequency modulation at light loads improve light load efficiency. The family requires few external components and terminal arrangement allows simple, optimum PCB layout. Protection features include thermal shutdown, V_{CC} under voltage lockout, cycle-by-cycle current limit, and output short circuit protection. The LM43602-Q1 device is available in the HTSSOP / PWP 16-pin leaded package (5.1 mm × 6.6 mm × 1.2 mm).

Main care-about for an alternative DC/DC step down voltage converters are:

- Converter with internal FETs or module for minimum external component count
- Input transient tolerance of minimum 36V
- Synchronous regulator for high efficiency
- At least 1 A of source current
- Good thermal dissipation
- Q100 reliability graded
- Small foot print

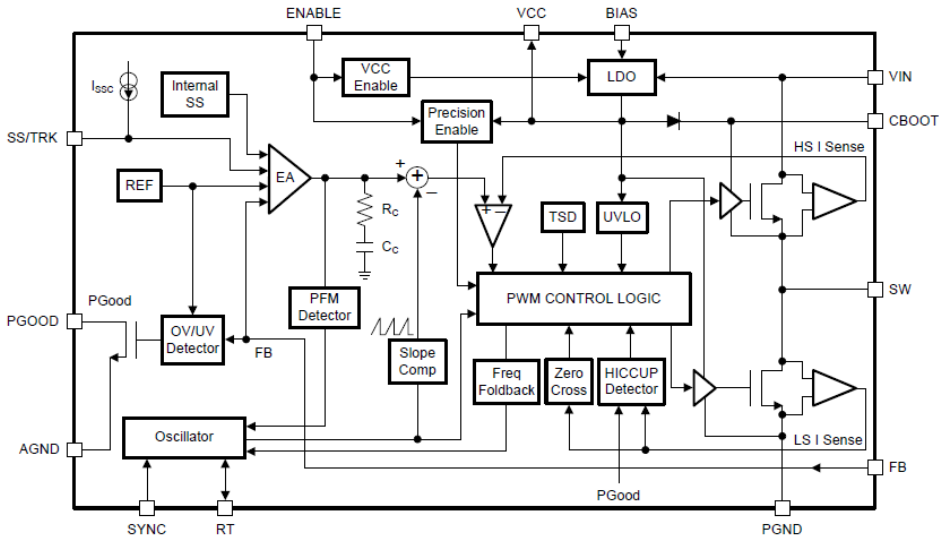


Figure 3 Functional Block Diagram for LM43602-Q1

Table 5 Pin Function for LM43602-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NUMBER		
SW	1,2	P	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to power inductor.
CBOOT	3	P	Boot-strap capacitor connection for high-side driver. Connect a high quality 470 nF capacitor from CBOOT to SW.
VCC	4	P	Internal bias supply output for bypassing. Connect bypass capacitor from this pin to AGND. Do not connect external loading to this pin. Never short this pin to ground during operation.
BIAS	5	P	Optional internal LDO supply input. To improve efficiency, it is recommended to tie to V_{OUT} when 3.3 V ≤ V_{OUT} ≤ 28 V, or tie to an external 3.3 V or 5 V rail if available. When used, place a bypass capacitor (1 to 10 µF) from this pin to ground. Tie to ground when not in use. BIAS pin voltage should not exceed VIN.
SYNC	6	A	Clock input to synchronize switching action to an external clock. Use proper high speed termination to prevent ringing. Connect to ground if not used.
RT	7	A	Connect a resistor R_T from this pin to AGND to program switching frequency. Leave floating for 500 kHz default switching frequency.
PGOOD	8	A	Open drain output for power-good flag. Use a 10 kΩ to 100 kΩ pull-up resistor to logic rail or other DC voltage no higher than 12 V.
FB	9	A	Feedback sense input pin. Connect to the midpoint of feedback divider to set V_{OUT}. Do not short this pin to ground during operation.
AGND	10	G	Analog ground pin. Ground reference for internal references and logic. Connect to system ground.
SS/TRK	11	A	Soft-start control pin. Leave floating for internal soft-start slew rate. Connect to a capacitor to extend soft start time. Connect to external voltage ramp for tracking.
EN	12	A	Enable input to the internal LDO and regulator. High = ON and low = OFF. Connect to VIN, or to VIN through resistor divider,or to an external voltage or logic source. Do not float.
VIN	13,14	P	Supply input pins to internal LDO and high side power FET. Connect to power supply and bypass capacitors C_{IN}. Path from VIN pin to high frequency bypass C_{IN} and PGND must be as short as possible.
PGND	15,16	G	Power ground pins, connected internally to the low side power FET. Connect to system ground, PAD, AGND, ground pins of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
PAD	17	—	Low impedance connection to AGND. Connect to PGND on PCB. Major heat dissipation path of the die. Must be used for heat sinking to ground plane on PCB.

(1) P = Power, G = Ground, A = Analog

4.2 Other TI parts

4.2.1 DS90UB913A-Q1

FPD-Link III with Power-Over-Coax

The DS90UB913A-Q1 is a 25-100MHz 10/12- Bit DC-Balanced FPD-Link III Serializer with Bidirectional Control Channel. The DS90UB913A/DS90UB914A chipset offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single differential pair. The DS90UB913A-Q1/914A-Q1 chipsets incorporate differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The Serializer/Deserializer pair is targeted for connections between imagers and video processors in an ECU (Electronic Control Unit). This chipset is ideally suited for driving video data requiring up to 12 bit pixel depth plus two synchronization signals along with bidirectional control channel bus.

Key Specifications

- 1.8-V, 2.8-V or 3.3-V-Compatible Parallel Inputs on Serializer
- Single Power Supply at 1.8 V
- Coaxial or Single Differential Pair Interconnect
- 25-MHz to 100-MHz Input Pixel Clock Support
- Programmable Data Payload:
  - 10-bit Payload up to 100 MHz
  - 12-bit Payload up to 75 MHz
- Embedded Clock with DC-Balanced Coding to Support AC-Coupled Interconnects
- Automotive Grade Product: AEC-Q100 Grade 2 Qualified
- Small Serializer Footprint (5 mm × 5 mm)

5 Design Considerations

5.1 Remote Power Delivery

This section gives an overview of two widely known and used methods to power devices in remotely location. When providing power to remote device using long cables it is important to use electromagnetic interference (EMI) best design practices to avoid noise coupling and data distortion.

5.1.1.1 Power Feed through Coaxial Cable

The system input voltage is expected to be 12V nominal from the engine control unit (ECU) which is deliver via power over coaxial (POC) along with a single ended data path carrying two data channels, the backward channel with frequency bandwidth of 1 MHz to 4 MHz and a forward channel Carrying the coded and serialized data from the imager with a frequency bandwidth from about 70 MHz to 700 MHz. The unused data pin (DOUT–, RIN–) should have a 0.047-µF capacitor in series and terminated with a 50-Ω resistor.

Two filters needs to be implemented at the power receiver side, one low pass filter for the DC signal, and a high pass filter for the AC signal carrying the data.

1. **High pass filter (DC voltage)**
   The high pass filter needs to block the DC signal and have low impedance at the band of interest to allow the AC signal to pass without corrupting the data.
   A simple 0.1uF 603 capacitor with low parasitic inductance and low equivalent series resistance will do the work.

2. **Low pass filter (AC signal)**
   The second section needs to allow the DC voltage to pass without interfering with the data path and also have to block any noise coming from the voltage management system. This circuitry is more complex because it requires an inductor to block the high frequencies and inductors are less ideal than capacitor and come in bigger sizes. To avoid interference with the data path the filter must have impedance 20X higher than the characteristic impedance; in the case of 50Ω cox line the impedance must be greater than 1kΩ from 1 MHz up to 700 MHz.

   Taking the above information into account it is recommended to use two inductors in series to compensate for the resonant frequency and parasitic capacitance of the inductors. A 100 µH in series with a 4.7µ inductor will have overall impedance greater than 1 kΩ from 1MHz to 1 GHz. A resistor can be placed in parallel with each inductor to keep the inductance from spiking too high. A ferrite bead is can be added for filtering out coupled Electro-Magnetic Interference (EMI) in the coaxial cable. The capacitors are simply bulk capacitance to reduce current ripple to the input of the power supplies.

   Chose and adequate saturation current because usually the value specified in the inductor data sheet means when the inductance value has fallen by 10 % and it will then behave as a capacitor. Use magnetically shielded inductor and do not route any tracks under the component to avoid any magnetic coupling with adjacent components or conductor traces, also shielded inductors have lower DC resistance than an unshielded inductor, this translate to lower wire heating losses which is related to power coper loses.

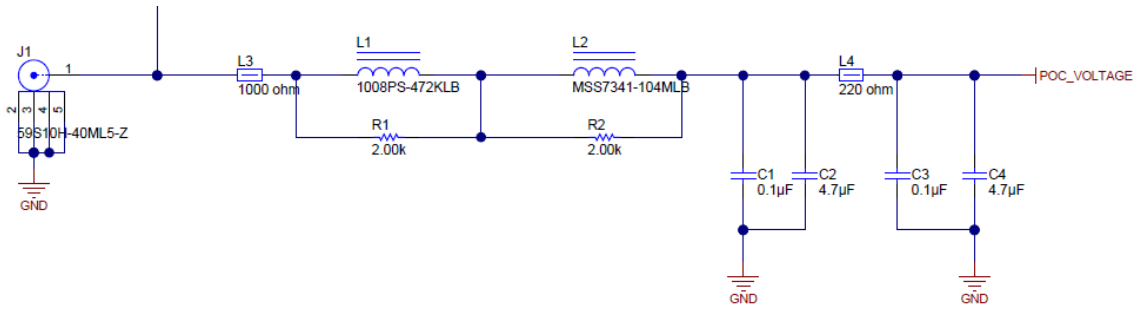


Figure 4 Power over coaxial cable

For more information about power over coaxial filter design please refer to TI application report *Sending Power over Coax in DS90UB913A Designs (*SNLA224)

5.1.2 Power Feed through Shielded Twisted Pair Cable

The basic concept to deliver power through a shielded twisted pair (TPS) is similar to power over coaxial, the goal is to transmit DC voltage along with the high speed bidirectional data transmitter signal through the same media.

The main concern is to isolate the forward and backward high frequency signal from the DC voltage. The DC voltage is extracted from the center of a power feed inductor (Bias Injection Choke) like the KA4909-AL, and the AC signal can be decoupled using capacitors in series with the differential lines.

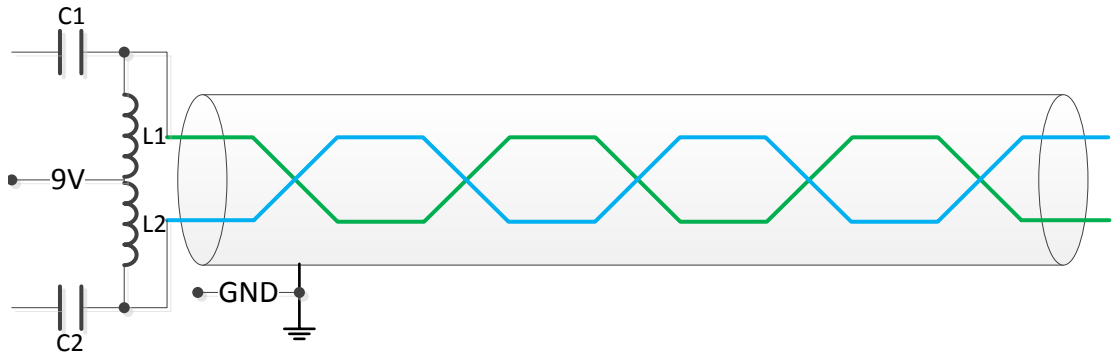


Figure 5 Power over Twisted Pair

For detail information about delivering power to remote device using differential pair please refer to the *Combine power feed and data link via cable for remote peripherals* technical document.

5.2 Data Serializer Power Supply Requirements

This section provides power requirements of a typical Serializer; the DS90UB913A-Q1 FPD-Link III Serializer is used as an example.
For detail information about digital/analog pin configuration and application implementation please refer to the DS90UB913A-Q1 datasheet (SNLS443B)

5.2.1 DS90UB913A -Q1 Voltage Pins

Table 6 DS90UB913A-Q1 Power Connections

NAME	PIN NUMBER	VOLTAGE	FILTERING COMPONENTS	DESCRIPTION
VDDPLL	10	1.8 V	0.01µ, 0.1µ, 4.7µF	Power, PLL Power, 1.8 V ±5%. Analog
VDDT	11	1.8 V	0.01µ, 0.1µ, 4.7µF	Power, Tx Analog Power, 1.8V ±5%. Analog
VDDCML	14	1.8 V	0.01µ, 0.1µ, 4.7µF	Power, CML & Bidirectional Channel Driver Power, 1.8 V ±5%. Analog
VDDD	28	1.8 V	0.01µ, 0.1µ,	Power, Digital Power, 1.8 V ±5%. Digital
VDDIO or 3.3 V ±10%.	25	1.8 V ±5% or 2.8±10% or 3.3 V ±10%	0.01µ, 0.1µ,	Power, Power for I/O stage. The single-ended inputs and SDA, SCL are powered from VDDIO. VDDIO Digital can be connected to a 1.8 V ±5% or 2.8±10%
VSS ground plane (GND) with at least 9 vias.	DAP	GND		Ground, DAP must be grounded. DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connected to the

5.2.2 DS90UB913A-Q1 Power up Requirements

The DS90UB913A-Q1 requires delaying the PDB V_{DC} after all other power supplies have settled to the recommended operating voltage. An external RC network can be connected to the PDB pin to ensure PDB arrives after all the VDD has stabilized.

A delay to the power up sequence can be implemented with either a simple RC circuit or by implanting a robust supply voltage supervisor like the TPS3836E18-Q1 with 10ms/200ms selectable delay time.

5.2.3 DS90UB913A-Q1 Input Voltage Requirements

Table 8 shows the power requirements for the DS90UB913A-Q1

Table 7 Worst Case Current Consumption

NAME	CONDITIONS	CURRENT [mA]	POWER [mW]
VDDT	RL=100 Ω VDDn = 1.80 V, VDDIO = 3.6 V f = 75 MHz, 12-bit high frequency mode Default Registers	I_{DDT} = 84	151
VDDIO	RL=100 Ω VDDIO = 3.6 V f = 75 MHz, 12-bit high frequency mode Default Registers	I_{DDIOT} = 8	28.8

Table 9 shows the input voltage tolerance of the DS90UB913A-Q1, the input voltage has to be stable within the maximum and minimum voltage limits to avoid erroneous operation.

Table 8 DS90UB913A-Q1 Input Voltage Tolerance

NAME	VOLTAGE	TOLERANCE
VDDT	1.8V	±5% (±75mV)
VDDIO	3.3V	±10% (±330mV)

5.3 CMOS Image Sensor Power Supply Requirements

This section provides power requirements of a typical CMOS sensor. The OV10635 HD HDR imager CMOS sensor from OmniVision is used as an example to show the power requirements of a typical CMOS sensor.
For detail information about digital/analog pin configuration and application implementation please refer to OV10635 datasheet it can be obtained from OmniVision Technologies corp.

5.3.1 CMOS Image Sensor Power Considerations

The analog supply voltage for most CMOS sensors used in cameras ranges from 1.5 to 3.3V. A clean voltage supply is required for these voltage rails.

Table 9 CMOS OV10635 Sensor Power Supply requirements

PARAMETER	NAME	VOLTAGE	CURRENT [mA]	POWER [mW]
Core Voltage	DVDD	1.5V	160	240 mW
Analog power	AVDD	3.3V	@3.3V: I_{TYP}= 81	267 mW
I/O Power and	DOVDD	3.3V or 1.8V		

Table 10 CMOS OV10635 sensor input voltage tolerances

NAME	VOLTAGE	TOLERANCE
DVDD	1.5V	±5% (±75mV)
AVDD	1.8V	±5% (±75mV)
DOVDD	3.3V or 1.8V	@3.3V ±10% @1.8V ±5%

The DOVDD can be powered either from 3.3V or 1.8V

5.4 Total Power Supply Requirements

The table 6 provides the total typical power requirement for the Serializer, CMOS image sensor and a typical 8 MHz clock oscillator.

Table 11 Total Power Requirements

VOLTAGE	CMOS SENSOR [mW]	SERIALIZER [mW]	ASEMB_8MHZ[3] (Clock)	TOTAL POWER [mW]
1.5V	240	N/A	N/A	**240**
1.8V	N/A	151	N/A	**151**
3.3V	267	28.8	27 $mW_{\_MAX}$	**323**
			TOTAL	**714**

From the details mentioned in the previous sections we can conclude that the most critical voltage rails with tight voltage limits are the 1.5 V and 1.8 V, these voltage rails have a tolerance of ±5%. Table 7 shows the system voltage requirements and minimum and maximum voltage limits.

Table 12 Total Power Requirements

VOLTAGE	CURRENT (mA)	V_{MIN}	V_{MAX}
1.5V	160	1.42	1.57
1.8V	84	1.72	1.87
3.3V	104	2.97	3.63

[3] Information about ASEMB_8MHZ was obtained from datasheet (LINK)

6 Design Implementation Guidelines

The following system considerations apply only for the conditions of this design. For different conditions it is essential to verify the ratings and operating conditions on the datasheets of the parts mentioned in this design. If the parameters does not fit the application consider one of the alternative parts on section 3 or perform and easy parametric search at http://www.ti.com

6.1 Linear Regulator

The LP5907 requires at least a 1 µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards to the pin. In practical designs the output capacitor may be located up to 10 cm away from the LDO. This means that there is no need to have a capacitor close to the output pin, a remote capacitor at the supplied device will be sufficient. The remote capacitor feature helps to minimize the number of capacitors in the system.

The recommendation is to keep parasitic wiring inductance less than 35 nH. For the applications with fast load transients, it is recommended to use an input capacitor equal to or larger to the sum of the capacitance at the output node for the best load transient performance.

Adding higher capacitor values will reduces the transient response, but also increases the response time for the output voltage to reach the nominal voltage.

6.1.1 Thermal Performance

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The actual power being dissipated in the device can be represented by Equation 1

$$\boldsymbol{P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}} \quad \textbf{(1)}$$

$T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (R θ JA), as given by Equation 2

$$T_{A\_MAX} = -(\theta_{JA} \times P_D) + T_{J\_MAX} \quad (2)$$

The typical ambient temperature of the 1.5 V and 1.8 V LDO was calculated using Equation 1 and Equation 2.

INPUT VOLTAGE	OUTPUT VOLTAGE	Load Current	THEORETICAL $T_{A\text{-}MAX}$
3.3 V	1.5 V	84 mA	94° C
3.3 V	1.8 V	160 mA	133° C

The computed T_{A_MAX} can be consider as a highly conservative scenario, because a system board rarely approximates the test JEDEC board used to determine $R_{\theta JA,}$. The PCB board layout strongly influences the thermal dissipation of the device; an optimized layout will have a lower $R_{\theta JA}$ than the JEDEC which means that will have a higher T_{A_MAX}.
For detail information about how to design an optimized board for lower thermal resistance please refer to application report (SNVA183B)

6.2 Step Down Voltage Converter Implementation

This section gives a high-level description of the compensation components of the LM43602-Q1 synchronous step down voltage converter. For function and description of the device pins mentioned in this section please refer to section 3.2.2 .

Table 13 Design parameters

PARAMETER	VALUE
V_{IN}	12V nominal
V_{OUT}	3.3V
I_{OUT_MAX}	2 A
Switching frequency	500 KHz

Note: This section gives an overview of the application implementation for LM43602-Q1, but for further details and information about the device performance, implementation, applications and component selections please refer to datasheet (SNVSA83A)

6.2.1 Switching Frequency

To avoid interference with the AM radio band, all switching frequencies need to either be greater than 1700 kHz or lower than 540 kHz.
To set the switching frequencies in the LM43602-Q1 a resistor needs to be connected from R_T pin to ground. The following equation can be used to calculate the R_T value

R_T (kΩ) = 40200 / Freq (kHz) - 0.6

Table 14 shows resistors values that will set the switching frequency to a frequency outside of the AM band.

Table 14 Resistor Values to Set Switching Frequency

F_S (KHz)	R_T (KΩ)
200	200
350	115
500	80.6 or open
2000	19.6
2200	17.8

6.2.2 Output Voltage Selection

For an output voltage of 3.3 V and greater, the BIAS pin can be connected to the output in order to increase light load efficiency.

The output voltage is set by an external resistor divider network, comprised of top feedback resistor (R_{FBT}) and bottom feedback resistor (R_{FBB}). It is recommends to set the value of the R_{FBT} to 100 kΩ to minimize ground current, the R_{FBB} can be calculated using the equation below

$$\boldsymbol{R_{FBB}} = \frac{\boldsymbol{V_{FB}}}{\boldsymbol{V_{OUT}} - \boldsymbol{V_{FB}}} \times \boldsymbol{R_{FBT}} \quad \textbf{(3)}$$

A 43.2 kΩ resistor can be used for R_{FBB} to set the output voltage to 3.3 V.

6.2.3 Inductor Selection

The main principles to select the appropriate inductor are inductance, peak to peak ripple current, maximum load current, frequency of operation and the converter duty cycle. Higher inductance gives lower ripple current and hence lower output voltage ripple with the same output capacitors. Lower inductance could result in smaller, less expensive component, and faster transient response.

The following equation can be used to calculate the correct inductor for a system with 12V input voltage and 3.3V output voltage and 2A peak current.

Converter duty cycle

$$D = \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Inductance range:

$$\frac{(V_{IN}-V_{OUT})\times D}{0.4\times F_S\times I_{L\_MAX}} \leq L \leq \frac{(V_{IN}-V_{OUT})\times D}{0.2\times F_S\times I_{L\_MAX}} \quad (5)$$

Peak to peak inductor current ripple has to be within 20% and 40%

$$\Delta i_L = \frac{(V_{IN}-V_{OUT})\times D}{L\times F_S} \quad (6)$$

Inductors ripple current ratio:

$$r = \frac{\Delta i_L}{I_{OUT}} \quad (7)$$

Terms key
Δ iL = Peak to peak ripple current
D = Duty cycle
r = Ripple current ratio
F_s = Switching frequency

A 6.8 µH mid-range inductor from the calculated inductance range of equation (2) will provide an adequate current ripple.

6.2.4 Compensation capacitors

Boot strap capacitor

Every LM43602-Q1 design requires a bootstrap capacitor, CBOOT. The recommended bootstrap capacitor value is 0.47 μ F and rated at 6.3 V or higher. The bootstrap capacitor is located between the SW pin and the CBOOT pin. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

VCC Capacitor

The VCC capacitor is located at the output voltage of the internal LDO. To insure stability of the part, place a minimum of 2.2 µF, 10V capacitor from this pin to ground.

BIAS Capacitors

The LM43602-Q1 integrates an internal LDO to generate VCC for control circuitry and MOSFET drivers. The nominal voltage for VCC is 3.2 V. The VCC pin is the output of the LDO must be properly bypassed. A high quality ceramic capacitor with 2.2 µF to 10 µF capacitance and 6.3 V or higher rated voltage should be placed as close as possible to VCC and grounded to the exposed PAD and ground pins. The VCC output pin should not be loaded, left floating, or shorted to ground during operation. Shorting VCC to ground during operation may cause damage to the LM43602-Q1.

Input Capacitors

The LM43602-Q1 device requires high frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. The typical recommended value for the high frequency decoupling capacitor is between 4.7 µF to 10 µF. A high-quality ceramic type X5R or X7R with low equivalent series resistance (ESR) is recommended.

Output Capacitor

Capacitors with small ESR and large capacitance are desired for applications with fast large load transients to improve load regulation. A good known technique to avoid using big capacitors is to place a couple of smaller capacitors in parallel; this will lower the ESR and compensate for their independent resonant frequency.

The following equation gives an approximation for an absolute minimum output cap required:

$$C_{OUT} > \frac{1}{F_S \times \Delta V_{OUT}/I_{OUT}} \times \left[\left(\frac{r^2}{12} \times (1 + (1 - D)\right) + \left((1 - D) \times (1 + r)\right)\right] \quad (8)$$

Along with this for the same requirement, the max ESR should be calculated as per the following inequality:

$$ESR < \frac{1-D}{F_S \times C_{OUT}} \times \left(\frac{1}{r} 0.5\right) \quad (9)$$

A general guideline for COUT range is that COUT should be larger than the minimum required output capacitance calculated by Equation 8, and smaller than 10 times the minimum required output capacitance or 1 mF. In applications with VOUT less than 3.3 V, it is critical that low ESR output capacitors are selected. This will limit potential output voltage overshoots as the input voltage falls below the device normal operating range. To optimize the transient behavior a feed-forward capacitor could be added in parallel with the upper feedback resistor. For this design example, three 47 µF,10 V, X7R ceramic capacitors are used in parallel.

Feedforward capacitor

To improve the phase boost an external feedforward capacitor C_{FF} can be added in parallel with R_{FBT}. C_{FF} is chosen such that phase margin is boosted at the crossover frequency without C_{FF}. A simple estimation for the crossover frequency without C_{FF} (f_x) is shown in the following equation, assuming C_{OUT} has very small ESR.

$$f_x = \frac{4.35}{V_{OUT} \times C_{OUT}} \quad (10)$$

Indicates that the crossover frequency is geometrically centered on the zero and pole frequencies caused by the C_{FF} capacitor. A 330 pF COG capacitor will be sufficient for the given parameters.

$$C_{FF} = \frac{1}{2\pi f_x} \times \frac{1}{\sqrt{R_{FBT} \times \left(\frac{R_{FBT}}{R_{FBB}}\right)}} \quad (11)$$

8 Test Data

The test data in this section only applies to the parameters mentioned in this document for alternative configuration it is recommended to review the datasheet of the cited devices.
This section provides test results for the LP5907-Q1.

8.1 Test Equipment

The following table shows the test equipment used in the upcoming sections.

Table 15 Test equipment

Test equipment	Part number
Oscilloscope	Agilent DPO4014B
Linear voltage supply	Agilent E3631A
Multimeter	Agilent E34401A
Network Analyzer	Agilent E5061B ENA

8.2 Power Supply Ripple Rejection

The output voltage ripple rejection ratio is calculated by comparing the regulated output voltage of the LP5907-Q1 with the input voltage ripple over a frequency range of 10Hz to 10MHz.

Test parameters:
$C_{IN} = C_{OUT} = 1\mu F$
$V_{IN} = V_{OUT} + 1V$
V_{IN_AC} = Sweep from 10Hz to 1MHz
Room Temperature = 25° C
EN pin tied to V_{IN}

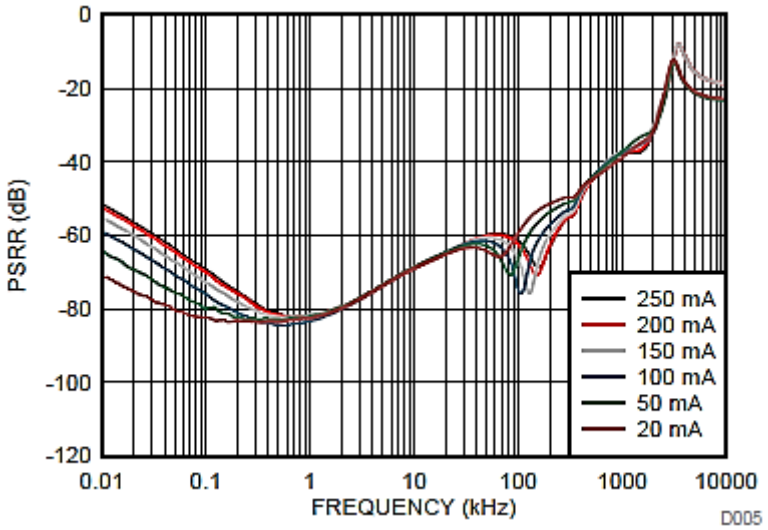


Figure 6 Power Supply Ripple Rejection

Figure 7 shows the clean regulated output voltage of the LP5907 when a ripple voltage of 50mV +3.3V_{DC} signal is applied at the LP5907 input pin.

V_{IN_DC} = V_{EN} = 3.3 V
V_{IN_AC} = 50 mV_{P-P} at 3 MHz

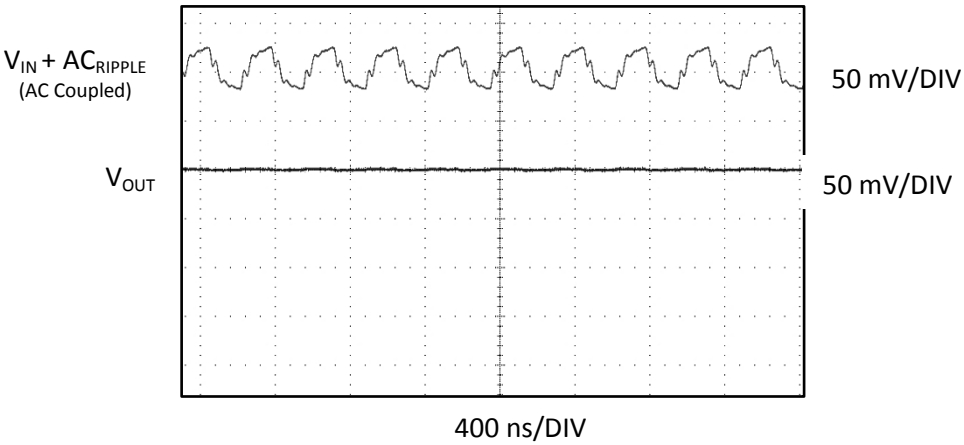


Figure 7 Input voltage ripple versus regulated V_{OUT}

8.3 Noise density

Output noise voltage is the root mean square (RMS) output noise voltage over a given range of frequencies (10 Hz to 100 kHz) under the conditions of a constant output current and a ripple-free input voltage.

The graph below shows the output noise at various load conditions.

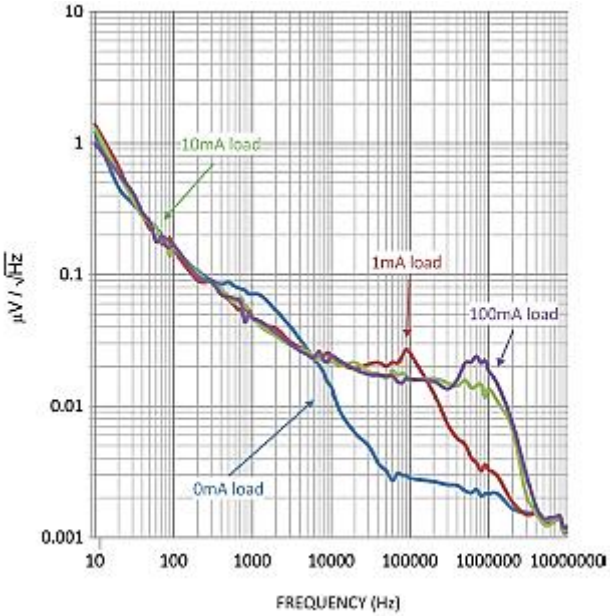


Figure 8 Noise Density

8.4 Line Transient and Regulation

The LP5907-Q1 line regulation test is defined as the change in output voltage from nominal value resulting from a change in input voltage.

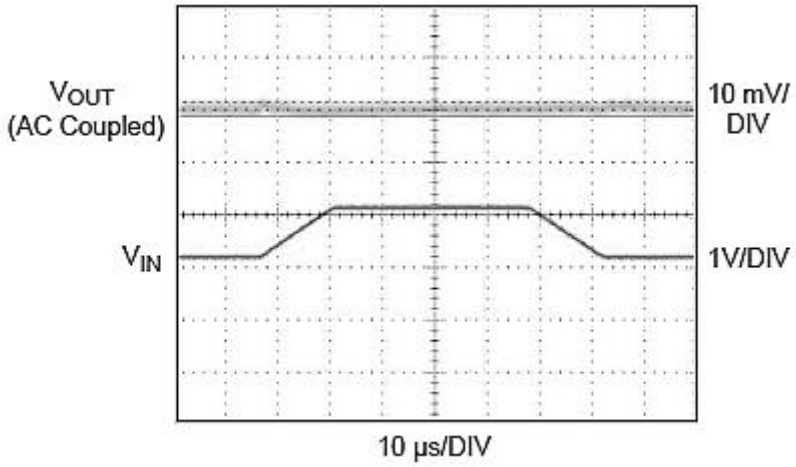


Figure 9 Line Transient Regulation

8.5 Load transient test

Load transient regulation is defined as the change in output voltage from nominal value as the load current suddenly increases.

8.5.1 Load Transient/Regulation LP5907_1.5

Test parameters

v_{OUT} = 1.5V
v_{IN} = 3.3V
C_{IN} = C_{OUT} = 1 µF
Room Temperature

Load delta = 0 mA ←→ 250 mA

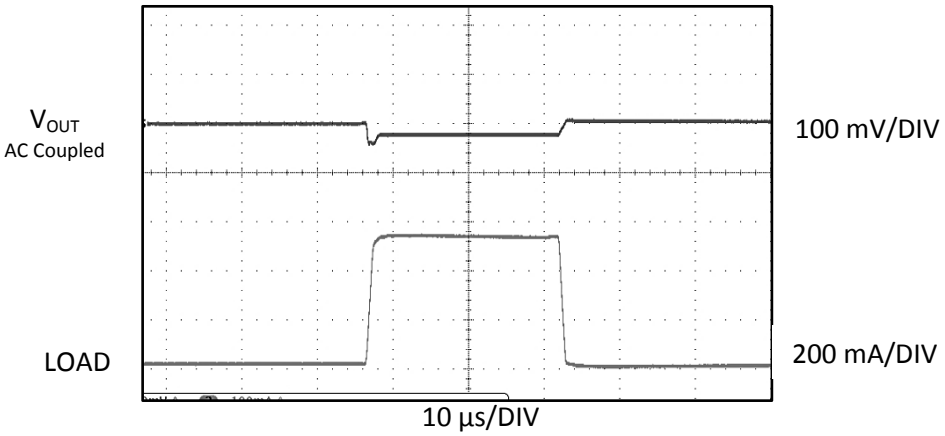


Figure 10 LP5907-Q1_1.5 Load Transient

8.5.2 Load Transient/Regulation LP5907-Q1_1.8

Test parameters

v_{OUT} = 1.8V
v_{IN} = 3.3V
C_{IN} = C_{OUT} = 1 µF
Room Temperature

Load = 0 mA ←→ 250 mA

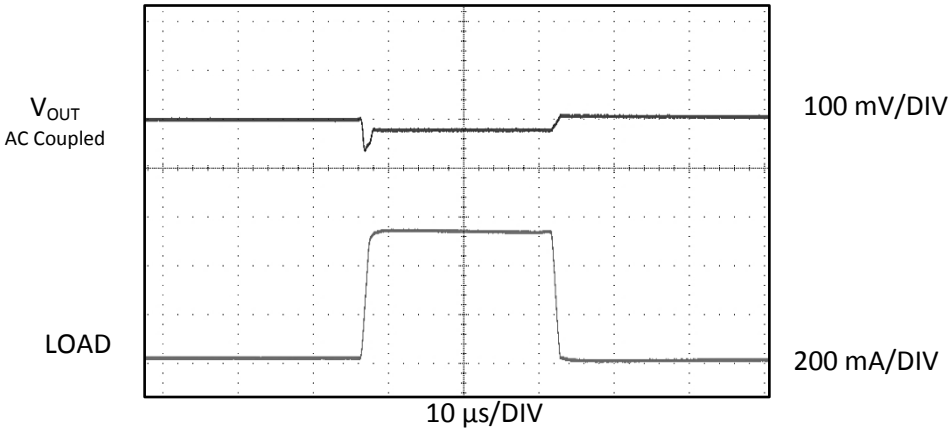


Figure 11 LP5907-Q1_1.8 Load Transient

8.5.3 Load Transient/Regulation LM43602-Q1

Test parameters

V_{IN} = 12V
V_{OUT} = 3.3V
F_S = 500 kHz
I_{Load} = 0 A ←→ 1A

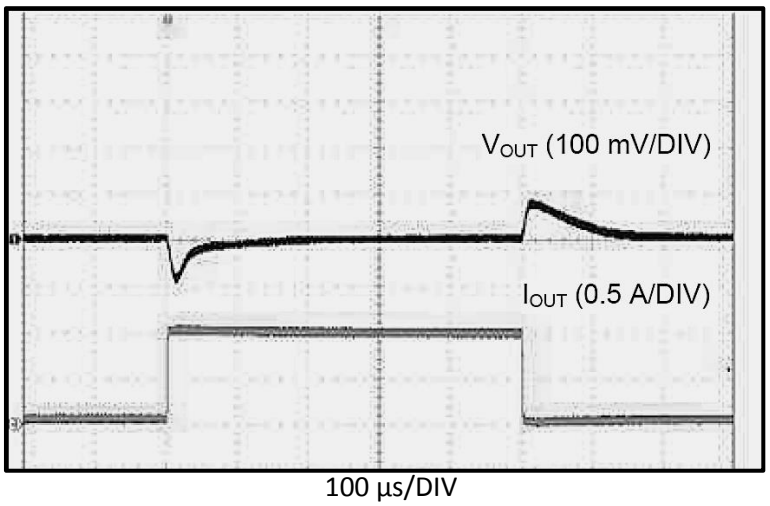


Figure 12 LM43602-Q1 Load Transient

8.6 Power up

The LP5907-Q1 takes about 60 µs from zero voltages to reach 90% of the nominal output voltage.

Test parameters:

$C_{IN} = C_{OUT}$ = 1µF
$V_{IN} = V_{OUT}$ + 1V

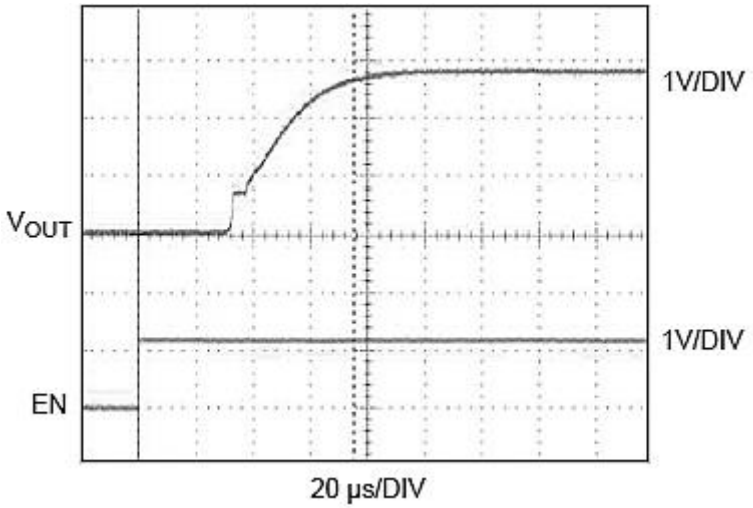


Figure 13 LP5907-Q1 power up timing

8.7 LM43602 Efficiency

Whit a load of 1A and 12V input and 5V output the LM43602-Q1 has an efficiency of 94% at room temperature.

Test parameters

v_{OUT} = 12V
v_{IN} = 5V
Switching frequency = 500 KHz
Room Temperature

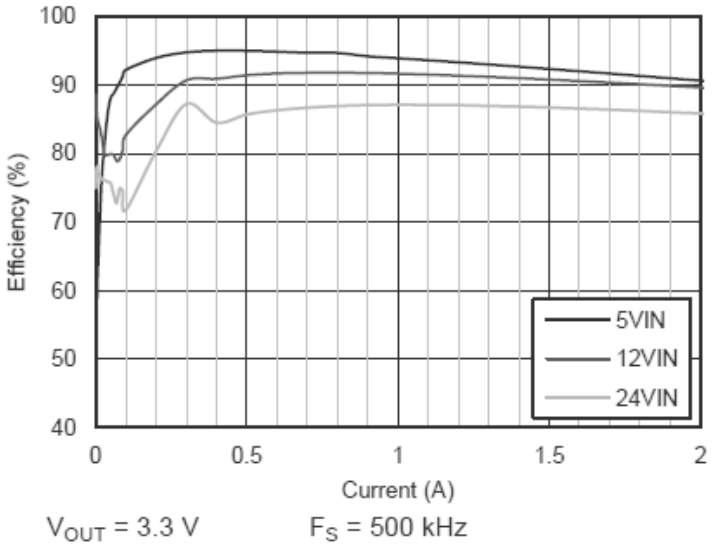


Figure 14 Efficiency at Room Temperature

9 Design Files

9.1 Schematics

To download the Schematics for each board, see the design files at http://www.ti.com/tool/TIDA-00535

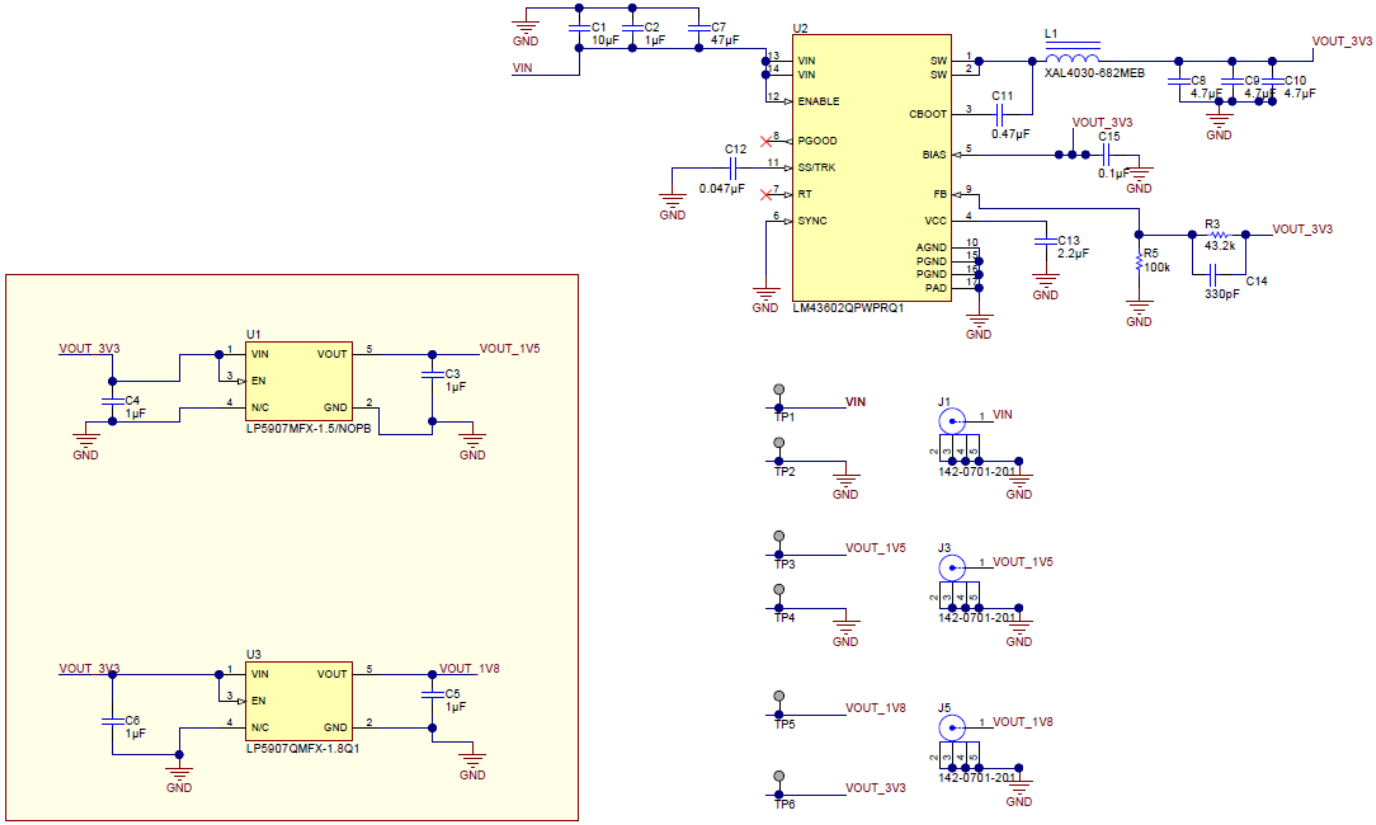


Figure 15 TIDA-00535 Schematic

9.2 Bill of Materials

To download the Bill of Materials, see the design files at http://www.ti.com/tool/TIDA-00535

Note: The Integrated circuits in this design are available in Automotive AEC Q100 Qualified Grade 1. All passives and other components selected in this design may not be qualified for automotive applications. The user is required to verify that all components in the design meet the qualification and safety requirements for their specific application.

9.3 Layout Guidelines

9.3.1 LM43602-Q1

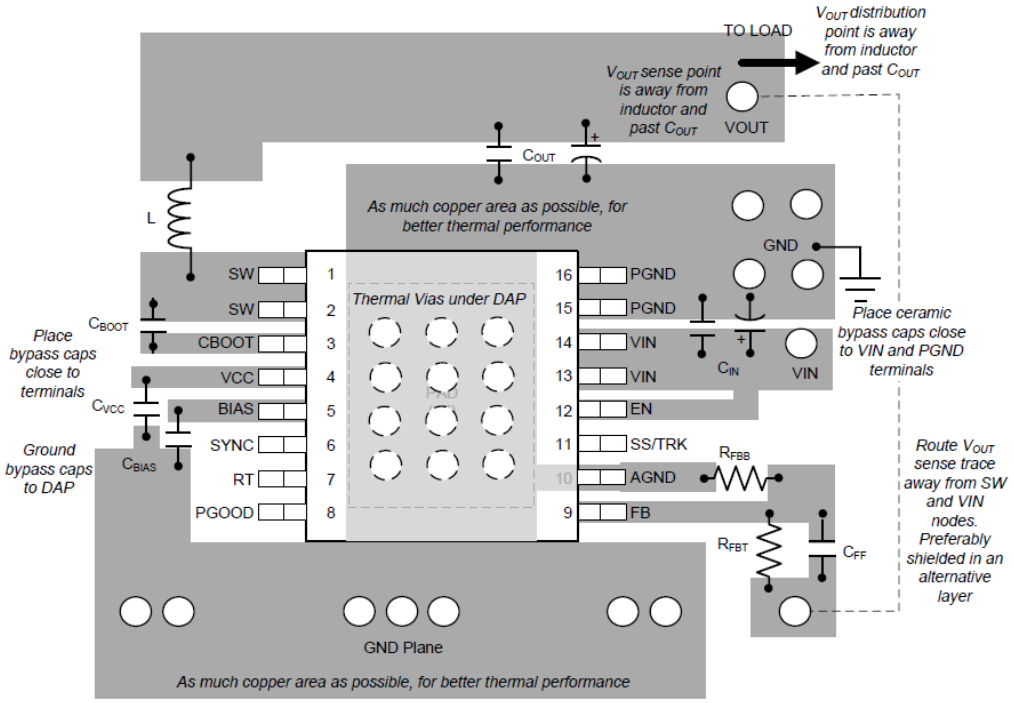


Figure 16 LM43602-Q1 Layout Guidelines

- Place ceramic high frequency bypass C_{IN} as close as possible to the LM43602-Q1 VIN and PGND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the PGND pins and PAD.
- Place bypass capacitors for VCC and BIAS close to the pins and ground the bypass capacitors to device ground.
- Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB} should be located close to the FB pin. Place Cff directly in parallel with R_{FBT}. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shieldig layer.
- Use ground plane in one of the middle layers as noise shielding and heat dissipation path.
- Have a single point ground connection to the plane. The ground connections for the feedback, soft-start, and enable components should be routed to the ground plane. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
- Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
- Provide adequate device heat-sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

9.3.2 LP5907

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5907, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP5907 ground pin using as wide, and as short, of a copper trace as is practical.
Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions

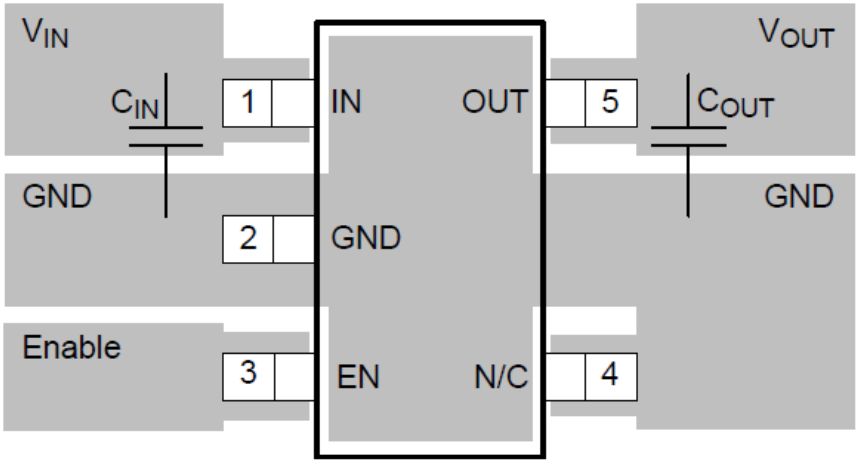


Figure 17 LP5907 Layout Guidelines

9.4 PCB Design Files

To download the PCB design files, see the design files at
http://www.ti.com/tool/TIDA-00535

- Gerber's and NC drills
- Layers prints

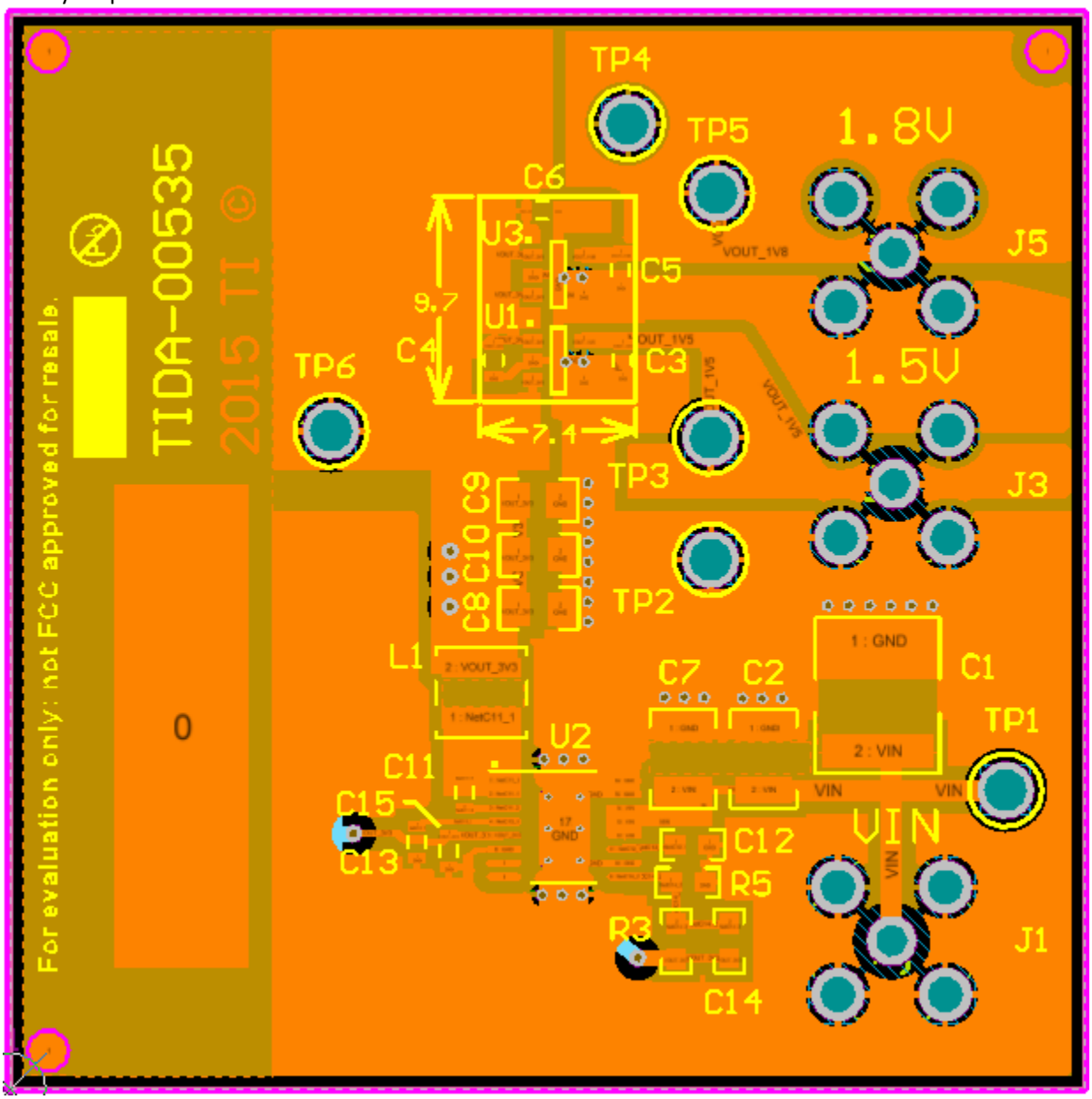


Figure 18 TIDA-00535 Top Layer Print

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11 Terminology

TI Glossary: SLYZ022 This glossary lists and explains terms, acronyms, and definitions.

12 About the Author

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