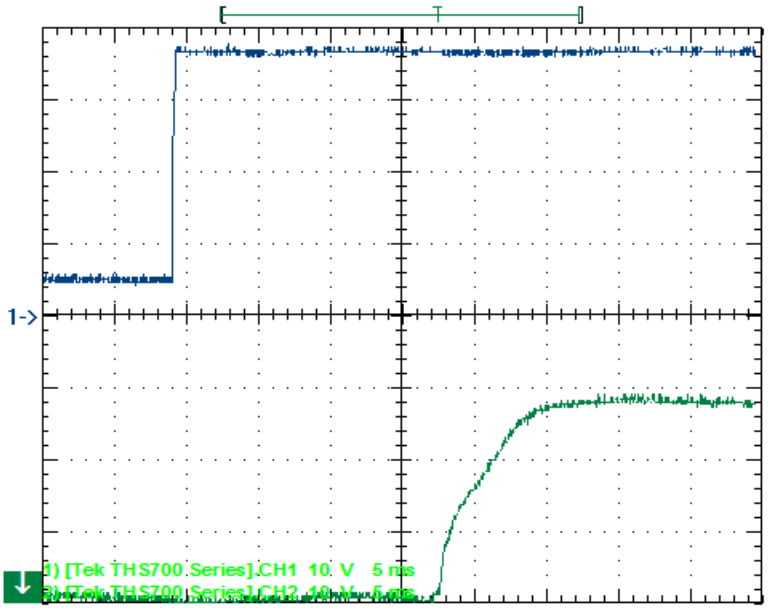
PMP10202RevB Test Results

Topology: Active Clamp Forward
Device: UCC2897A
Unless otherwise mentioned the measurements were done with about 2A output current.

This design is dedicated to a RF application – design topic is low reflected ripple and low output ripple. So the converter itself is powered across a differential input filter, the output filter uses ceramics only. Due to constant load the output capacitance is pretty low, but fully sufficient for constant current. A minimum load >100mA is required to ensure BIAS power.

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set to 36V.



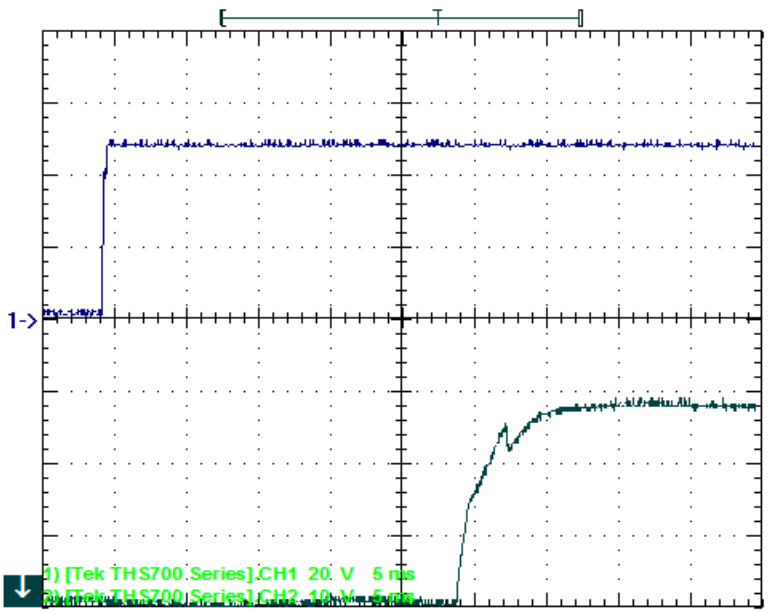
Ch1=> input voltage 10V/div

Ch2=> output voltage 10V/div

5ms/div

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set to 48V.



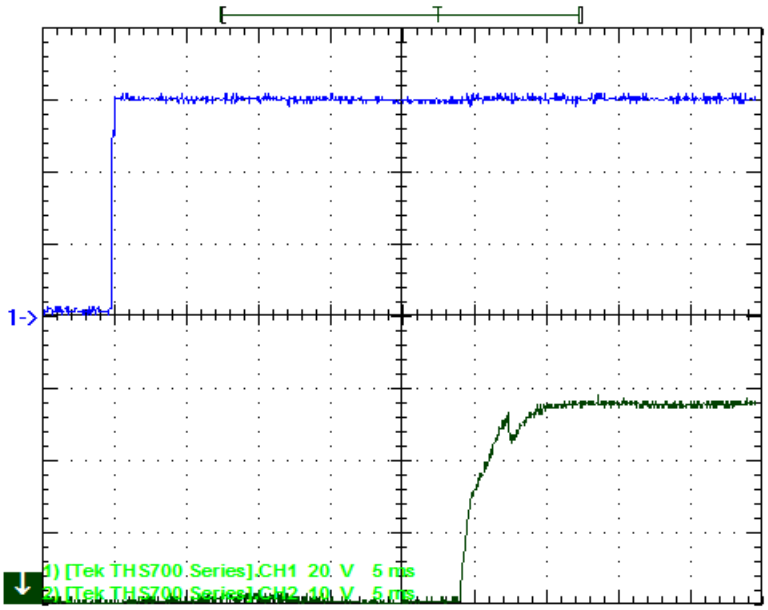
Ch1=> input voltage 20V/div

Ch2=> output voltage 10V/div

5ms/div

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set to 60V.



Ch1=> input voltage 20V/div

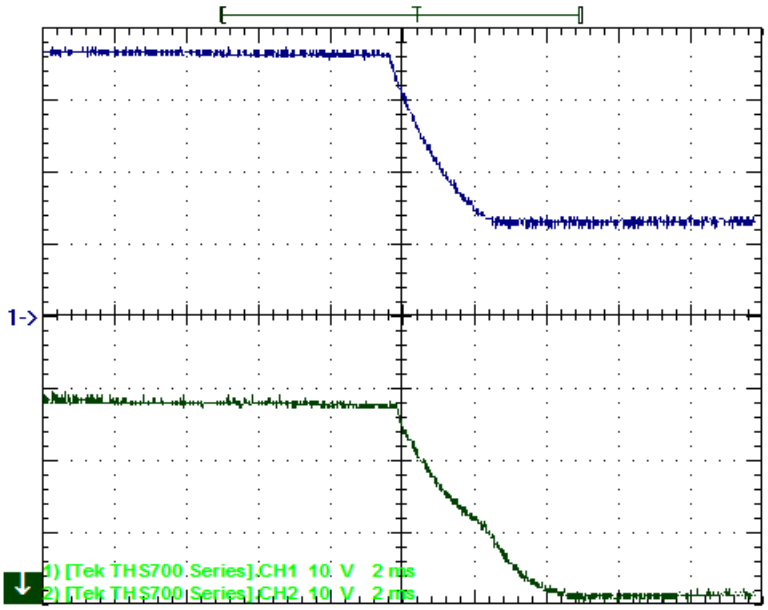
Ch2=> output voltage 10V/div

5ms/div

Figure 3

2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set to 36V. The power supply was disconnected.



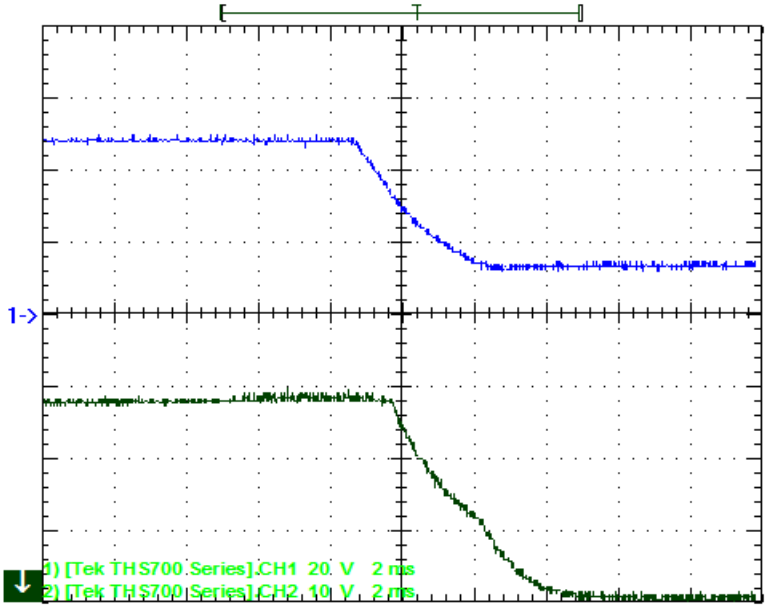
Ch1=> input voltage 10V/div

Ch2=> output voltage 10V/div

2ms/div

Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set to 48V. The power supply was disconnected.



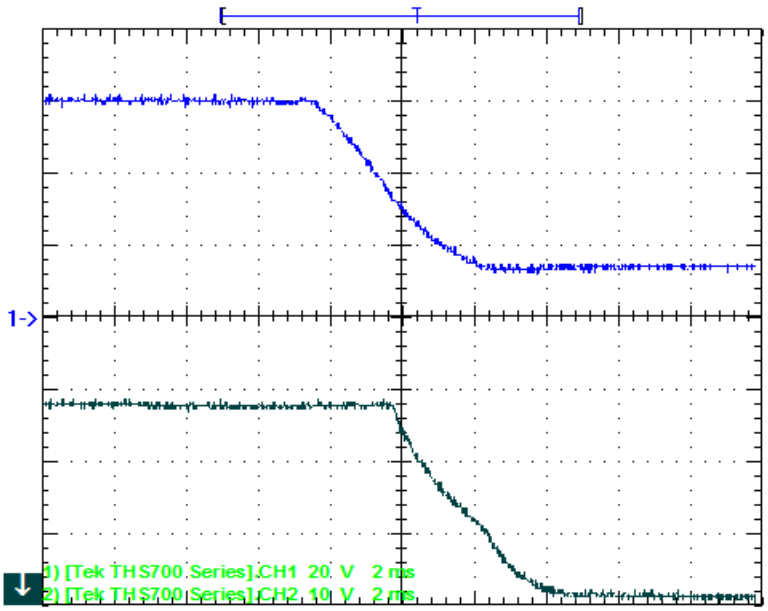
Ch1=> input voltage 20V/div

Ch2=> output voltage 10V/div

2ms/div

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set to 60V. The power supply was disconnected.



Ch1=> input voltage 20V/div

Ch2=> output voltage 10V/div

2ms/div

Figure 6

3 Efficiency

The efficiency curves are shown in the Figure 7 below. Measurements were done with resistor load. Inductor is MSS1210-224KE, suited up to 1.6Amps load.

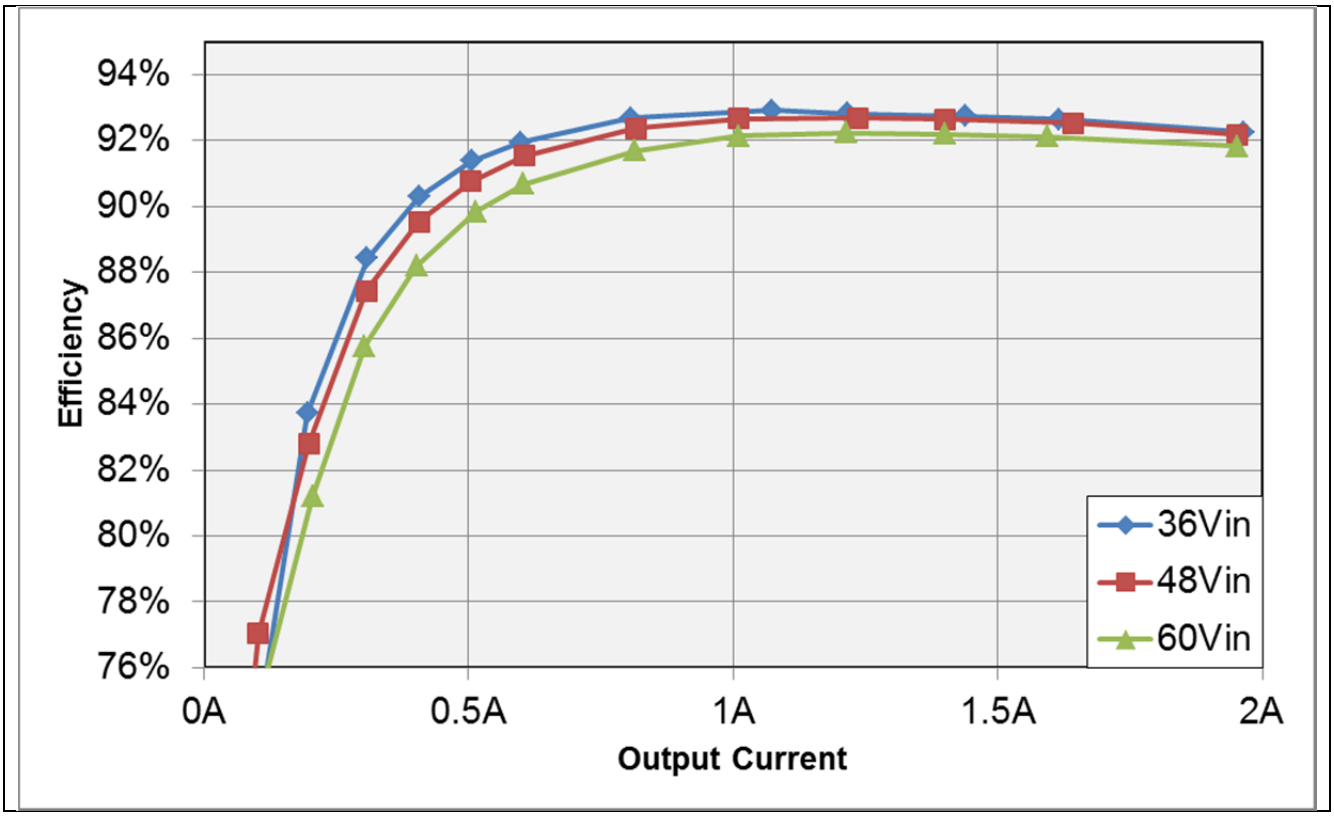


Figure 7

4 Load Regulation

The load regulation of the output is shown in the Figure 8 below. Measurements were done with resistor load.

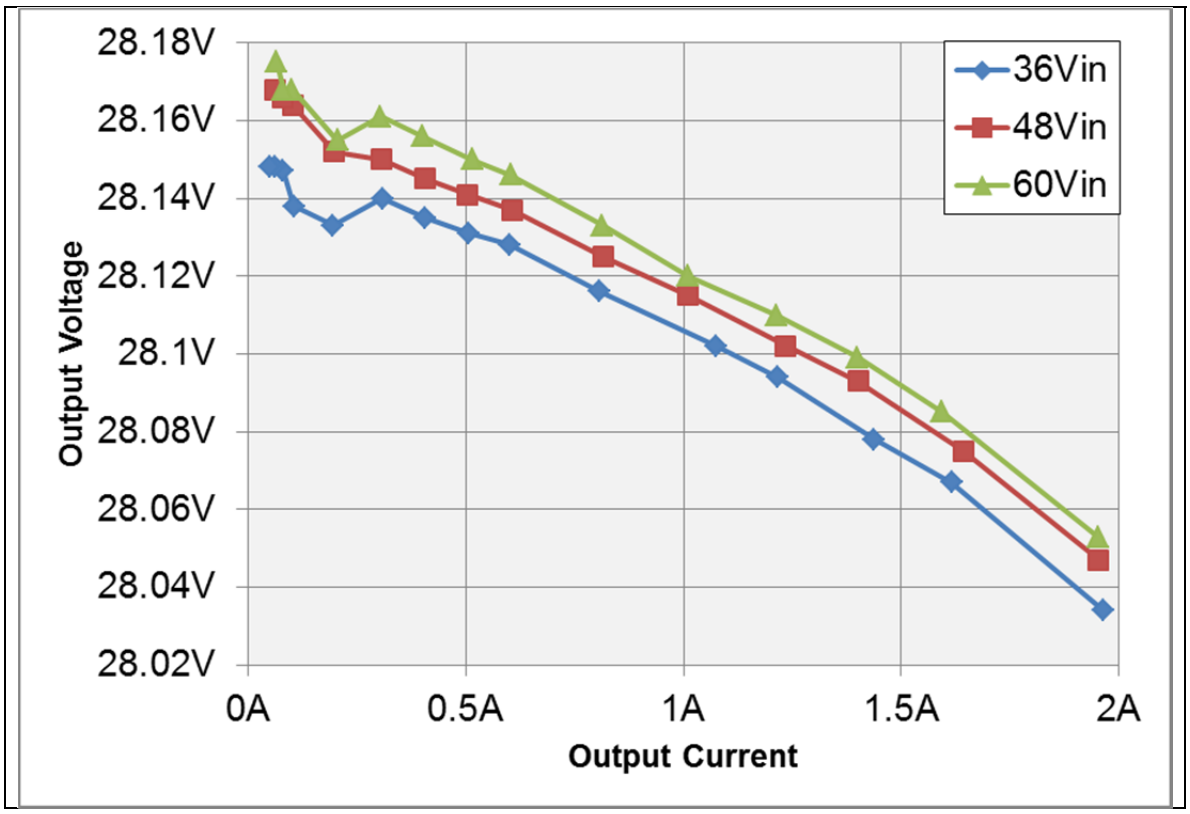


Figure 8

5 Line Regulation

The line regulation is shown in Figure 9. Measurements were done with electronic EL 100.

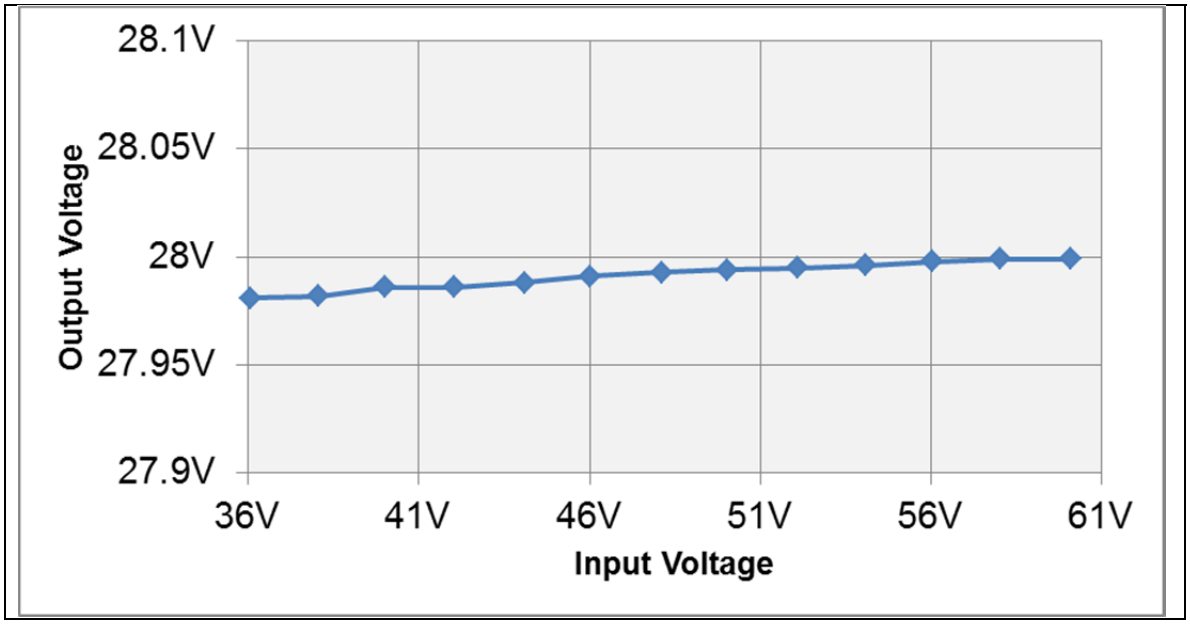


Figure 9

With the same setup the efficiencies are shown in Figure 10.

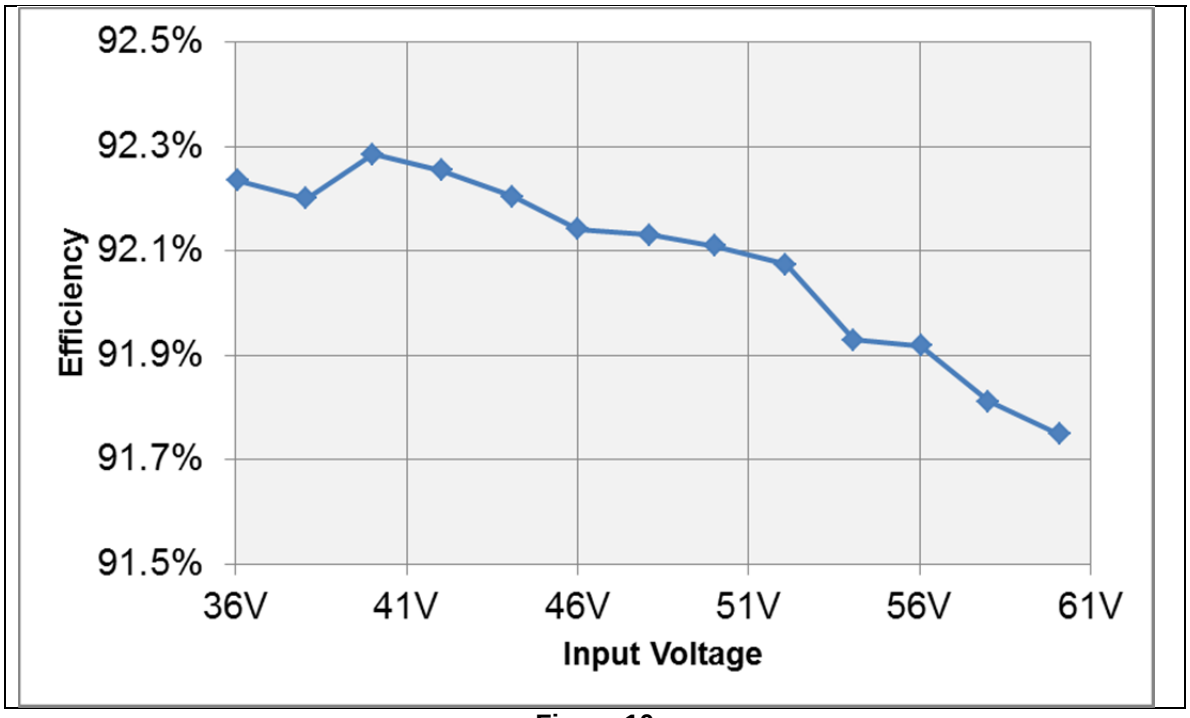
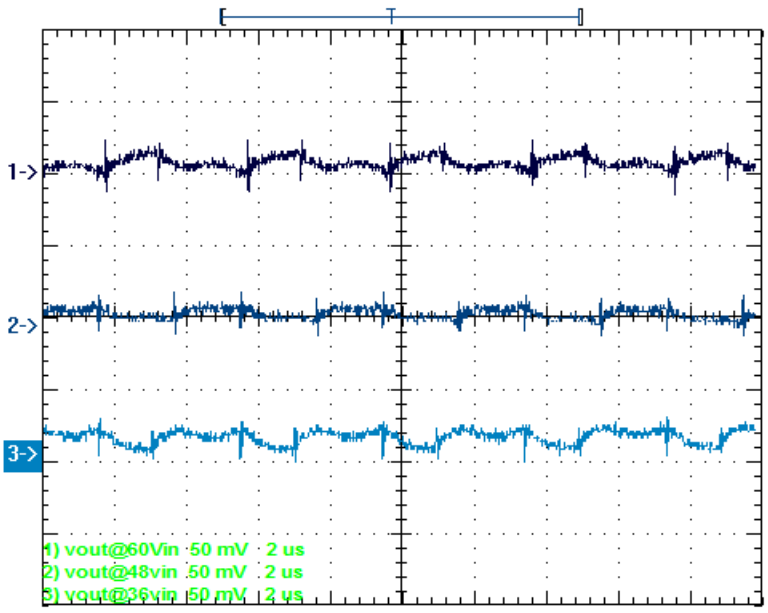


Figure 10

6 Output Ripple Voltage

The output ripple voltage (measured at J2 bottom side) is shown in Figure 11



Ch1 => output voltage@60Vin 50mV/div

Ch2 => output voltage@48Vin 50mV/div

Ch3 => output voltage@36Vin 50mV/div

AC coupled

20MHz bw

2µs/div

Figure 11

The output voltage ripple voltage is well below specified 100mVpp, here 40mVpp,
means only 0.14% for a 28V output.

The filtered reflected input voltage ripple is around 40mVpp, at the converter input close to 1Vpp; This, differential filter provides roughly an attenuation of 40mV/880mV, means -27dB.

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 12 (measured at J1 bottom side).

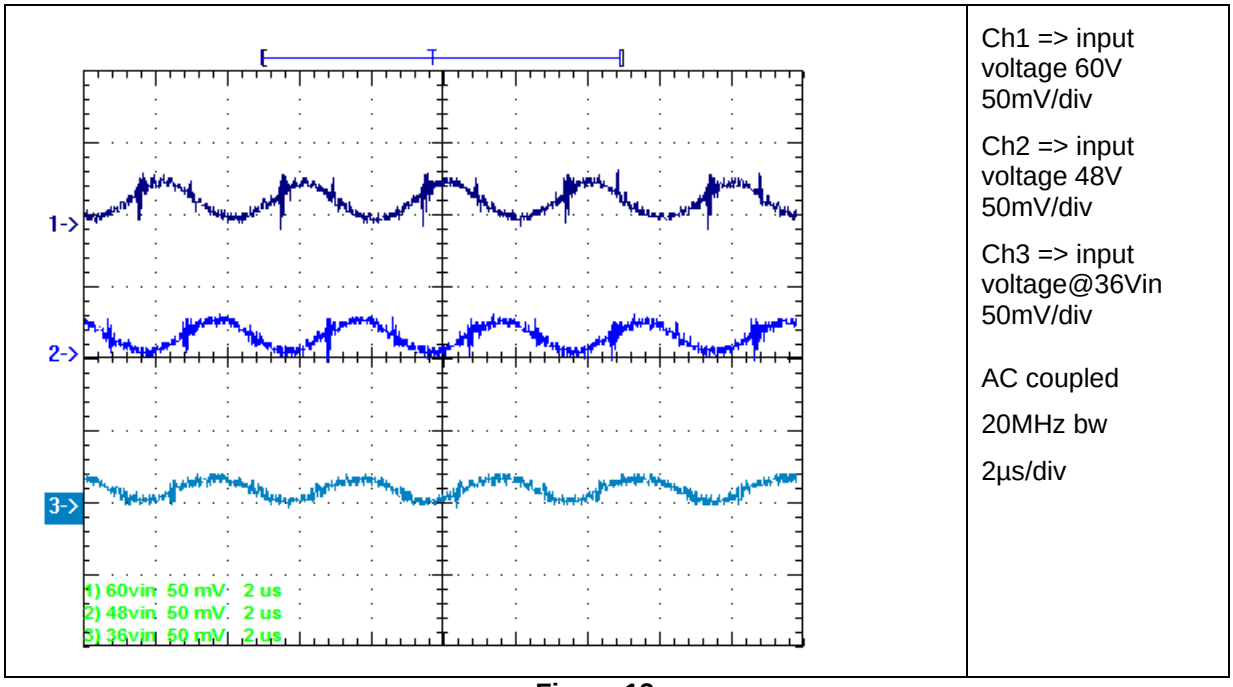


Figure 12

The input ripple voltage is shown in Figure 13 (measured near C9).

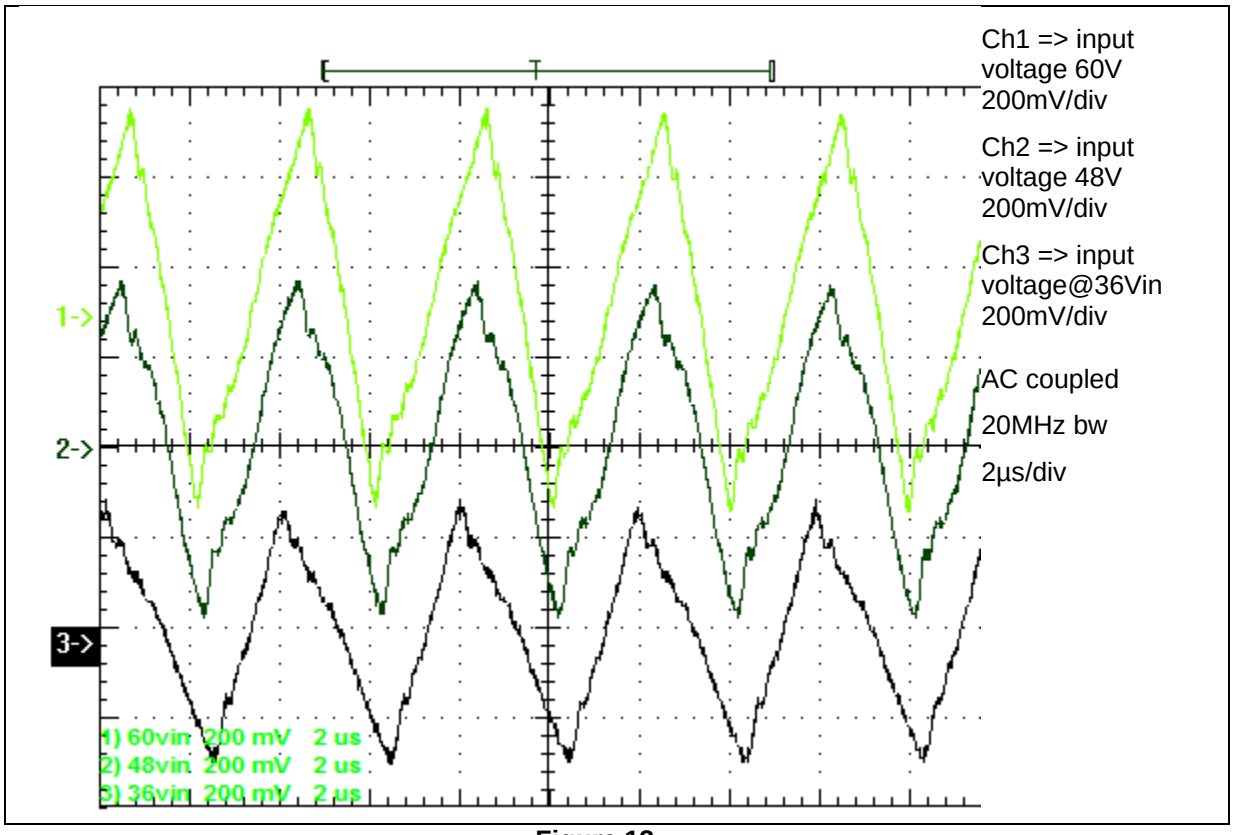
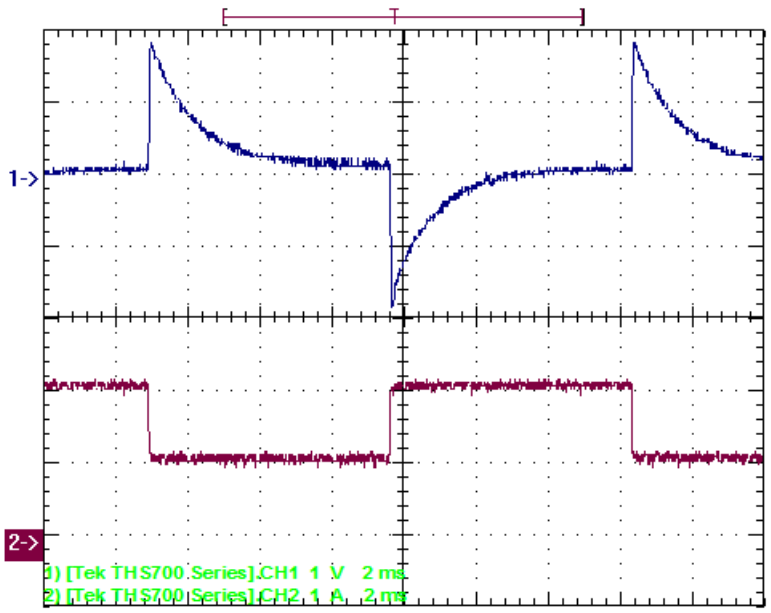


Figure 13

8 Load Transients

The Figure 14 shows the response to load transients. The load is switching from 1A to 2A with a frequency of 75Hz. The input voltage was set to 36V



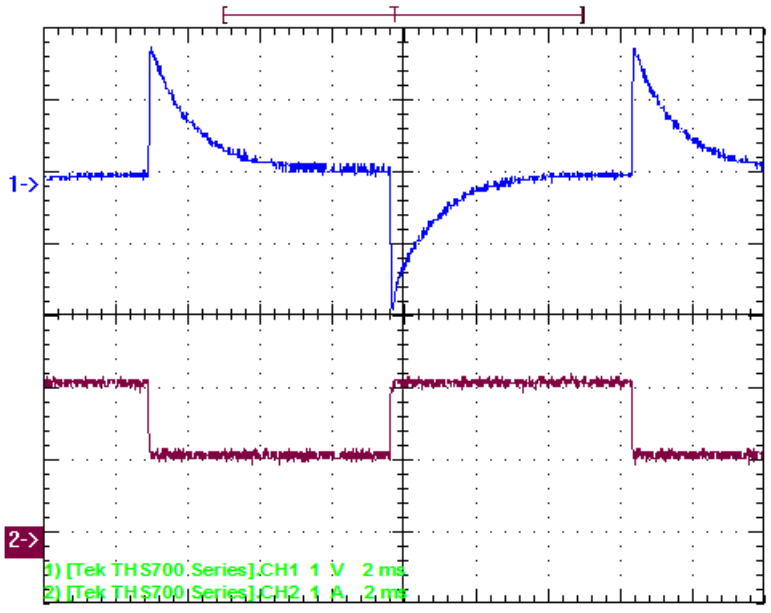
Ch1 => output voltage 1V/div

Ch2=> output current 1A/div

2ms/div

Figure 14

The Figure 15 shows the response to load transients. The load is switching from 1A to 2A with a frequency of 75Hz. The input voltage was set to 48V



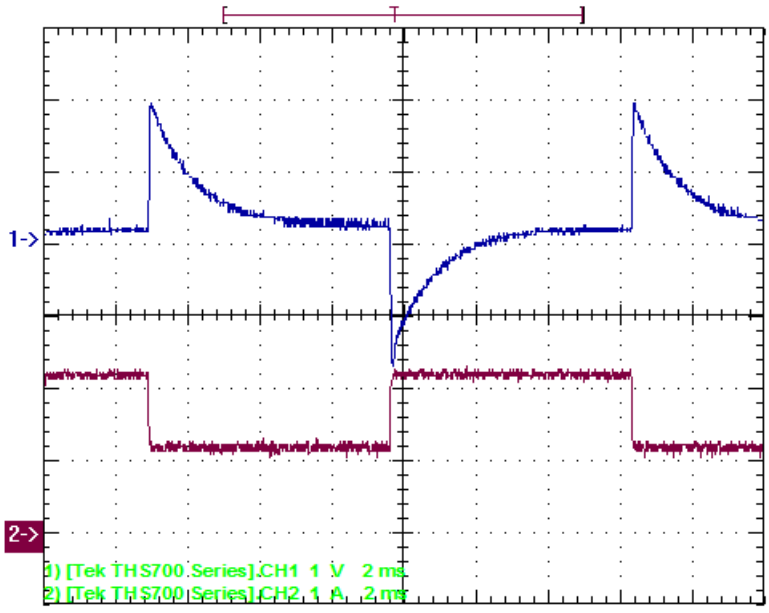
Ch1 => output voltage 1V/div

Ch2=> output current 1A/div

2ms/div

Figure 15

The Figure 16 shows the response to load transients. The load is switching from 1A to 2A with a frequency of 75Hz. The input voltage was set to 60V



Ch1 => output voltage 1V/div

Ch2=> output current 100mA/div

20MHz bandwidth setting

2ms/div

Figure 16

The converter itself is designed for CONSTANT load, transient response around du 2V for a transient di of 1A; this means a deviation of 7%.

For dynamic loads output capacitance needs to be increased and loop to be adjusted.

For loads <100mA BIAS needs to be changed from buck to peak detection or additional auxiliary power via diode ORing.

For continuous load >1.5A the output inductor needs a custom design (220uH, 2.5Arms, 3.0Asat, shielded, ferrite)

9 Control Loop Frequency Response

Figure 17 shows the loop response. 2A-load applied. The input voltage was set to 36V (Electronic load).

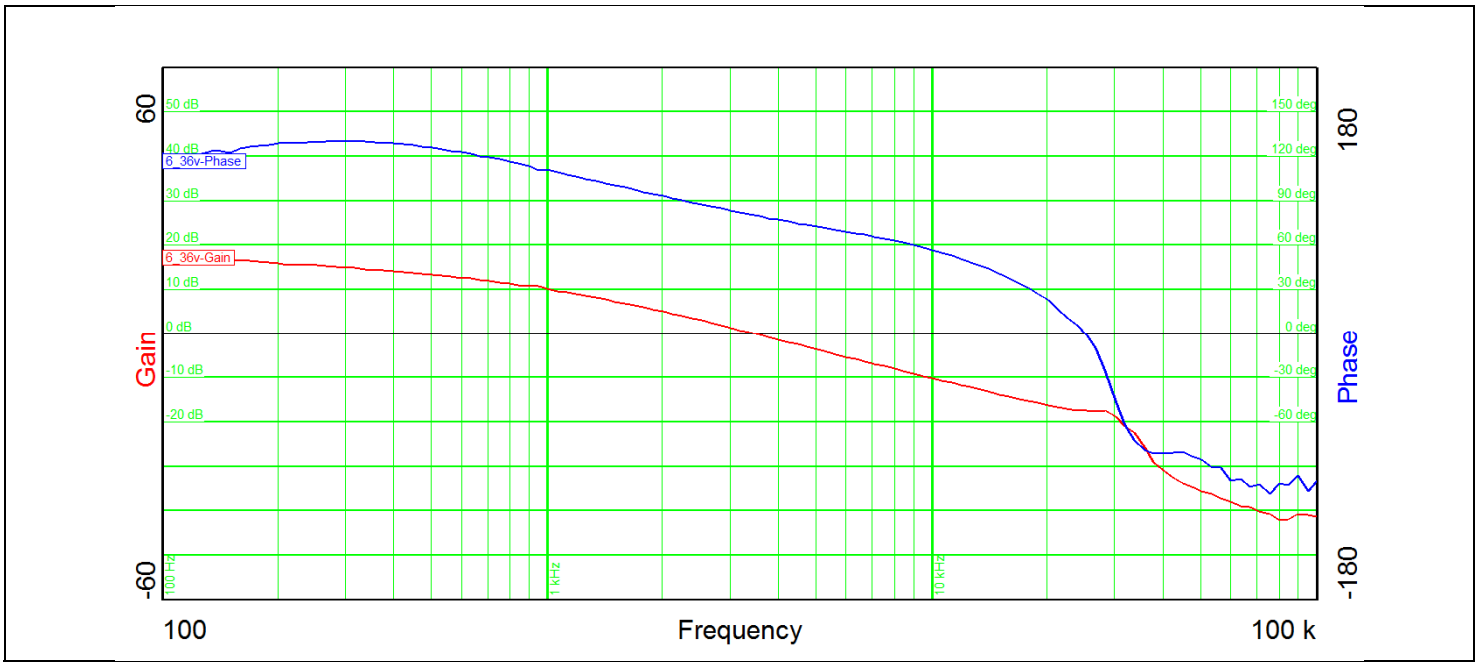


Figure 17

Figure 18 shows the loop response. 2A-load applied. The input voltage was set to 36V (resistor load)

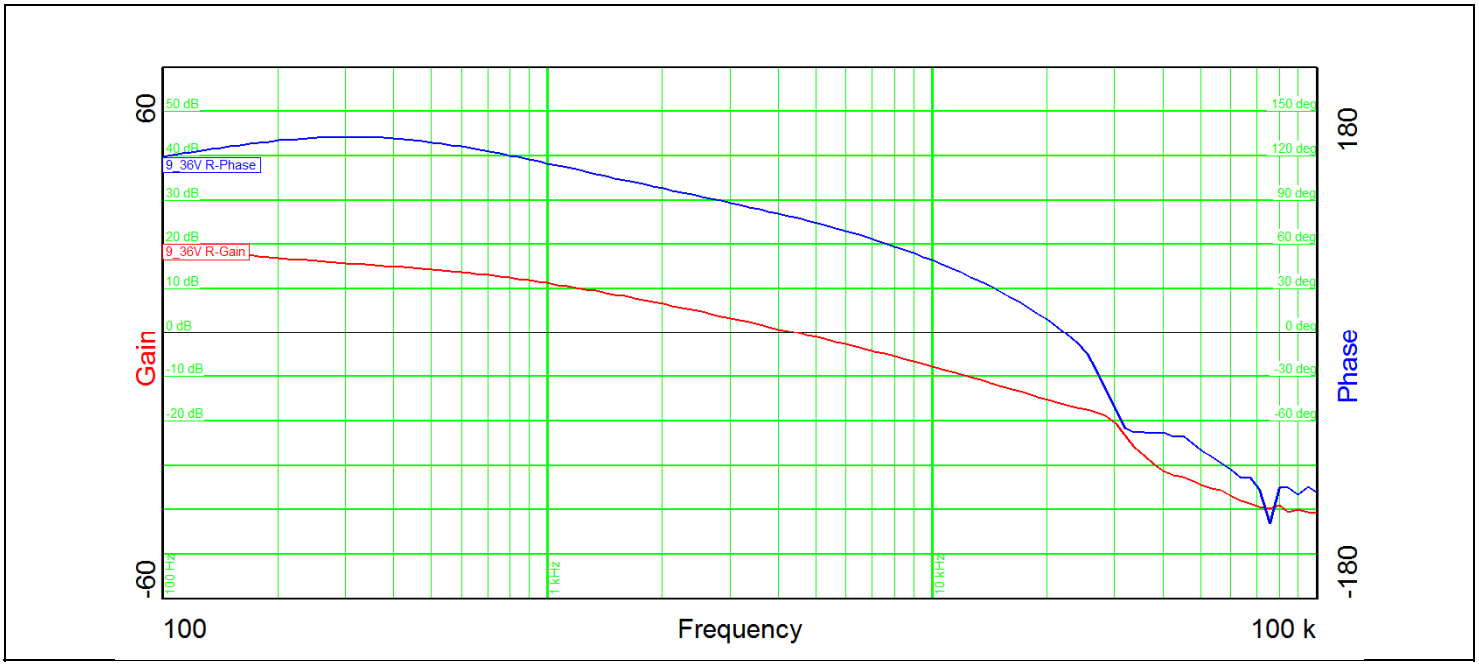


Figure 18

Figure 19 shows the loop response. 2A-load applied. The input voltage was set to 48V (Electronic load)

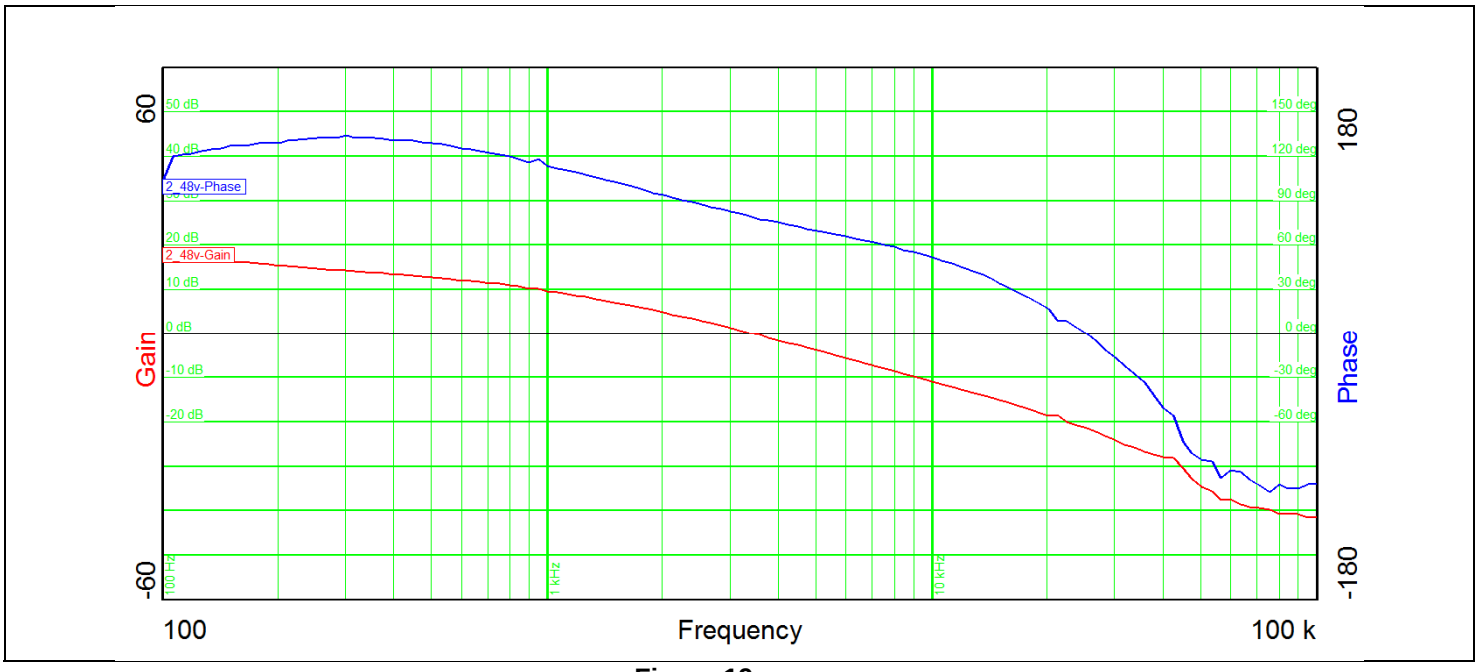


Figure 19

Figure 20 shows the loop response. 2A-load applied. The input voltage was set to 48V (resistor load).

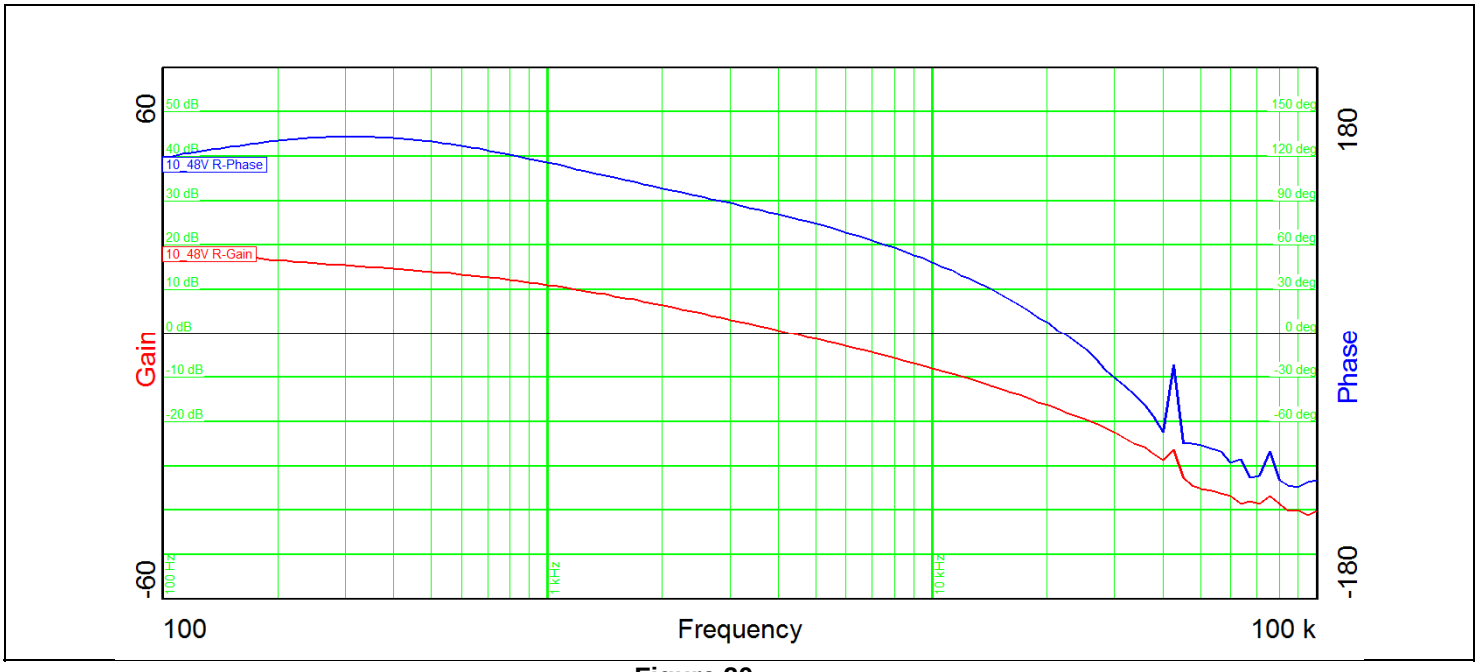


Figure 20

Figure 21 shows the loop response. 2A-load applied. The input voltage was set to 60V (Electronic load).

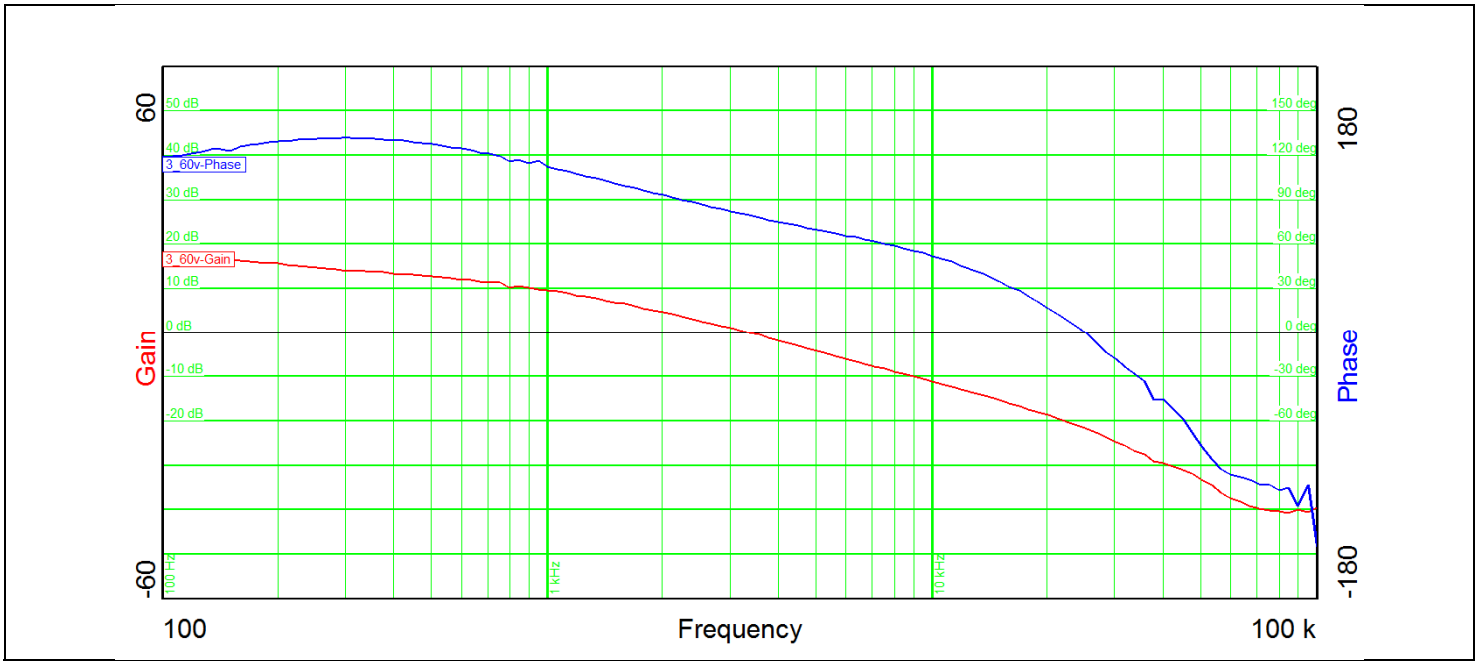


Figure 21

Figure 22 shows the loop response. 2A-load applied. The input voltage was set to 60V(resistor load).

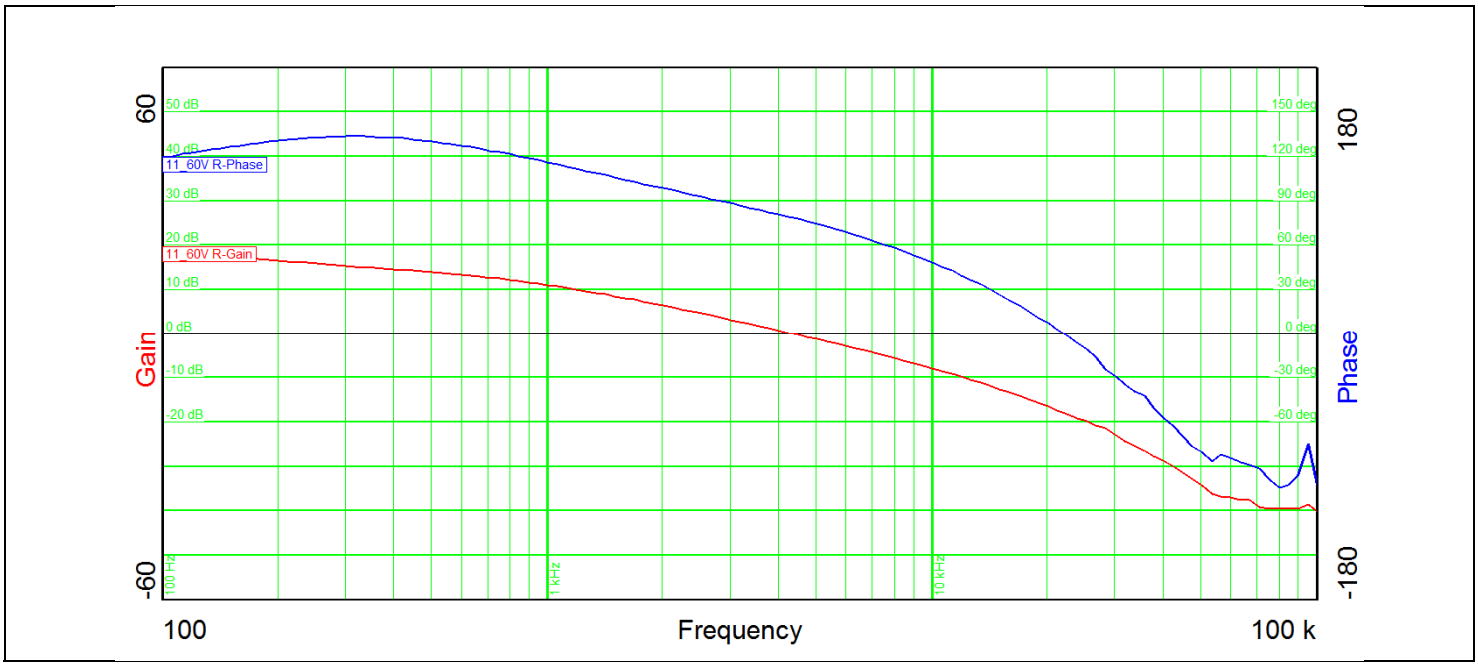


Figure 22

Table 1 summarizes the results from the frequency response measurements with electronic load.

Vin	36V	48V	60V
Bandwidth (kHz)	3.49	3.46	3.34
Phase margin	80°	79°	80°
slope (20dB/decade)	-1.15	-0.97	-1.17
gain margin (dB)	-17.5	-21.5	-21.7
slope (20dB/decade)	-0.35	-1.56	-1.54
freq (kHz)	24.9	25.2	25

Table 1

Table 2 summarizes the results from the frequency response measurements with resistor load.

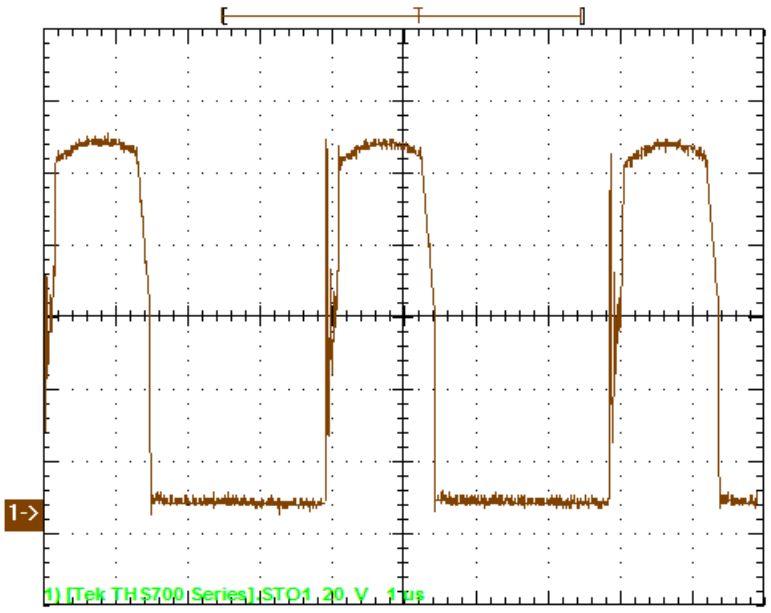
Vin	36V	48V	60V
Bandwidth (kHz)	4.43	4.36	4.36
Phase margin	78°	78°	78°
slope (20dB/decade)	-1.02	-1.02	-1.01
gain margin (dB)	-16.4	-17.6	-17.9
slope (20dB/decade)	-1.13	-1.7	-1.75
freq (kHz)	22.3	22	22

Table 2

10 Miscellaneous Waveforms

10.1 Input Voltage = 36V

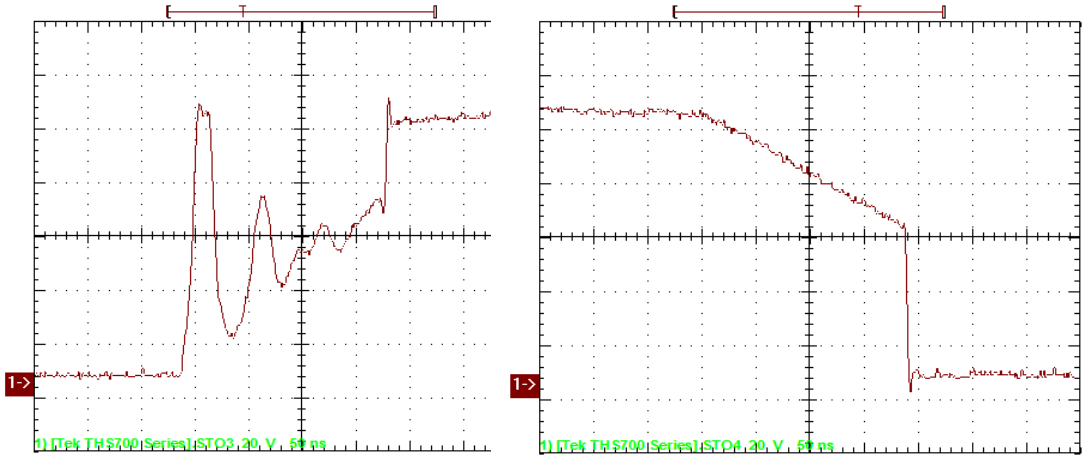
The waveform of the voltage on switchnode Q2 (drain-source) is shown in Figure 23.



Ch1 =>
20V/div

1µs/div

full bandwidth

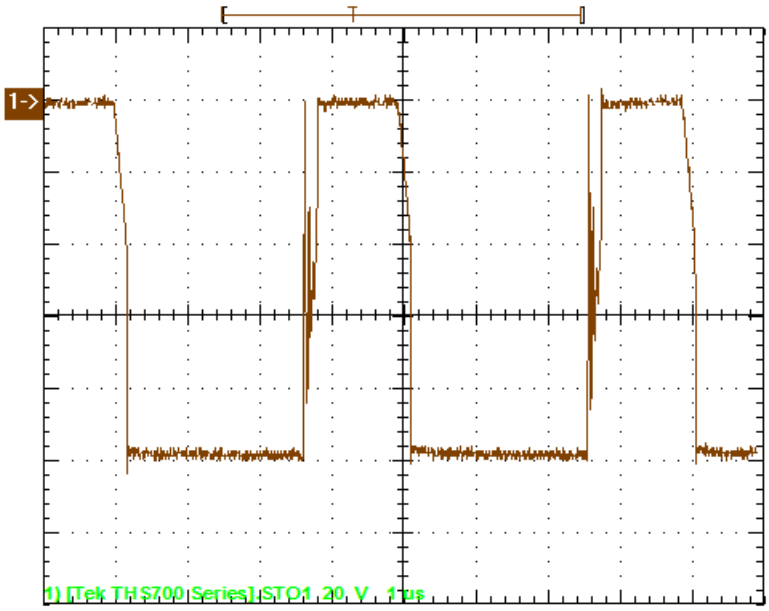


Ch1 =>
20V/div
50ns/div

Figure 23

Delay resistor RT of 2.2kOhm offers a shiny drain waveform – but less QR switching and less efficiency; screenshots are taken w/ RT of 16kOhm. Placing 2k55 to 16k in parallel and switching 2k55 shows the difference; 2k2 means hard switching.

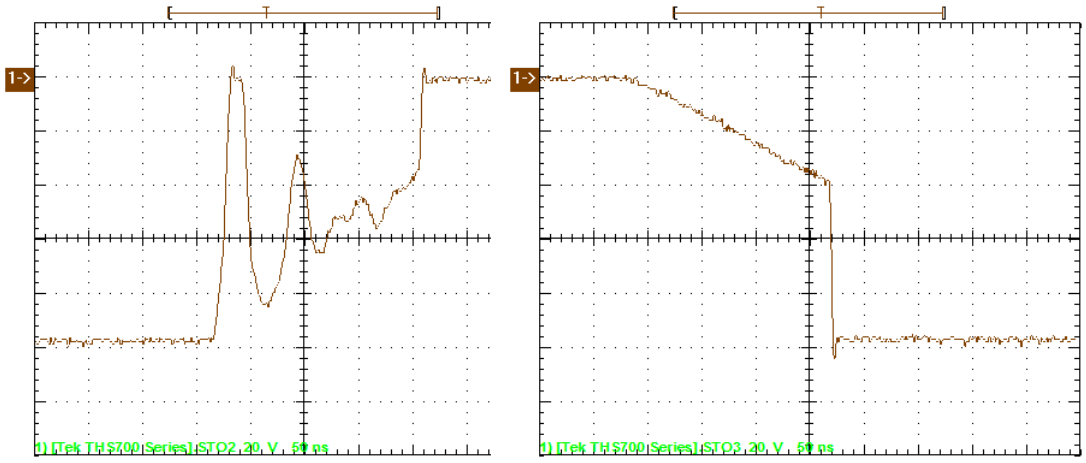
The waveform of the voltage on Q1 (PMOS) drain-source is shown in Figure 24.



Ch1 =>
20V/div

1µs/div

full bandwidth



Ch1 =>
20V/div
50ns/div

Figure 24

The waveform of the voltage at the transformer output is shown in Figure 25.

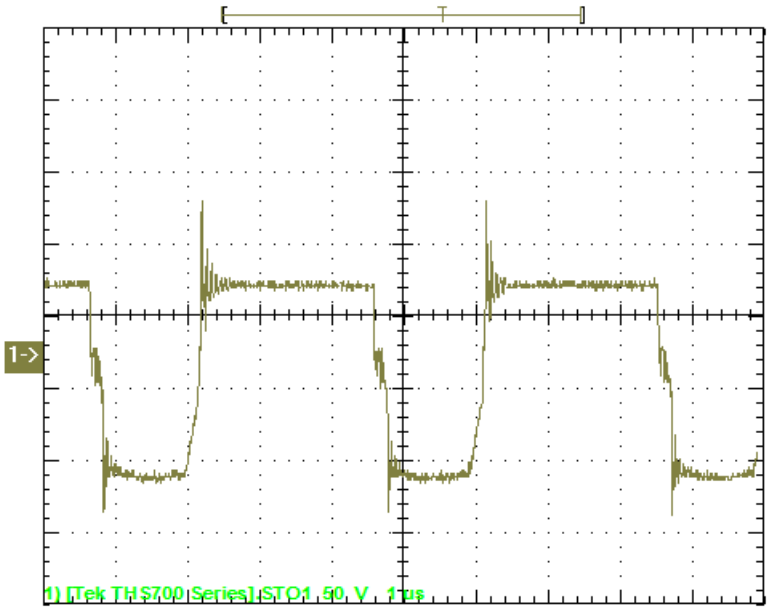
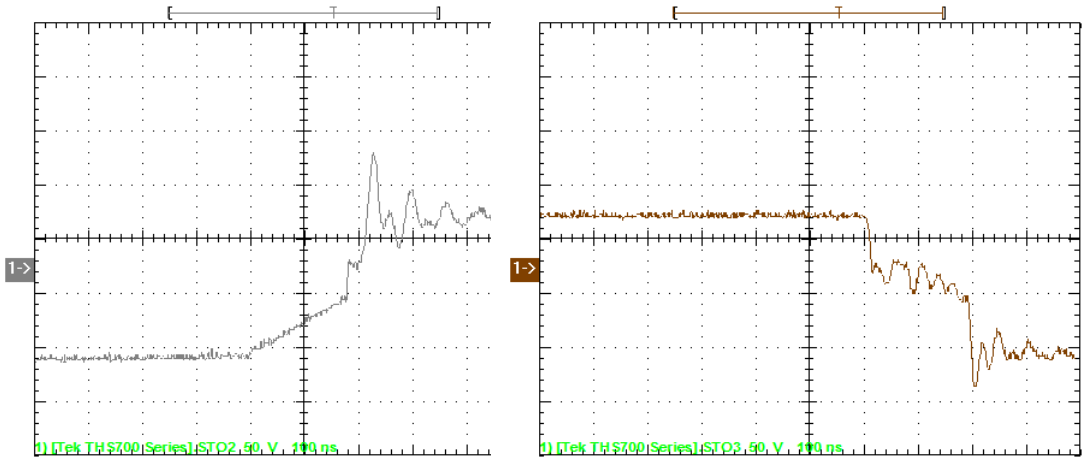
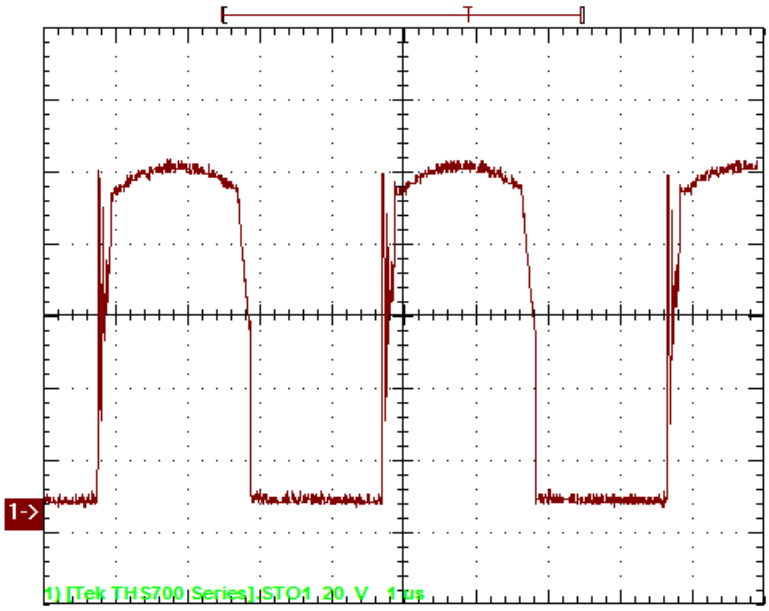
	Ch1 => 50V/div 1µs/div full bandwidth
	Ch1 => 50V/div 100ns/div

Figure 25

10.2 Input Voltage = 48V

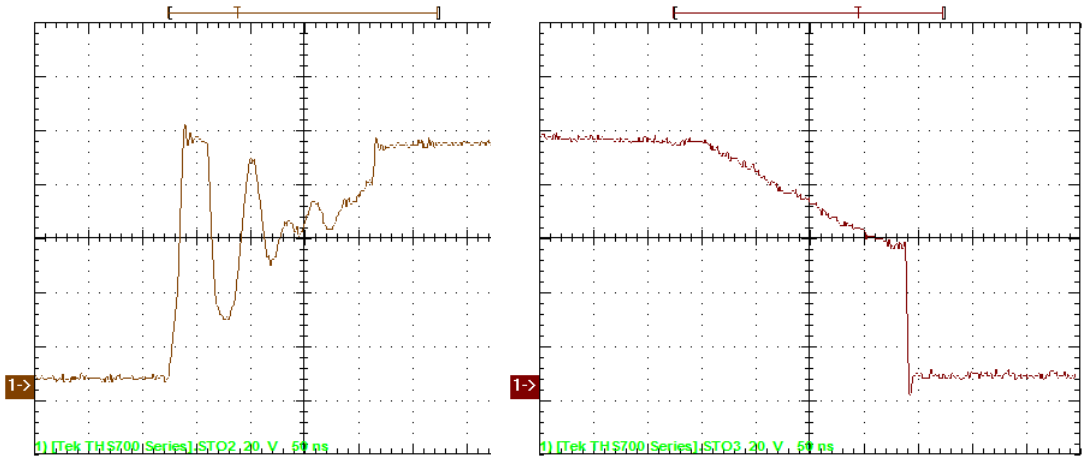
The waveform of the voltage on switchnode Q2 (drain-source) is shown in Figure 26.



Ch1 =>
20V/div

1µs/div

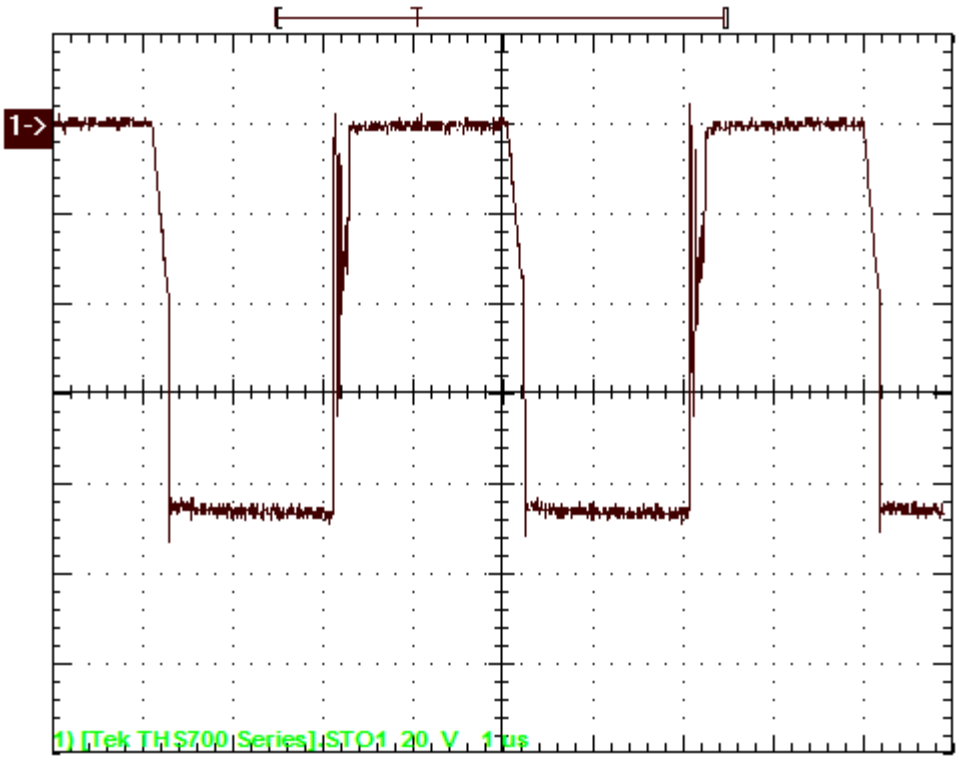
full bandwidth



Ch1 =>
20V/div
50ns/div

Figure 26

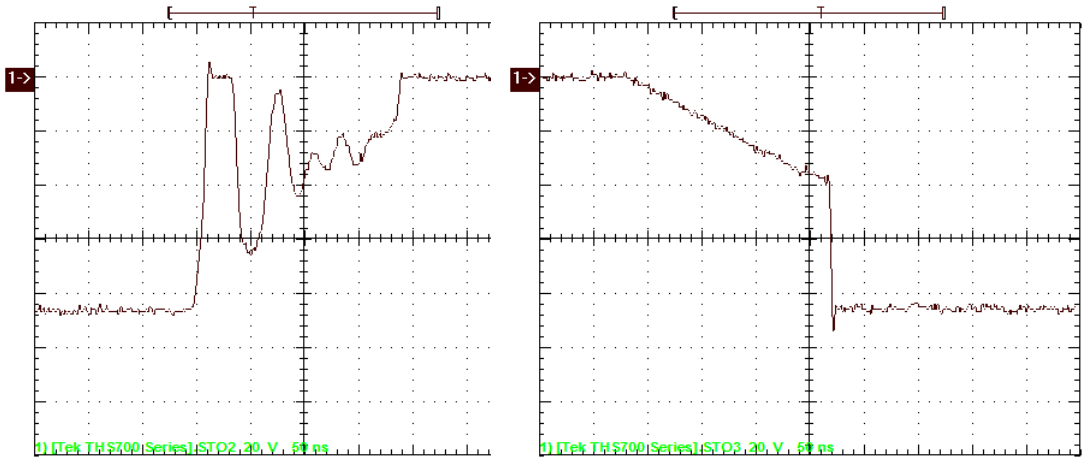
The waveform of the voltage on Q1 (PMOS) drain-source is shown in Figure 27.



Ch1 =>
20V/div

1µs/div

full bandwidth



Ch1 =>
20V/div
50ns/div

Figure 27

The waveform of the voltage at the transformer output is shown in Figure 28.

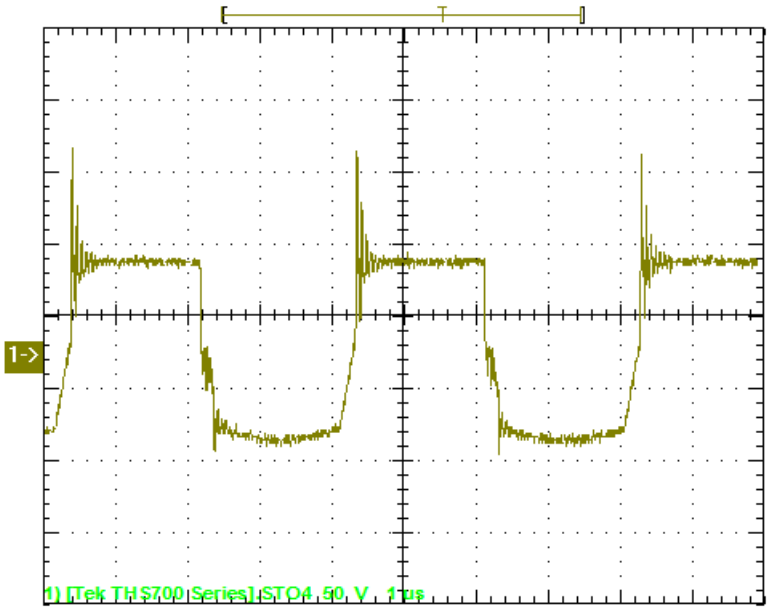
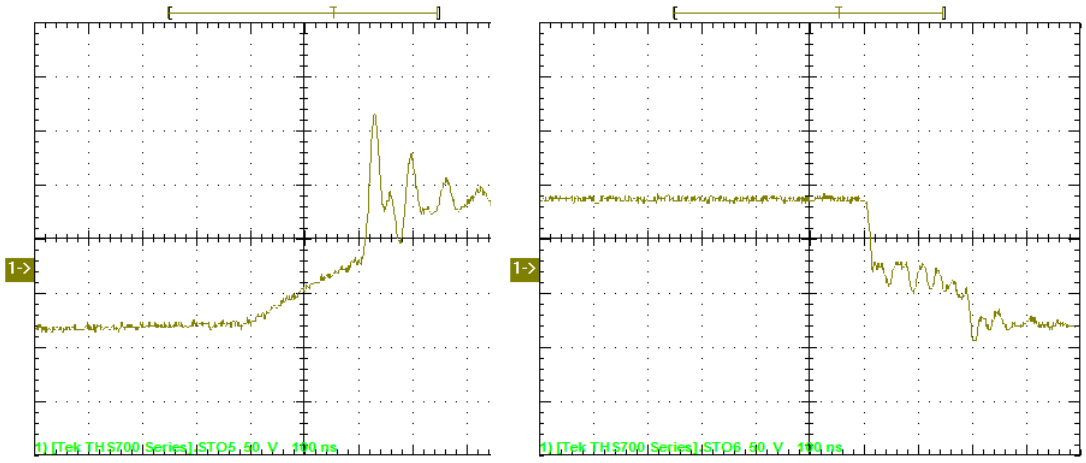
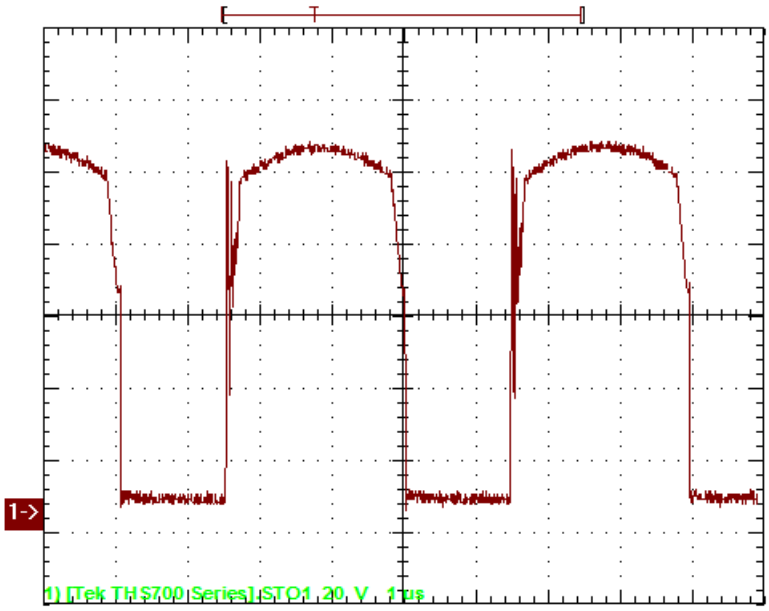
	Ch1 => 50V/div 1µs/div full bandwidth
	Ch1 => 50V/div 100ns/div

Figure 28

10.3 Input Voltage = 60V

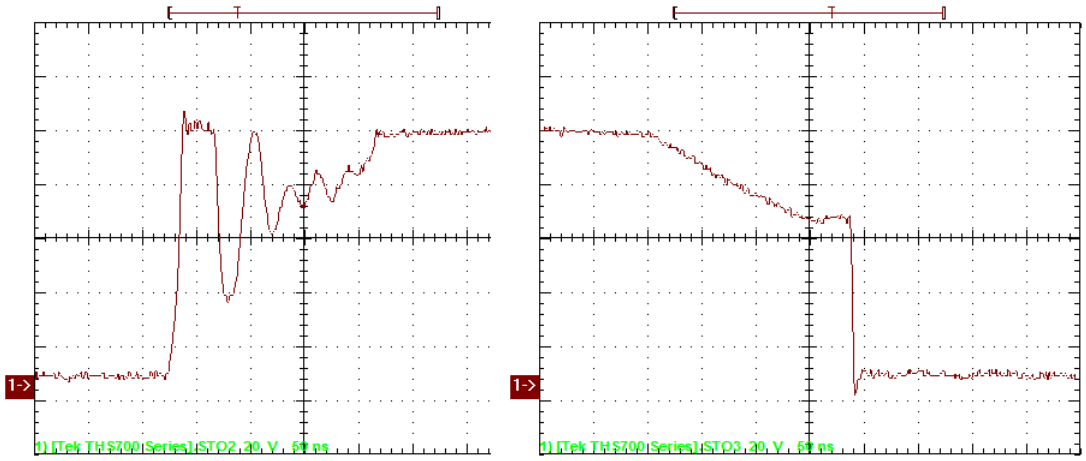
The waveform of the voltage on switchnode Q2 (drain-source) is shown in Figure 29.



Ch1 =>
20V/div

1µs/div

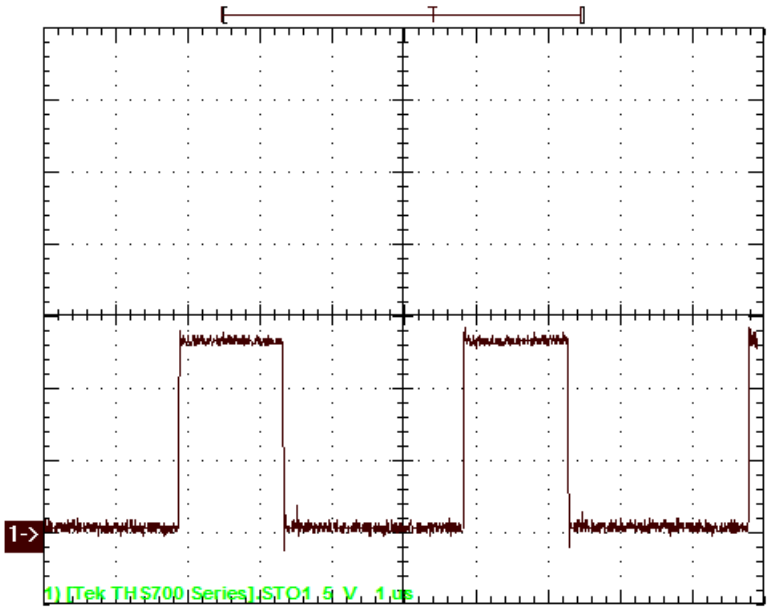
full bandwidth



Ch1 =>
20V/div
50ns/div

Figure 29

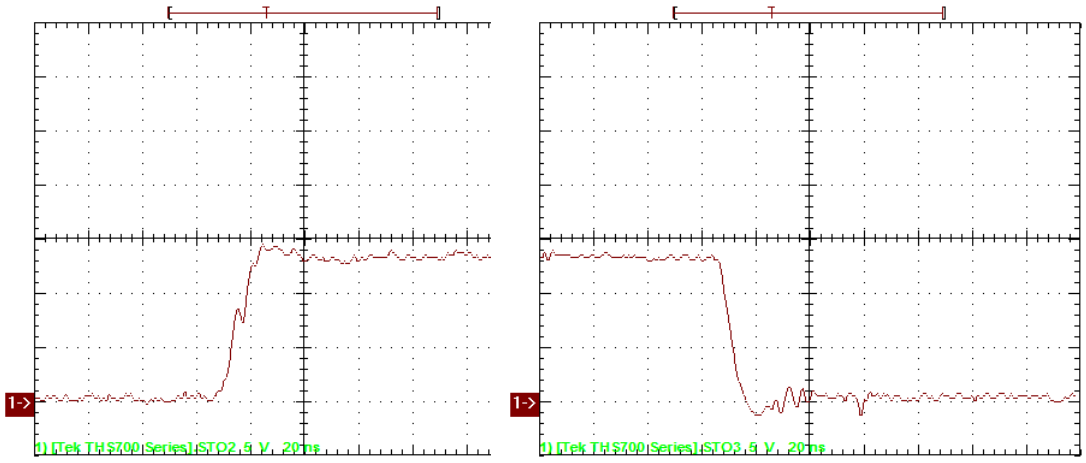
The waveform at Q2 gate-source is shown in Figure 30



Ch1 =>
5V/div

1µs/div

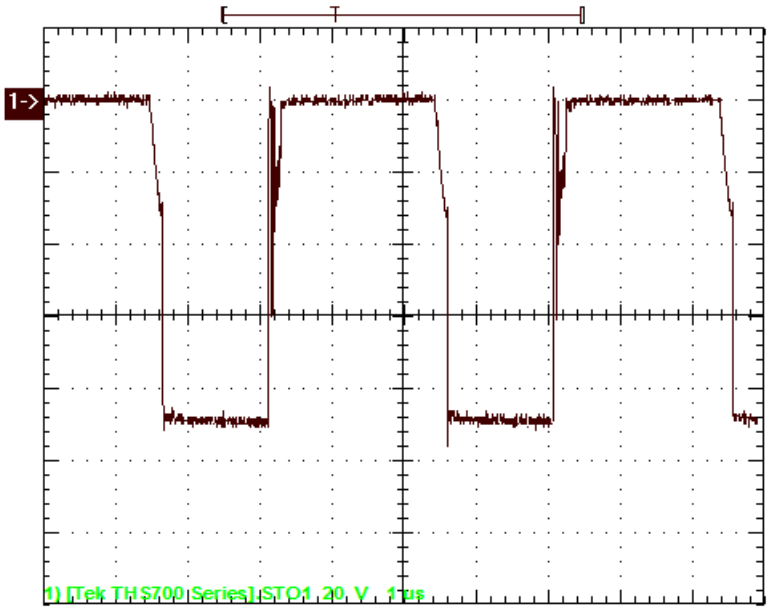
full bandwidth



Ch1 =>
5V/div
20ns/div

Figure 30

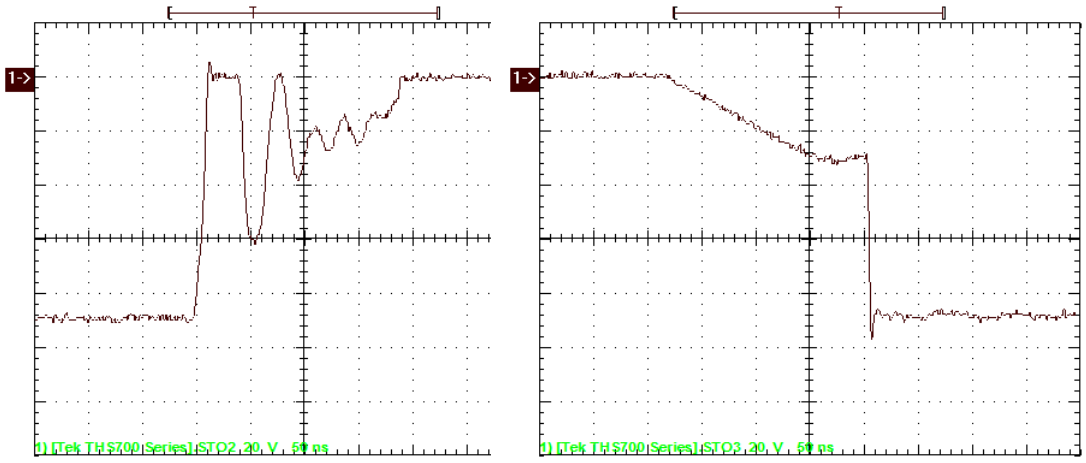
The waveform of the voltage on Q1 (PMOS) drain-source is shown in Figure 31.



Ch1 =>
20V/div

1µs/div

full bandwidth



Ch1 =>
20V/div
50ns/div

Figure 31

The waveform of the voltage on Q1 (PMOS) gate-source is shown in Figure 32.

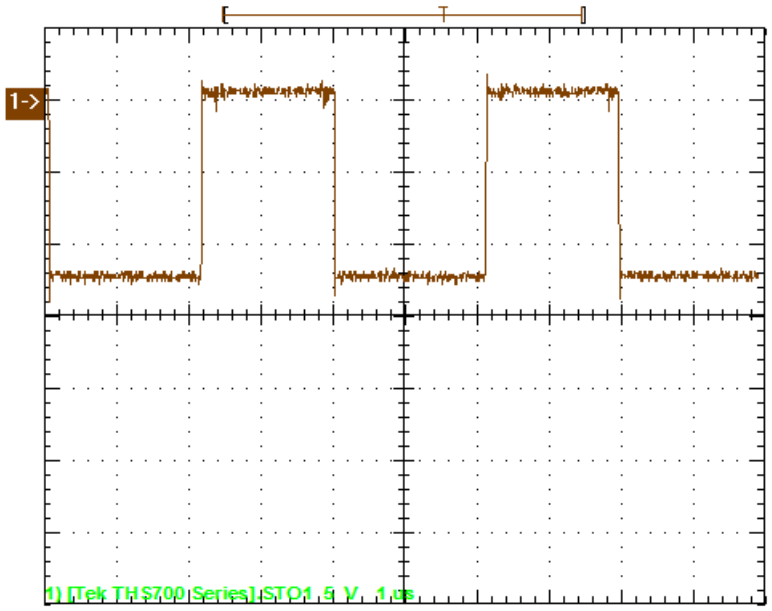
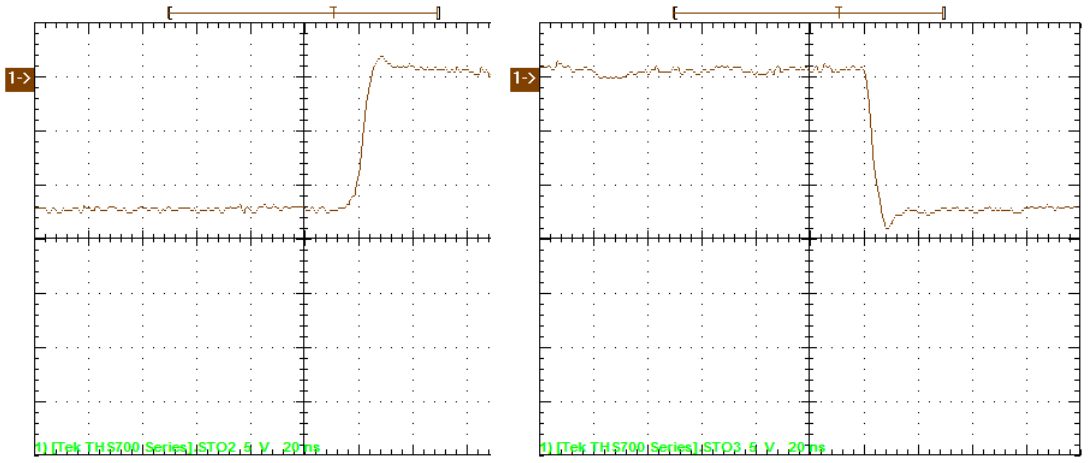
	Ch1 => 5V/div 1µs/div full bandwidth
	Ch1 => 5V/div 20ns/div

Figure 32

The waveform of the voltage at the transformer output is shown in Figure 33.

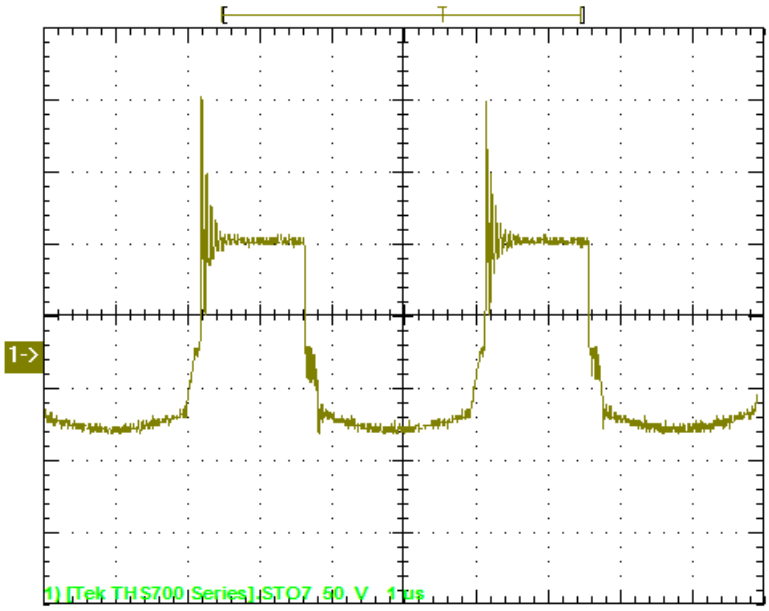
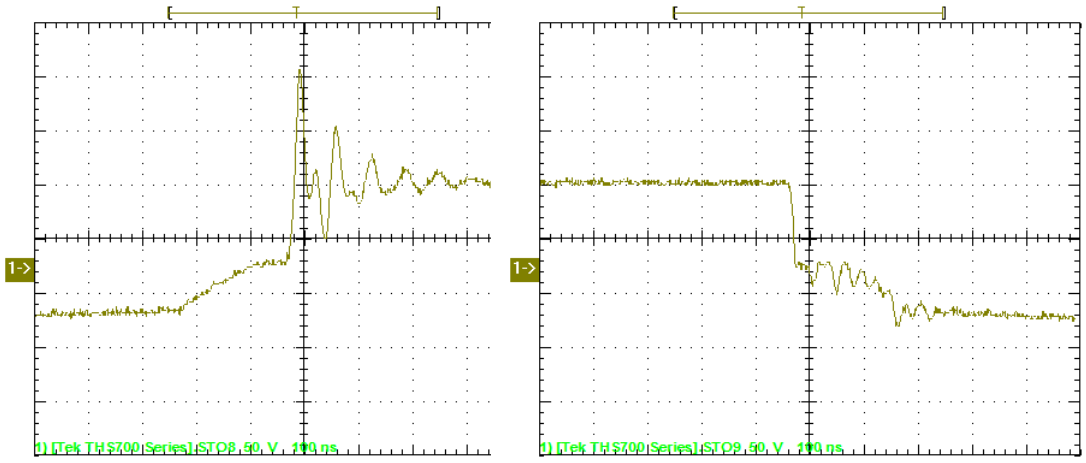
	Ch1 => 50V/div 1µs/div full bandwidth
	Ch1 => 50V/div 100ns/div

Figure 33

11 Thermal Image

Figure 34 shows the thermal image at 48V input voltage and 1A output current.

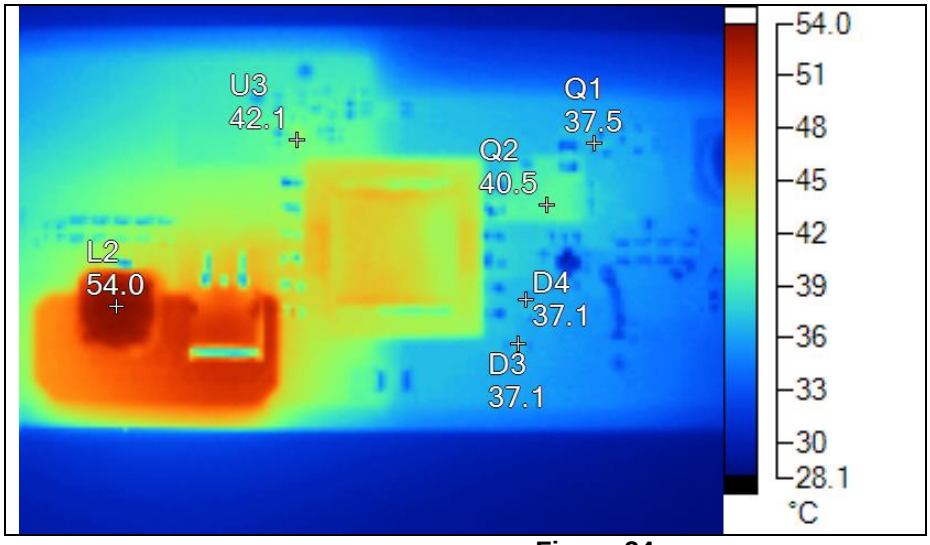


Figure 34

Figure 35 shows the thermal image at 48V input voltage and 1.5A output current.

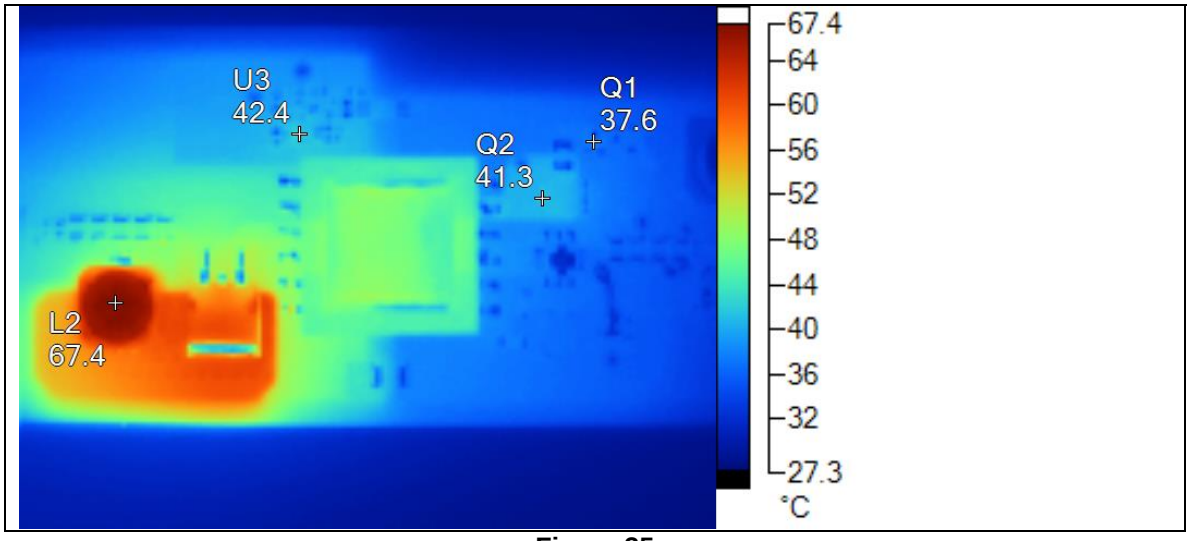


Figure 35

Figure 36 shows the thermal image at 48V input voltage and 2A output current.

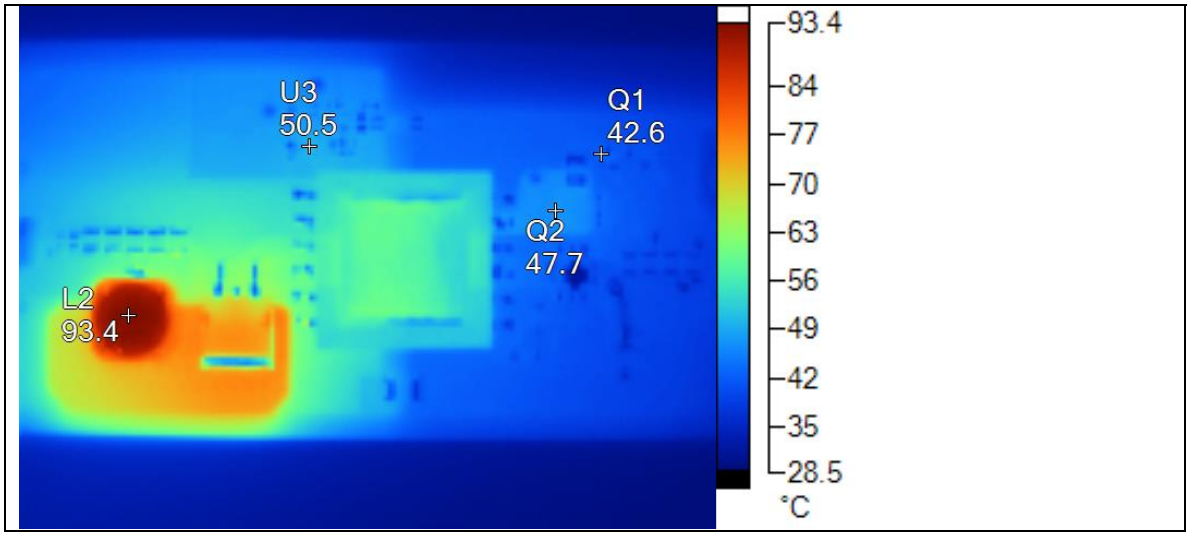


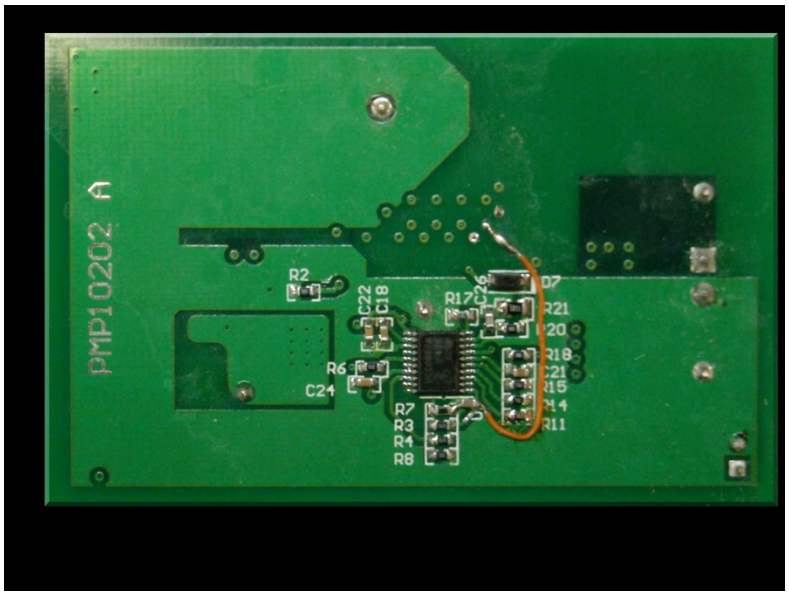
Figure 36

Table 3 sumarizes the last three figures.

Name	1A	1.5A	2A
L2	54.0°C	67.4°C	**93.4°C**
Q2	40.5°C	41.3°C	47.7°C
U3	42.1°C	42.4°C	50.5°C
Q1	37.5°C	37.6°C	42.6°C
D3	37.1°C		
D4	37.1°C		

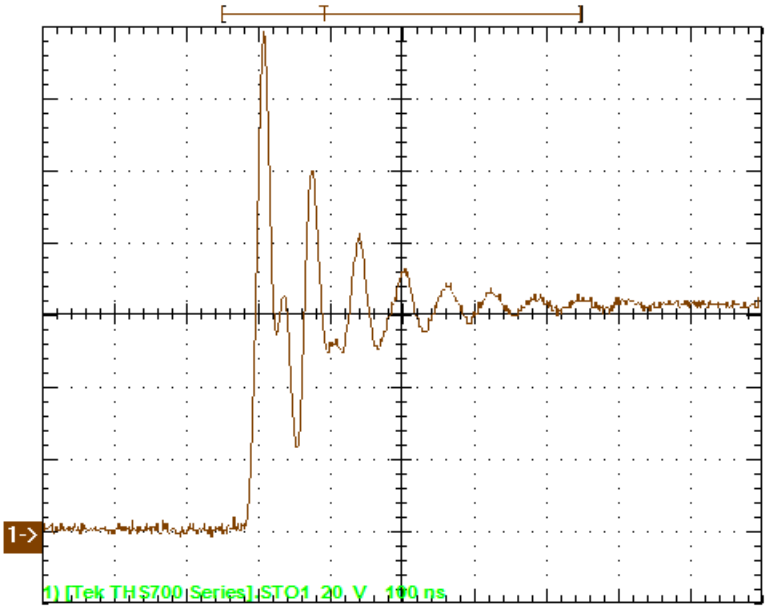
Table 3

For continuous output current >1.5A the output inductor needs a custom design *(220uH, 2.5Arms, 3.0Asat, shielded, ferrite)*



12 Addendum

Added RC-snubber on switchnode (secondary side) to GND2 across lowside Schottky.
Figure 37 is the waveform of the switchnode without snubber circuit.

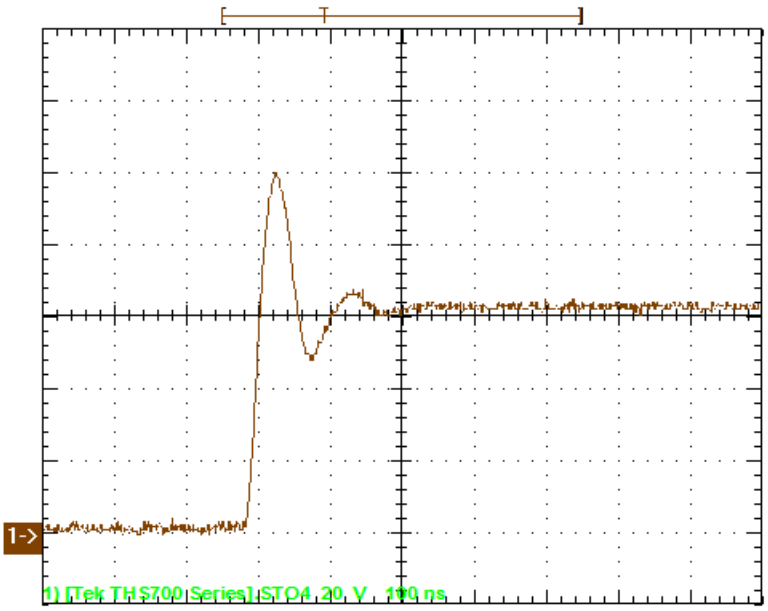


Ch1 =>
20V/div

100ns/div
full bandwidth

Figure 37

Figure 38 is the waveform of the switchnode with snubber (here used 430pF+27Ohms)



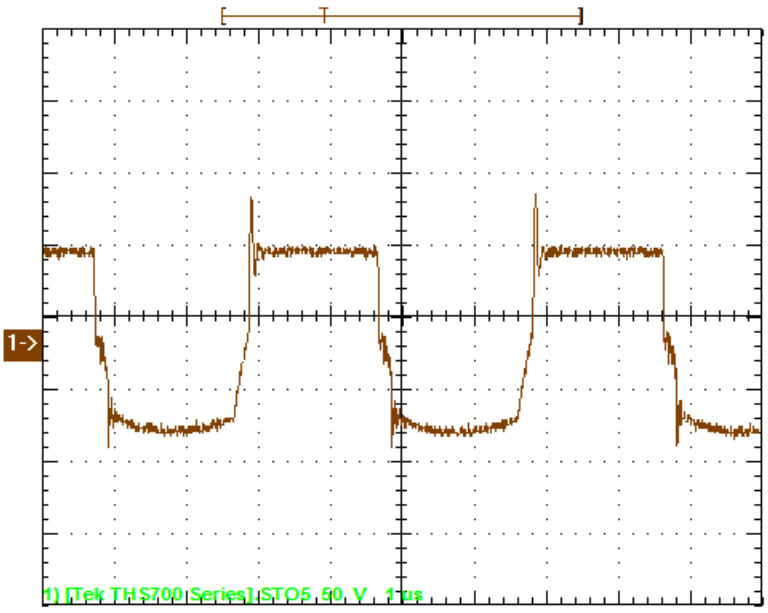
Ch1 =>
20V/div

100ns/div
full bandwidth

Figure 38

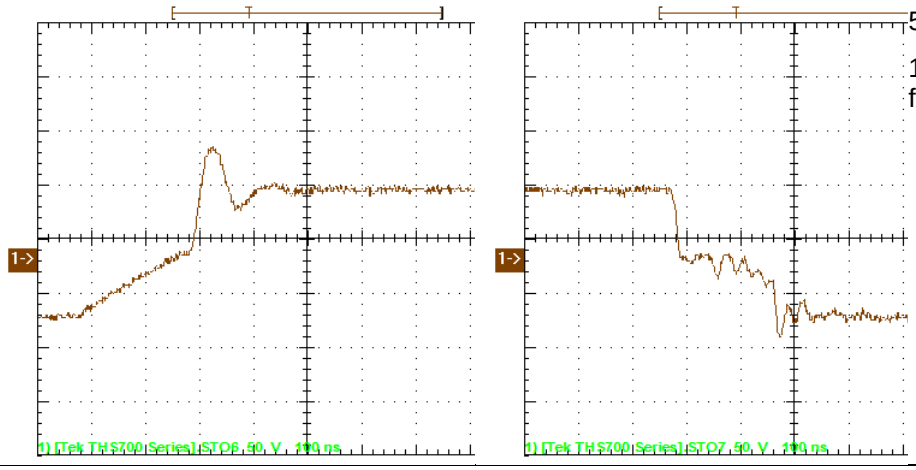
RF noise and overshoot could be reduced simply by adding 470pF (E6) / 33 Ohms (E6) or similar.

Figure 38 is the waveform of the transformer output (with snubber). See Figure 28 to compare the waveform with the waveform without snubber



Ch1 =>
50V/div

1µs/div
full bandwidth



Ch1 =>
50V/div

100ns/div
full bandwidth

Figure 39

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