TI Designs: TIDA-00701

100-W, 24-V, High Efficiency, High PF, Industrial Power Supply With Precision Current and Power Limit

TEXAS INSTRUMENTS

TI Designs

The TIDA-00701 design is a 100-W, 24-V, industrial AC-DC power supply designed for use in Industrial and Instrumentation systems such as process controls, factory automation, and machinery control. This reference design has a front-end power factor correction (PFC) circuit designed using the UCC28051 PFC controller, followed by quasi-resonant (QR) flyback converter implemented using the UCC28740 CC-CV flyback controller with optocoupled feedback for voltage and primary-side regulation (PSR) for constant current regulation and all the necessary protections built in. Hardware is designed and tested to pass conducted emissions, surge, and EFT requirements. The key highlights of reference design are:

- Reduced component count design to achieve NEC Class-2 and Limited Power Source (LPS) norms
- Meets ENERGY STAR® Rating, the 2013 EU eco-design directive Energy-related Products (ErP) Lot 6, and stringent current THD norms
- Robust output supply protected for output overcurrent, output short-circuit, output overvoltage, and over-temperature conditions

Design Resources

TIDA-00701	Design Folder
UCC28051	Product Folder
UCC28740	Product Folder
UCC24630	Product Folder
LM5050-2	Product Folder
TMP302	Product Folder
CSD18504Q5A	Product Folder

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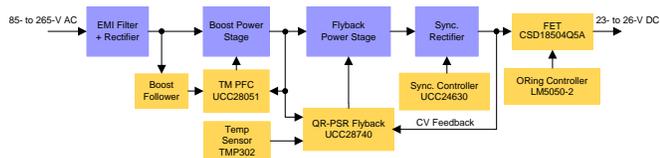
Design Features

- Wide Operating Input Range 85- to 265-V AC With Full Power Delivery Over Entire Range
- High Efficiency of 88% at 115-V AC and > 89% at 230-V AC for Wide Load Range From 40% to 100% Load. No External Cooling Needed up to 60°C Ambient Operation
- High Power Factor > 0.97 at Both 115- and 230-V AC for 100% Load. Meets Current THD Regulations as per IEC 61000-3-2, Class-A
- Precision Current Limit Within ±1%
- Very Low Standby Power of < 400 mW
- Start-up With High Load Capacitance up to 8500 µF
- Built-in Loss-less ORing Feature for Paralleling Multiple Modules
- Meets the Requirements of Conducted Emissions Standard – EN55011 Class B, EFT Norm IEC6000-4-4 –Level-3, and Surge Norm IEC61000-4-5 – Level-3
- Small PCB Form Factor (120 × 82 mm)

Featured Applications

- Industrial DIN Rail Power
  - Process Control
  - Factory Automation
- Telecommunications
- Medical Power Supplies
- Security Systems
- Data Monitoring and Controls

100-W, 24-V, High Efficiency, High PF, Industrial Power Supply With Precision Current and Power Limit

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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS						
Input voltage	V_{INAC}		85	115/230	265	VAC
Frequency	f_{LINE}		47	50	60	Hz
No load power	P_{NL}	V_{INAC} = 230 V, I_{OUT} = 0 A			0.4	W
Brownout voltage	V_{IN_UVLO}				80	VAC
Output conditions						
Output voltage			23	24	26	V
Output current					3.8	A
Line regulation					0.5	%
Load regulation					0.5	%
Output voltage ripple				20	50	mV
Output power				91.2[1]	98.8[2]	W
Hold-up time	t_{HOLD}	V_{INAC} = 115 V		> 30		ms
		V_{INAC} = 230 V		> 50		ms
Primary-to-secondary insulation				4		kV
SYSTEM CHARACTERISTICS						
Efficiency	η	V_{IN} = 230-V AC, I_{OUT} = 50% to 100% V_{IN} = 115-V AC, I_{OUT} = 50% to 100%			>89 88	%
Protections		Output overvoltage (settable)				
		Output overcurrent				
		Output short circuit				
		Input UVLO				
		Thermal shutdown (temperature at the sense point)				
		Output open loop protection				
		Input brownout protection				
Operating ambient		Open frame	–40	25	60	°C
Power line harmonics			As per IEC61000-3-2 Class-A			
Conducted emissions			As per EN55022/11 Class-B			
EFT			As per IEC-61000-4-4, Level-3			
Surge			As per IEC-61000-4-5, Level-3			
Dimensions		Length × Breadth × Height	120 × 82 × 35			mm

[1] 91.2 W at 24-V output
[2] 98.8 W at 26-V output

2 System Description

Industrial AC-DC power supplies are used in various applications such as process control, data logging, machinery control, instrumentation, factory automation and security systems. These AC-DC supplies provide a convenient means for powering DC operated devices including programmable logic controllers (PLCs), sensors, transmitters and receivers, analyzers, motors, actuators, solenoids, relays, and so on. These supplies are convection cooled, meaning no cooling fans are needed. They operate over a wide input range from 85- to 265-V AC, delivering full load for entire input voltage range. The output voltages from these supplies range from 5 to 56 V with power ratings from 7.5 to 480 W. Many of these supplies can be connected in parallel for higher power applications.

This reference design is a 100-W industrial power supply, designed with specific focus to meet the NEC Class-2 and Limited Power Source (LPS) norms. The design consists of a transition mode (TM) boost converter with variable frequency operation and a QR PSR flyback DC/DC converter. Input voltage range is 85- to 265-V AC$_{RMS}$ and the output voltage range is 23 to 26 V, with 24-V nominal operation. The output voltage range is settable using potentiometer present on the board. Industrial power supplies have requirements of high efficiency over their entire operating voltage range and wide load variations from 50% to 100% load. This design demonstrates high efficiency operation in a small form factor (120 × 82 mm) and delivers continuous 98.8 W of power over the entire input operating voltage range from 85- to 265-V AC. It gives an efficiency of > 89% for 230-V AC nominal operation and 88% for 115-V AC nominal operation.

The front-end boost PFC converter is designed with a boost follower configuration, in which the boost voltage can be varied based on AC input voltage as long as the boosted voltage is above the peak input voltage. Boost follower configuration aids in reducing switching losses in PFC regulator.

This reference design eliminates multiple feedback loops for open loop detection, current limit and power limiting, by using a precise PSR constant voltage-constant current (CC-CV) flyback controller UCC28740. Eliminating discrete circuitry and associated components, which are generally used to implement multiple feedback loops for protection and power limiting, aid in increasing of the lifetime of the product. In addition, high efficiency of DC/DC converter is achieved using the UCC28740 controller with built-in resonant-ring valley-switching operation.

The design has secondary side rectification implemented using the UCC28630 synchronous rectification controller to achieve high efficiency and optimize power loss. The design has a loss-less ORing circuit implemented using the LM5050-2 ORing controller for paralleling multiple modules to meet extended high power needs. The design has low standby power of < 400 mW and meets ENERGY STAR rating requirements as well as 2013 EU eco-design directive ErP Lot 6.

The EMI filter is designed to meet EN55011 class-B conducted emission levels. The design is fully tested and validated for various parameters such as regulation, efficiency, EMI signature, output ripple, startup, and switching stresses.

Overall, the design meets the key challenges of industrial power supplies to provide safe and reliable power with all protections built-in, while delivering high performance with low power consumption and low bill-of-material (BOM) cost.

2.1   Conventional versus Present Implementation

A conventional implementation of a typical 100-W industrial power supply is shown in Figure 1. In such a system, two optocouplers are used to feedback the output current and output voltage information to the flyback controller. These optocouplers along with their associated discrete feedback components add cost to the system and increase component count. Further, each or both of the optocouplers can fail simultaneously for similar stressed fault condition, which can be detrimental and can cause system failure.
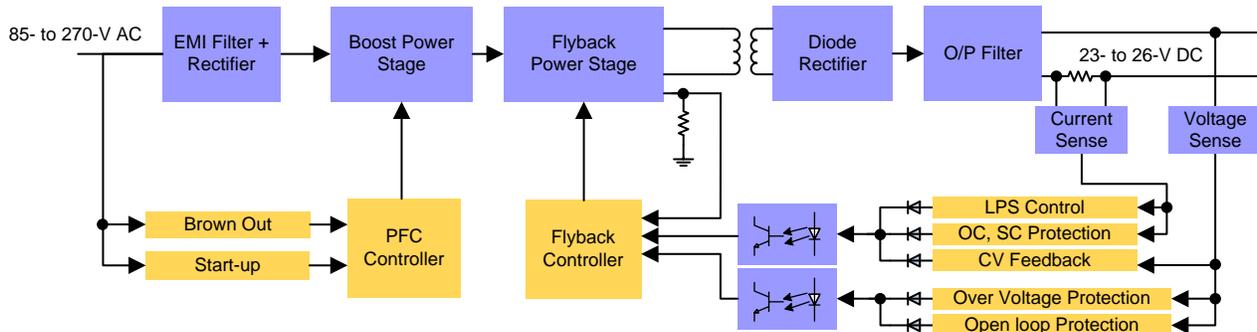
Figure 1. Conventional Implementation of 100-W Industrial Power Supply

The present implementation is shown in Figure 2. It uses the UCC28740, the latest generation CC-CV flyback controller with optocoupled feedback for voltage and PSR for constant current regulation and all the necessary protections built in. The current control is achieved by primary-side current sensing and voltage control is achieved by optocoupler feedback. An additional loop based on auxiliary winding voltage sensing also acts as redundant feedback and increases the life time of the system. The high level of integration of controls in the UCC28740 controller aids in lowering the component count and reducing cost.
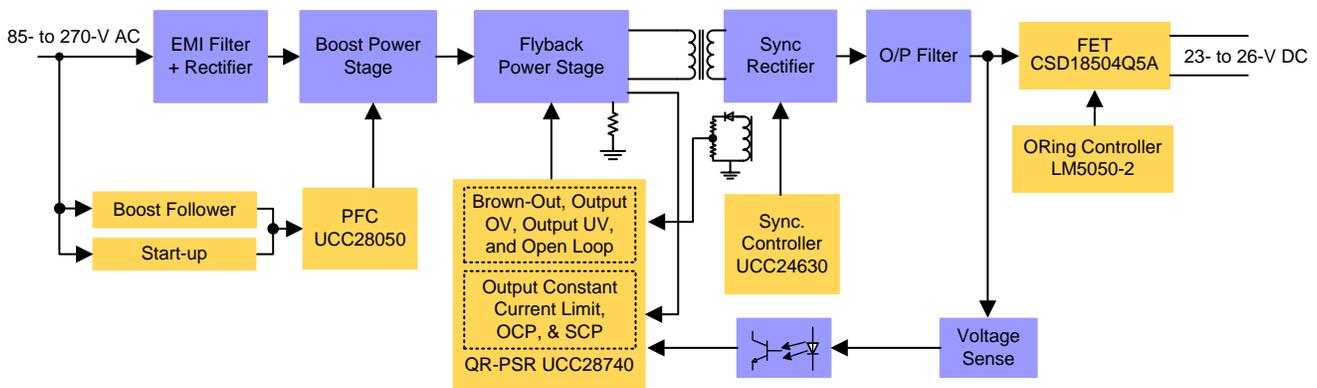
Figure 2. Present Implementation of 100-W Industrial Power Supply

3 Block Diagram
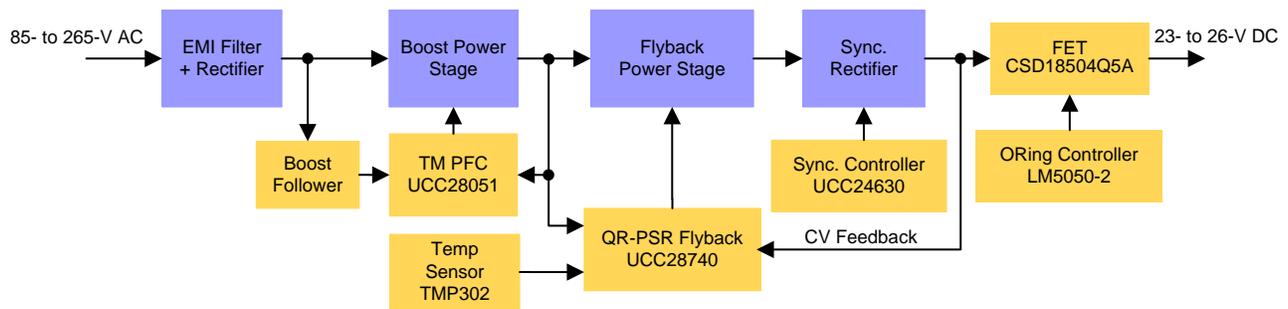
Figure 3. Block Diagram of 100-W Industrial Power Supply

3.1 Highlighted Products and Key Advantages

The following are the highlighted products used in this reference design. Key features for selecting the devices for this reference design are elucidated in the following sections. Find complete details of the highlighted devices in their respective product datasheets.

3.1.1 UCC28051 Transition Mode PFC Controller

To implement the low cost, small form factor PFC design at 100-W power, the UCC28051 is preferred controller as it offers series of benefits to meet IEC-61000-3-2 class-A THD norms and achieve high power factor for wide input voltage range of operation.

The UCC28051 transition mode PFC controller is designed for low-to-medium power applications requiring compliance with IEC 1000-3-2 harmonic reduction standard. It has all the built-in features needed to control a boost pre-regulator power stage operating in transition mode (also referred to as boundary conduction mode or critical conduction mode operation). Its integrated gate driver of ±0.75 A drive current eliminates the need for an external gate driver.

Key features that make this device unique are:

- Transition mode PFC controller for low implementation cost
- Improved transient response with slew-rate comparator
- Zero power detect to prevent overvoltage protection (OVP) during light load conditions
- Accurate internal V_{REF} for tight output regulation
- Two undervoltage lockout (UVLO) options, OVP, open-feedback protection and enable circuits

3.1.2   UCC28740 CV-CC Flyback Controller

To implement the high performance, small form factor flyback design at 100-W power, the UCC28740 is preferred because it offers a series of benefits to address the next generation DIN rail power supply needs of low reduced feedback loops for precision current limit and power limit. This eliminates the need of external current sensing on secondary side and multiple optocoupler feedback loops for open loop detection and power limiting.

The UCC28740 isolated-flyback power supply controller provides CV output regulation using an optical coupler to improve transient response to large load steps. CC regulation is accomplished through PSR techniques. This device processes information from optocoupled feedback and from an auxiliary flyback winding for precise high-performance control of output voltage and current. An internal 700-V startup switch, dynamically-controlled operating states, and a tailored modulation profile support ultra-low standby power without sacrificing startup time or output transient response. The drive output interfaces to a MOSFET power switch. Discontinuous conduction mode (DCM) with valley-switching reduces switching losses. Modulating the switching frequency and primary current peak amplitude (FM and AM) keeps the conversion efficiency high across the entire load and line ranges.

Key features that make this device unique are:

- Optocoupled feedback regulation for CV and PSR for CC
- Enables ±1% voltage regulation and ±5% current regulation across line and load
- 100-kHz max switching frequency enables high power density charger designs
- QR valley switching operation for highest overall efficiency
- Frequency jitter scheme to ease EMI compliance
- Wide VDD range (35 V) allows small bias capacitor
- Drive output for MOSFET
- Enables <10-mW system standby and no load power
- Protection functions: Overvoltage, low line, and overcurrent
- SOIC-7 package

3.1.3   UCC24630 Synchronous Rectifier Controller With Ultra-Low Standby Current

High efficiency designs need synchronous rectification to optimize the power loss. The UCC24630 provides great benefits and simplicity in design, offering near-ideal diode rectifier function.

The UCC24630 SR controller is a high performance controller and driver for N-Channel MOSFET power devices used for secondary-side synchronous rectification. The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also reduces primary-side losses as well, due to compounding of efficiency gains. Utilizing TI's patented volt-second balancing control method, the UCC24630 is ideal for flyback power supplies over a wide output voltage range because the IC is not connected directly to the MOSFET drain. The UCC24630 controller offers a programmable false-trigger filter, a frequency detector to automatically switch to standby mode during low power conditions and pin fault protections. The UCC24630 is compatible with DCM, TM, and CCM operation. The wide VDD operating range, wide programming range of the VPC voltage, and blanking time allows the device to be used in a variety of flyback converter designs.

Key features that make this device unique are:

- Volt-second balance SR on-time control
- 5- to 24-V output voltage flyback converters
- 150-µA IC current consumption at no load
- Auto low power detect and standby mode for minimal standby power impact
- Compact SOT-23-6 package
- Operating frequency up to 200 kHz
- Pin fault protection for open and short

3.1.4 LM5050-2 High-Side ORing FET Controller

To achieve high efficiency, it is more important to have lower losses. For an ORing function, a diode results in heavy loss due to its high forward voltage drop. As ORing function results in continuous power dissipation, it is preferred that FET has very low losses. The LM5050-2 is best fit as it provides accurate high-voltage ORing FET control in a tiny package.

The LM5050-2 controller provides charge pump gate drive for an external N-Channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction.

Key features that make this device unique are:

* Wide operating input voltage range, V_{IN}: 5 to 75 V
* 100-V transient capability
* Charge pump gate driver for external N-channel MOSFET
* Fast 50-ns response to current reversal
* FET test mode indicates shorted FET
* 2-A peak gate turn-off current
* Minimum V_{DS} clamp for faster turn-off
* Package: SOT-6 (thin SOT-23-6)

3.1.5 TMP302 Easy-to-Use, Low-Power, Low-Supply Temperature Switch

The TMP302 is a temperature switch in a micro package (SOT563). The TMP302 offers low power (15-μA maximum) and ease-of-use through pin selectable trip points and hysteresis. These devices require no additional components for operation. They can function independent of microprocessors or microcontrollers. The TMP302 is available in several different versions.

Key features that make this device unique are:

* Low supply voltage range: 1.4 to 3.6 V
* Low power: 15 μA (maximum)
* Trip-point accuracy: ±0.2°C (typical) from 40°C to 125°C
* Pin-selectable trip points
* Open-drain output
* Pin-selectable hysteresis: 5°C and 10°C

3.1.6 CSD18504Q5A 40-V N-Channel NexFET™ Power MOSFET

For continuous ON ORing functions, it is important to select a MOSFET with low $R_{DS(ON)}$ and compatible with the ORing controller. The CSD18504Q5A is the best fit for this design.

Key features that make this device unique are:

* Very low $R_{DS(on)}$ of 5.6 mΩ
* Ultra-low Q_g and Q_{gd}
* Low thermal resistance

4 System Design Theory

This reference design provides 100 W of continuous power over a wide AC input range from 85- to 230-V AC with power factor correction. The UCC28051 controls a PFC boost front-end power stage to generate DC output voltage, while the UCC28740 QR flyback controller converts the PFC output to isolated 24 V and 3.8 A. The total system efficiency is over 89% with a 230-V AC input and over 88% with a 115-V AC input under full load conditions. The design has a precise current limit and limits the power to less than 100 W under all fault conditions. In addition, several protections are embedded into this design, which includes input UVP and output short-circuit protection.

Low EMI, high efficiency, high power factor, and reliable power supply are the main focus of this design for targeted applications.

4.1 PFC Regulator Stage Design

Power factor correction shapes the input current of the power supply to maximize the real power available from the mains. In addition, it is important to have PFC comply with low harmonic (low THD) regulatory requirements such as IEC61000-3-2. Currently, two modes of operation have been widely utilized for PFC implementations. For higher power circuits, the topology of choice is the boost converter operating in continuous conduction mode (CCM) and with average current mode control. For lower power applications, typically the TM or critical conduction mode (CrM) boost topology is utilized.

For low power levels such as 100 W, it is advisable to use TM operation as it offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less expensive diodes without sacrificing efficiency. In addition, variable frequency operation results in distributed EMI spectrum and low emissions.

4.2 PFC Circuit Component Design

The design process and component selection for this design are illustrated in the following sections.

4.2.1 Circuit Component Design – Design Goal Parameters

Table 2 elucidates the design goal parameters for PFC converter design. These parameters will be used in further calculations for selection of components.

Table 2. Design Goal Parameters for PFC Converter

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{AC}	Input voltage	85	115/230	265	VAC
f_{LINE}	Input frequency	47	50/60	63	Hz
	Brownout voltage		70		VAC
OUTPUT					
V_{DCBUS}	Output voltage (boost follower)	250		400	VDC
P_{DCBUS}	Output power		110		W
PF	Power factor			0.99	
	Line regulation			<1%	
	Load regulation			<1%	
f_S	Minimum PFC switching frequency	45			kHz
η_{PFC}	Targeted efficiency		95%		

4.2.2 Input Current Calculations and Fuse Selection

The input fuse and bridge rectifier are selected based upon the input current calculations.

As the design is done for boost follower configuration, determine first the range of PFC output voltage variation needed for downstream converter operation. For this design, the boost voltage is designed to vary from 230- to 400-V DC for input AC voltage range of 85- to 265-V AC operation.

The boost PFC converter is designed for output power of 110 W, considering the downstream DC-DC converter operating at > 90% to 92% efficiency.

Determine P_{IN}, the maximum input power averaged over the AC line period:

$$P_{IN} = \frac{P_{DCBUS}}{\eta_{PFC}} = \frac{110\ W}{0.95} = 115\ W \tag{1}$$

Determine the maximum and minimum average output current:

$$I_{DCBUS(max)} = \frac{P_{DCBUS}}{V_{DCBUS(min)}} = \frac{110\ W}{230\text{-V DC}} = 0.478\ A \tag{2}$$

$$I_{DCBUS(max)} = \frac{P_{DCBUS}}{V_{DCBUS(min)}} = \frac{110\ W}{400\text{-V DC}} = 0.275\ A$$

Determine the maximum and minimum RMS input current:

$$I_{IN\_RMS(max)} = \frac{P_{DCBUS}}{\eta_{PFC} \times V_{IN(min)} \times PF} = \frac{110\ W}{0.95 \times 85\text{-V AC} \times 0.99} = 1.376\ A \tag{3}$$

Determine the maximum input current ($I_{IN(max)}$), and the maximum average input current, ($I_{IN\_AVG(max)}$) based upon the calculated RMS value, assuming the waveform is sinusoidal:

$$I_{IN(max)} = \sqrt{2} \times I_{IN\_RMS(max)} = \sqrt{2} \times 1.376\ A = 1.95\ A \tag{4}$$

$$I_{IN\_AVG(max)} = \frac{2}{\pi} \times I_{IN(max)} = \frac{2}{\pi} \times 1.95\ A = 1.24\ A \tag{5}$$

4.2.3 Bridge Rectifier

The maximum input AC voltage is 265-V AC, so the DC voltage can reach voltage levels of up to 375-V DC. Considering a safety factor of 30%, it is recommended to select a component with voltage rating greater than 500-V DC. The input bridge rectifier must have an average current capability that exceeds the input average current ($I_{IN\_AVG(max)}$). To optimize the power loss due diode forward voltage drop, a higher current bridge rectifier is recommended.

For this design, a 600-V, 6-A diode GBU6J was chosen for input rectification. The forward voltage drop of bridge rectifier diode, V_{F_BRIDGE} = 0.8 V.

The maximum power loss in the input bridge, P_{BRIDGE}, can be calculated as:

$$P_{BRIDGE} = 2 \times V_{F\_BRIDGE} \times I_{IN\_AVG(max)} = 2 \times 0.8\ V \times 1.24\ A = 1.98\ W \tag{6}$$

4.2.4 Inductor Selection

The boost inductor is selected based on the maximum ripple current at the peak of minimum line voltage and the minimum switching frequency. The minimum switching frequency (f_S) needs to be set at a frequency above the audible range. For this design, $f_{S(min)}$ was selected to be 45 kHz. Equation 7 can be used to calculate the required inductor for the power stage for a critical conduction design:

$$L_{PFC(min)} = \frac{V_{AC(min)}^2 \times (V_{DCBUS(min)} - \sqrt{2} \times V_{AC(min)})}{2 \times f_{s(min)} \times V_{DCBUS(min)} \times P_{IN}} \tag{7}$$

$$L_{PFC(min)} = \frac{85\ V^2 \times (230\ V - \sqrt{2} \times 85\ V)}{2 \times 45 \times 230\ V \times 115\ W} = 331\ \mu H$$

Also, calculate the maximum inductance required:

$$L_{PFC(max)} = \frac{V_{AC(max)}^2 \times (V_{DCBUS(max)} - \sqrt{2} \times V_{AC(max)})}{2 \times f_{s(min)} \times V_{DCBUS(max)} \times P_{IN}}$$

(8)

$$L_{PFC(max)} = \frac{265\,V \times (400\,V - \sqrt{2} \times 265\,V)}{2 \times 45 \times 400\,V \times 115\,W} = 429\,\mu H$$

Select the minimum of the two values calculated in Equation 9 and Equation 10. The inductance used for this design is 330 µH.

The peak value of the inductor current is calculated as:

$$I_{L(peak)} = 2 \times \sqrt{2} \times \frac{P_{IN}}{V_{AC(min)}} = 2 \times \sqrt{2} \times \frac{115\,W}{85\,V} = 3.83\,A$$

(9)

The RMS value of inductor current is calculated as:

$$I_{L\_RMS} \approx \frac{1}{\sqrt{6}} \times I_{L(peak)} = 1.56\,A$$

(10)

4.2.5 Boost Switching FET Selection

The main switch selection is driven by the amount of power dissipation allowable. It is important to choose a device that minimizes gate charge and capacitance and minimizes the sum of switching and conduction losses at a given frequency.

$$I_{Q(RMS)} = I_{L(peak)} \times \sqrt{\frac{1}{6} - 4 \times \sqrt{2} \times \frac{V_{AC(min)}}{9 \times \pi \times V_{DCBUS(max)}}}$$

(11)

$$I_{Q(RMS)} = 3.83\,A \times \sqrt{\frac{1}{6} - 4 \times \sqrt{2} \times \frac{85\,V}{9 \times \pi \times 400\,V}} = 1.35\,A$$

The maximum voltage across the FET will be the maximum output boost voltage (that is, 400 V). Considering a de-rating of 30%, the voltage rating of the MOSFET should be > 520-V DC.

The IPA60R330P6 MOSFET of 600 V and 12 A at 25°C / 7.6 A at 100°C is selected for this design. An appropriately sized heat sink is used for MOSFET.

4.2.6 Boost Diode Selection

The diode selection is based on reverse voltage, forward current, and switching speed.

$$I_{D(AVG)} = I_{DCBUS(max)} = 0.478\,A$$

(12)

$$I_{D(RMS)} = I_{L(peak)} \times \sqrt{\sqrt{2} \times \frac{V_{AC(min)}}{\pi \times V_{DCBUS(max)}}} = 3.83\,A \times \sqrt{\sqrt{2} \times \frac{85\,V}{\pi \times 400\,V}} = 1.18\,A$$

(13)

The maximum voltage across the diode will be the maximum output boost voltage (that is, 400 V). Considering de-rating of 30%, the voltage rating of the MOSFET should be > 520-V DC.

With this information, the MURS360T diode is selected for this design.

4.2.7 Output Capacitor Selection

The hold-up time is the main requirement in determining the output capacitance. ESR and the maximum RMS ripple current rating may also be important, especially at higher power levels.

$$C_{OUT(min)} \geq \frac{2 \times P_{DCBUS} \times t_{holdup}}{(V_{DC(115\text{-}V\ AC)}^2 - V_{holdup}^2)}$$

(14)

For voltage follower configuration, the DC bus voltage at 115-V AC will be ~300-V DC. The holdup voltage is considered to 180 V. This will be minimum voltage operating point for downstream DC/DC converter operation.

$$V_{holdup} = 180\ V$$

$$C_{OUT(min)} \geq \frac{2 \times 110\ W \times 21.3\ ms}{(300\ V^2 - 180\ V^2)} = 81.3\ \mu F$$

The actual value used in design is 82 μF.

$$I_{COUT(RMS)} = \frac{P_{DCBUS}}{V_{DCBUS(min)}} \times \sqrt{\frac{16 \times V_{DCBUS(min)}}{3 \times \pi \times V_{AC(min)} \times \sqrt{2}} - 1}$$

(15)

$$I_{COUT(RMS)} = \frac{110\ W}{250\ V} \times \sqrt{\frac{16 \times 250\ V}{3 \times \pi \times 85\ V \times \sqrt{2}} - 1} = 0.7\ A$$

4.2.8 Sense Resistor

The current sense resistor value needs to be chosen to limit the output power and se the full dynamic range of the multiplier during normal steady state operation. The current-sense resistor needs to trip the peak current limit comparator at 130% of the maximum output power. V_{CSENSE} is the peak current limit comparator's threshold of 1.7 V.

$$R_{S\_PFC} = \frac{V_{CSENSE}}{1.3 \times I_{L(peak)}} = \frac{1.7\ V}{1.3 \times 3.83\ A} = 0.34\ \Omega$$

(16)

R_{SEN_PFC} selected is 0.030 Ω.

A lower value of current sense is required to have normal full load operation over entire operating voltage range during boost follower configuration.

4.2.9 Multiplier Setup

The multiplier is used to shape the input current waveform and must be set up correctly to get proper PFC. Select resistors at multiplier pin R_{AC1} and R_{AC2} so that their ratio uses the full dynamic range of the multiplier input at the peak line voltage, yet their values are small enough to make the effects of the multiplier bias current negligible. In order to use the maximum range of the multiplier, select the divider ratio so that V_{MULTIN} evaluated at the peak of the maximum AC line voltage is the maximum of the minimum dynamic input range of MULTIN, which is 2.5 V.

$$\frac{R_{AC1}}{R_{AC2}} = \left(\frac{\sqrt{2}}{2.5} \times V_{AC(max)} \right) - 1$$

(17)

Choose R_{AC1} so that it has at least 100 μA at the peak of the minimum AC operating line voltage.

In extreme cases, switching transients can contaminate the MULTIN signal, and it can be beneficial to add capacitor C_{AC1} at multiplier pin. Select the value of C_{AC1} so that the corner frequency of the resulting filter is greater than the lowest switching frequency.

4.2.10 Output Voltage Set Point

Select the divider ratio of R_{FB1} and R_{FB2} to set the V_{REF} voltage to 2.5 V at the desired output voltage. The current through the divider should be at least 200 μA.

Multiple resistors in series are used due to the maximum allowable voltage across each. Using the internal 2.5-V reference, V_{REF}, the bottom divider resistor, R_{FB2}, is selected to meet the output voltage design goals.

$$R_{FB2} = \frac{2.5 \text{ V} \times 1.02 \text{ M}\Omega}{400 \text{ V} - 2.5 \text{ V}} = 6.41 \text{ k}\Omega \tag{18}$$

A standard value 6.49-kΩ resistor for R_{FB2} results in a nominal output voltage set point of 395 V.

A small capacitor on V_{O_SNS} pin must be added to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 6 to 10 μs so as not to significantly reduce the control response time to output voltage deviations.

$$C_{VSENSE} = \frac{6 \text{ μs}}{R_{FB2}} = 936 \text{ pF} \tag{19}$$

The closest standard value of 1 nF was used on VO_SNS pin for a time constant of 10.66 μs.

4.2.11 Control Loop Compensation

The transconductance amplifier is compensated with a zero, f_{ZERO}, at the f_{PWM_PS} pole and a pole, f_{POLE}, placed at 20 Hz to reject high-frequency noise and roll off the gain amplitude. The overall voltage loop crossover, f_V, is desired to be at 10 Hz. The compensation components of the transconductance amplifier are selected accordingly.

4.3 QR Flyback Converter With PSR

Flyback converters provide a cost effective solution for AC/DC conversion needs. They are widely used for AC/DC converters up to 150 W. There are three modes of operation: discontinuous mode (DCM), quasi-resonant mode (QRM), and continuous conduction mode (CCM). For lower power applications, the DCM or QRM is preferred as they have reduced power losses and optimal peak currents in low power applications. As the output wattage increases, CCM becomes more efficient due to the reduced peak and RMS currents.

Flyback converters designed with PSR flyback controllers eliminate the use of conventional optocoupler-based feedback. The PSR flyback controllers sense the voltage feedback through auxiliary winding and current feedback through current sense resistor used in series with switching FET. In addition, PSR flyback controllers provide a wide range of protections and accurate limiting of both current and power.

The UCC28740 controller has both PSR feedback and opto-feedback enhancing the reliability of the system.

4.4 Flyback Circuit Component Design

The UCC28740 is a flyback controller provides CV mode control and CC mode control for precise output regulation. While in CV operating range, the controller uses an optocoupler for tight voltage regulation and improved transient response to large load steps. Accurate regulation while in CC mode is provided by primary-side control. The UCC28740 uses frequency modulation, peak primary current modulation, valley switching, and valley hopping in its control algorithm to maximize efficiency over the entire operating range.

Table 3 elucidates the design goal parameters for flyback converter design. These parameters will be used in further calculations to select components.

Table 3. Design Goal Parameters for Flyback Converter

PARAMETER		MIN	TYP	MAX	UNIT
INPUT					
V_{INDC}	DC input voltage range (from PFC output)	180	325	400	VAC
OUTPUT					
V_{OUT}	Output voltage	22	24	26	VDC
I_{OUT}	Output current		3.8		VDC
P_{OUT}	Output power (max)		98.8		W
	Line regulation			<1%	
	Load regulation			<1%	
F_{MAX}	Maximum desired switching frequency			65	kHz
η	Targeted efficiency		92%		

4.4.1 Input Bulk Capacitance and Minimum Bulk Voltage

Maximum DC input power is determined by the V_{OCV}, I_{OCC}, and full-load efficiency targets. As the converter is designed to operate a variable voltage range from 23 to 26 V, the primary output is considered to be Primary output: $V_{OUT} = V_{OCV} = 26$ V.

The converter is designed for 3.8 A of maximum output current on primary output and is designed to limit the current at 3.8 A for overload conditions. So,

$$I_{OCC} = 3.8 \text{ A} \tag{20}$$

The total maximum output power need is

$$P_{OUT} = V_{OUT} \times I_{OCC} = 26 \times 3.8 = 60.0 \text{ W} \tag{21}$$

To calculate the component ratings, the minimum targeted efficiency is considered as η = 85 %.

$$P_{IN} = \left(\frac{P_{OUT}}{\eta} \right) = \frac{60.0}{0.85} = 70.588 \text{ W} \tag{22}$$

Because a PFC front-end is used in this design, the PFC output capacitor will be input capacitance for the flyback converter.

$$C_{BULK} = 82 \text{ } \mu F \tag{23}$$

The minimum voltage operation of flyback is defined by the holdup voltage of the PFC converter during brown-out conditions.

$$V_{holdup} = 180 \text{ V} \tag{24}$$

Considering a maximum of 20-V ripple voltage on the capacitor:

$$V_{BULK(min)} = V_{holdup} - 20 \text{ V} = 160 \text{ V} \tag{25}$$

4.4.2 Transformer Parameter Calculations: Turns Ratio, Primary Inductance, and Peak Primary Current

The target maximum switching frequency at full-load, the minimum input-capacitor bulk voltage, and the estimated DCM QR time determine the maximum primary-to-secondary turns-ratio of the transformer.

Initially determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency, F_{MAX}, and DCM resonant time. For DCM resonant frequency, assume 500 kHz if an estimate from previous designs is not available. At the TM operation limit of DCM, the interval required from the end of secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period (t_R), or 1 µs assuming a 500-kHz resonant frequency. The maximum allowable MOSFET on-time D_{MAX} is determined using Equation 26.

$$D_{MAX} = 1 - D_{MAGCC} - F_{MAX} \times \frac{t_R}{2} \tag{26}$$

where:

- t_R is the estimated period of the LC resonant frequency at the switch node
- D_{MAGCC} is defined as the secondary-diode conduction duty-cycle during CC operation and is fixed internally by the UCC28740 at 0.425.

$$t_R = 2 \ \mu s$$

$$D_{MAX} = 1 - 0.425 - 65 \ kHz \times \frac{2 \ \mu s}{2} = 0.51$$

When D_{MAX} is known, the maximum primary-to-secondary turns-ratio is determined with Equation 27. The total voltage on the secondary winding must be determined, which is the sum of V_{OCV}, V_F, and V_{OCBC}.

$$N_{PS(max)} = \frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \tag{27}$$

V_{OCBC} is the additional voltage drop of post filter inductor and any other target cable-compensation voltage added to V_{OCV} (provided by an external adjustment circuit applied to the shunt-regulator). Set V_{OCBC} equal to 0 V if not used. In this TI Design, as post LC filter is used, V_{OCBC} is considered as the voltage drop across the inductor.

$$V_{OCBC} = DCR_L \times I_{OCC} = 6.75 \ m\Omega \times 3.8 \ A = 25.65 \ mV$$

$$N_{PS(max)} = \frac{0.51 \times 160 \ V}{0.425 \times (26 \ V + 0.4 \ V + 0.02565 \ V)} = 7.265$$

A higher turns-ratio generally improves efficiency, but may limit operation at a low input voltage.

The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage, so these should be reviewed. The UCC28740 controller requires a minimum on time of the MOSFET ($t_{ON(min)}$) and minimum secondary rectifier conduction time ($t_{DM(min)}$) in the high line and minimum load condition. The selection of F_{MAX}, L_P, and R_{CS} affects the minimum $t_{ON(min)}$ and $t_{DM(min)}$.

The secondary rectifier and MOSFET voltage stress can be determined by Equation 28 and Equation 29.

$$V_{REV} = \frac{V_{IN(max)} \times \sqrt{2}}{N_{PS}} + V_{OCV} + V_{OCBC} \tag{28}$$

For the MOSFET V_{DS} voltage stress, an estimated leakage inductance voltage spike (V_{LK}) needs to be included.

$$V_{DSPK} = (V_{IN(max)} \times \sqrt{2}) + (V_{OCV} + V_F + V_{OCBC}) \times N_{PS} \times V_{LK} \tag{29}$$

Equation 30 determines if $t_{ON(min)}$ exceeds the minimum t_{ON} target of 280 ns (maximum t_{CSLEB}). Equation 31 verifies that $t_{DM(min)}$ exceeds the minimum t_{DM} target of 1.2 μs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)} \times \sqrt{2}} \times \frac{I_{PP(max)}}{K_{AM}}$$

(30)

$$T_{DM(min)} = \frac{t_{ON(min)} \times V_{IN(max)} \times \sqrt{2}}{N_{PS} \times (V_{OCV} + V_F)}$$

(31)

To determine optimum turns-ratio N_{PS}, design iterations are generally necessary to optimize and evaluate system-level performance trade-offs and parameters mentioned in Equation 28 to Equation 31. The design spreadsheet provides easy way to perform the iterations and arrive at optimum value for NPS (see Section 7.7).

When the optimum turns-ratio N_{PS} is determined from a detailed transformer design, use this ratio for the following parameters. For this design, $N_{PS} = 4.0$ is selected on optimization.

The UCC28740 CC regulation is achieved by maintaining D_{MAGCC} at the maximum primary peak current setting. The product of D_{MAGCC} and $V_{CST(max)}$ defines a CC-regulating voltage factor V_{CCR}, which is used with N_{PS} to determine the current-sense resistor value necessary to achieve the regulated CC target, I_{OCC} (see Equation 32).

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}}$$

(32)

Because a small portion of the energy stored in the transformer does not transfer to the output, a transformer efficiency term is included in Equation 32. This efficiency number includes the core and winding losses, the leakage-inductance ratio, and a bias-power to maximum-output-power ratio. For example, an overall-transformer efficiency of 0.9 is a good estimate based on 3.5% leakage inductance, 5% core and winding loss, and 0.5% bias power. Adjust these estimates appropriately based on each specific application.

$$R_{CS} = \frac{0.318 \text{ V} \times 4.0 \times \sqrt{0.9}}{2 \times 3.8 \text{ A}} = 0.159 \text{ } \Omega$$

$V_{CCR(min)}$ is the minimum CC regulation factor and device parameter = 0.318 V.

The standard value of current sense resistor selected is $R_{CS} = 0.159 \text{ } \Omega$. A parallel resistor to R_{CS} is added in the schematic for ease of adjustment of values.

To calculate primary inductance, first determine the transformer primary peak current using Equation 33. Peak primary current is the maximum current-sense threshold divided by the current-sense resistance:

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}}$$

(33)

$$I_{PP(max)} = \frac{0.81 \text{ V}}{0.159 \text{ } \Omega} = 5.094 \text{ A}$$

$$I_{PP(nom)} = \frac{0.773 \text{ V}}{0.159 \text{ } \Omega} = 4.862 \text{ A}$$

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. Primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in Equation 34.

$$L_P = \frac{2 \times (V_{OCV} + V_F + V_{OCBC}) \times I_{OCC}}{\eta_{XFMR} \times I_{PP(max)}^2 \times f_{MAX}} \tag{34}$$

$$L_P = \frac{2 \times (26\ V + 0.4\ V + 0.02565\ V) \times 3.8}{0.9 \times 4.862\ A^2 \times 65\ kHz} = 145.2\ \mu H$$

The actual primary inductance selected is L_P = 160 µH.

N_{AS} is determined by the lowest target operating output voltage while in CC regulation and by the VDD UVLO turnoff threshold of the UCC28740. Additional energy is supplied to VDD from the transformer leakage-inductance, which allows a lower turns-ratio to be used in many designs.

$$N_{AS} = \frac{V_{VDD(off)} + V_{FA}}{V_{OCC} + V_F} = \frac{8.15\ V + 0.9\ V}{12\ V + 0.4\ V} = 0.73 \tag{35}$$

4.4.3 Transformer Parameter Calculations: Primary and Secondary RMS Currents

With the primary inductance of 160 µH, the absolute maximum switching frequency is calculated from Equation 34:

$$f_{MAX} = \frac{2 \times (24\ V + 0.4\ V + 0.02565\ V) \times 3.8}{0.9 \times 4.862\ A^2 \times 160\ \mu H} = 54.2\ kHz \tag{36}$$

The maximum switching period is

$$t_{SW} = \frac{1}{f_{MAX}} = \frac{1}{54.2\ kHz} = 18.45\ \mu s \tag{37}$$

The actual maximum ON-time is given by

$$t_{ON(max)} = \frac{I_{PP(nom)} \times L_P}{V_{BULK(min)}} = \frac{4.862\ A \times 160\ \mu H}{160\ V} = 4.862\ \mu s \tag{38}$$

The maximum duty cycle of operation (D_{MAX}) is

$$D_{MAX} = \frac{t_{ON(max)}}{t_{SW}} = \frac{4.862\ \mu s}{18.45\ \mu s} = 0.264 \tag{39}$$

The transformer primary RMS current (I_{PRMS}) is

$$I_{PRMS} = I_{PP(nom)} \times \sqrt{\frac{D_{MAX}}{3}} = 4.862\ A \times \sqrt{\frac{0.264}{3}} = 1.442\ A \tag{40}$$

The transformer secondary peak current RMS current ($I_{SEC(max)}$) is

$$I_{SEC(max)} = I_{PP(nom)} \times N_{PS} = 4.862\ A \times 4.0 = 19.448\ A \tag{41}$$

The transformer secondary RMS current (I_{SRMS}) is

$$I_{SEC\_RMS} = I_{SP(max)} \times \sqrt{\frac{D_{MAG}}{3}} = 19.448 \times \sqrt{\frac{0.425}{3}} = 7.32\ A \tag{42}$$

Based on these calculations, a Würth Electronik transformer was designed for this application (part number 750343004), which has the following specifications:

- N_{PS} = 4.0
- N_{PA} = 5.6
- L_P = 160 µH
- L_{LK} = 3.5 µH (which denotes the primary leakage inductance)

4.4.4 Main Switching Power MOSFET Selection

The drain-to-source RMS current, I_{DS_RMS}, through switching FET is calculated as

$$I_{DS\_RMS} = \frac{I_{PP(max)}}{\sqrt{3}} \times \sqrt{D_{MAX}} = \frac{5.094}{\sqrt{3}} \times \sqrt{0.264} = 1.511 \text{ A} \tag{43}$$

It is recommend to select a MOSFET with 5 times the I_{DS_RMS} calculated.

The maximum voltage across the FET can be estimated using Equation 29. Considering a de-rating of 25%, the voltage rating of the MOSFET should be 650-V DC.

The AOTF11S65L MOSFET of 650 V and 11 A at 25°C / 8 A at 100°C is selected for this design.

The recommended clamping voltage on drain is

$$V_{DRAIN\_Clamp} = 0.95 \times V_{DS} - \left(\sqrt{2} \times V_{IN(max)} + N_{PS} \times (V_{OCV} + V_F + V_{OCBC}) \right) \tag{44}$$

$$V_{DRAIN\_Clamp} = 0.95 \times 650 \text{ V} - \left(\sqrt{2} \times 265 \text{ V} + 4.0 \times (26.42565 \text{ V}) \right) = 137.1 \text{ V}$$

4.4.5 Rectifying Diode and Synchronous Rectification MOSFET Selection

Calculate secondary output diode or synchronous rectifier FET reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$):

$$V_{DIODE\_BLOCKING} = \frac{\sqrt{2} \times V_{IN(max)} + V_{DRAIN\_Clamp}}{N_{PS}} + V_{OUT\_OVP} + V_{OCBC} \tag{45}$$

$$V_{DIODE\_BLOCKING} = \frac{\sqrt{2} \times 265 \text{ V} + 137.1 \text{ V}}{4.0} + 30 \text{ V} + 0.02565 \text{ V} = 157.98 \text{ V}$$

The required minimum average rectified output current is

$$I_{DOUT} = I_{SEC\_RMS} = 7.319 \text{ A} \tag{46}$$

A synchronous rectifier FET is recommended for low power loss and high efficiency needs. For this design, the IRFI4227PBF-ND is selected optimizing the on-state losses.

4.4.6 Select Output Capacitors

For this design the output capacitor (C_{OUT}) for output was selected to prevent V_{OUT} (= 26 V) from dropping below the minimum output voltage (V_{OTRM}) during transients' up to 0.30 ms and ripple voltage less than 50 mV.
$V_{OTRM} = 25.7 \text{ V}$

$$C_{OUT} \geq \frac{\dfrac{I_{OUT}}{2} \times (t)}{V_{OUT} - V_{OTRM}} \tag{47}$$

$$C_{OUT} \geq \frac{\dfrac{3.8 \text{ A}}{2} \times (0.30 \text{ ms})}{(26 - 25.7)} = 1900 \text{ }\mu\text{F}$$

Considering the allowable output ripple voltage of 120 mV (5%), the ESR of the capacitor should be

$$ESR = \frac{V_{OUT\_RIPPLE}}{I_{SEC(max)}} = \frac{120 \text{ mV}}{19.448 \text{ A}} = 6.17 \text{ m}\Omega \tag{48}$$

$$I_{COUT\_RMS} = \sqrt{(I_{SEC\_RMS})^2 - (I_{OUT})^2} = \sqrt{(7.319)^2 - (3.8)^2} = 6.255 \text{ A} \tag{49}$$

A 1200-µF × 2, 35-V capacitor was selected on the output. A post LC filter is used to suppress the common mode noise at the output.

4.4.7 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation.

The capacitance on VDD must supply the primary-side operating current used during startup and between low frequency switching pulses. The largest result of two independent calculations denoted in Equation 50 and Equation 51 determines the value of C_{VDD}.

At startup, when $V_{VDD(on)}$ is reached, C_{VDD} alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum operating voltage in CC regulation, V_{OCC}. Now the auxiliary winding sustains VDD for the UCC28740 above UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, I_{OCC}. Equation 50 assumes that all of the output current of the converter is available to charge the output capacitance until V_{OCC} is achieved. For typical applications, Equation 50 includes an estimated $q_G f_{SW(max)}$ of average gate-drive current and a 1-V margin added to V_{VDD}.

$$C_{VDD} \geq \frac{(I_{RUN} + q_G f_{SW(max)}) \times \dfrac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{VDD(on)} - (V_{VDD(off)} + 1\,V)}$$

(50)

$$C_{VDD} \geq \frac{(1\,mA + 2.65\,mA) \times (3080\,\mu F \times 12)}{(23\,V - 8.15\,V - 1) \times 3.8\,A} = 2.56\,\mu F$$

During a worst-case un-load transient event from full-load to no-load, C_{OUT} overcharges above the normal regulation level for duration of t_{OV} until the output shunt-regulator loading is able to drain V_{OUT} back to regulation. During t_{OV}, the voltage feedback loop and optocoupler are saturated, driving maximum I_{FB} and temporarily switching at $f_{SW(min)}$. The auxiliary bias current expended during this situation exceeds that normally required during the steady-state no-load condition. Equation 51 calculates the value of C_{VDD} (with a safety factor of 2) required to ride through the t_{OV} duration until steady-state no-load operation is achieved.

$$C_{VDD} \geq \frac{2 \times I_{AUXNL(max)} \times t_{OV}}{V_{VDDFL} - (V_{VDD(off)} + 1\,V)}$$

(51)

$$C_{VDD} \geq \frac{2 \times (1.2\,mA) \times (20\,ms)}{(18.2\,V - 8.15\,V - 1)} = 5.33\,\mu F$$

To address the start-up of the converter for heavy capacitive loads (that is, around 8000 to 10,000 µF), a higher value of C_{VDD} is needed. For current design, a 10-µF capacitor is used.

4.4.8 Open-Loop Voltage Regulation versus Pin Resistor Divider, Line Compensation Resistor

The resistor divider at the VS pin determines the output voltage regulation point of the flyback converter. Also, the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(run)}}$$

(52)

where

- N_{PA} is the transformer primary-to-auxiliary turns-ratio
- $V_{IN(run)}$ is the AC$_{RMS}$ voltage to enable turn-on of the controller (run);in case of DC input, leave out the $\sqrt{2}$ term in the equation
- $I_{VSL(run)}$ is the run-threshold for the current pulled out of the VS pin during the switch on-time (see Section 6: Electrical Characteristics of the UCC28740 datasheet)

$$R_{S1} = \frac{120\text{-}V\ DC}{5.6 \times 275\,\mu A} = 77.9\,k\Omega$$

A standard resistor of 71.5 kΩ is selected.

The low-side VS pin resistor is selected based on the desired V_{OUT} regulation voltage in open-loop conditions and sets maximum allowable voltage during open-loop conditions.

$$R_{S2} = \frac{R_{S1} \times V_{OVPTH}}{N_{AS} \times (V_{OV} - V_F) - V_{OVPTH}}$$

(53)

where

- V_{OV} is the maximum allowable peak voltage at the converter output
- V_F is the output-rectifier forward drop at near-zero current
- N_{AS} is the transformer auxiliary-to-secondary turns-ratio
- R_{S1} is the VS divider high-side resistance
- V_{OVPTH} is the overvoltage detection threshold at the VS input (see Section 6: Electrical Characteristics of the UCC28740 datasheet)

$$R_{S2} = \frac{71.5 \text{ k}\Omega \times 4.6 \text{ V}}{0.714 \times (28 \text{ V} - 0.4 \text{ V}) - 4.6 \text{ V}} = 21.77 \text{ k}\Omega$$

A standard resistor of 19.6 kΩ is selected.

The UCC28740 maintains tight CC regulation over varying input line by using the line-compensation feature. The line-compensation resistor (R_{LC}) value is determined by current flowing in R_{S1} and the total internal gate-drive and external MOSFET turnoff delay. Assuming an internal delay of 50 ns in the UCC28740:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P}$$

(54)

where

- R_{CS} is the current-sense resistor value
- t_D is the current-sense delay including MOSFET turn-off delay (add ~50 ns to MOSFET delay)
- N_{PA} is the transformer primary-to-auxiliary turns ratio
- L_P is the transformer primary inductance
- K_{LC} is a current-scaling constant (see Section 6: Electrical Characteristics of the UCC28740 datasheet)

$$R_{LC} = \frac{28.6 \times 71.5 \text{ k}\Omega \times (77 \text{ ns} + 50 \text{ ns}) \times 4.0}{160 \text{ }\mu\text{H}} = 1.032 \text{ k}\Omega$$

A standard resistor of 1.21 kΩ is selected.

4.4.9 Feedback Elements

The output voltage is set through the sense-network resistors R_{FB1} and R_{FB2}. A potentiometer is used to provide flexibility of setting the range of output voltage between 23 to 26 V. The design spreadsheet has all relevant equations for characterization of the optocoupler and its adjustments of the initial values to accommodate variations of the UCC28740 (see Section 7.7). Also, using the design sheet, the shunt-regulator parameters can be optimized for overall system performance.

The shunt-regulator compensation network, Z_{FB}, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used.

4.5 Synchronous Rectifier Controller Component Design

The UCC24630 is a high-performance controller driver for N-channel MOSFET power devices used for secondary-side synchronous rectification. The UCC24630 is designed to operate as a companion device to a primary-side controller to help achieve efficient synchronous rectification in switching power supplies. The controller features a high-speed driver and provides appropriately timed logic circuitry that seamlessly generates an efficient synchronous rectification system. With its current emulator architecture, the UCC24630 has enough versatility to be applied in DCM, TM, and CCM. The UCC24630 SR on-time adjustability allows optimizing for PSR and SSR applications. Additional features such as pin fault protection, dynamic VPC threshold sensing, and voltage sense blanking time and make the UCC24630 a robust synchronous controller. CCM dead-time protection shuts off the DRV signal in the event of an unstable switching frequency.

The design procedure for selecting the component circuitry for use with the UCC24630 is detailed in the following sections.
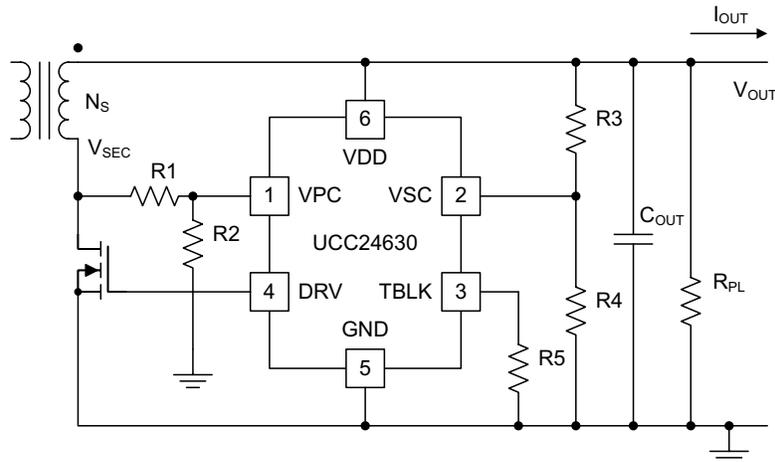
Figure 4. UCC24630 Circuit Component Design

For ease of understanding, Figure 4 is used for reference of all associated component calculations.

4.5.1 VPC Pin Elements

Determining the VPC and VSC divider resistors is based on the operating voltage ranges of the converter and Ratio$_{VPC\_VSC}$ gain ratio. Referring to Figure 4, the following equation determines the VPC divider values. For R2, a value of 10 kΩ is recommended for minimal impact on time delay and low-resistor dissipation. A higher R2 value reduces resistor divider dissipation but may increase the DRV turn-on delay due to the time constant of ~2 pF pin capacitance and divider resistance. A lower R2 value can be used with the tradeoff of higher dissipation in the resistor divider. A factor of 10% over the VPC threshold, V_{VPCEN}, is shown in Equation 55 for design margin.

For minimal power dissipation: R2 = 10 kΩ.

$$R_1 = \frac{\frac{V_{IN(min)}}{N_{PS}} + V_{OUT(min)} - V_{VPC\_EN} \times 1.1}{V_{VPCC\_EN}} \times R_2$$

(55)

where

- $V_{IN(min)}$ is the converter minimum primary bulk capacitor voltage
- $V_{OUT(min)}$ is the minimum converter output voltage in normal operation
- V_{VPCEN} is the VPC enable threshold, use the specified maximum value
- N_{PS} is the transformer primary-to-secondary turns ratio

$$R_1 = \frac{\dfrac{55}{4.0} + 22\ V - 0.45\ V \times 1.1}{0.45\ V} \times 10\ k\Omega = 783.3\ k\Omega$$

A standard resistor of 750 kΩ is selected.

The operating voltage range on the VPC pin should be within the range of 0.45 V < V_{VPC} < 2 V. Referring to Figure 4, if V_{VPC} is greater than 2.3 V, the dynamic range is exceeded and Ratio$_{VPC\_VSC}$ is reduced; in this condition, the DRV on-time is less than expected. If V_{VPC} is greater than 2.6 V for 500 ns, a fault is generated and DRV is disabled for the cycle (see Section 7.3.5: Pin Fault Protection of the UCC24630 datasheet). To ensure the maximum voltage is within range, confirm with Equation 56 (for $V_{VPC(min)}$, substitute $V_{IN(max)}$ and $V_{OUT(max)}$ for $V_{IN(min)}$ and $V_{OUT(min)}$, respectively).

$$V_{VPC(max)} = \frac{\left(\dfrac{V_{IN(max)}}{N_{PS}} + V_{OUT(max)}\right) \times R2}{R1 + R2} \tag{56}$$

where

- $V_{IN(max)}$ is the converter maximum primary bulk capacitor voltage
- $V_{OUT(max)}$ is the maximum converter output voltage at OVP
- N_{PS} is the transformer primary-to-secondary turns ratio

$$V_{VPC(max)} = \frac{\left(\dfrac{410}{4.0} + 30\ V\right) \times 10\ k\Omega}{760\ k\Omega} = 1.743\ V$$

$$V_{VPC(min)} = \frac{\left(\dfrac{60}{3.9} + 22\ V\right) \times 10\ k\Omega}{760\ k\Omega} = 0.492\ V$$

Therefore, V_{VPC} is within the recommended range of 0.45 to 2 V.

4.5.2 VSC Pin Elements

The program voltage on the VSC pin is determined by the VPC divider ratio and the device's parameter Ratio$_{VPC\_VSC}$. The current emulator ramp gain is higher on the VPC pin by the multiple Ratio$_{VPC\_VSC}$, so the VSC resistor divider ratio is reduced by the same Ratio$_{VPC\_VSC}$ accordingly. Determine the VSC divider resistors using Equation 57. To minimize resistor divider dissipation, a recommended range for R4 is 25 to 50 kΩ. Higher R4 values results in increasing offset due to VSC input current, I_{VSC}. Lower R4 values increases the resistor divider dissipation. To ensure DRV turn off slightly before the secondary current reaches zero, 10% margin is shown for initial values.

A standard resistor of 47.5 kΩ is selected for R4.

$$R3 = \left(\left(\frac{\dfrac{R1 + R2}{R2}}{\text{Ratio}_{VPC\_VSC} \times 1.1}\right) - 1\right) \times R4 \tag{57}$$

where

- Ratio$_{VPC\_VSC}$ is the device parameter VPC and VSC gain ratio, use a value of 4.15

$$R3 = \left(\left(\frac{\dfrac{(750 + 10)\ k\Omega}{10\ k\Omega}}{4.15 \times 1.1}\right) - 1\right) \times 47.5\ k\Omega = 743.3\ k\Omega$$

A standard resistor of 750 kΩ is selected for R3.

The operating voltage on the VSC pin should be within the range of 0.3 V < V_{VSC} < 2 V. Referring to Figure 4, if V_{VSC} is greater than 2.3 V, the dynamic range is exceeded and $Ratio_{VPC\_VSC}$ is increased; in this condition the DRV on time is more than expected. To ensure the VSC pin voltage is within range, confirm with Equation 58 and Equation 59.

$$\frac{R4}{R3 + R4} \times V_{OUT(min)} \geq 0.3 \text{ V} \tag{58}$$

$$\frac{R4}{R3 + R4} \times V_{OUT(max)} \leq 2.0 \text{ V} \tag{59}$$

where

- $V_{OUT(min)}$ is the minimum converter output operating voltage of the SR controller
- $V_{OUT(max)}$ is the maximum converter output operating voltage of the voltage at OVP

$$V_{VSC(max)} = \frac{(10 \text{ k}\Omega) \times 30 \text{ V}}{760 \text{ k}\Omega} = 0.394 \text{ V}$$

$$V_{VSC(min)} = \frac{(10 \text{ k}\Omega) \times 22 \text{ V}}{760 \text{ k}\Omega} = 0.289 \text{ V}$$

Therefore, V_{VSC} is within the recommended range of 0.3 to 2 V.

4.5.3 t_{BLK} Input

The blanking time is set with resistor R5. Select the blanking time to meet the following criteria based on minimum primary on-time at high line.

$$t_{VPC\_BLK} = (t_{PRI} \times 0.85) - 120 \text{ ns} = (650 \text{ ns} \times 0.85) - 120 \text{ ns} = 432.5 \text{ ns} \tag{60}$$

To determine the resistor value for t_{VPC_BLK}, use Equation 61 to select from a range of 200 ns to 1 μs.

$$R5 = \frac{t_{VPC\_BLK} - 100 \text{ ns}}{18 \text{ pF}} \tag{61}$$

where

- t_{VPC_BLK} is the target blanking time

$$R5 = \frac{(432.5 \text{ ns} - 100 \text{ ns})}{18 \text{ pF}} = 18.47 \text{ k}\Omega$$

A standard resistor of 18 kΩ is selected.

4.6 *LM5050-2 ORing Circuit Component Design*

The important MOSFET electrical parameters are the maximum continuous drain current ID, the maximum source current (that is, the body diode), the maximum drain-to-source voltage $V_{DS(max)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source ON resistance $R_{DS(on)}$. The maximum continuous drain current, ID, rating must be exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as or slightly higher than the drain current, but the body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$:

$$\text{Gate charge time} = \frac{Q_g}{I_{GATE(on)}}$$

(62)

The maximum drain-to-source voltage, $V_{DS(max)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the LM5050 gate drive capabilities. Logic level MOSFETs are recommended, but sub-Logic level MOSFETs can also be used.

The dominate MOSFET loss for the LM5050 active ORing controller is conduction loss due to source-to-drain current to the output load and the $R_{DS(on)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(on)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(on)}$ may not always give desirable results for several reasons:

- Reverse transition detection: A higher $R_{DS(on)}$ will provide increased voltage information to the LM5050 reverse comparator at a lower reverse current level. This will give an earlier MOSFET turn-off condition should the input voltage become shorted to ground. This will minimize any disturbance of the redundant bus.
- Reverse current leakage: In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse) without activating the LM5050 reverse comparator. A higher $R_{DS(on)}$ will reduce this reverse current level. Selecting a MOSFET with an $R_{DS(on)}$

Selecting a MOSFET with an $R_{DS(on)}$ that is too large will result in excessive power dissipation. Additionally, the MOSFET gate will be charged to the full value that the LM5050 can provide as it attempts to drive the drain-to-source voltage down to the $V_{SD(REG)}$ of 20 mV (typical). This increased gate charge will require some finite amount of additional discharge time when the MOSFET needs to be turned off.

As a guideline, select $R_{DS(on)}$ to provide at least 20 mV and no more than 100 mV at the nominal load current.

$$\left(\frac{20\ mV}{I_D}\right) \leq R_{DS(on)} \leq \left(\frac{100\ mV}{I_D}\right)$$

(63)

Based on this analysis, the CSD18504Q5A is selected for this design.

To calculate power dissipation in MOSFET:

$$P_{DISS} = I_D{}^2 \times R_{DS(on)}\ max = 3.8\ A^2 \times 6.6\ m\Omega = 95.3\ mW$$

(64)

5   Getting Started Hardware

5.1   Test Equipment Needed for Board Validation

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multi-meters
- Electronic or resistive load

5.2   Test Conditions

Input Voltage Range
The AC source should be capable of varying between V_{INAC}: 85- and 265-V AC. Set input current limit to 2.5 A.

Output
Connect an electronic load capable of 40 V and a load variable in range from 0 to 6 A. A rheostat or resistive decade box can be used in place of an electronic load.

5.3   Test Procedure

1. Connect the AC source at input terminals (Pin-2,3 of connector J1) of the reference board.
2. Connect output terminals (Pin-3,4 and Pin-1,2 of connector J2) to electronic load or rheostat, maintaining correct polarity. Pin-3,4 are V_{OUT} output terminal pins, and Pin-1,2 are GND terminal pins.
3. Set and maintain a minimum load of about 10 mA.
4. Increase gradually the input voltage from 0 V to turn on voltage of 85-V AC.
5. Turn on the load to draw current from the output terminals of the converter.
6. Observe the startup conditions for smooth switching waveforms.

6 Test Results

The test results are divided into multiple sections that cover the steady state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, conducted emission measurements, and Surge and EFT measurements.

6.1 Performance Data

6.1.1 Efficiency and Regulation With Load Variation

Table 4 shows the efficiency, power factor and regulation performance data at a 115-V AC input, for both CV and CC operation.

Table 4. Efficiency and Regulation Performance at 115-V AC Input

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)
CV OPERATION							
115	0.08	0.87	7.8	24.0	0.26	6.2	78.5
115	0.13	0.96	14.5	24.0	0.51	12.2	83.7
115	0.25	0.99	27.8	24.0	1.00	24.1	86.5
115	0.48	1.00	55.0	24.0	2.01	48.2	87.6
115	0.71	1.00	81.9	23.9	3.01	72.0	87.8
115	0.91	1.00	104.1	23.9	3.83	91.5	87.9
CC OPERATION							
115	0.84	1.00	96.1	22.0	3.83	84.4	87.9
115	0.76	1.00	87.5	20.0	3.84	76.9	87.9
115	0.69	1.00	78.9	18.0	3.85	69.3	87.8
115	0.61	1.00	70.4	16.0	3.85	61.6	87.5
115	0.96	0.57	62.8	14.0	3.88	54.3	86.4

Table 5 shows the efficiency, power factor, and regulation performance data at a 230-V AC input, for both CV and CC operation.

Table 5. Efficiency and Regulation Performance at 230-V AC Input

V_{INAC} (V)	I_{INAC} (A)	PF	P_{INAC} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	EFF (%)
CV OPERATION							
230	0.06	0.60	8.1	24.0	0.26	6.2	76.2
230	0.09	0.69	14.6	24.0	0.51	12.2	83.6
230	0.14	0.87	27.9	24.0	1.00	24.1	86.3
230	0.25	0.95	54.4	24.0	2.01	48.1	88.5
230	0.36	0.97	80.9	23.9	3.01	71.9	88.9
230	0.45	0.98	102.5	23.9	3.83	91.6	89.3
CC OPERATION							
230	0.42	0.98	94.5	22.0	3.83	84.3	89.2
230	0.38	0.98	86.3	20.0	3.84	76.8	88.9
230	0.35	0.97	78.0	18.0	3.84	69.1	88.6
230	0.31	0.97	69.7	16.0	3.84	61.5	88.2
230	0.56	0.47	61.0	14.0	3.85	53.8	88.2

6.1.2   Standby Power

The standby power was noted at multiple AC input voltages with a constant negligible load on output DC bus and with PFC controller enabled and disabled. The results are tabulated in Table 6.

Table 6. Standby Power Loss of Converter

V_{INAC} (VAC)	I_{INAC} (mA)	P_{INAC} (W)	V_{OUT} (V)
115	11	0.14	24
230	21	0.37	24

No load power is contributed by:
• Resistors used for X-capacitor discharge
• Operation of PFC and flyback controllers

Standby power can be further optimized by shutting down the PFC power stage during no-load operation.

6.2   *Performance Curves*

6.2.1   Efficiency and Power Factor With Load and Line Variation

Figure 5 and Figure 6 show the measured efficiency of the system with AC input voltage variation during CV and CC operations, respectively.
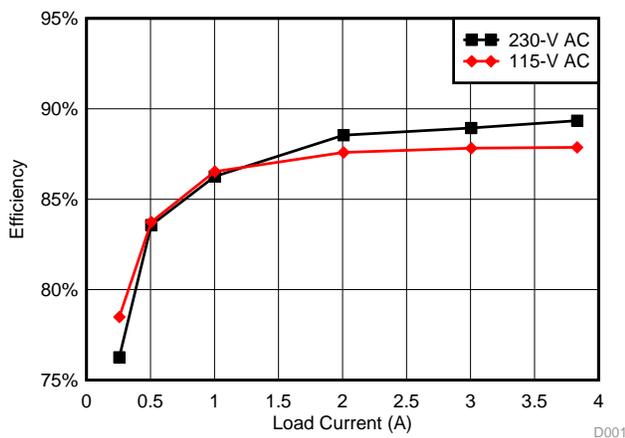
Figure 5. Efficiency versus Output Load Current in CV Mode
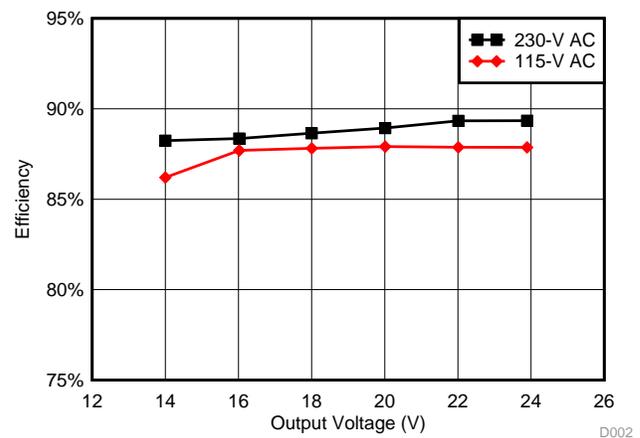
Figure 6. Efficiency versus Output Voltage in CC Mode

Figure 7 shows the measured input power factor with AC input voltage variation in CV operation mode.
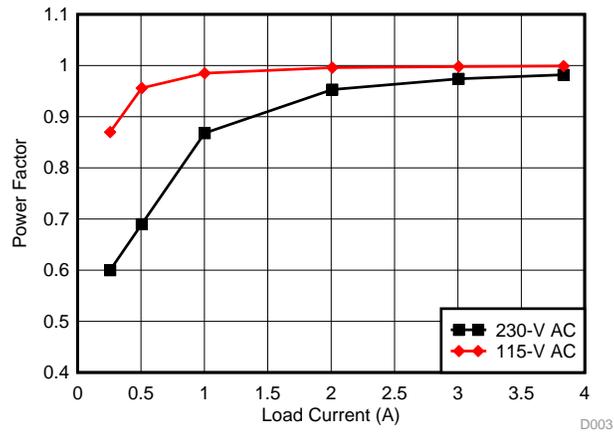
Figure 7. Input Power Factor versus Output Load Current in CV Mode

6.2.2 Load Regulation in CV and CC Modes

Figure 8 and Figure 9 show the measured load regulation of the PSU with AC input voltage variation.
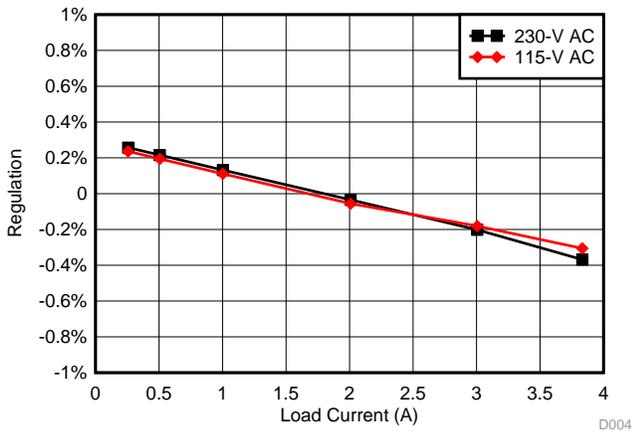
Figure 8. Output Voltage Variation With Load Current in CV Mode
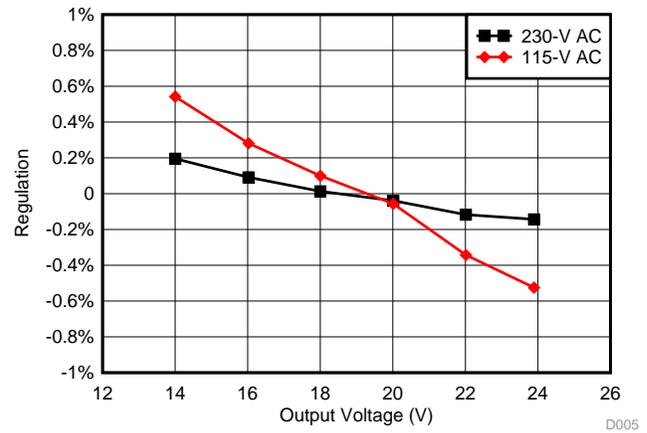
Figure 9. Output Current Variation With Load Voltage in CC Mode

6.2.3 AC Line Regulation and Efficiency With AC Input Voltage Variation

Figure 10 shows the efficiency of the PSU with AC line voltage variation, and Figure 11 shows the output voltage regulation with AC line voltage variation.
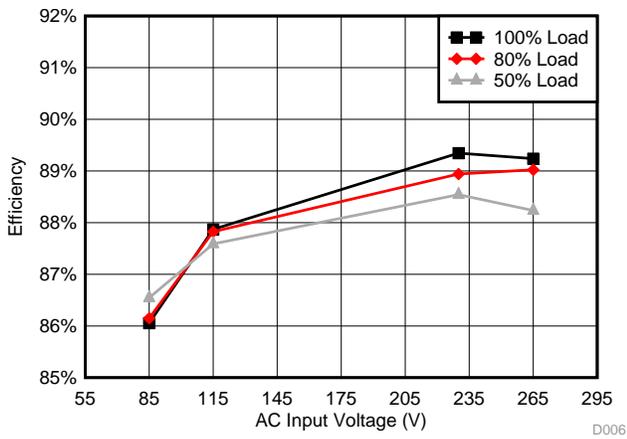
Figure 10. Efficiency Variation With Input AC Voltage in CV Mode
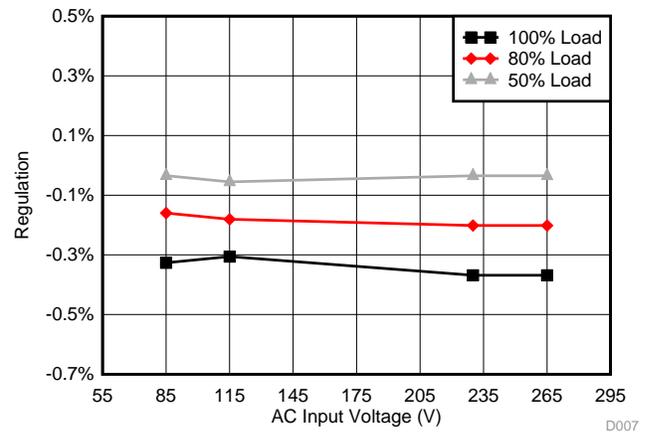
Figure 11. Load Voltage Variation With Input AC Voltage in CV Mode

6.2.4 CC-CV Operation, Power Limit, and Foldback

Figure 12 shows the transition between CV and CC modes, and Figure 13 shows the power limiting feature of the converter with output voltage foldback for high load conditions.
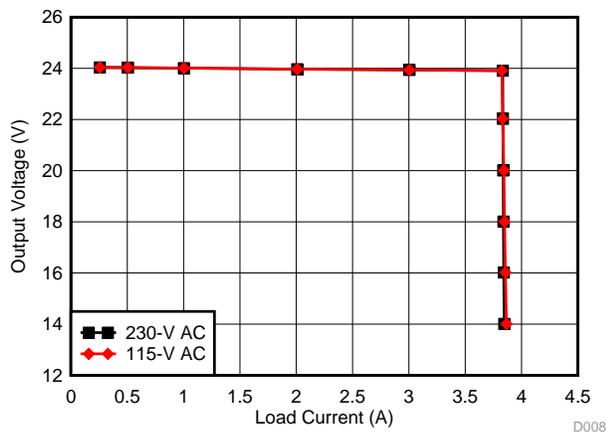
Figure 12. CC-CV Operation
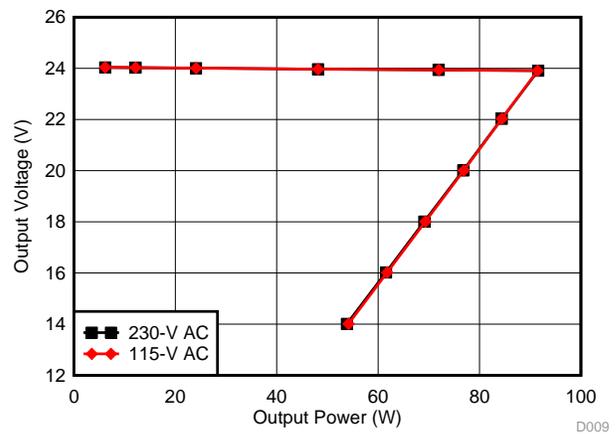
Figure 13. Power Limit and Foldback Characteristics

6.3 Functional Waveforms

6.3.1 Switching Node Waveforms

Waveforms at the PFC switching node were observed along with the MOSFET current for 115- and 230-V AC under full load (3.8 A) conditions.

Figure 14 shows the PFC switching node waveform and MOSFET current at input voltage equal to 115-V AC and full load. Figure 15 shows the PFC switching node waveform and MOSFET current at input voltage equal to 230-V AC and full load.
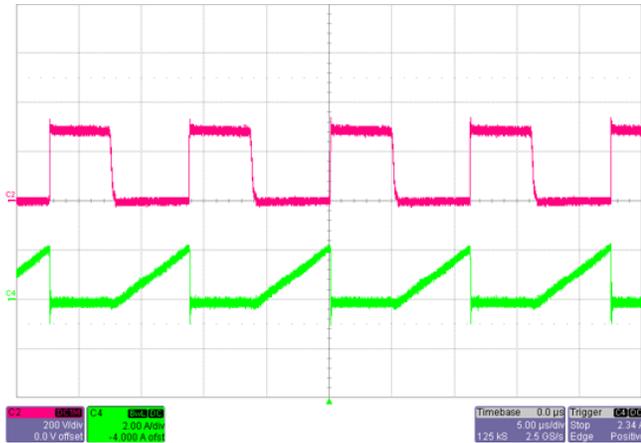
Figure 14. PFC Switching Node Waveform and MOSFET Current at V$_{INAC}$ = 115-VAC, Full Load
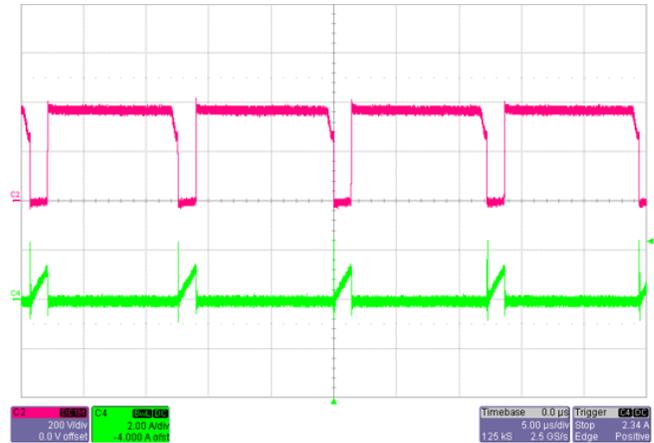
Figure 15. PFC Switching Node Waveform and MOSFET Current at V$_{INAC}$ = 230-VAC, Full Load

NOTE: Red trace: Drain voltage, 200 V/div; Green trace: Drain current, 2 A/div

Waveforms at flyback switching node were observed along with the MOSFET current for 115- and 230-V AC under full load (3.8 A) conditions.

Figure 16 shows the flyback converter switching node waveform and MOSFET current at input voltage equal to 115-V AC and full load. Figure 17 shows the flyback converter switching node waveform and MOSFET current at input voltage equal to 230-V AC and full load.
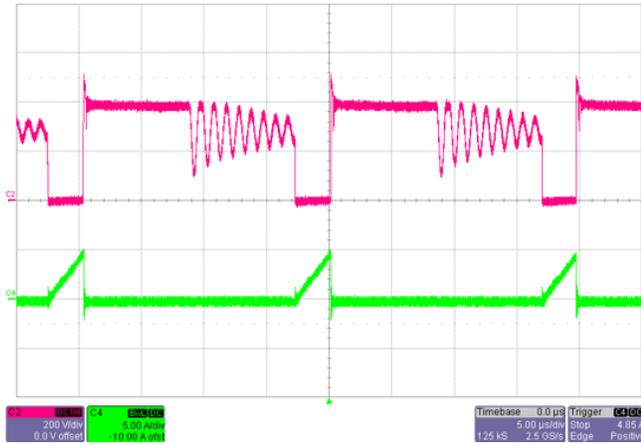
Figure 16. Flyback Converter Switching Node Waveform and MOSFET Current at V_{INAC} = 115-V AC, Full Load
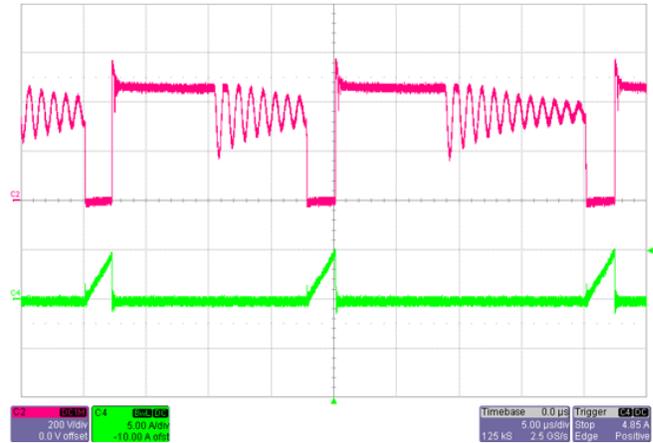
Figure 17. Flyback Converter Switching Node Waveform and MOSFET Current at V_{INAC} = 230-V AC, Full Load

NOTE: Red trace: Drain voltage, 200 V/div; Green trace: Drain current, 5 A/div

6.3.2 Output Synchronous Rectifier Drain-to-Source Voltage (V_DS) Waveforms

Waveforms at secondary output across the synchronous rectifier were observed at both 115- and 230-V AC under full load (2.5 A) conditions. The maximum voltage across the synchronous switching FET is well within the maximum V_{DS} breakdown voltage of FET (200 V).

Figure 18 shows the synchronous rectifier FET switching node waveform and MOSFET current at input voltage equal to 115-V AC and full load. Figure 19 shows the synchronous rectifier FET switching node waveform and MOSFET current at input voltage equal to 230-V AC and full load.
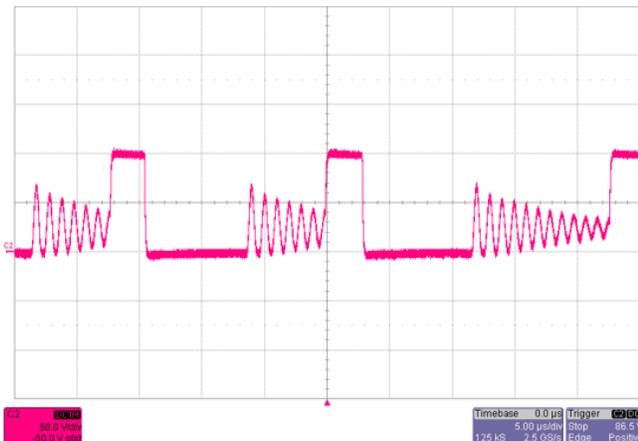
Figure 18. Output Synchronous FET Drain-to-Source (V_DS) Waveform at V_INAC = 115-V AC, Full Load
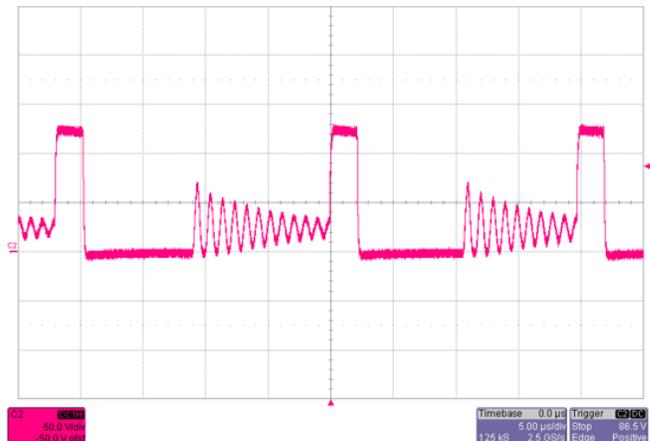
Figure 19. Output Synchronous FET Drain-to-Source (V_DS) Waveform at V_INAC = 230-V AC, Full Load

NOTE: Red trace: Drain-to-source voltage, 50 V/div

6.3.3 Inrush Current Waveform

Inrush current drawn by the system is observed and recorded at maximum input voltage of 230-V AC. The corresponding waveform can be seen in Figure 20.
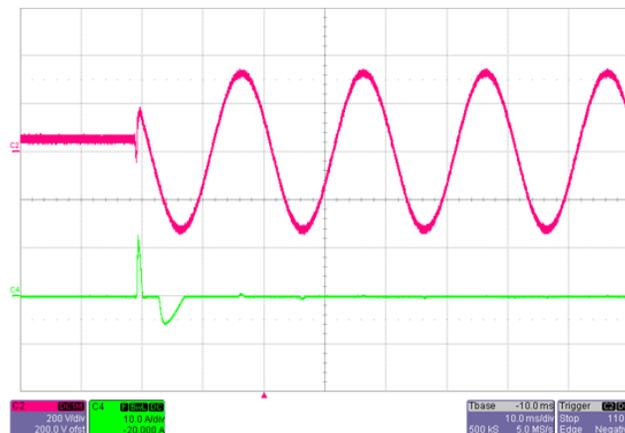
Figure 20. Input Voltage and Input Inrush Current at V_INAC = 230 V, Full Load

NOTE: Red trace: Drain voltage, 200 V/div; Green trace: Drain current, 10 A/div

6.3.4   Input Voltage and Current Waveform

Figure 21 and Figure 22 show the input current waveform at 115- and 230-V AC, respectively, under full load condition.
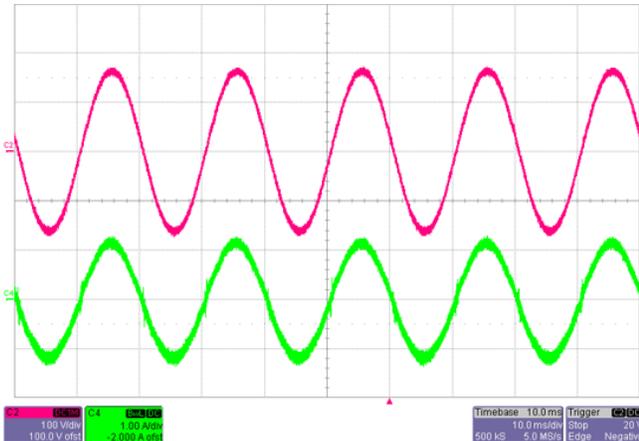
Figure 21. Input Voltage and Current Waveforms at V$_{INAC}$ = 115 V, Full Load
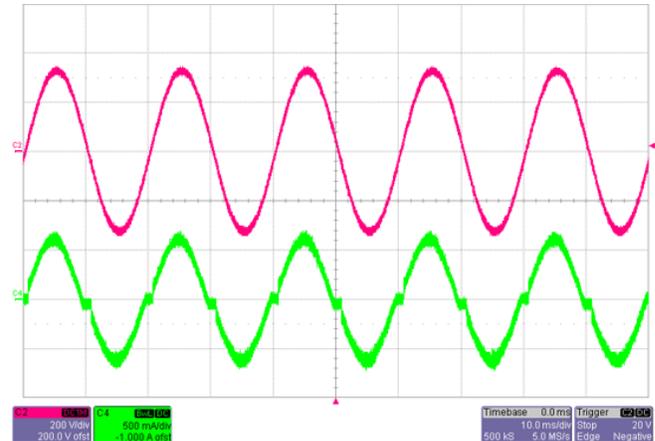
Figure 22. Input Voltage and Current Waveforms at V$_{INAC}$ = 230 V, Full Load

NOTE: Red trace: Drain voltage, 100 V/div; Green trace: Drain current, 1 A/div

6.3.5   Output Ripple

The output voltage ripple is observed at 24-V DC output and full load of 3.8 A, at both 115- and 230-V AC.

Figure 23 and Figure 24 show the output voltage ripple under full load condition at 115- and 230-V AC inputs, respectively. The peak-to-peak ripple voltage is less than 20 mV.
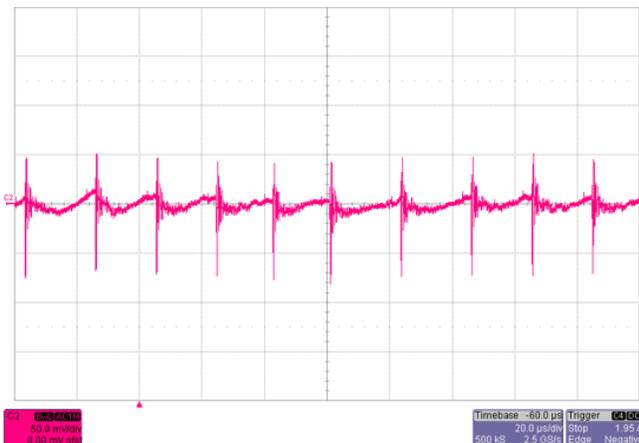
Figure 23. Output Voltage Ripple at V$_{INAC}$ = 115 V and Full Load
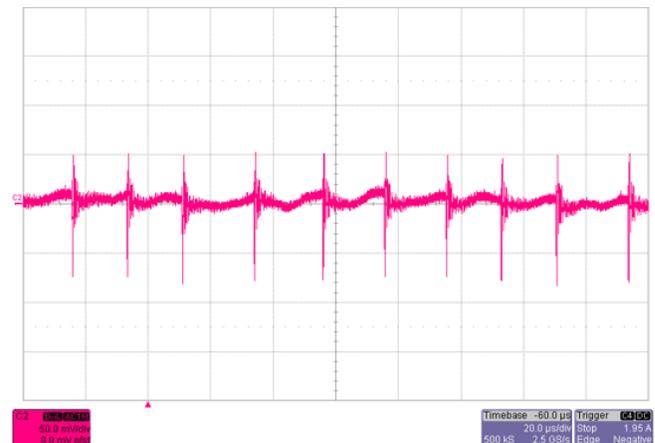
Figure 24. Output Voltage Ripple at V$_{INAC}$ = 230 V and Full Load

NOTE: Red trace: Output voltage in AC coupling mode, 50 mV/div

6.4   Transient Waveforms

6.4.1   Turn-On Characteristics

The 24-V output turn on at full load (3.8 A) was recorded with resistive load at 115- and 230-V AC. Figure 25 and Figure 26 show the output voltage and current waveforms during startup with resistive load (full load) at input voltage of 115- and 230-V AC, respectively.
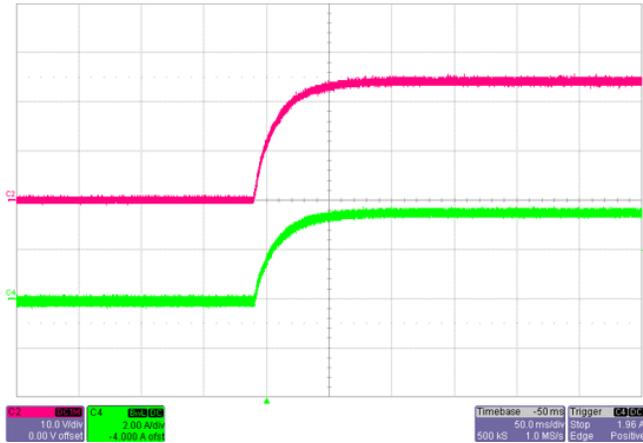
| Figure 25. Output Turn ON Waveform at V_{INAC} = 115 V and Resistive Load of 6.3 Ω | Figure 26. Output Turn ON Waveform at V_{INAC} = 230 V and Resistive Load of 6.3 Ω |
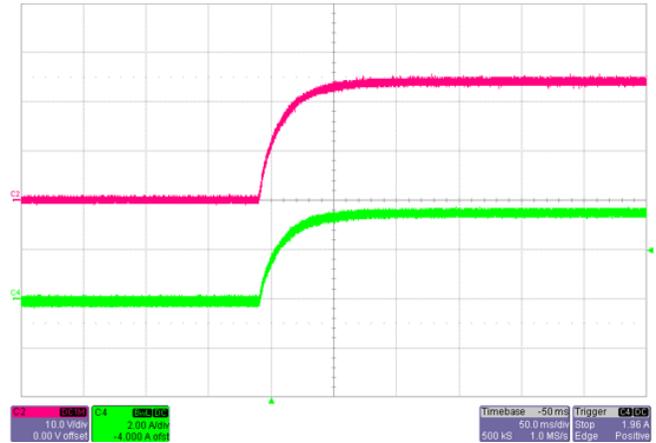
NOTE: Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div

6.4.2   Turn-On Characteristics With Heavy Capacitive Load of 8700 µF

Turn-on performance was observed with heavy capacitive load by adding additional capacitance of 8700 µF externally. The behavior was recorded at no load and full load conditions the corresponding waveforms are shown in Figure 27 and Figure 28, respectively.
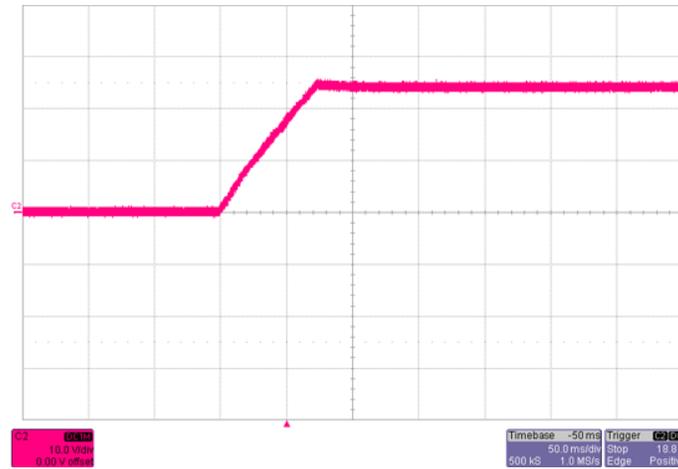
Figure 27. Output Turn ON Waveform With Additional 8700-µF Capacitance at Output and No Load

NOTE: Red trace: Output voltage, 10 V/div
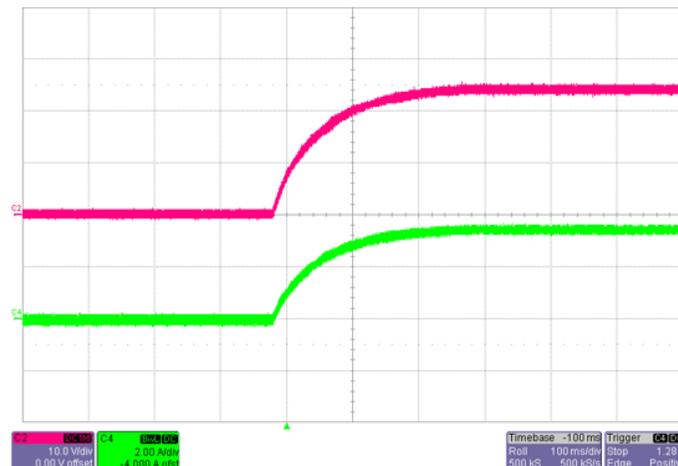
Figure 28. Output Turn ON Waveform With Additional 8500-µF Capacitance at Output and Resistive Load of 6.3 Ω

NOTE: Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div

6.4.3 Hold-up Time and Startup Delay Characteristics

Hold-up time was observed at 115- and 230-V AC under full load conditions. The unit can support full load operation for > 30 ms at 115-V AC and > 50 ms at 230-V AC operation.

Figure 29 and Figure 30 show the hold-up time waveforms under full load at input voltage of 115- and 230-V AC, respectively.
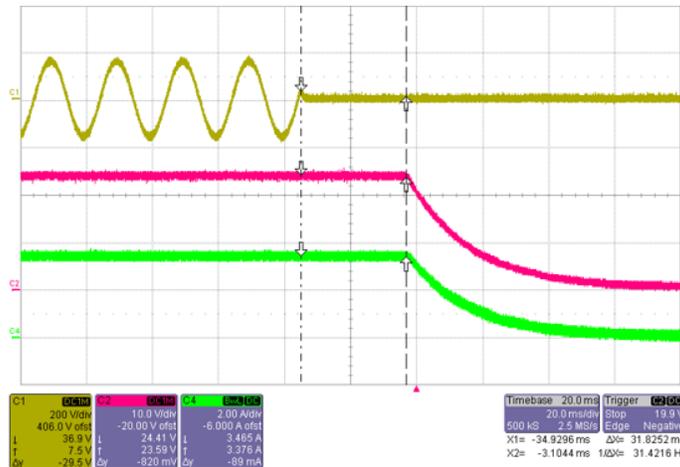
Figure 29. Hold-Up Time at 115-V AC

NOTE: Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div; Yellow trace: Input AC voltage: 200 V/div.
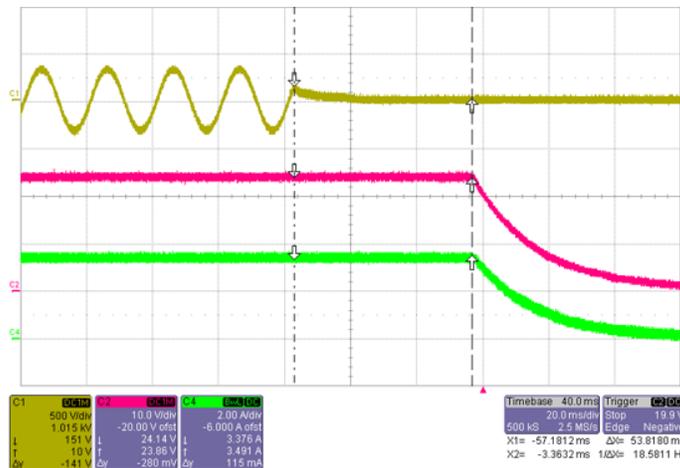
Figure 30. Hold-Up Time at 230-V AC

NOTE: Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div; Yellow trace: Input AC voltage: 500 V/div.

Startup delay time was observed at 115- and 230-V AC under no load conditions. Delay measured is shown in Figure 31 and Figure 32, respectively.
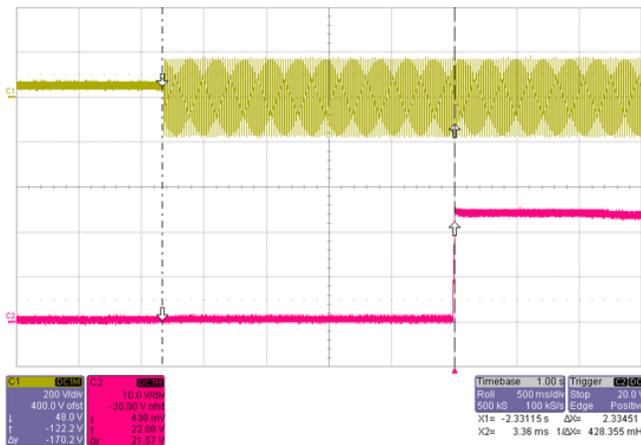
Figure 31. Startup Delay at 115-V AC
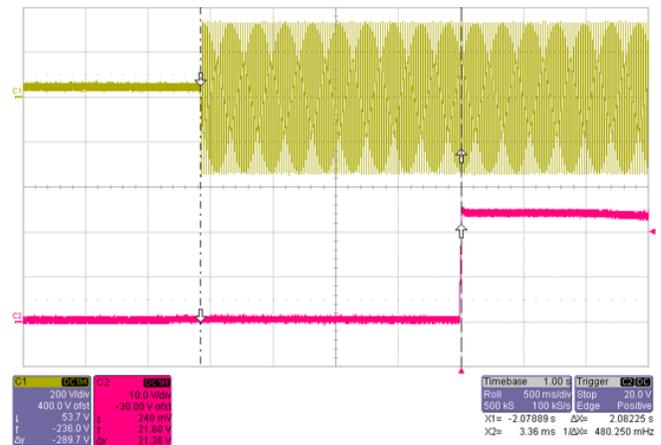
Figure 32. Startup Delay at 230-V AC

NOTE: Red trace: Output voltage, 10 V/div; Yellow trace: Input AC voltage: 200 V/div.

6.4.4 Transient Load Response

Load transient performance was observed using an electronic load with a 0.2-m wire between the converter and the load.

A load step from 0.38 to 3.43 A (10% to 100%) and vice-versa was applied at the output when the converter was operating at an input voltage of 230-V AC and an output voltage of 24-V DC. Figure 33 and Figure 34 show the output voltage transients under load step-up and load step-down, respectively.
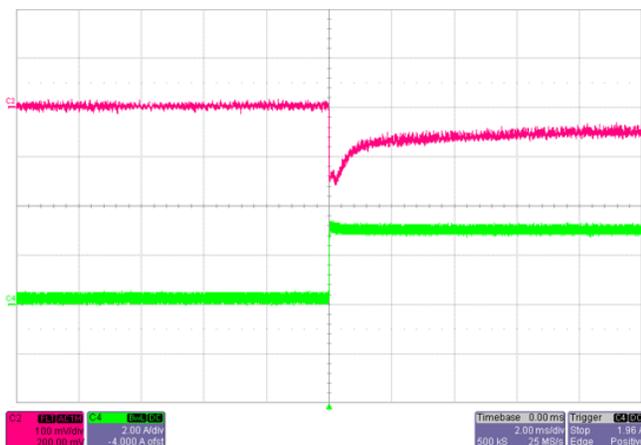
Figure 33. Output Voltage Waveform, Load Transient From 0.38 to 3.43 A
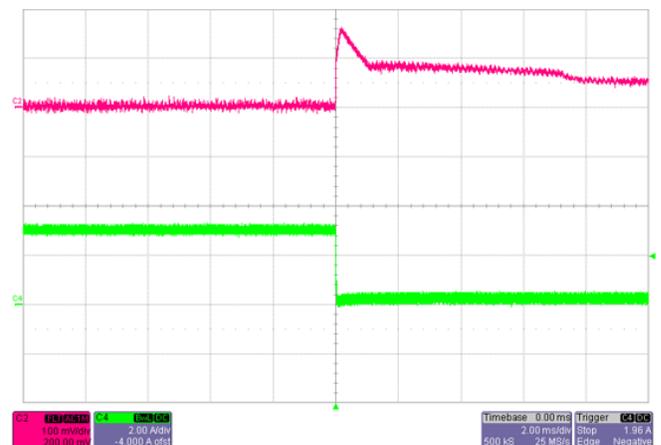
Figure 34. Output Voltage Waveform, Load Transient From 3.43 A to 0.38 A

NOTE: Red trace: Output voltage, 100 mV/div, AC coupling; Green trace: Output current, 2 A/div.

6.4.5 Overload Response

The converter was driven to an overload condition by applying a step change in load from a 50% load to a 150% resistive load. The performance of the converter output was observed and shown in Figure 35 and Figure 36.

During overload conditions, the maximum current is limited to 3.8 A and output voltage drops to regulate the power within the limits. On removal of overcurrent condition, the converter recovers back to CV operation.
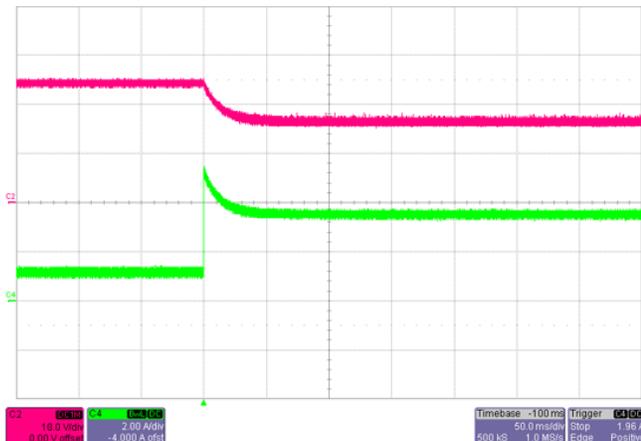
Figure 35. Output Voltage Waveform, Step Load Transient From 50% Load (17.1 Ω) to 150% Load (4.6 Ω)
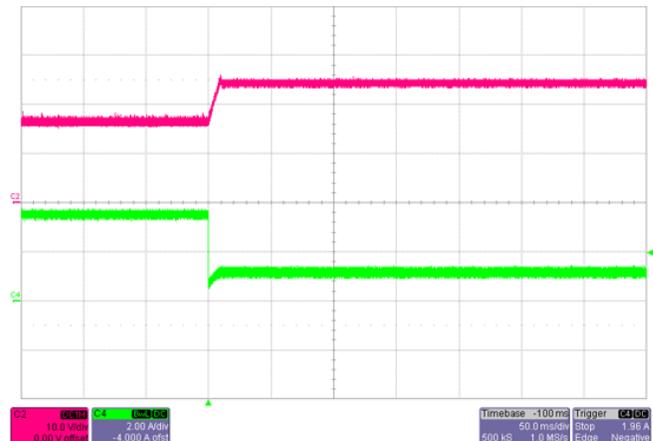
Figure 36. Output Voltage Waveform, Step Load Transient From 150% Load (4.6 Ω) to 50% Load (17.1 Ω)

NOTE: Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div.

6.4.6 Short-Circuit Response

A short was applied and removed to observe the output turn-off and auto-recovery cycle. When the short is applied, the converter shuts down and goes into hiccup mode. When the short is removed, the converter recovers back to normal. Figure 37 shows the output voltage and current waveform under short circuit and recovery when operating at an input voltage of 230-V AC and output voltage of 24-V DC.
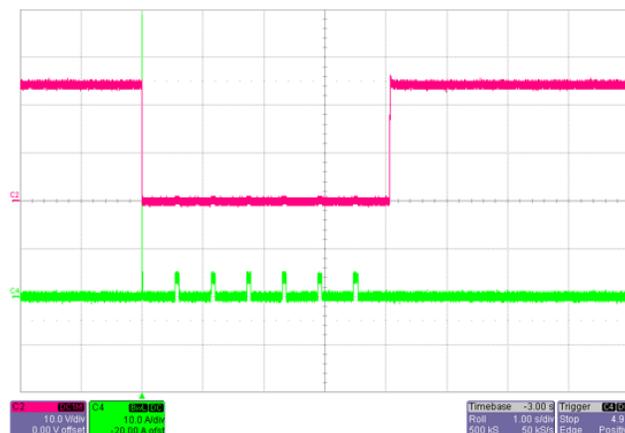
Figure 37. Response During Short Circuit and Auto-Recovery When Short is Removed

NOTE: Red trace: Output voltage, 10 V/div; Green trace: Output current, 10 A/div.

6.5 Conducted Emissions

Generally, conducted emissions will be more at full load. As a result, this operating point is chosen for measuring conducted EMI.

The test was performed at an input voltage of 230-V AC and with a 3.8-A resistive load connected to PSU output using short leads. The conducted emissions in a pre-compliance test setup were compared against EN55011 class-B limits and found to meet the Class-B limits comfortably. The results of the test are shown in Figure 38.
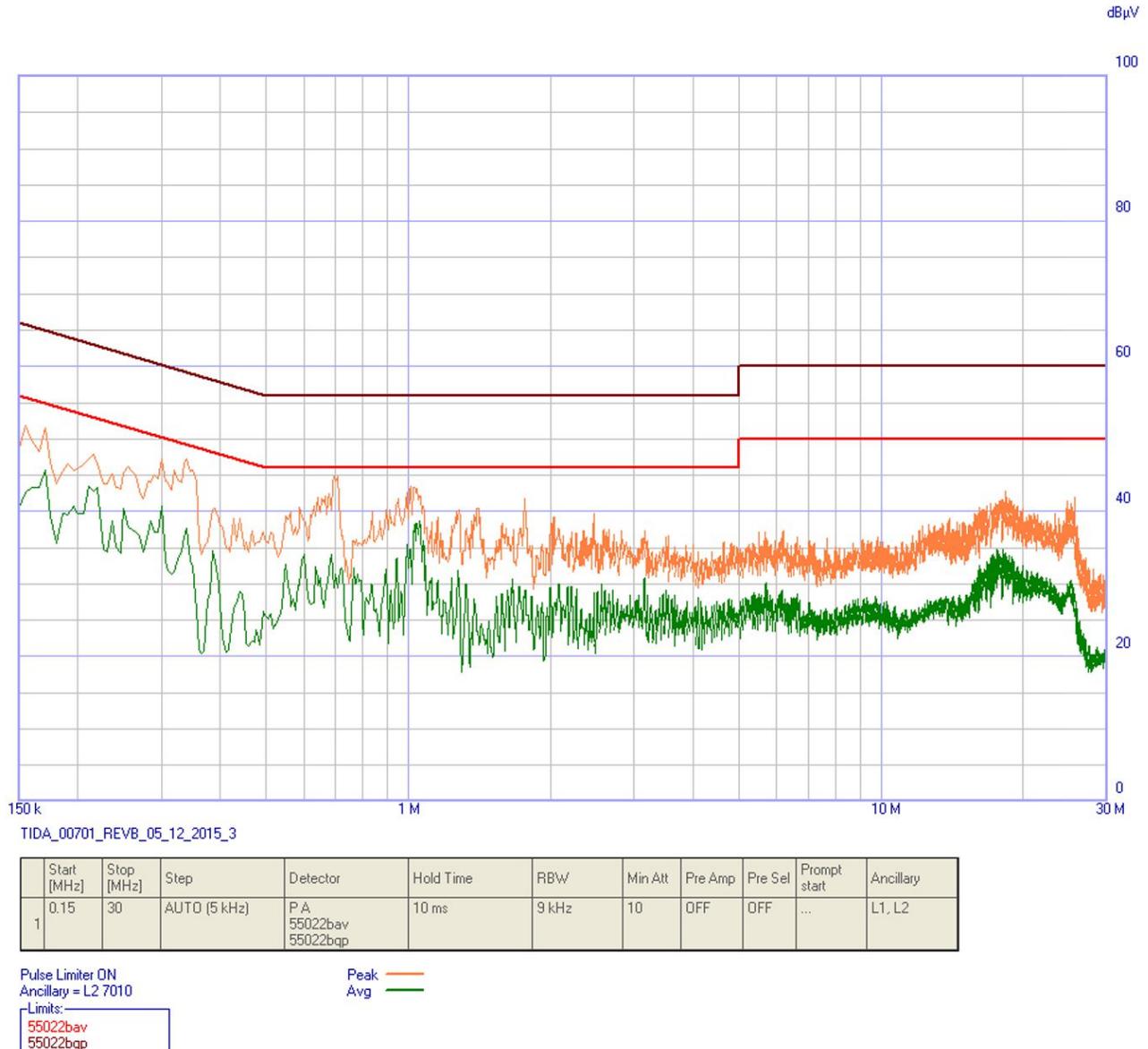
Figure 38. Conducted Emissions as per EN55011 Class B

6.6 Surge and EFT Test

Surge and EFT testing is done on the boards as per EN55014. The test condition and test results are tabulated in Table 7.

Table 7. Surge and EFT Test Results

BASIC STANDARD	PORT	REQUIREMENTS OF IEC 61000-6-2/EN 50082-2: IMMUNITY STANDARD FOR INDUSTRIAL ENVIRONMENTS	PERFORMANCE CRITERION REQUIRED	TEST RESULT
IEC/EN 61000-4-4: EFT, Level-3	AC input	±2 kV, 5 kHz	B[1]	Passed with performance criterion A[2]
IEC/EN 61000-4-5: Surges, Level-3	AC input	±4 kV line to earth, ±2 kV line to line	B[1]	Passed with performance criterion A[2]

[1] B: Temporary loss of function or degradation of performance which ceases after the disturbance ceases
[2] A: Normal performance within limits specified by the design/manufacturer

6.7 Thermal Measurements

Thermal images were captured at room temperature (25°C) with closed enclosure, no airflow, and full load conditions. The board ran for 30 minutes before capturing these thermal images.

6.7.1 Thermal Image for Lo-Line (115-V AC) Operation

Input voltage: 115-V AC, load on 24-V DC bus is 3.8 A, 91.2-W power output.
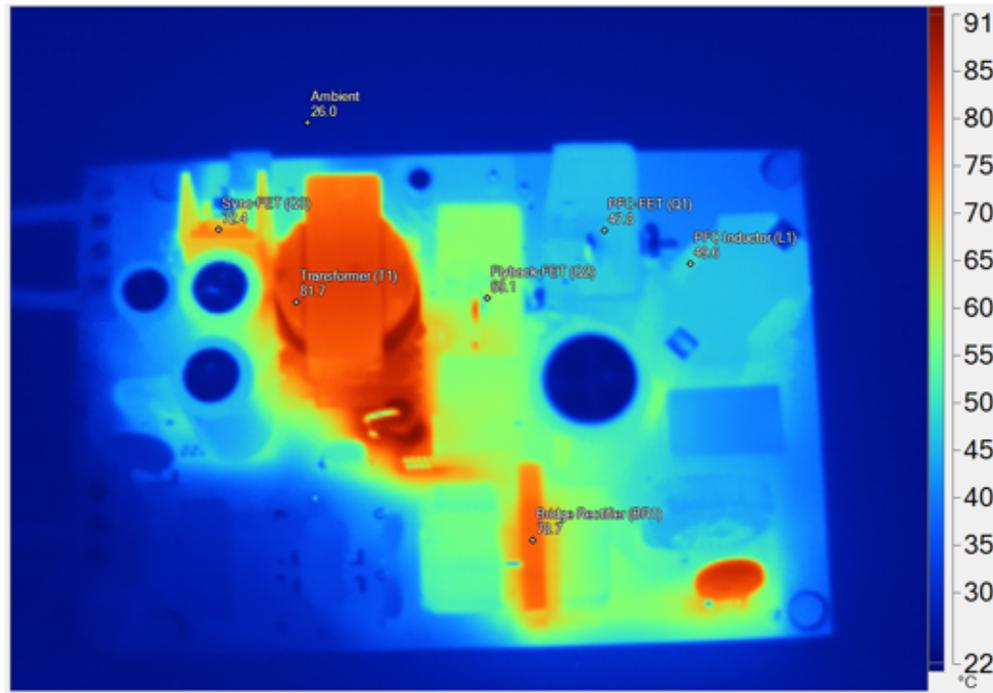
Figure 39. Top-Side Temperatures at 115-V AC Input and 91.2-W Output

Table 8. Highlighted Image Markers for Figure 39

NAME	TEMPERATURE
Ambient	26°C
Boost FET (Q1)	47.8°C
Flyback FET (Q2)	59.1°C
Flyback synchronous rectifier FET (Q3)	72.4°C
Inductor (L1)	49.6°C
Transformer (T1)	81.7°C

The temperatures are well contained to low values and have higher margins from respective device junction temperatures.

6.7.2 Thermal Image for High-Line (230-V AC) Operation

Input voltage: 230-V AC, load on 24-V DC bus is 3.8 A, 91.2-W power output.
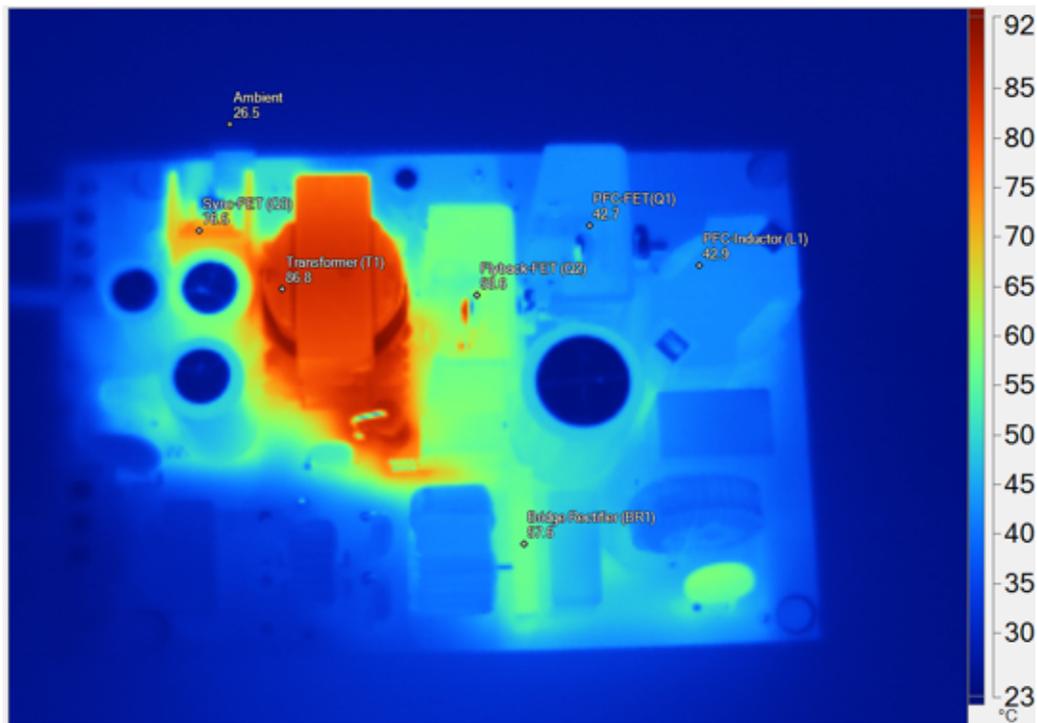
Figure 40. Top-Side Temperatures at 230-V AC Input and 91.2-W Output

Table 9. Highlighted Image Markers for Figure 40

NAME	TEMPERATURE
Ambient	26.5°C
Boost FET (Q1)	42.7°C
Flyback FET (Q2)	58.6°C
Flyback synchronous rectifier FET (Q3)	76.5°C
Inductor (L1)	42.9°C
Transformer (T1)	86.8°C

The temperatures are well contained to low values and have high enough margins from respective device junction temperatures.

7   Design Files

7.1   *Schematics*

To download the schematics, see the design files at TIDA-00701.

Figure 41. PFC Circuit Schematic
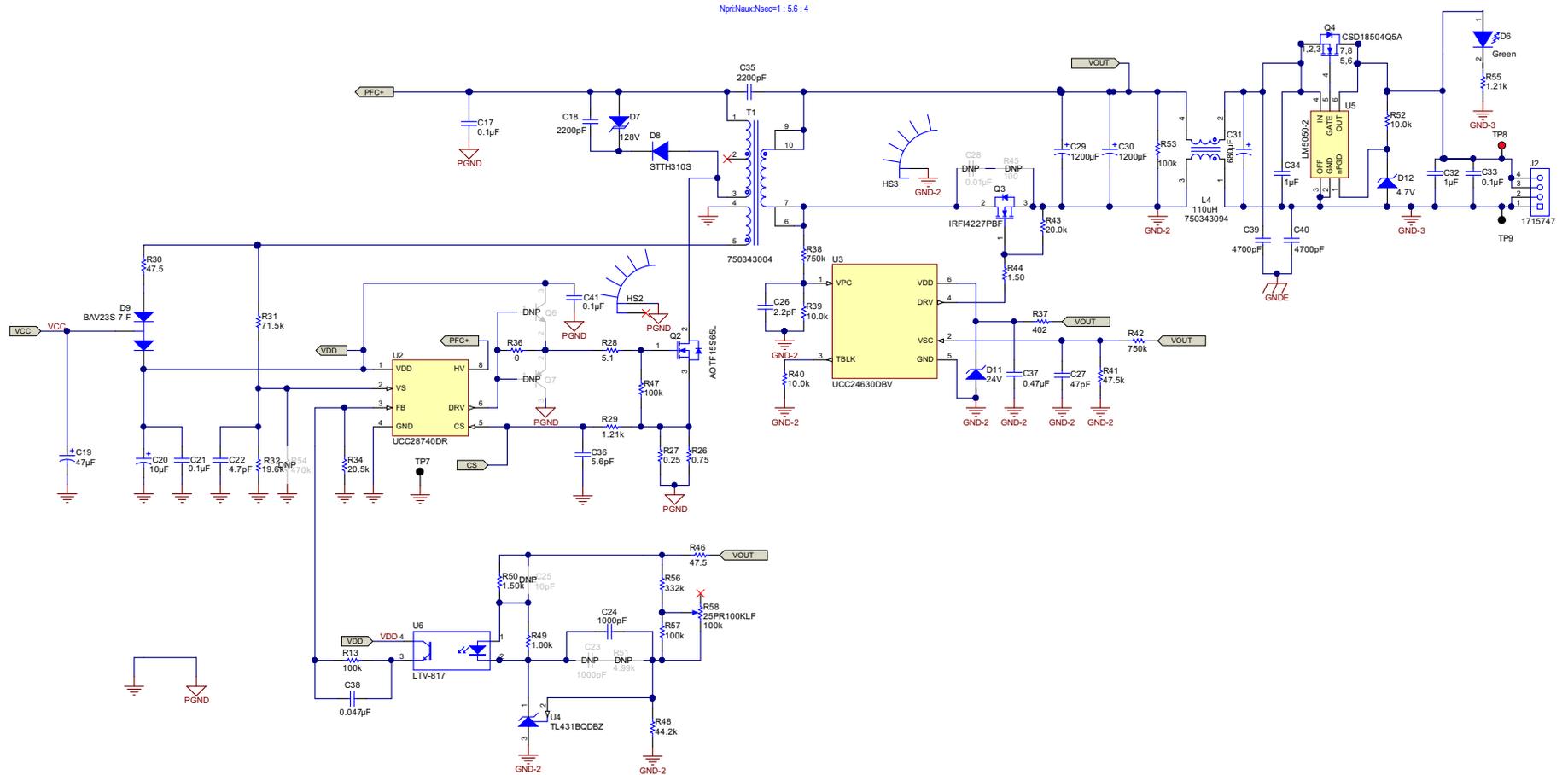
Figure 42. Flyback Circuit With Precision CC-CV Control Schematic

7.2   Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00701.

7.3   Layout Guidelines

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, attention to detail in the layout can save much time in troubleshooting later on.

7.3.1   Power Stage Specific Guidelines

The following are key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This will help in reducing EMI and improve converter overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces, with adequate clearance and ground shielding.
- For each power supply stage, keep power ground and control ground separately. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, layout should be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher peak currents and become hotter (i^2R).
- The heat-sinks of all the power switching components need to be tied to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route with short traces to reduce inductance.
- Choose the width of PCB traces based on an acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, UL 60950-1 safety standard is followed to maintain the creepage and clearance from live line to neutral line and to safety ground, as defined in the Tables 2K through 2N of this standard.
- Adapt thermal management to fit the end-equipment requirements.

7.3.2   Controller Specific Guidelines

The following are key guidelines for routing of controller components and signal circuits:

*   The optimum placement of decoupling capacitor is closest to the VCC/VDD and GND terminals of the device. Minimize the loop area formed by the bypass-capacitor connection and the GND terminal of the IC.
*   Use a copper plane or island as the reference ground for the control devices, a low current signal ground (SGND).
*   Locate all controller support components at specific signal pins close to their connection pin. Connect the other end of the component to the SGND with shortest trace length.
*   Keep the trace routing for the voltage sensing and current sensing circuit components to the device as short as possible to reduce parasitic effects on the current limit and current or voltage monitoring accuracy. These traces should not have any coupling to switching signals on the board.
*   Connect the SGND plane to a high current ground (main power ground) at a single point that is at the negative terminal of DC I/O capacitor, respectively.
*   Keep signal traces, if there is overlap, perpendicular to high-frequency, and high-current traces should be perpendicular to signal traces, not parallel to them. Shielding signal traces with ground traces can help reduce noise pick up.
*   Provide sufficient PCB trace spacing between the high-voltage connections (such as HV pin of UCC28740) and any low-voltage nets.
*   Refer to the placement and routing guidelines and layout example present in the UCC28740 datasheet.

7.3.3   Layer Plots

To download the layer plots, see the design files at TIDA-00701.

7.4   Altium Project

To download the Altium project files, see the design files at TIDA-00701.

7.5   Gerber Files

To download the Gerber files, see the design files at TIDA-00701.

7.6   Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00701.

7.7   Design Calculator Spreadsheet

To download the design calculator spreadsheet, see the design files at TIDA-00701.

8 References

1. Texas Instruments, *High Power Factor and High Efficiency — You Can Have Both*, Unitrode Power Supply Design Seminar SEM1800, Topic 1 (PDF)

2. Texas Instruments, *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Preregulator*, UCC38050 Application Note (SLUU138)

3. Texas Instruments, *Snubber Circuits: Theory, Design and Applications*, (SLUP100)

4. Texas Instruments, *Choosing Standard Recovery Diode or Ultra-Fast Diode in Snubber*, UCC28740 Application Note (SNVA744)

5. Texas Instruments, *Control Challenges for Low Power AC/DC Converters*, Unitrode Power Supply Design Seminar SEM2100, Topic 5 (SLUP325)

6. Texas Instruments and Underwriters Laboratories, *Safety Considerations in Power Supply Design*, Power Supply Design Seminar SEM1600, Topic 1 (PDF)

7. Texas Instruments, *Understanding Noise-Spreading Techniques and their Effects in Switch-Mode Power Applications*, Unitrode Power Supply Design Seminar SEM1800, Topic 2 (PDF)

8. Texas Instruments, *A High Efficiency Synchronous Rectifier Flyback for High Density AC/DC Adapter*, Application Report (SLUA604)

9. IEEE, *Digital Control Implementation to Reduce the Cost and Improve the Performance of the Control Stage of an Industrial Switch-Mode Power Supply*, D. Díaz, O. García, J.A. Oliver, P. Alou, F. Moreno, B. Duret, J.A. Cobos, 2011 (PDF)

8.1 Trademarks

All trademarks are the property of their respective owners.

9 Terminology

TI Glossary: This glossary lists and explains terms, acronyms, and definitions (SLYZ022)

PWM— Pulse width modulation

FETs, MOSFETs— Metal–oxide–semiconductor field-effect transistor

IGBT— Insulated gate bipolar transistor

ESD— Electrostatic discharge

RMS— Root mean square

10 About the Authors

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Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Revision A History

Changes from Original (December 2015) to A Revision   Page