TEXAS INSTRUMENTS

## Automotive Power Supply with Pre-Boost

- Input   2.7-16V, 32V peak

- Output   Boost   9.0V @ 1.7A   TPS40210-Q1
                 Pre-Buck   6.0V @ 2.2A   LM53603-Q1
                 5V-Buck   5.0V @ 1.1A   TPS62133-Q1
                 3.3V-Buck   3.3V @ 0.6A   TPS62130-Q1
                 1.32V-Buck   1.32V @ 1.0A   TPS62130-Q1

- The output capacitor of the boost converter (Rubycon 35ZL56MEFCTA6.3X11, 405mA rms) can handle the ripple current only for a short time (cranking e.g.). For continuous operation at full load, a low ESR / high ripple current capacitor is needed (for example Nichicon PCV1V820MCL7GS or Panasonic 35SVPF82M). For a Panasonic 35SVPF82M output capacitor, no modification of the compensation network is needed (was tested).

TEXAS
INSTRUMENTS
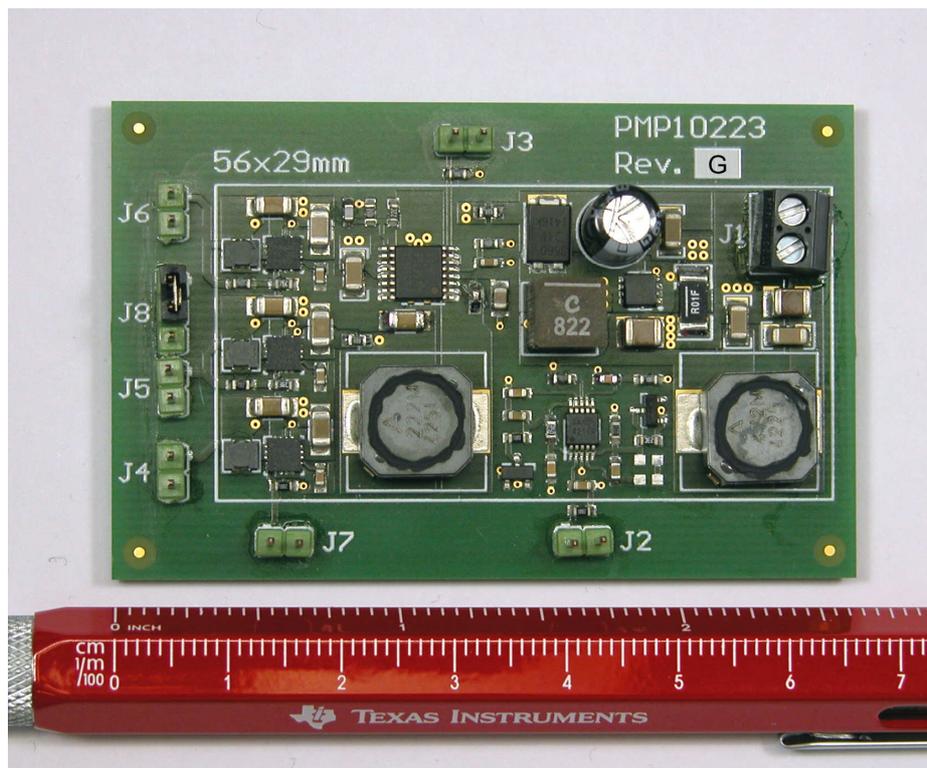
1   +9.0V Boost Converter

1.1   Switching Node (+9.0V Boost Converter)

The switching node is shown in Figure 1.
The input voltage is set to 7.0V with a 1.7A load on the 9.0V output.

Channel C2:   **Switching node**, -0.7V min, 12.1V max
2V/div, 2us/div
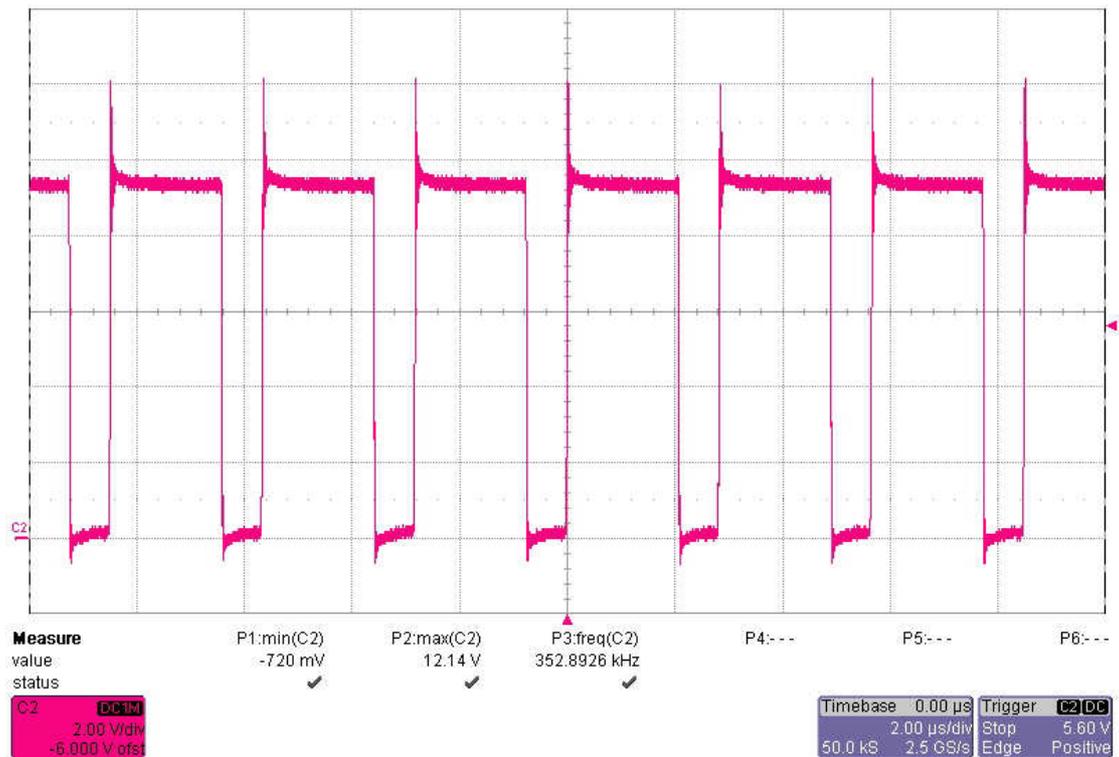
Figure 1

1.2 Transient Response (+9.0V Boost Converter)

The response to a load step is shown in Figure 2.

Channel C2: **Output voltage**, -988mV undershoot (11.0%), 1.25V overshoot (13.9%)
1V/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 0.85A to 1.7A and vice versa
1A/div, 1ms/div
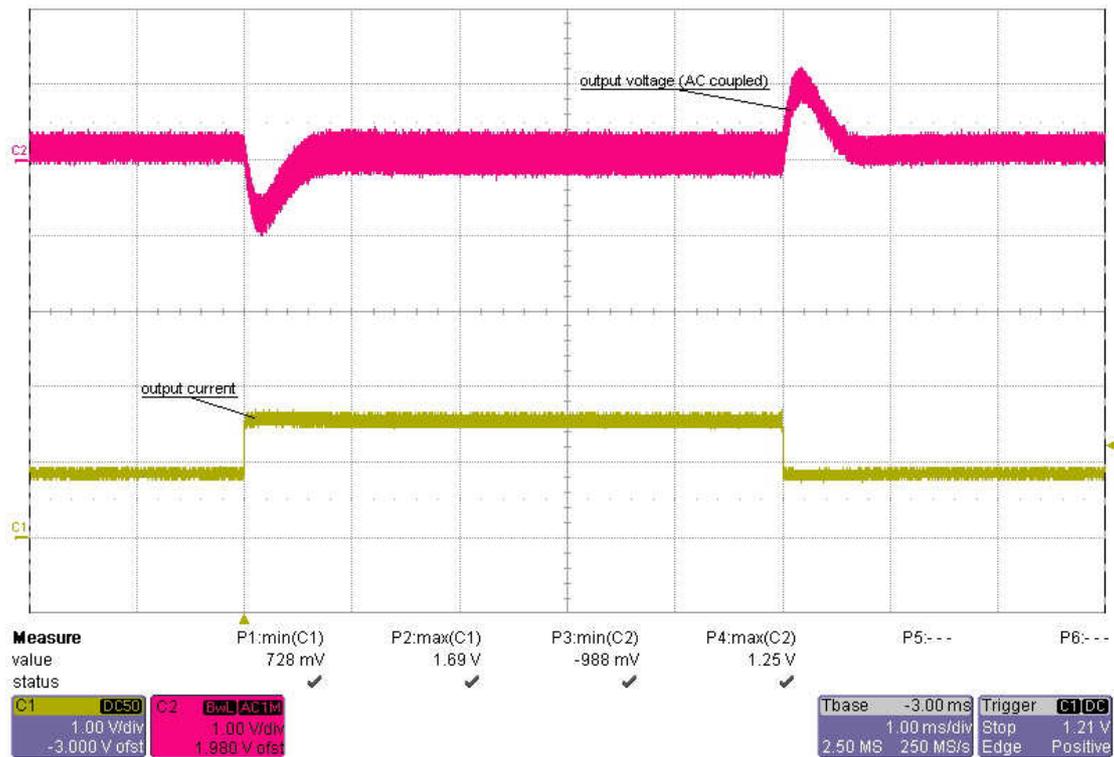
Figure 2

1.3   Frequency Response (+9.0V Boost Converter)

Figure 3 shows the loop response of the boost converter at a load of 1.7A.

2.7V input

- 62 deg phase margin @ crossover frequency of 325 Hz
- -13 db gain margin

5.0V input

- 76 deg phase margin @ crossover frequency of 517 Hz
- -22 db gain margin

7.0V input

- 78 deg phase margin @ crossover frequency of 632 Hz
- -26 dB gain margin
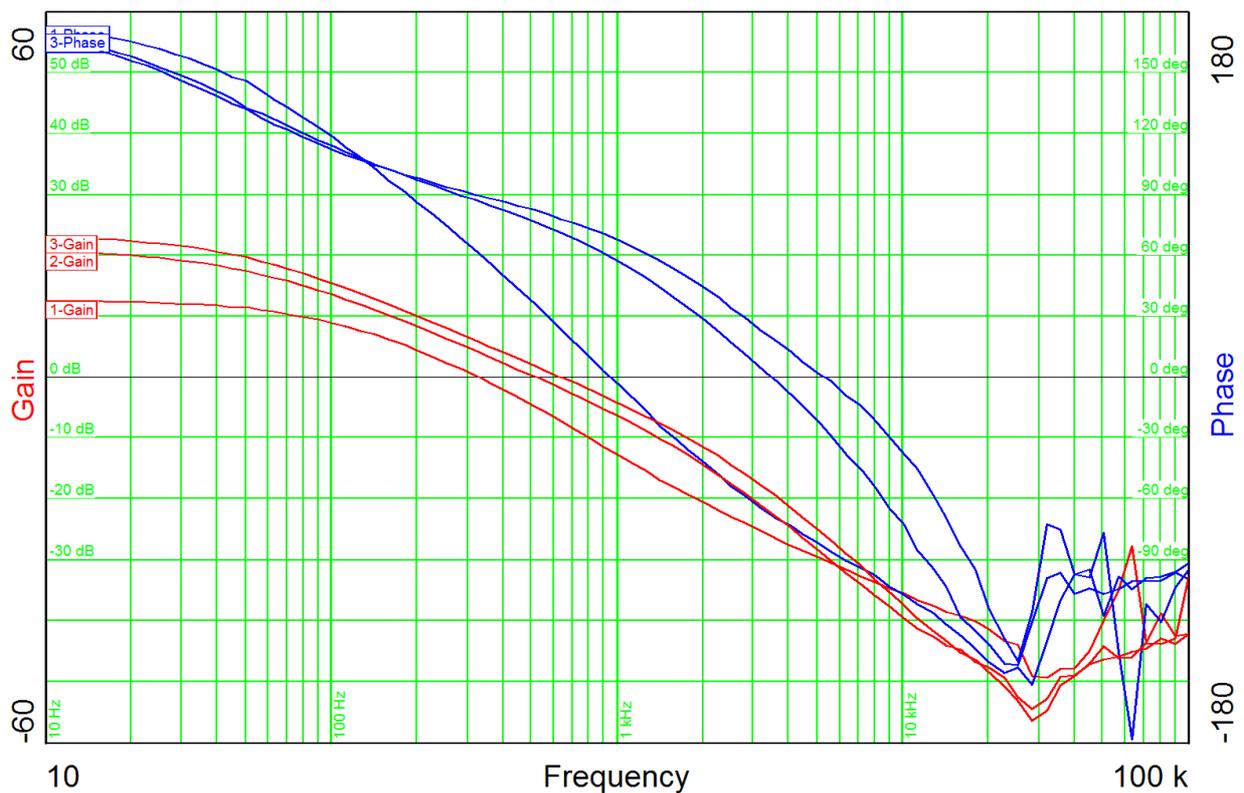
Figure 3

1.4 Efficiency (+9.0V Boost Converter)

The efficiency at 2.7V, 5.0V and 7.0V input voltage is shown in Figure 4.
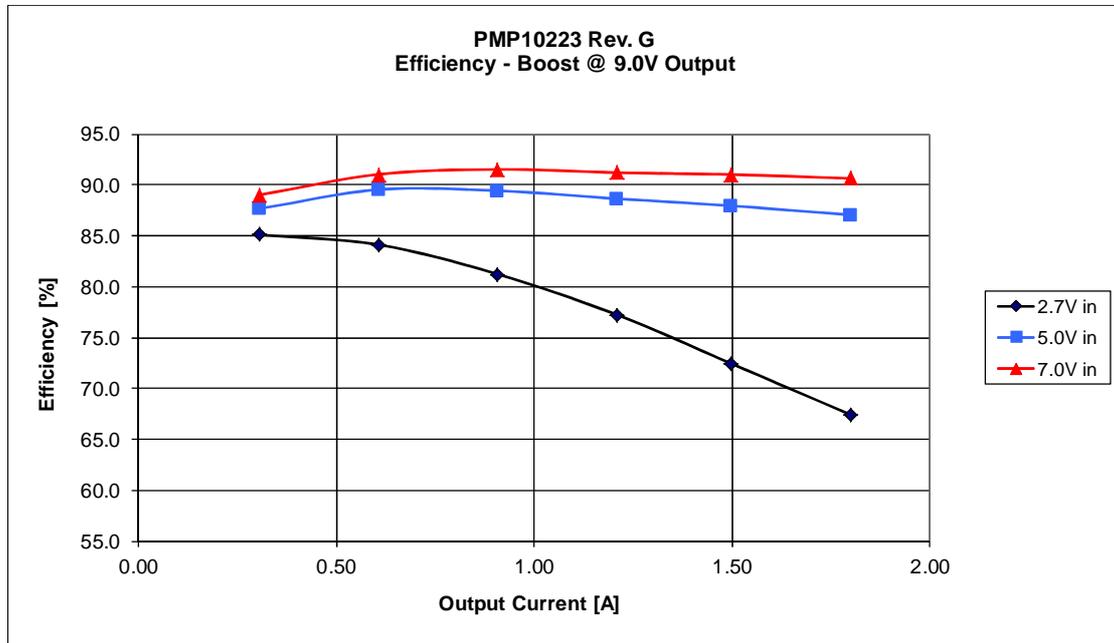
Figure 4

1.5 Load Regulation (+9.0V Boost Converter)

The load regulation of the boost converter is shown in Figure 5.
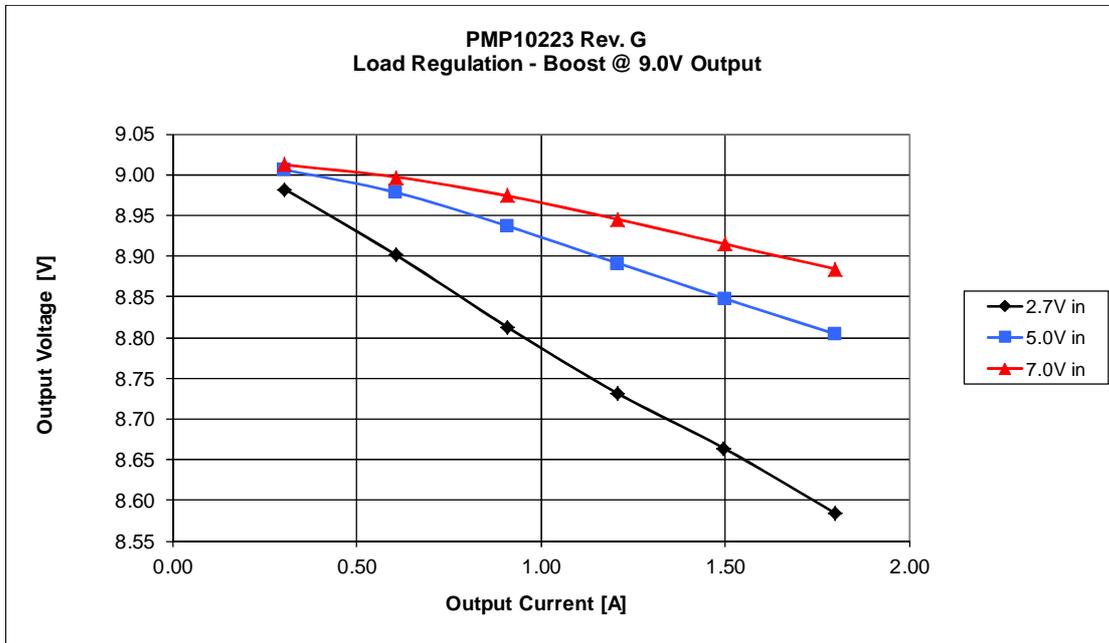
Figure 5

1.6   Output Voltage Ripple (+9.0V Boost Converter)

The output ripple of the 9.0V boost converter is shown in Figure 6.
The input voltage is set to 2.7V, 5.0V and 7.0V.

Channel M1:   **2.7V input voltage**, 400mV peak-peak
300mV/div, 2us/div

Channel M2:   **5.0V input voltage**, 270mV peak-peak
300mV/div, 2us/div

Channel M3:   **7.0V input voltage**, 150mV peak-peak
300mV/div, 2us/div
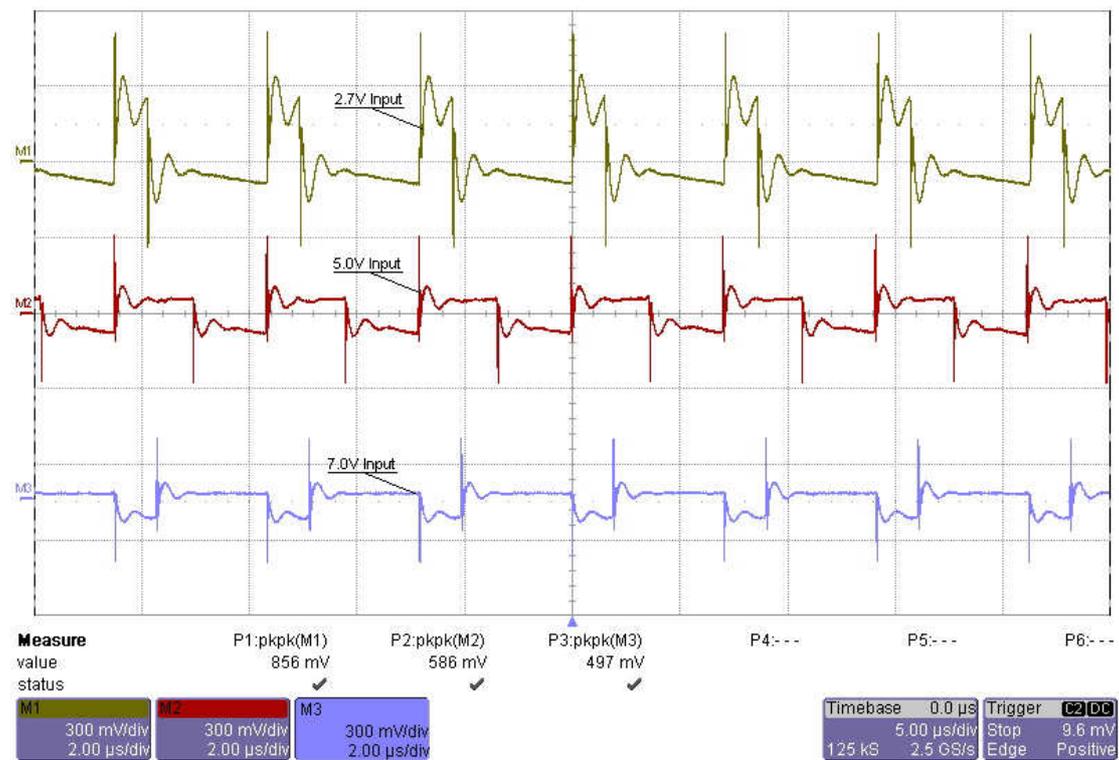
Figure 6

1.7   Input Voltage Ripple – Inductor Side (+9.0V Boost Converter)

The output ripple of the 9.0V boost converter is shown in Figure 7.
The input voltage is set to 2.7V, 5.0V and 7.0V.

Channel M1:   **2.7V input voltage**, 125mV peak-peak
100mV/div, 5us/div

Channel M2:   **5.0V input voltage**, 85mV peak-peak
100mV/div, 5us/div

Channel M3:   **7.0V input voltage**, 77mV peak-peak
100mV/div, 5us/div
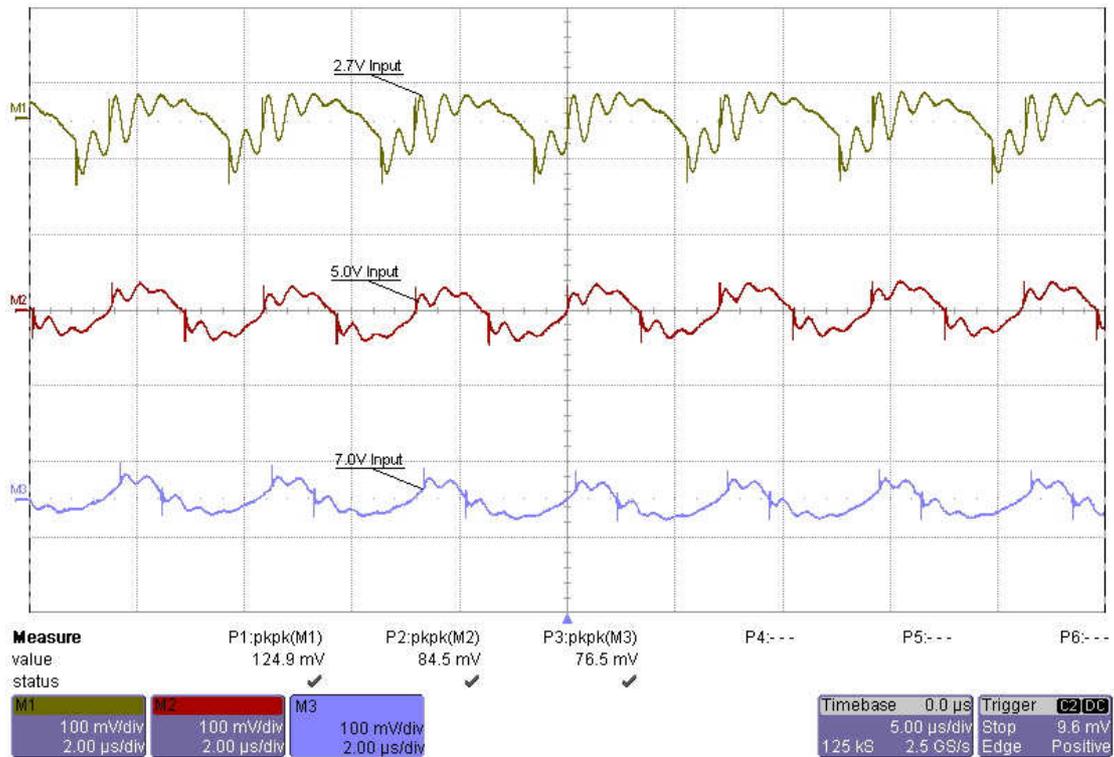
Figure 7

1.8   Input Voltage Ripple – Connector Side (+9.0V Boost Converter)

The output ripple of the 9.0V boost converter is shown in Figure 6.
The input voltage is set to 2.7V, 5.0V and 7.0V.

Channel M1:   **2.7V input voltage**, 47mV peak-peak
20mV/div, 2us/div

Channel M2:   **5.0V input voltage**, 20mV peak-peak
20mV/div, 2us/div

Channel M3:   **7.0V input voltage**, 12mV peak-peak
20mV/div, 2us/div

Figure 8

Power Management Solutions
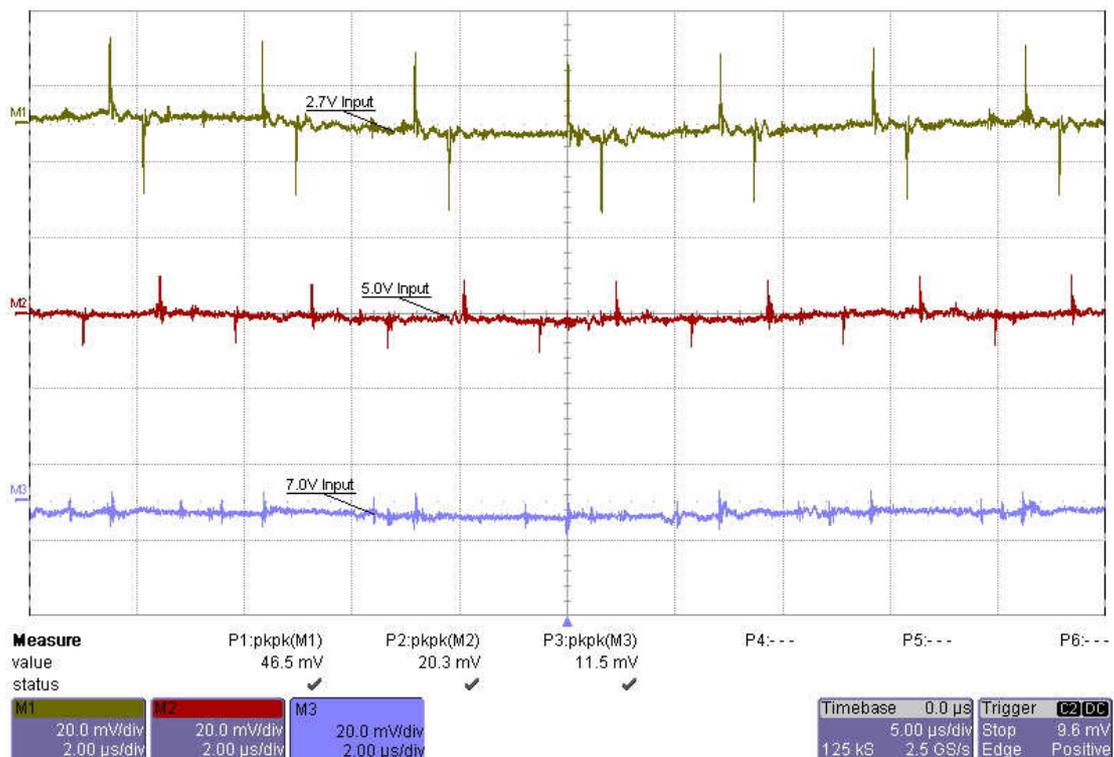
2   +6.0V Buck Converter

2.1   Switching Node (+6.0V Buck Converter)

The switching node is shown in Figure 9.
The input voltage is set to 12.0V with a 2.2A load on the 6.0V output.

Channel C2:   **Switching node**, -1.0V min, 13.0V max
   2V/div, 200ns/div

Measure	P1:min(C2)	P2:max(C2)	P3:freq(C2)	P4:- - -	P5:- - -	P6:- - -
value	-1.04 V	13.04 V	2.05146 MHz			
status	✓	✓	✓			

C2   DC 1M
2.00 V/div
-6.000 V ofst

Timebase   0 ns   Trigger   C2 DC
200 ns/div   Stop   5.96 V
5.00 kS   2.5 GS/s   Edge   Positive
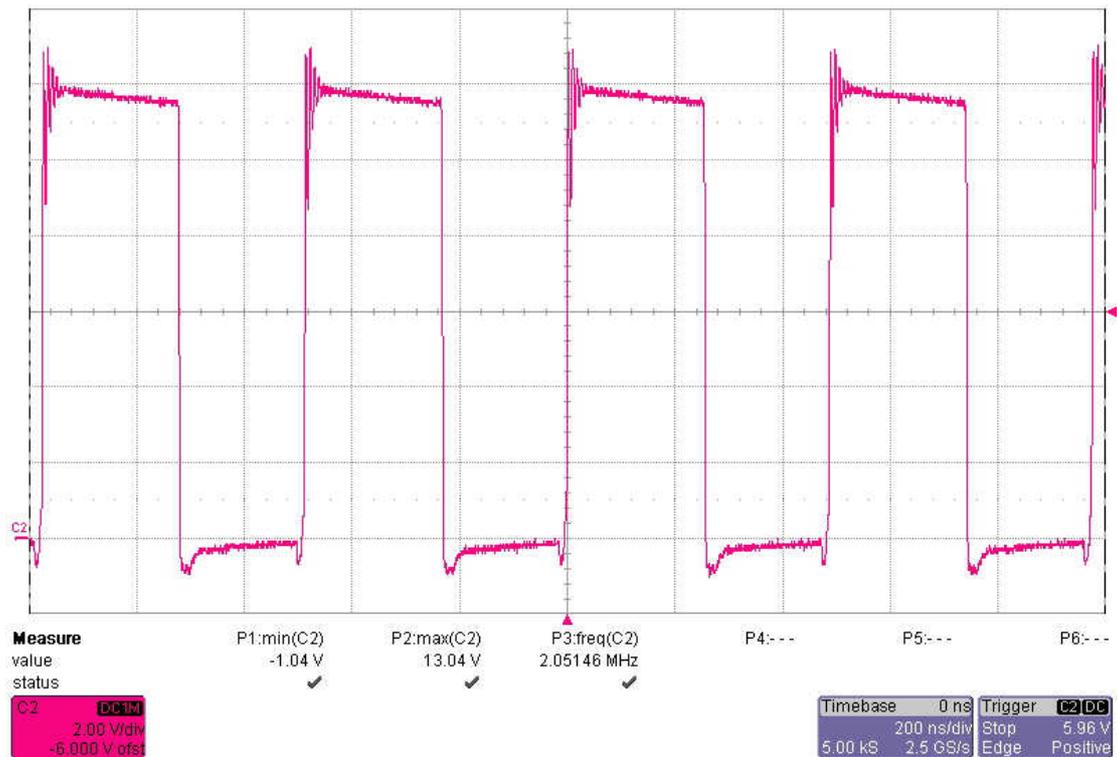
Figure 9

2.2 Transient Response (+6.0V Buck Converter)

The response to a load step is shown in Figure 10.

Channel C2: **Output voltage**, -48mV undershoot (0.8%), 45mV overshoot (0.8%)
50mV/div, 1ms/div, AC coupled

Channel C1: **Load current**, load step 1.0A to 2.0A and vice versa
1A/div, 1ms/div
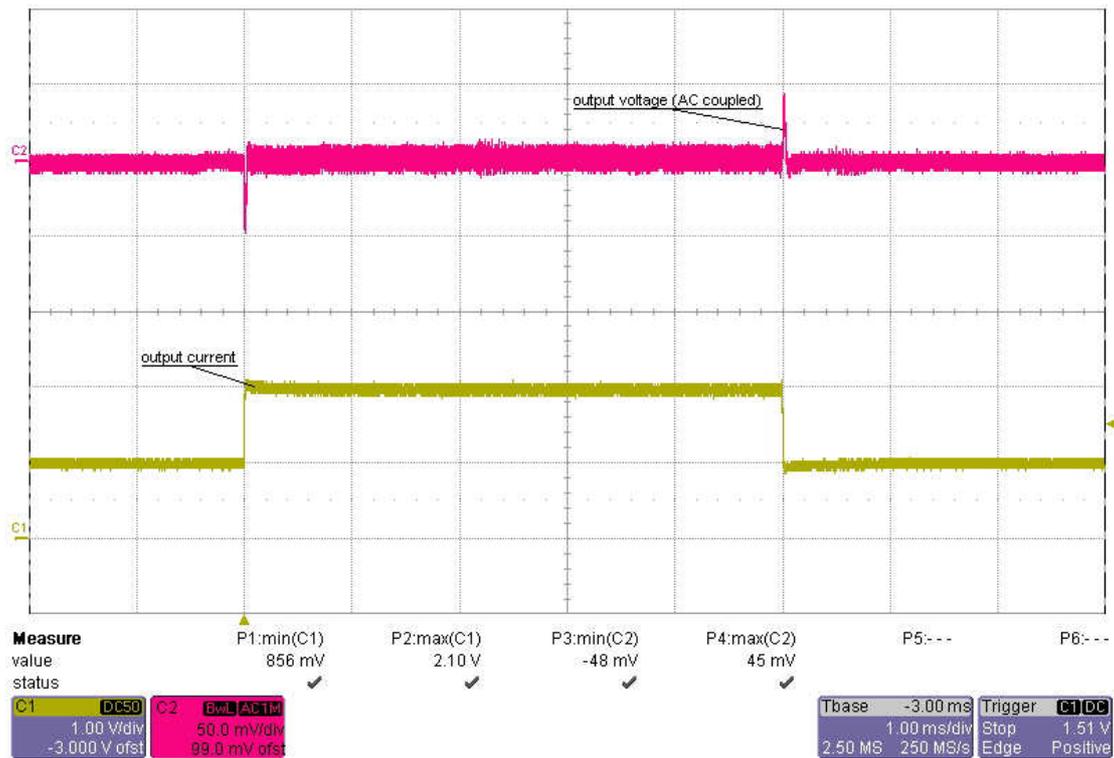
Figure 10

2.3 Frequency Response (+6.0V Buck Converter)

Figure 11 shows the loop response of the 6.3V buck converter at a load of 1.7A.

9.0V input

- 89 deg phase margin @ crossover frequency of 96.7 kHz
- -19 db gain margin

12.0V input

- 89 deg phase margin @ crossover frequency of 98.5 kHz
- -15 db gain margin

18.0V input

- 89 deg phase margin @ crossover frequency of 95.3 kHz
- -17 dB gain margin
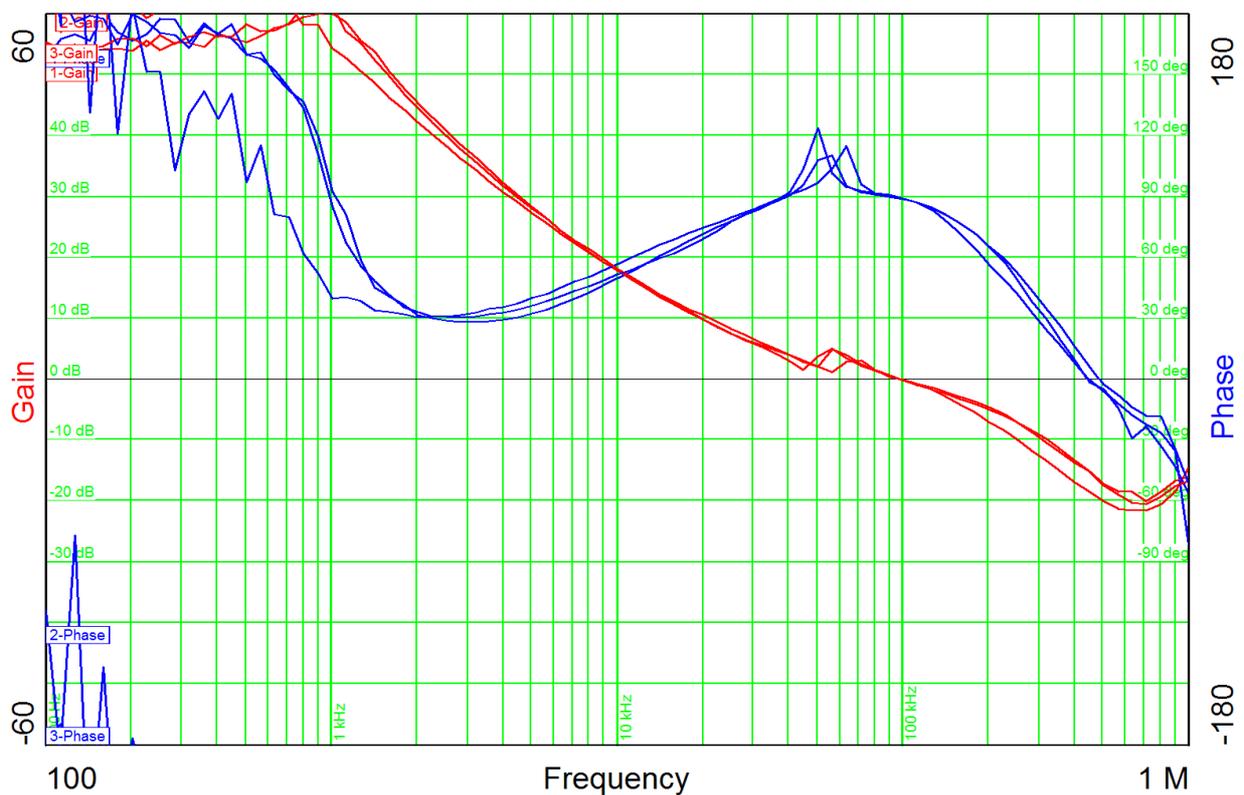
Figure 11

2.4   Efficiency (+6.0V Buck Converter)

The efficiency at 9.0V, 12V and 18.0V input voltage is shown in Figure 12.
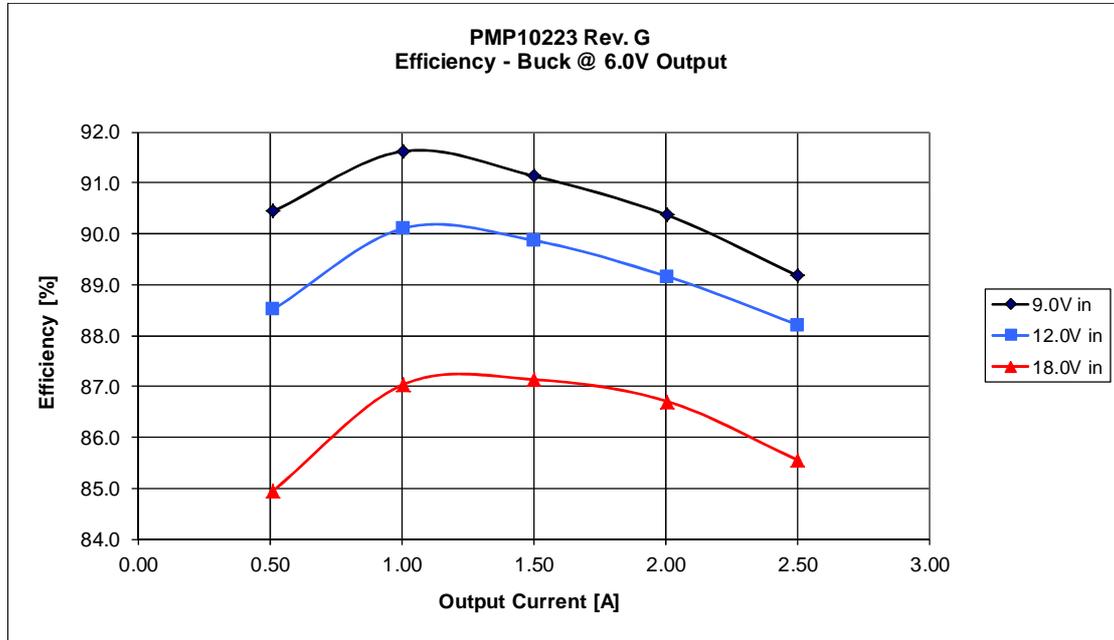
Figure 12

2.5 Load regulation (+6.0V Buck Converter)

The load regulation of the 6.0V buck converter is shown in Figure 13.
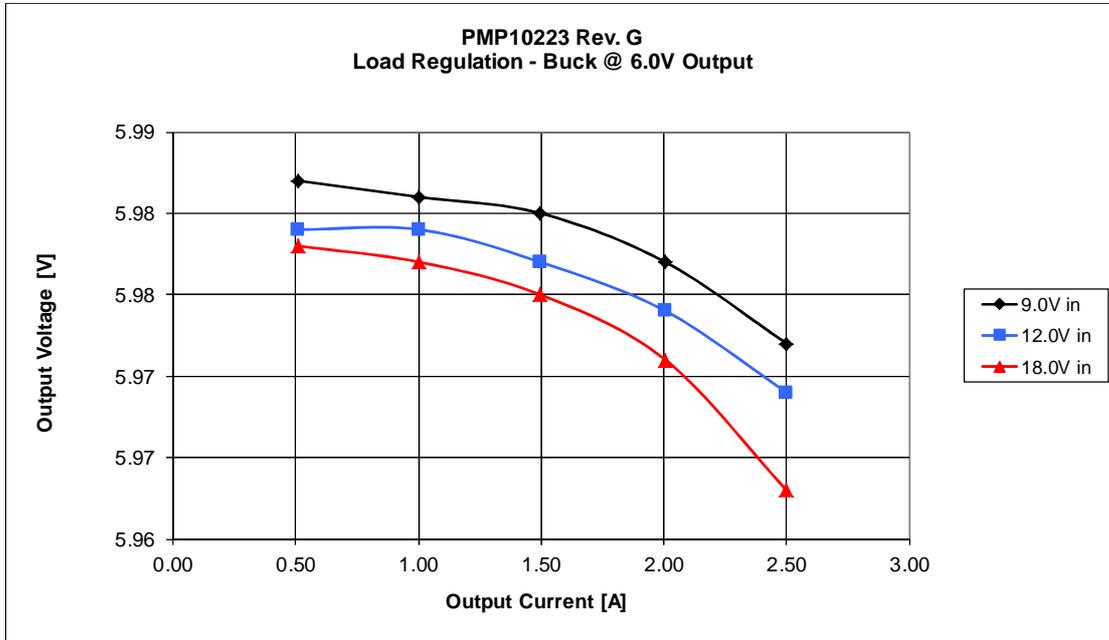
Figure 13

2.6 Output voltage ripple (+6.0V Buck Converter)

The output ripple of the 6.0V buck converter with 2.2A load is shown in Figure 14.
The input voltage is set to 12.0V.

Channel C2:   **12.0V input voltage**, 8mV peak-peak
                20mV/div, 200ns/div
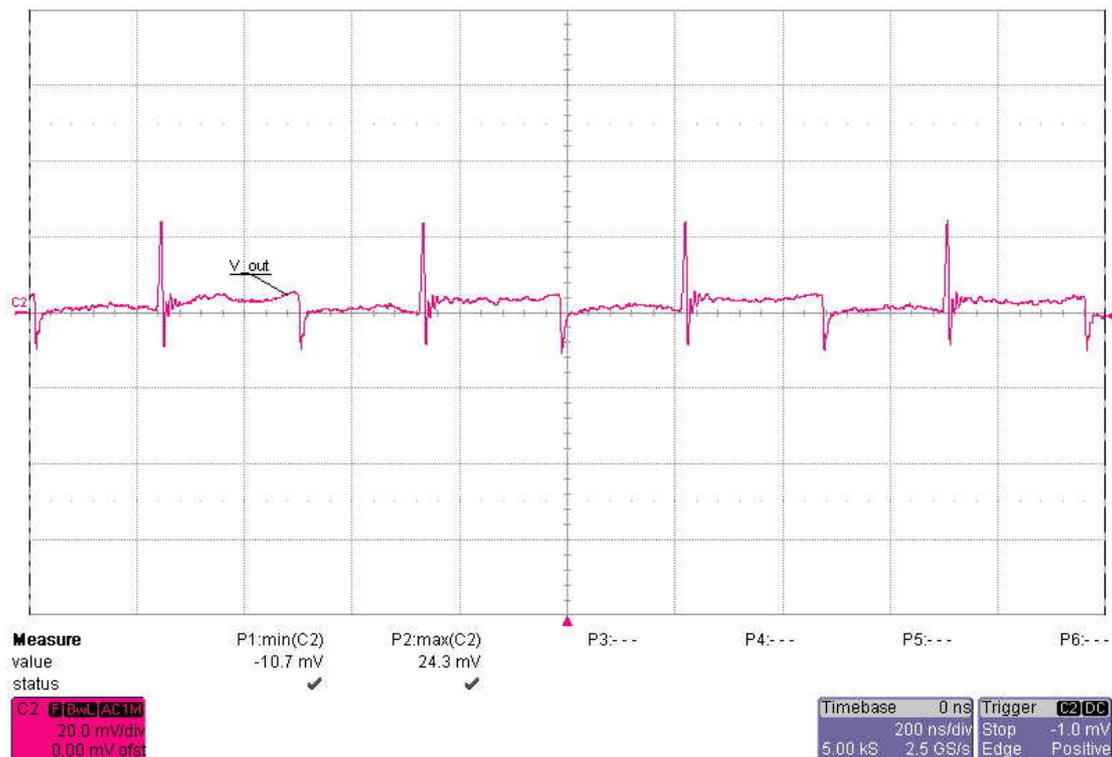
Figure 14

2.7 Startup (+6.0V Buck Converter)

The startup of the 6.0V buck with no load on the output is shown in Figure 15.

Channel C1: **12.0V Input voltage**
2V/div, 2ms/div

Channel C2: **6.0V Output voltage**
2V/div, 2ms/div
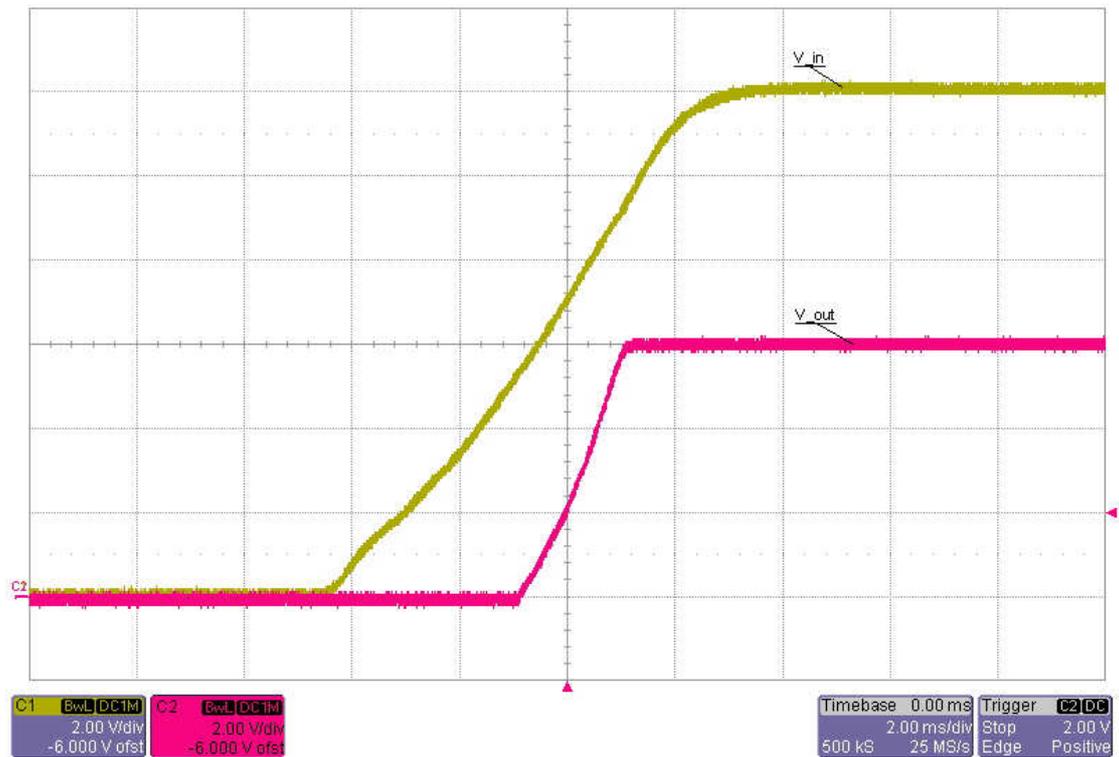
Figure 15

2.8 Shutdown (+6.0V Buck Converter)

The shutdown of the 6.0V buck with 2.2A load on the output is shown in Figure 16.

Channel C1:	**12.0V Input voltage**
	2V/div, 2ms/div
Channel C2:	**6.0V Output voltage**
	2V/div, 2ms/div
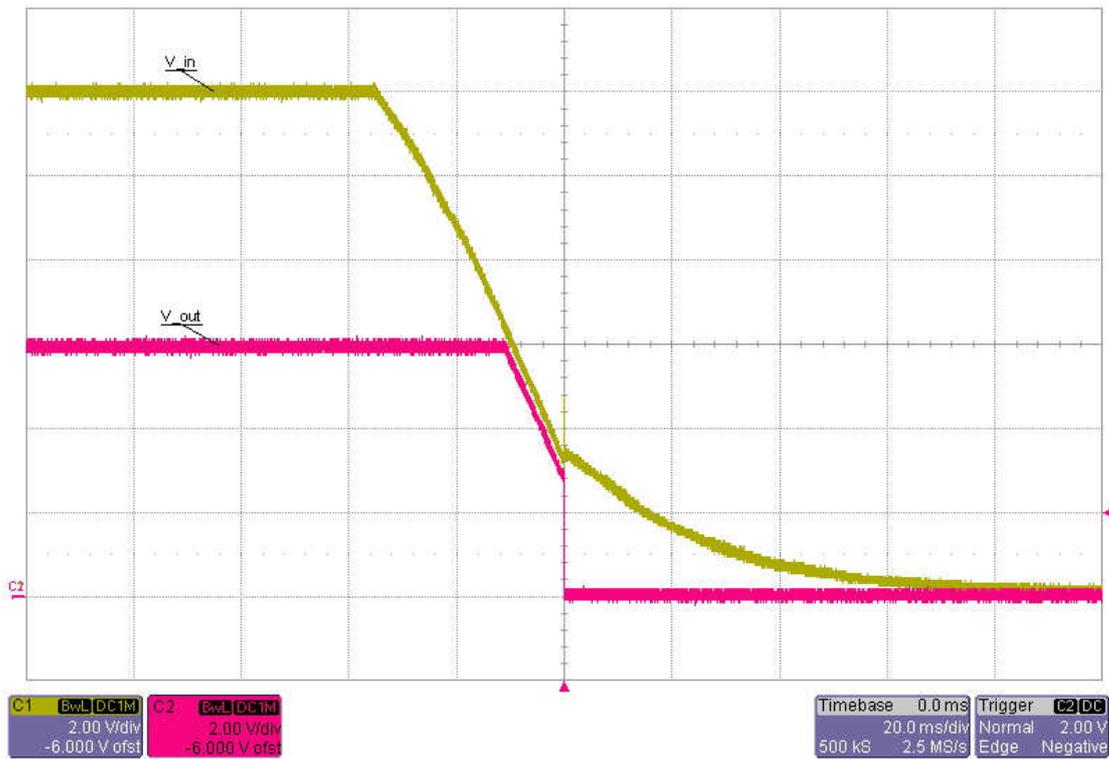
Figure 16

3   +5.0V Buck Converter

3.1   Switching Node (+5.0V Buck Converter)

The switching node is shown in Figure 17.
The input voltage is set to 6.0V with a 1.1A load on the 5.0V output.

Channel C2:   **Switching node**, -0.8V min, 6.9V max
1V/div, 500ns/div
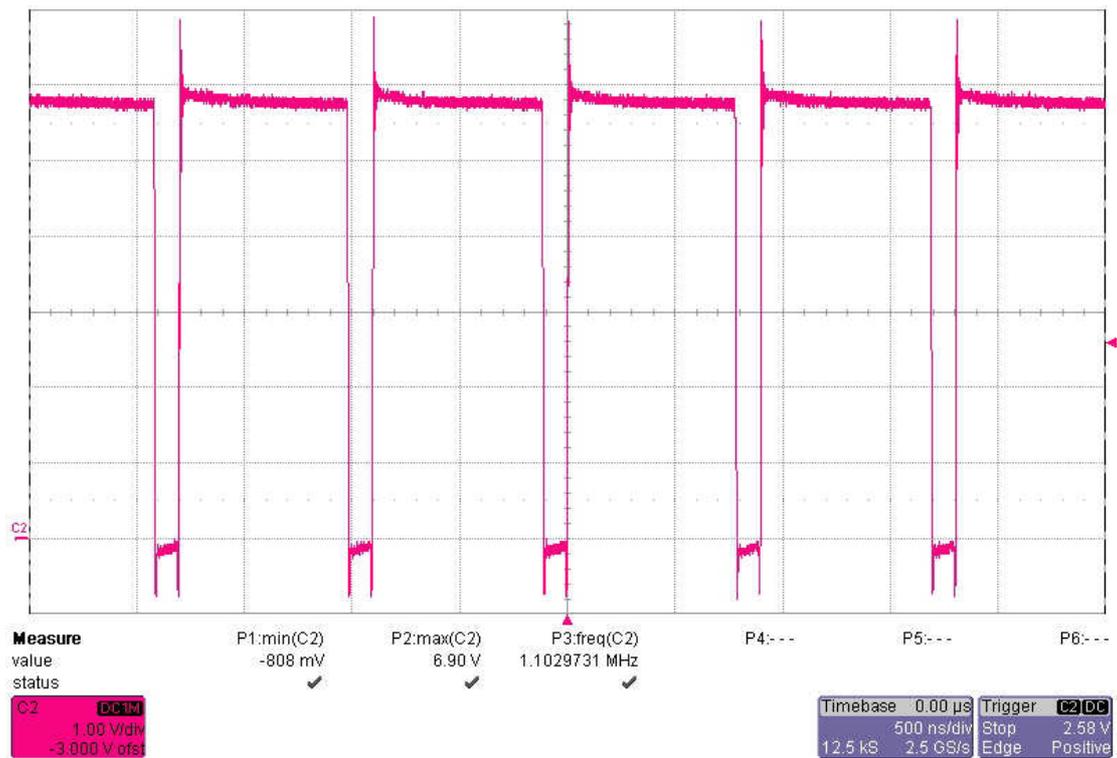
Figure 17

4 +3.3V Buck Converter

4.1 Switching Node (+3.3V Buck Converter)

The switching node is shown in Figure 18.
The input voltage is set to 6.0V with a 0.6A load on the 3.3V output.

Channel C2:   **Switching node**, -0.8V min, 7.0V max
   1V/div, 500ns/div

Measure	P1:min(C2)	P2:max(C2)	P3:freq(C2)	P4:- - -	P5:- - -	P6:- - -
value	-776 mV	6.97 V	2.575903 MHz			
status	✓	✓	✓			

C2 **DC1M**
1.00 V/div
-3.000 V ofst

Timebase   0.00 µs Trigger C2 DC
500 ns/div Stop   2.58 V
12.5 kS   2.5 GS/s Edge   Positive
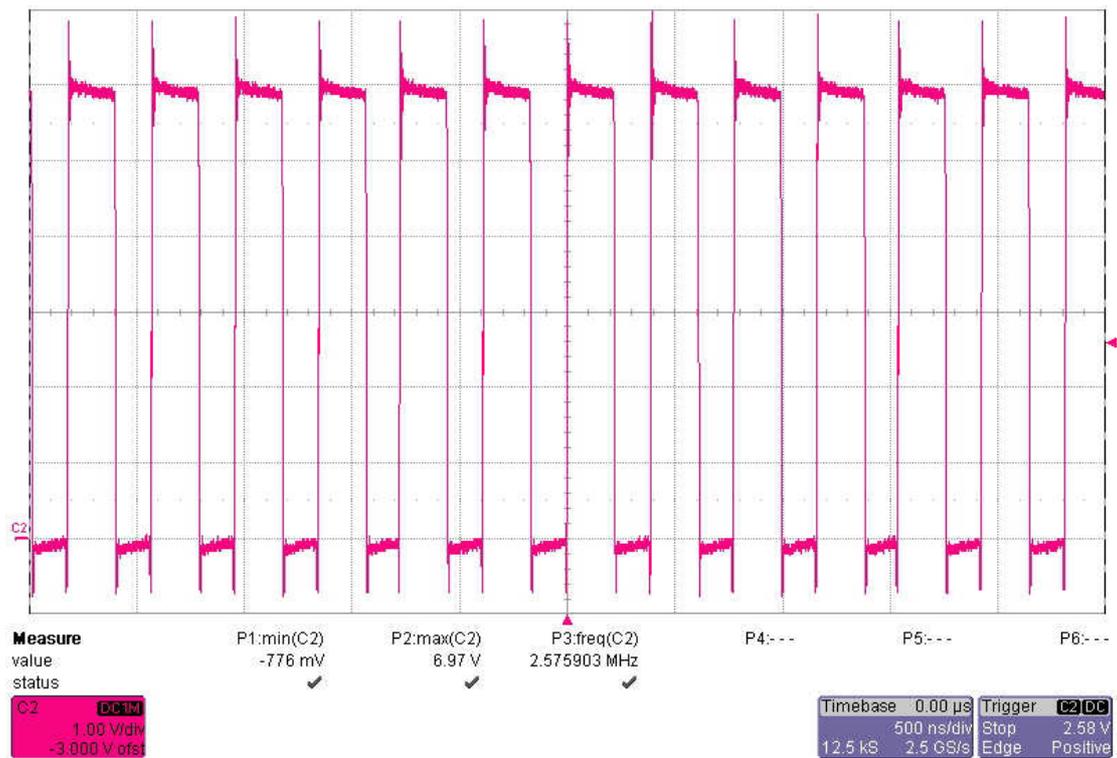
Figure 18

4.2 Frequency Response (3.3V Buck Converter)

Figure 19 shows the loop response of the 3.3V buck converter at a load of 0.6A.

6.0V input

- 79 deg phase margin @ crossover frequency of 22.0 kHz
- -22 dB gain margin
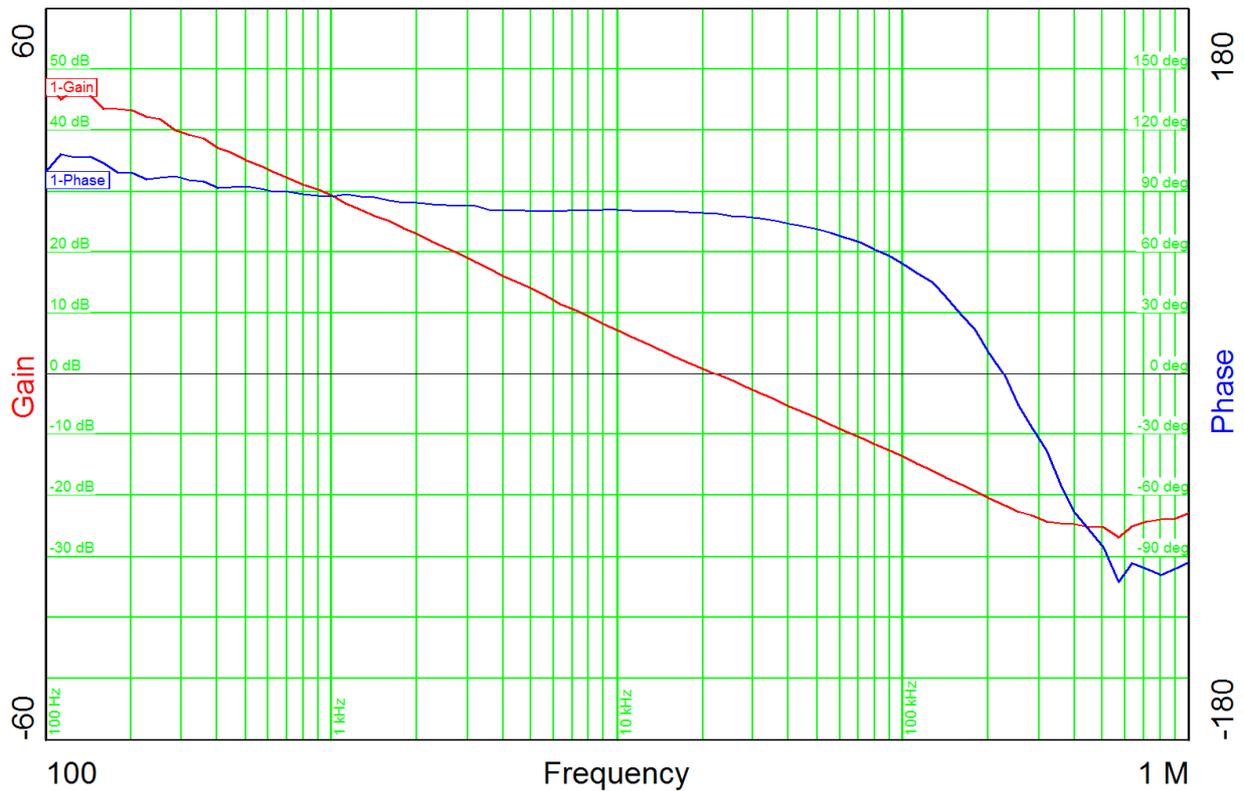
Figure 19

5 +1.32V Buck Converter

5.1 Switching Node (+1.32V Buck Converter)

The switching node is shown in Figure 20.
The input voltage is set to 6.0V with a 1.0A load on the 1.32V output.

Channel C2:   **Switching node**, -0.8V min, 6.1V max
                1V/div, 500ns/div
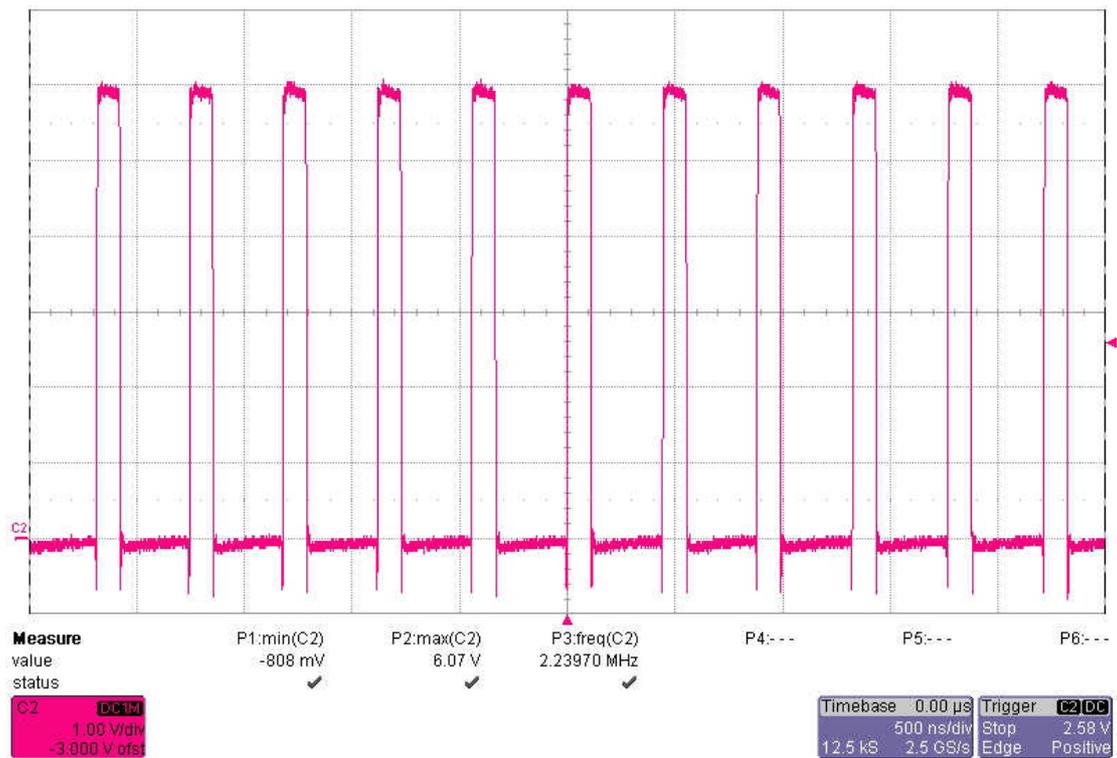
Figure 20

5.2   Frequency response (3.3V Buck Converter)

Figure 21 shows the loop response of the 1.32V buck converter at a load of 1.0A.

6.0V input

- 69 deg phase margin @ crossover frequency of 46.8 kHz
- -15 dB gain margin
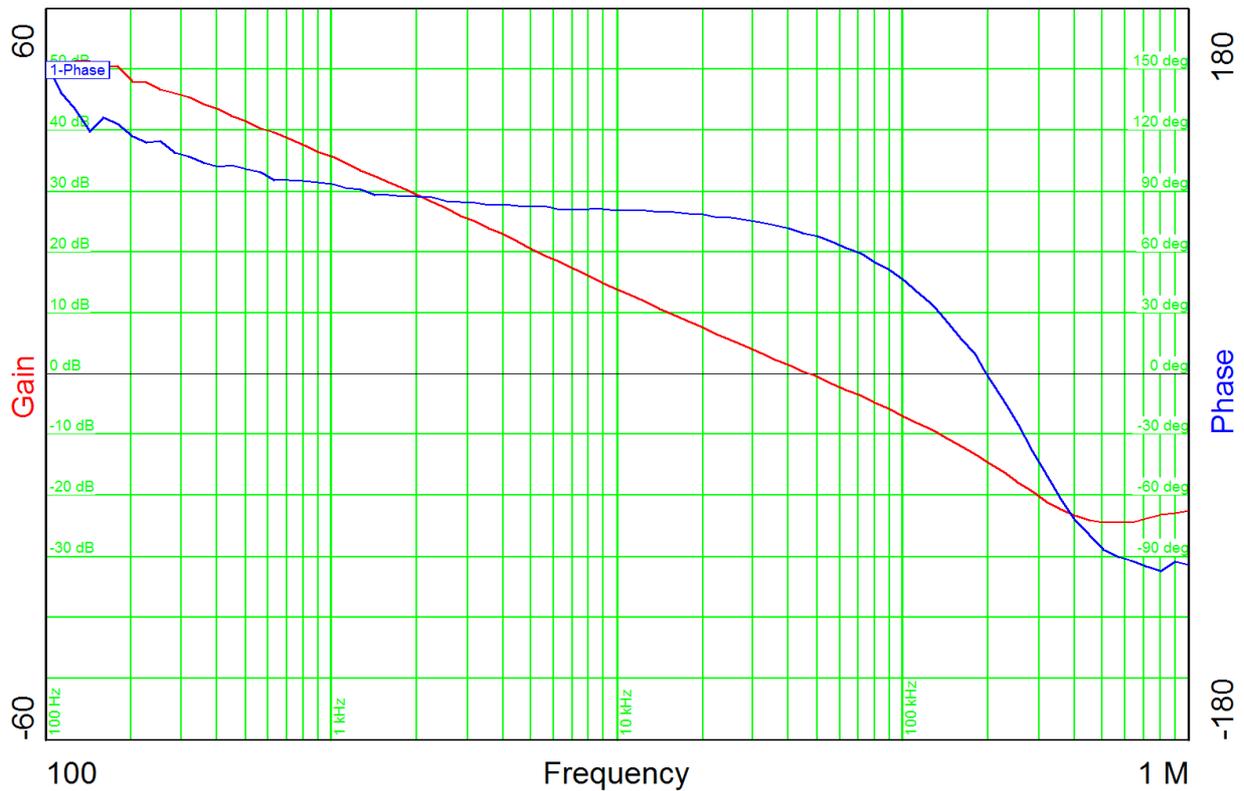
Figure 21

6   Thermal measurement

The thermal image (Figure 22) shows the circuit at an ambient temperature of 21 °C with an input voltage of 7.0V and a load of 1.1A on the 5.0V buck, 0.6A load on the 3.3V buck and 1.0A on the 1.32V buck.
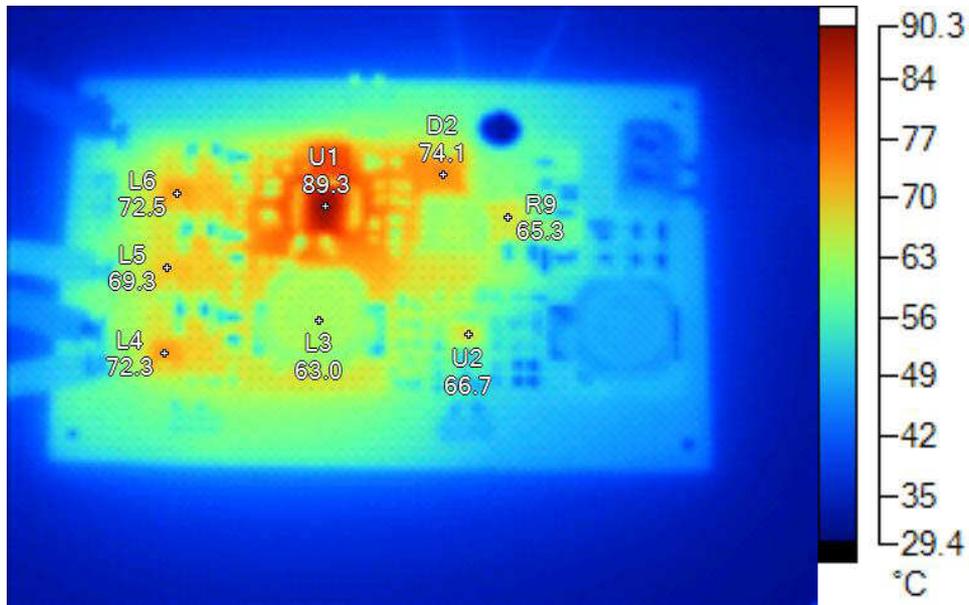
Figure 22

Name	Temperature	Emissivity	Background
U1	89.3°C	0.95	21.0°C
U2	66.7°C	0.95	21.0°C
L3	63.0°C	0.95	21.0°C
L6	72.5°C	0.95	21.0°C
L5	69.3°C	0.95	21.0°C
L4	72.3°C	0.95	21.0°C
D2	74.1°C	0.95	21.0°C
R9	65.3°C	0.95	21.0°C

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