Test Report
For PMP7979
1/15/2016

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1. Design Specifications

Vin Minimum	**12VDC**
Vin Maximum	**67VDC**
Vout	**54VDC**
Iout	**4.8A continuous**
Approximate Switching Frequency	**~100KHz**

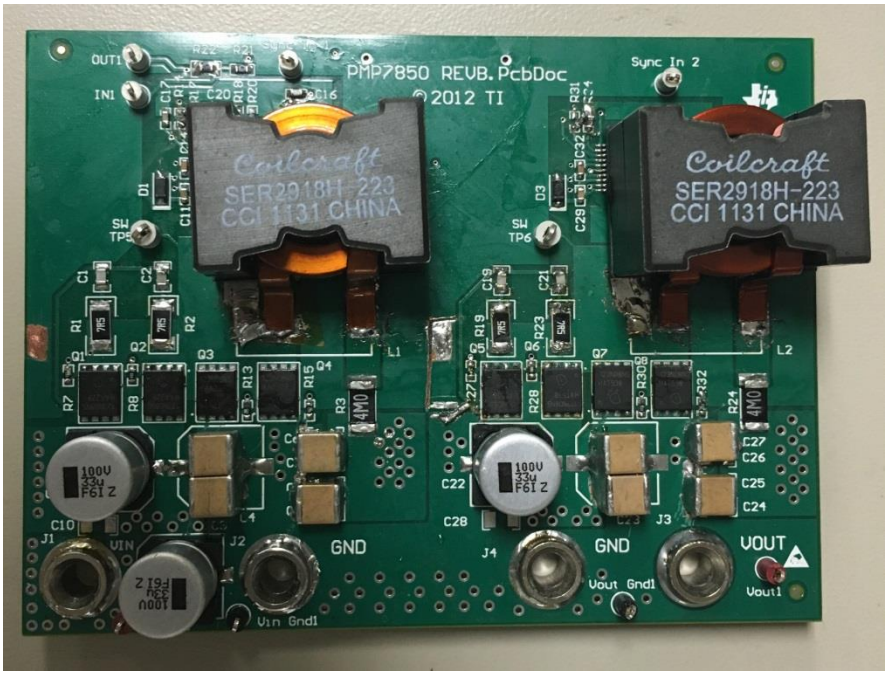
2. Circuit Description and PCB Details

PMP7979 is a synchronous dual-phase boost power supply using the LM5122 controllers. The design accepts an input voltage of 12V to 67V, and boosts a 54V output rail that's capable of sourcing 4.8A continuous current. The LM5122 has an internal current source to keep the high side FET to run at 100% duty cycle which allows a bypass operation when the input voltage is greater than the configured output voltage.

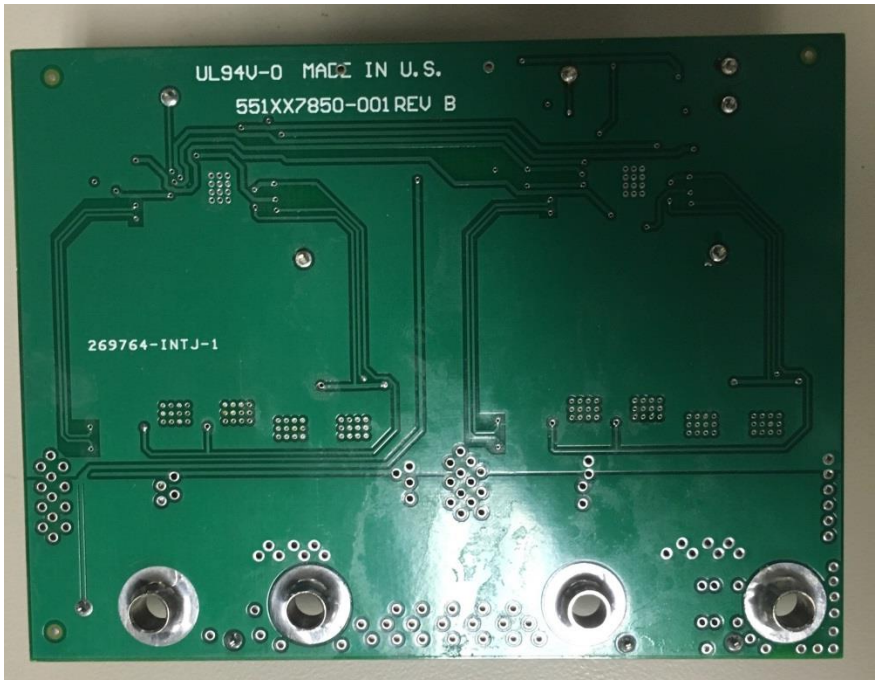
The design was built on PMP7850 with a dimension of 101mm * 76mm. Four layer PCB was used for the design, 1 oz. copper on top and bottom layer, 0.5 oz. copper on the internal layers.

3. PMP7979 Board Photos

Board Dimensions: 101mm x 76mm

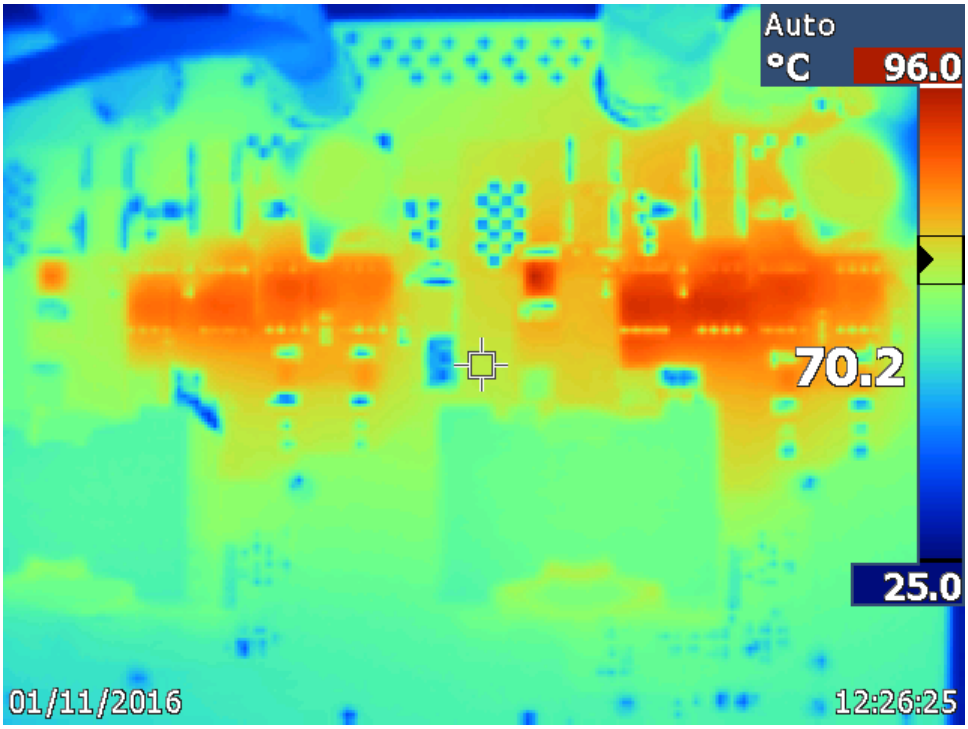


Board Photo (Top)

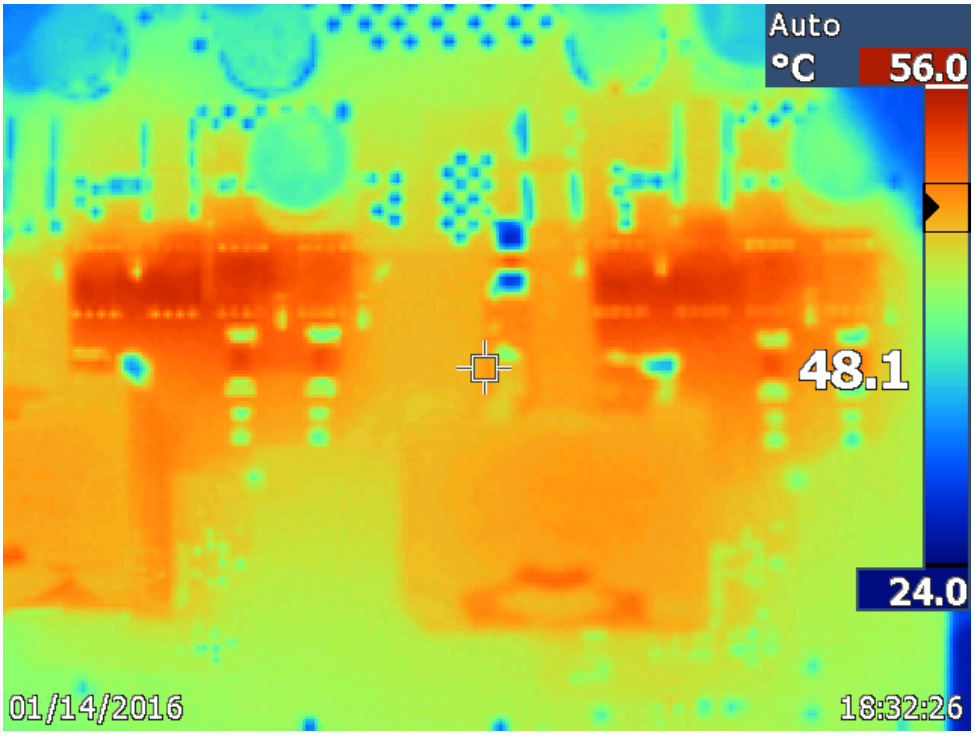


Board Photo (Bottom)

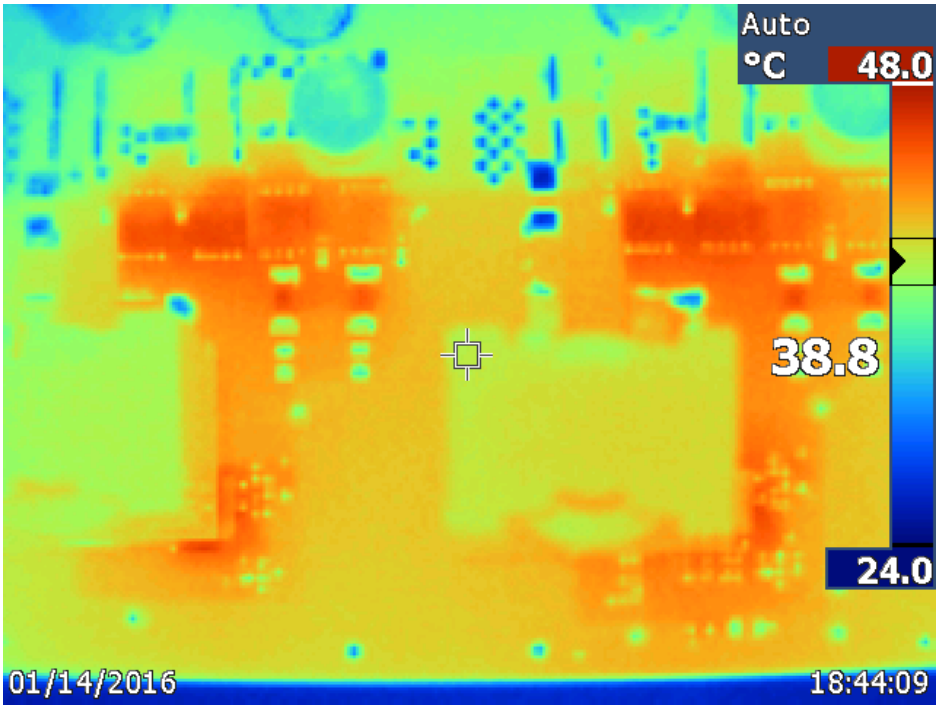
4. Thermal



Top Thermal image reaches equilibrium at 12Vin, 4.8A load.



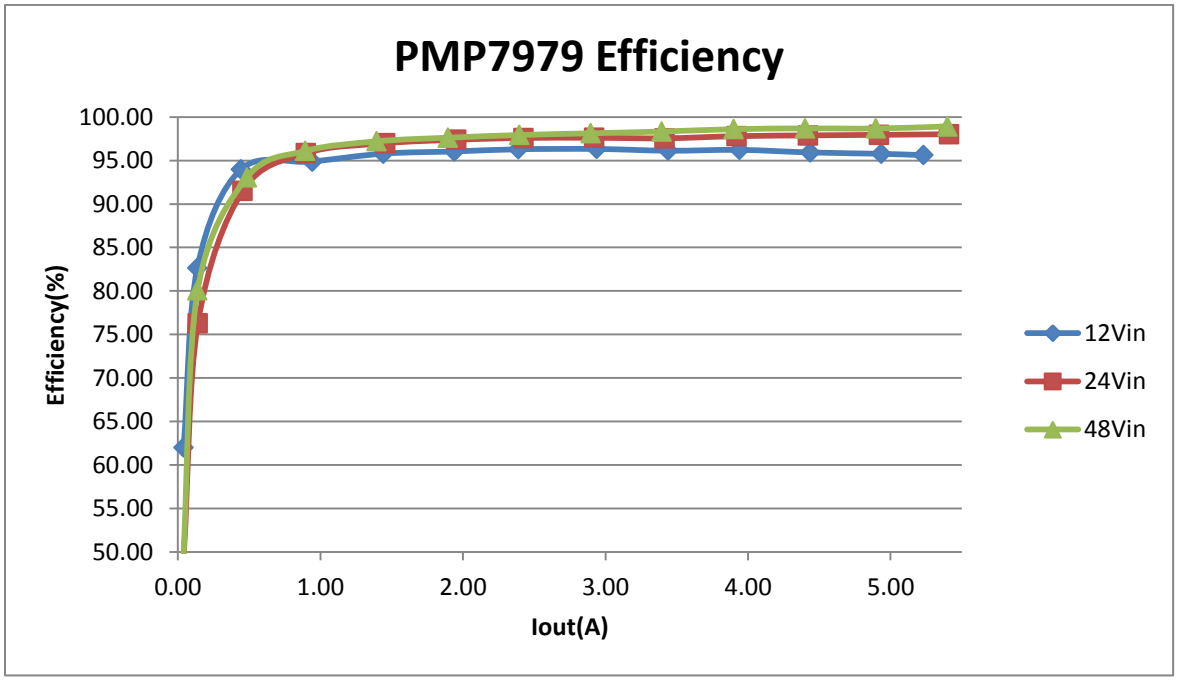
Top Thermal image reaches equilibrium at 24Vin, 4.8A load.



Top Thermal image reaches equilibrium at 48Vin, 4.8A load.

5. Efficiency

5.1 Efficiency Chart



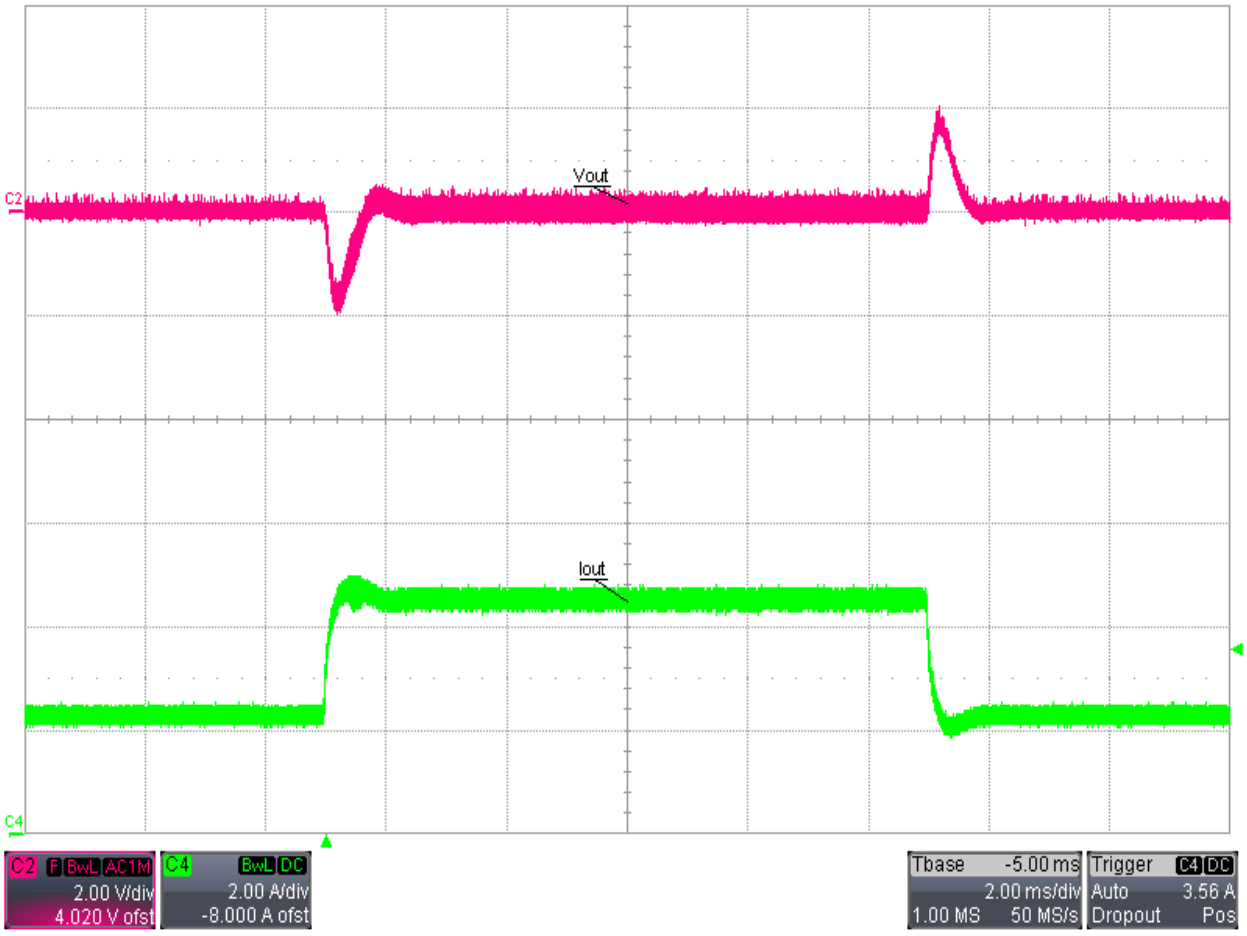
5.2 Efficiency Data

Vin(V)	Iin(A)	Pin(W)	Vout(V)	Iout(A)	Pout (W)	Losses(W)	Eff
12.00	0.09	1.13	53.95	0.00	0.00	1.13	0.00
12.00	0.29	3.48	53.95	0.04	2.16	1.32	62.01
12.00	0.74	8.88	53.96	0.14	7.34	1.54	82.64
12.00	2.12	25.38	53.96	0.44	23.85	1.53	93.97
12.00	4.47	53.58	53.96	0.94	50.83	2.75	94.87
12.00	6.77	81.24	53.97	1.44	77.82	3.42	95.79
12.00	9.09	109.02	53.97	1.94	104.70	4.32	96.04
12.00	11.16	133.86	53.98	2.39	128.89	4.97	96.29
12.00	13.73	164.76	53.98	2.94	158.70	6.06	96.32
12.00	16.10	193.20	53.99	3.44	185.72	7.48	96.13
12.00	18.43	221.10	54.00	3.94	212.74	8.36	96.22
12.00	20.81	249.72	54.00	4.44	239.54	10.18	95.93
12.00	23.20	278.40	54.02	4.94	266.62	11.78	95.77
12.00	24.64	295.68	54.03	5.23	282.71	12.97	95.61
Vin(V)	**Iin(A)**	**Pin(W)**	**Vout(V)**	**Iout(A)**	**Pout (W)**	**Losses(W)**	**Eff**
24.00	0.09	2.08	54.26	0.00	0.00	2.08	0.00
24.00	0.19	4.56	54.26	0.04	2.28	2.28	49.98
24.00	0.42	9.96	54.27	0.14	7.60	2.36	76.28
24.00	1.12	26.93	54.27	0.45	24.64	2.29	91.49
24.00	2.12	50.88	54.30	0.90	48.76	2.12	95.84
24.00	3.39	81.36	54.27	1.45	78.91	2.45	96.98
24.00	4.54	108.89	54.27	1.95	106.04	2.85	97.38
24.00	5.62	134.80	54.27	2.42	131.55	3.25	97.59
24.00	6.77	162.36	54.27	2.92	158.48	3.88	97.61
24.00	7.92	190.06	54.28	3.42	185.40	4.65	97.55
24.00	9.07	217.56	54.28	3.92	212.77	4.79	97.80
24.00	10.21	245.10	54.28	4.42	239.92	5.18	97.89
24.00	11.36	272.66	54.28	4.92	267.07	5.60	97.95
24.00	12.49	299.76	54.30	5.41	293.84	5.92	98.03
Vin(V)	**Iin(A)**	**Pin(W)**	**Vout(V)**	**Iout(A)**	**Pout (W)**	**Losses(W)**	**Eff**
48.00	0.04	1.70	54.30	0.00	0.00	1.70	0.00
48.00	0.08	4.03	54.30	0.04	1.95	2.08	48.49
48.00	0.20	9.36	54.31	0.14	7.49	1.87	80.07
48.00	0.59	28.25	54.31	0.48	26.29	1.96	93.05
48.00	1.05	50.52	54.31	0.89	48.55	1.97	96.10
48.00	1.62	77.88	54.30	1.39	75.70	2.18	97.20

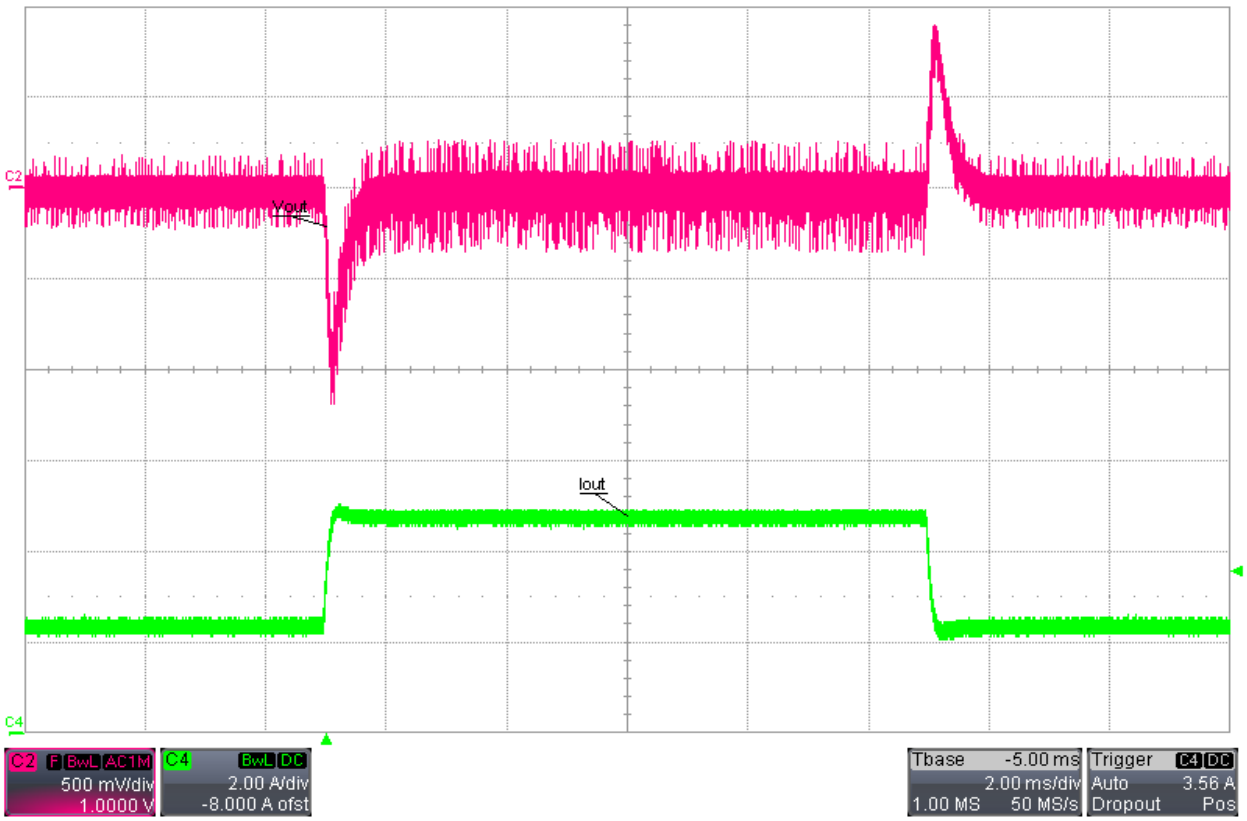
48.00	2.20	105.36	54.31	1.89	102.85	2.51	97.62
48.00	2.77	132.86	54.30	2.40	130.11	2.75	97.93
48.00	3.34	160.27	54.31	2.90	157.27	3.00	98.13
48.00	3.91	187.44	54.31	3.39	184.31	3.13	98.33
48.00	4.48	214.80	54.31	3.90	211.79	3.01	98.60
48.00	5.04	242.11	54.31	4.40	238.94	3.17	98.69
48.00	5.61	269.45	54.31	4.90	265.88	3.57	98.68
48.00	6.18	296.45	54.30	5.40	293.24	3.21	98.92

6 Waveforms

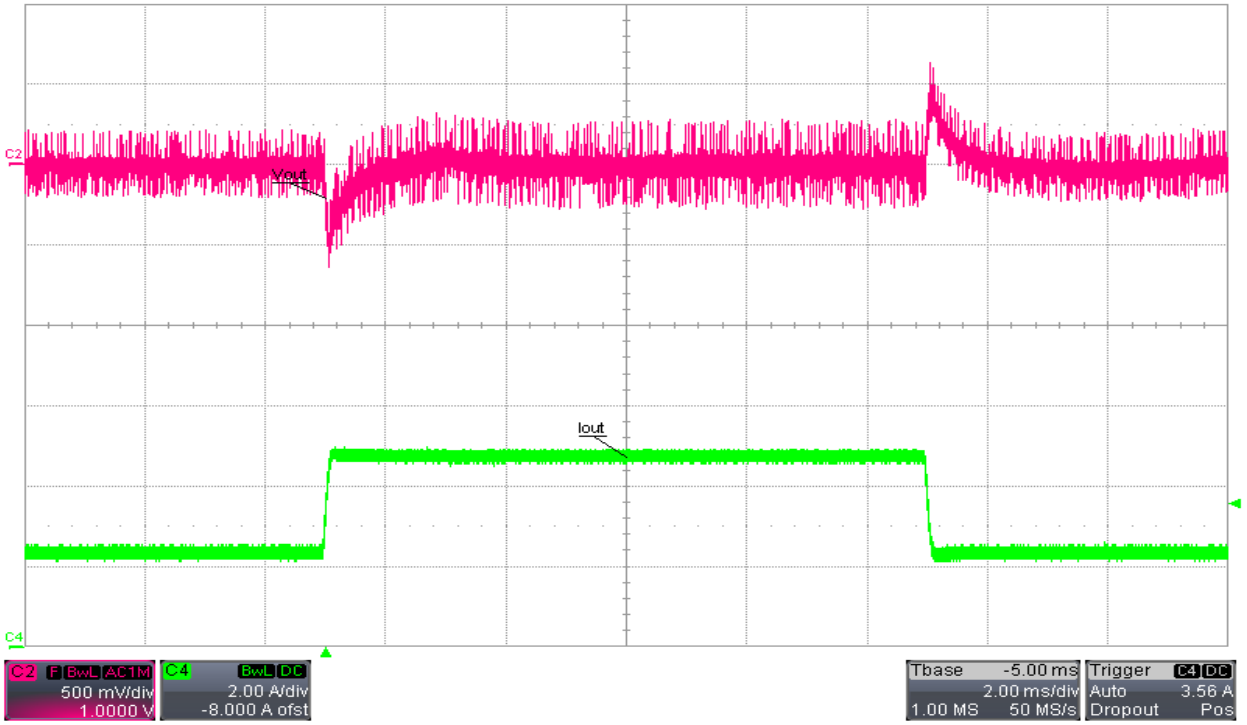
6.1 Load Transient Response



Load Transient Response at 12Vin and 2.4A-to-4.8A Load Step, Ch2 – Vout (AC coupled), Ch4- Iout.

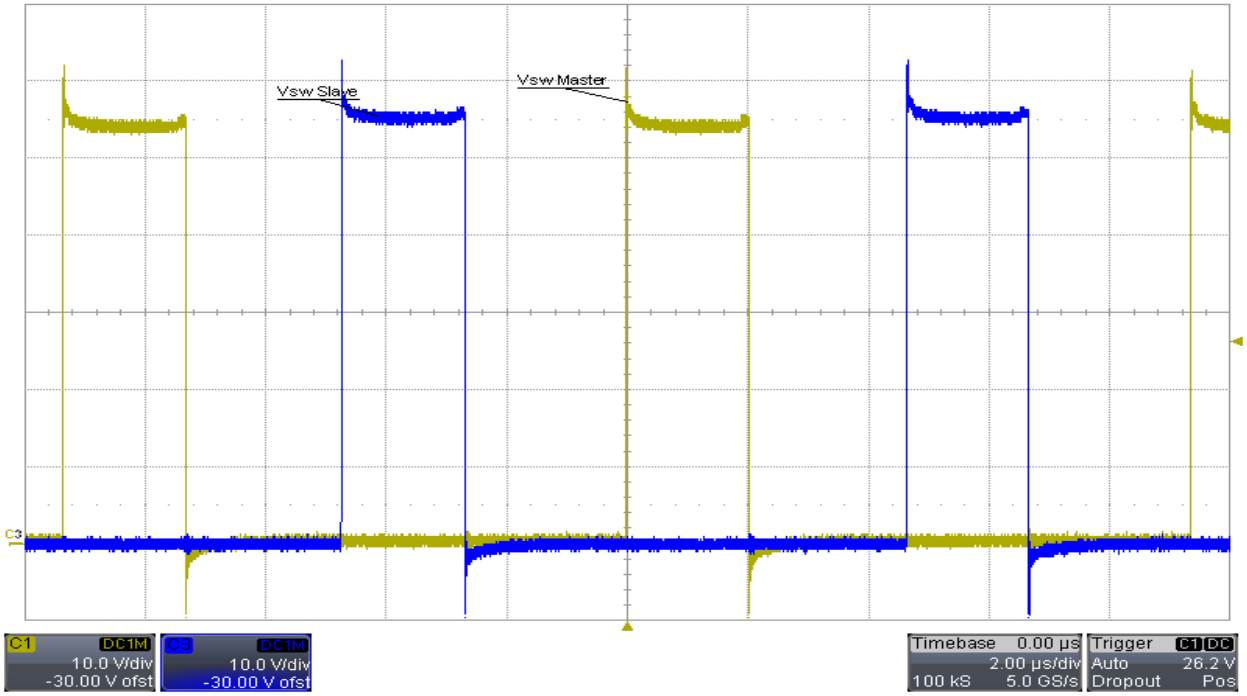


Load Transient Response at 24Vin and 2.4A-to-4.8A Load Step, Ch2 – Vout (AC coupled), Ch4- Iout.

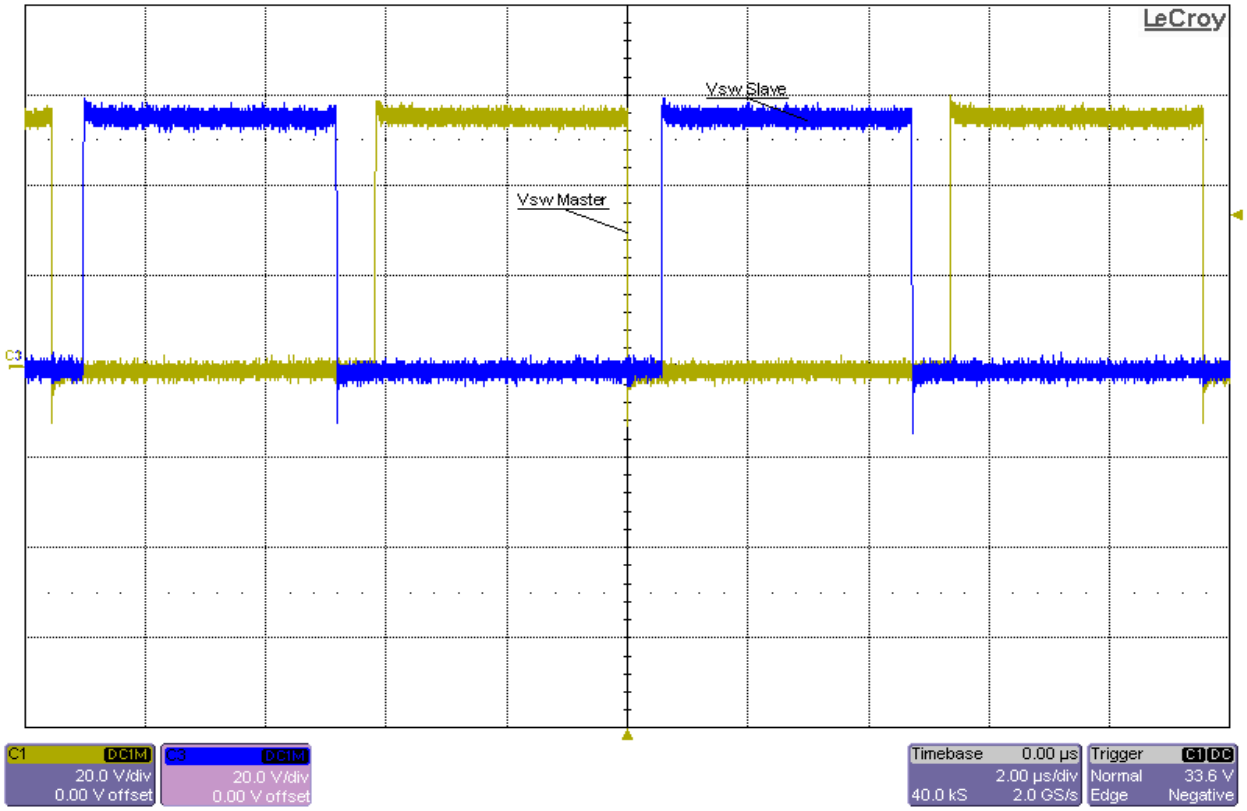


Load Transient Response at 48Vin and 2.4A-to-4.8A Load Step, Ch2 – Vout (AC coupled), Ch4- Iout.

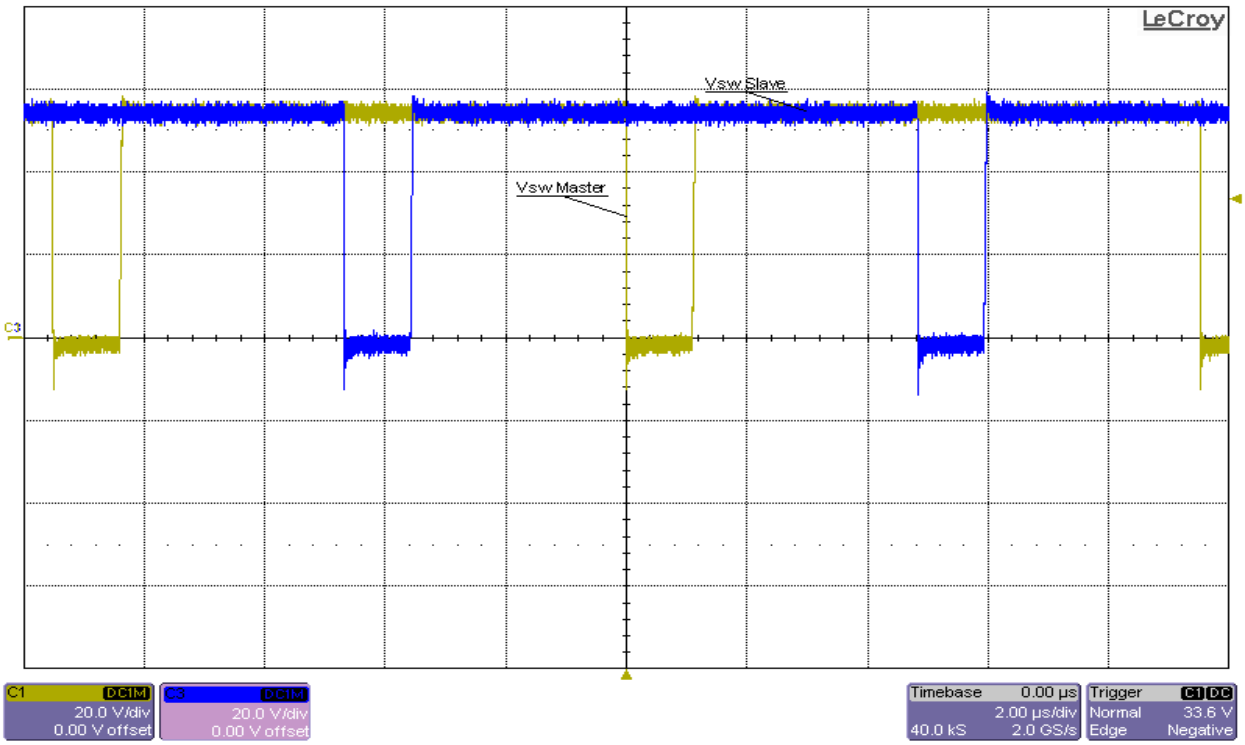
6.2 Switch Node Voltage and Output Ripple



Switch Node Voltage of 12Vin and Full Load. Ch1-SW Master, Ch2-SW Slave.

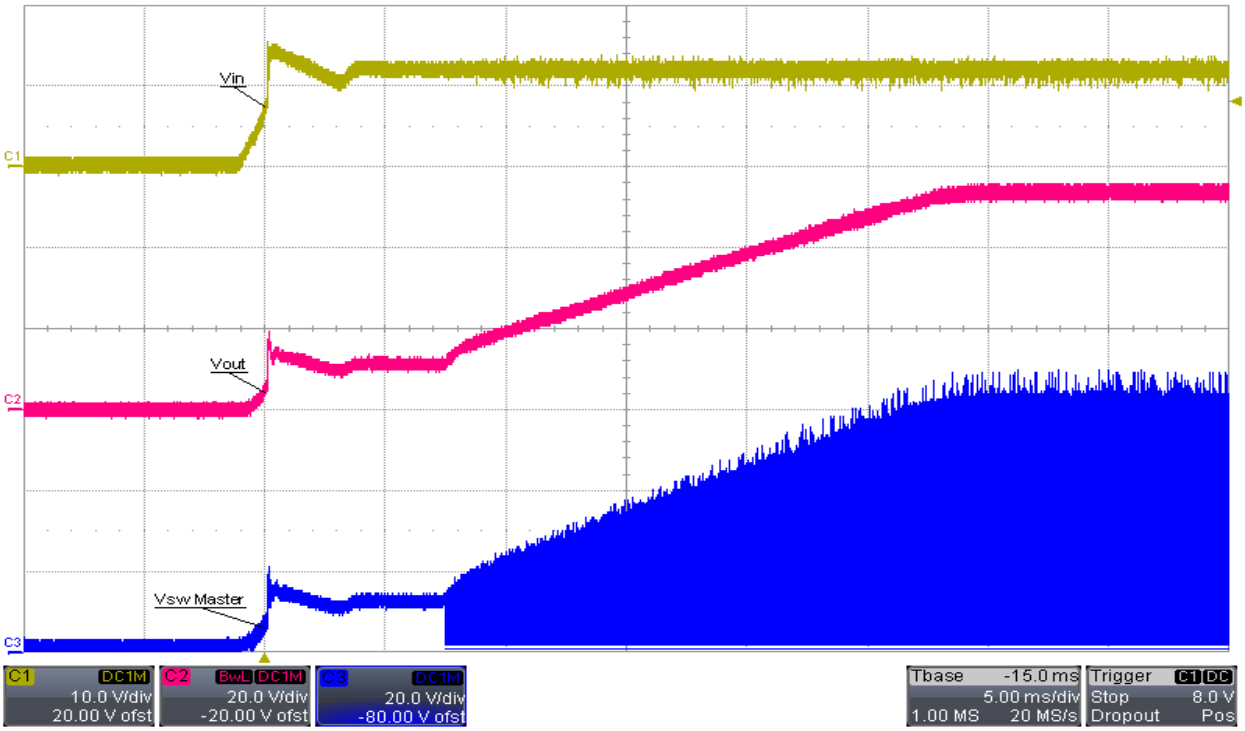


Switch Node Voltage of 24Vin and Full Load. Ch1-SW Master, Ch2-SW Slave.

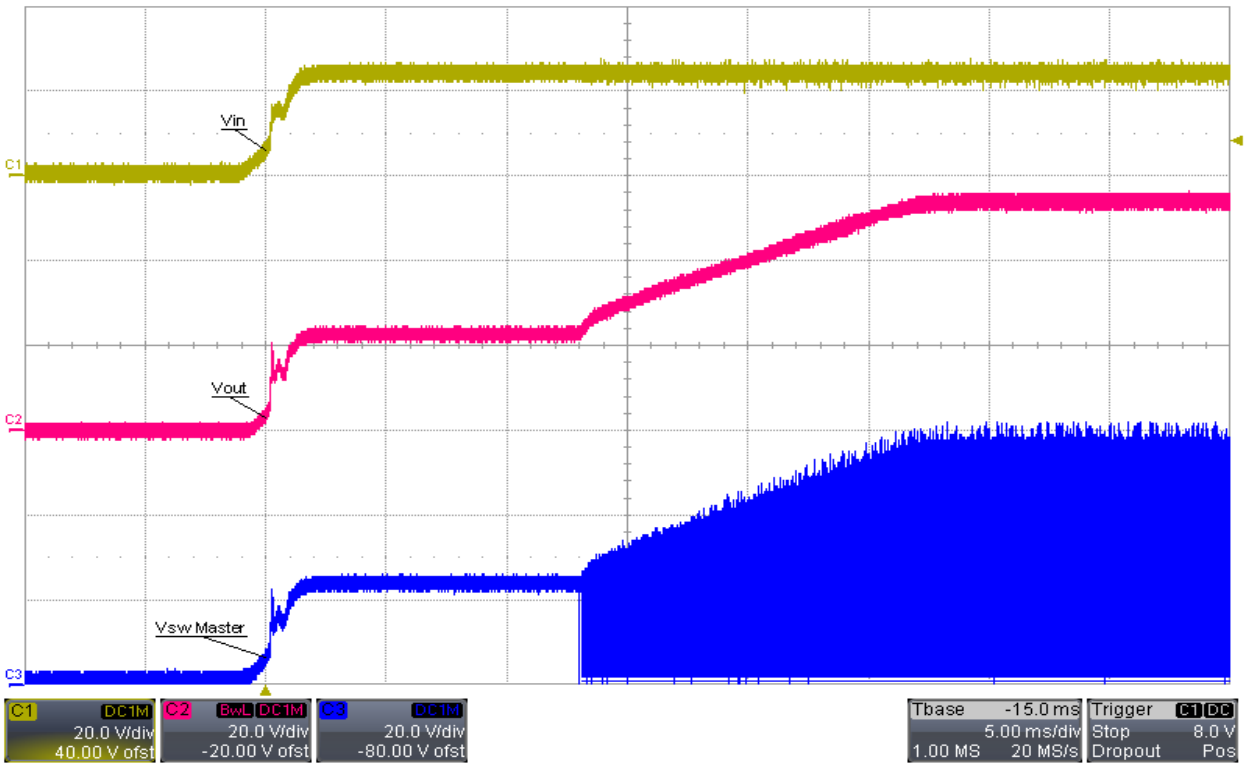


Switch Node Voltage of 48Vin and Full Load. Ch1-SW Master, Ch2-SW Slave.

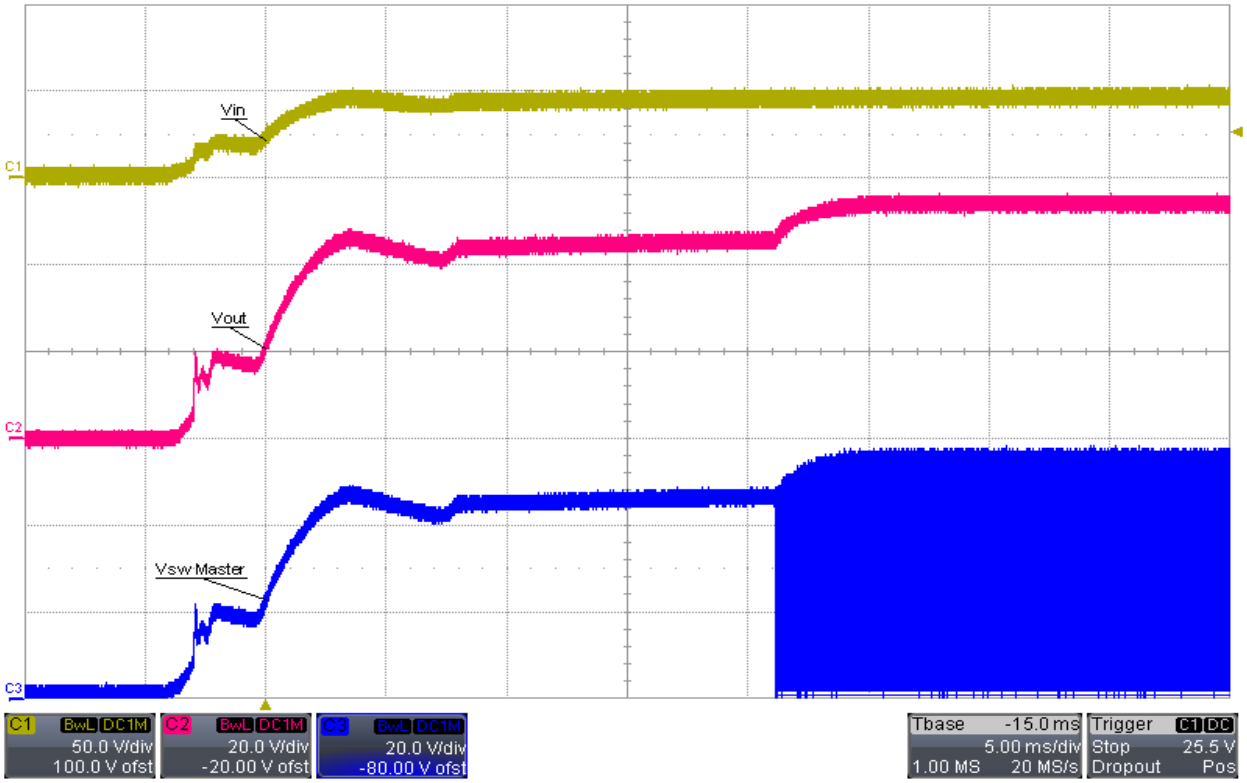
6.3 Start Up



Start-up from 12Vin and Full Load. Ch2-Vout, Ch1-Vin, Ch3-Vsw Master.

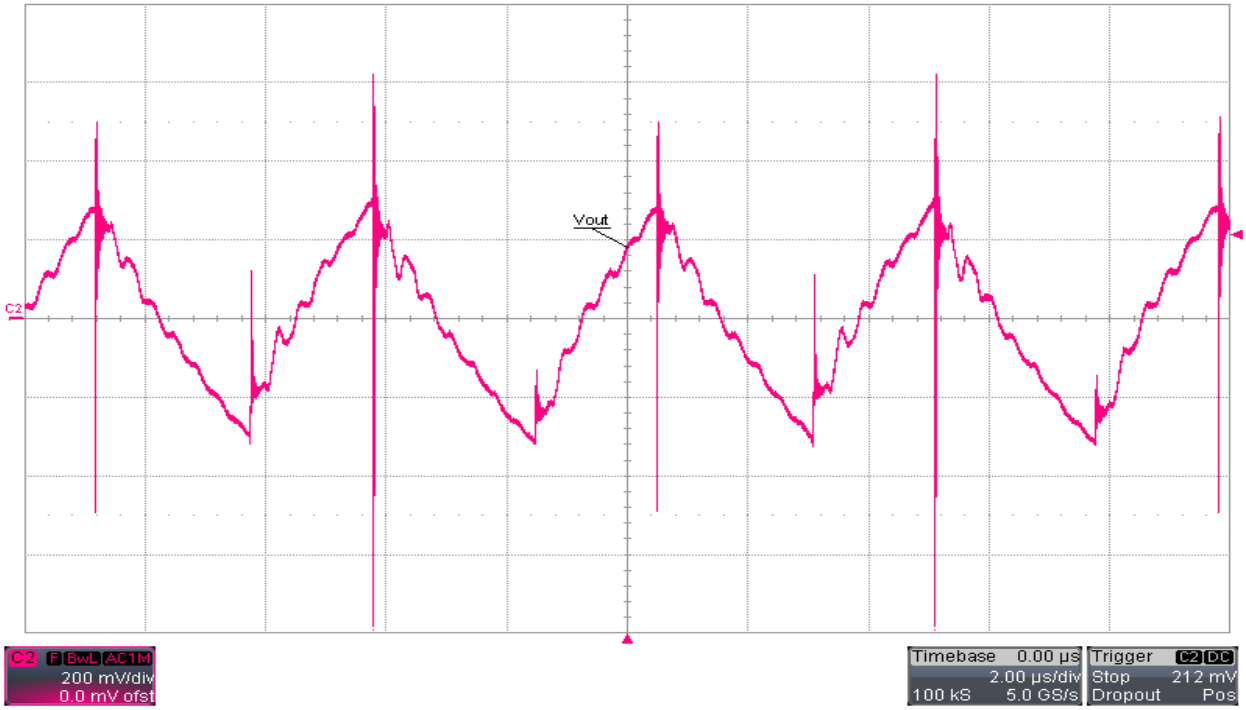


Start-up from 24Vin and Full Load. Ch2-Vout, Ch1-Vin, Ch3-Vsw Master.

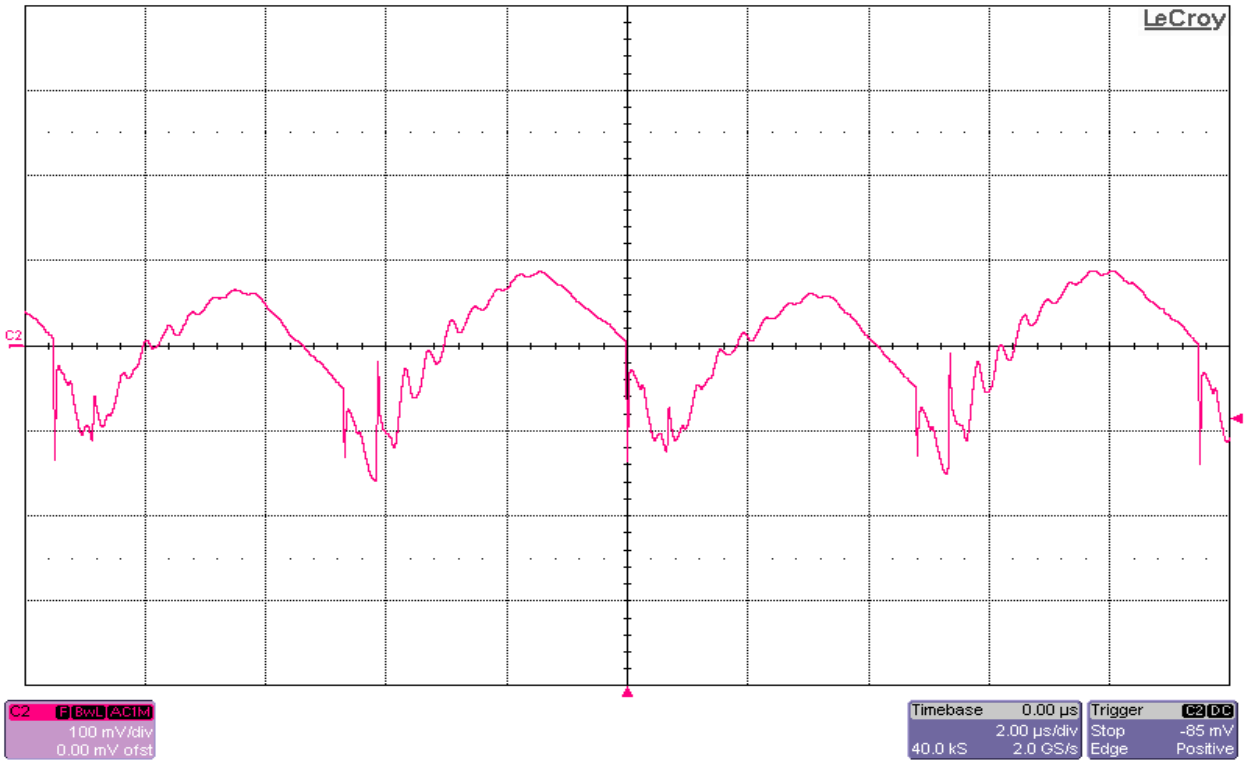


Start-up from 48Vin and Full Load. Ch2-Vout, Ch1-Vin, Ch3-Vsw Master.

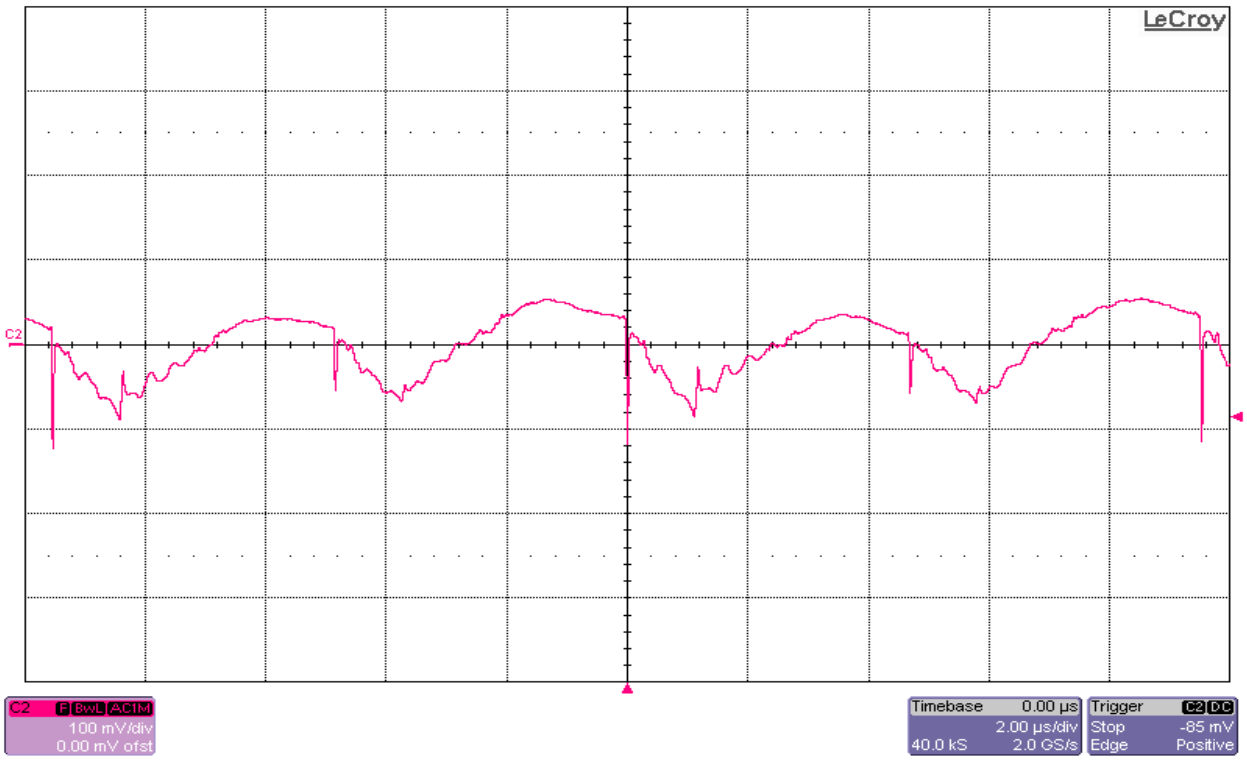
6.4 Output Ripple



Output Ripple at 12Vin and Full Load. Ch2-Vout.

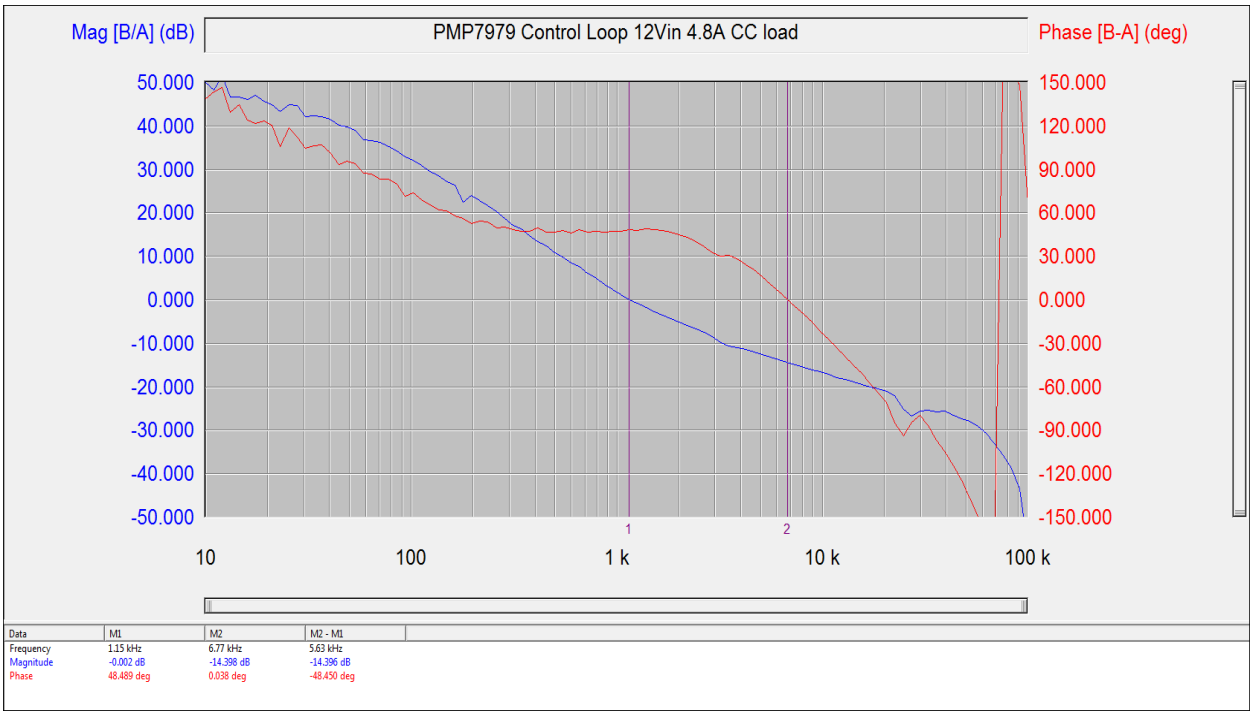


Output Ripple at 24Vin and Full Load. Ch2-Vout.

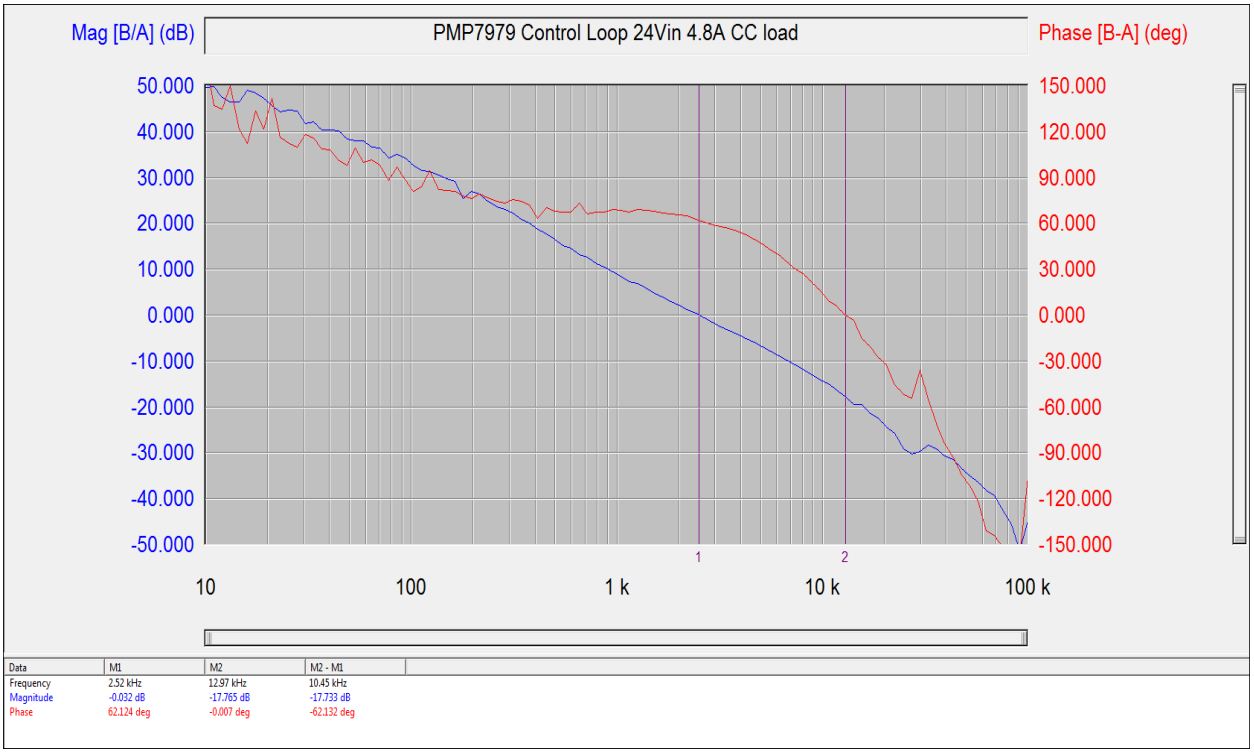


Output Ripple at 48Vin and Full Load. Ch2-Vout.

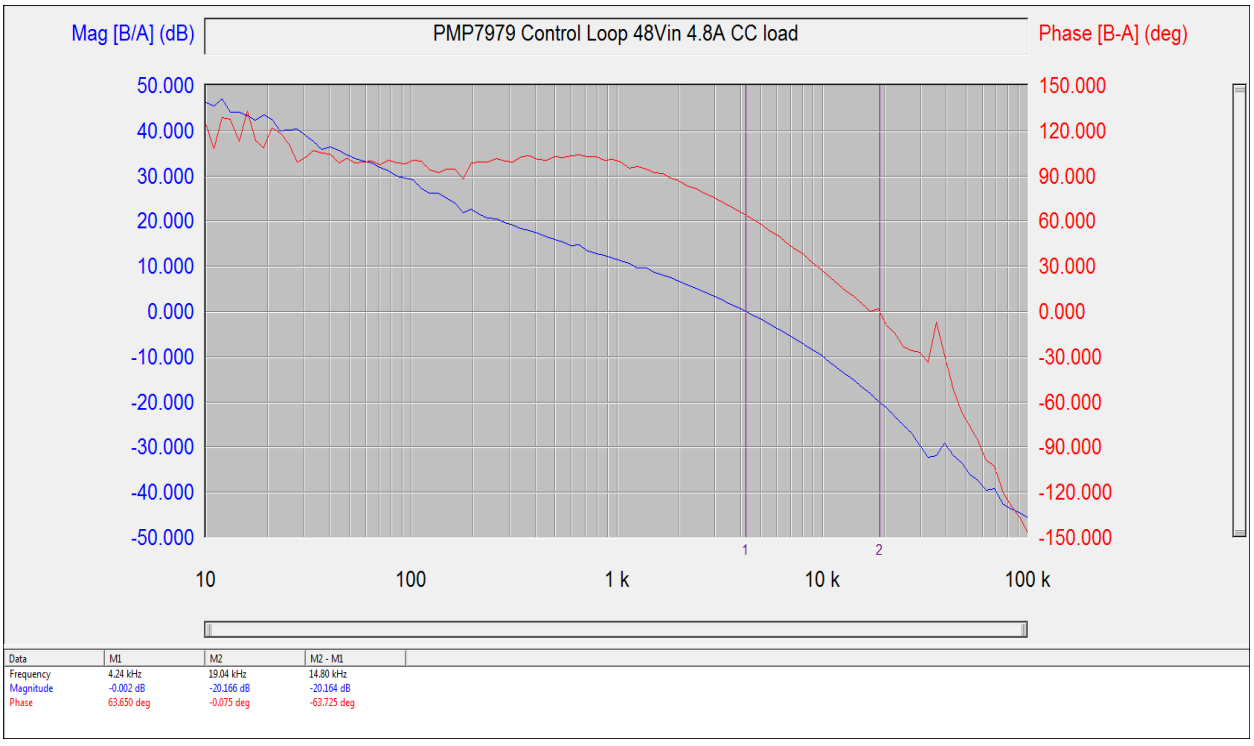
6.5 Frequency Analysis



Control Loop Analysis at 12Vin 4.8A Full Load, Phase Margin of 49 deg, Gain Margin of 14.4dB.

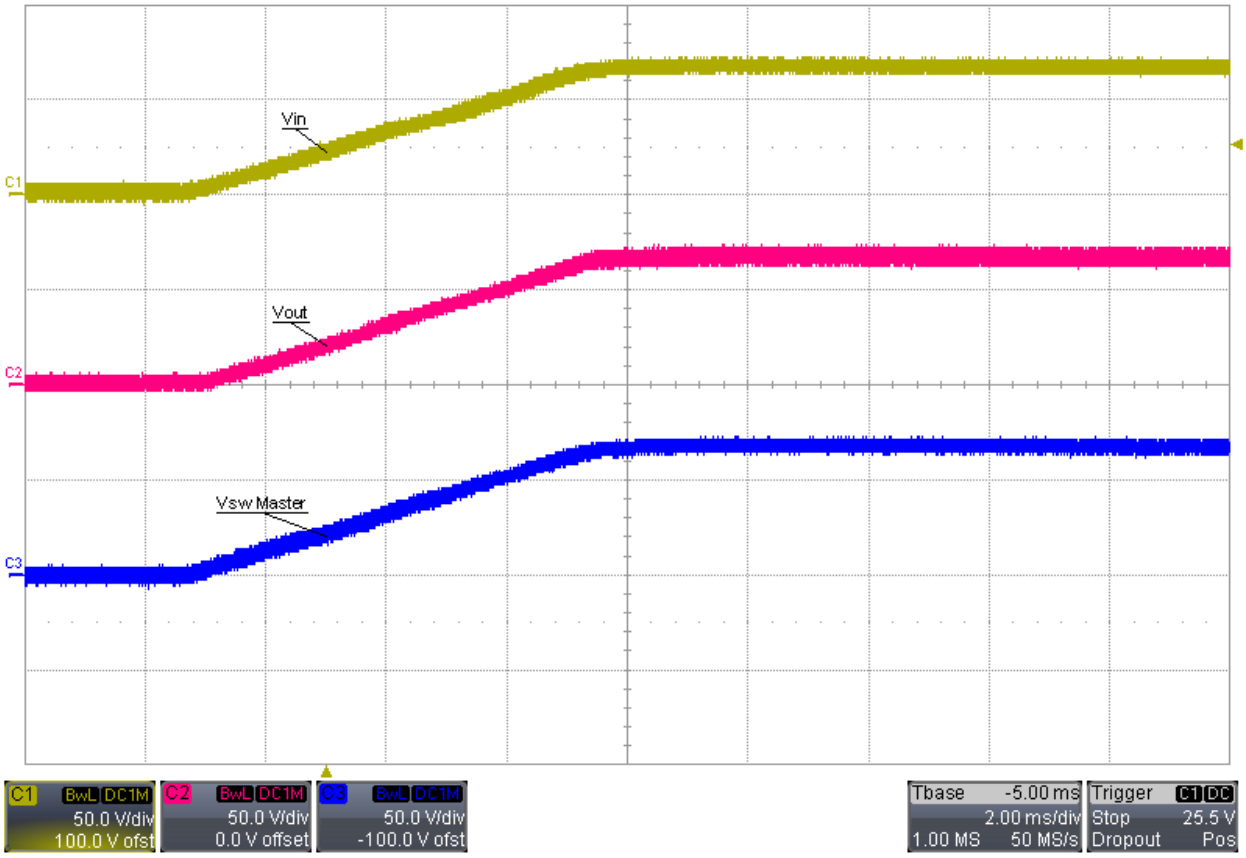


Control Loop Analysis at 24Vin 4.8A Full Load, Phase Margin of 62 deg, Gain Margin of 17.7dB.



Control Loop Analysis at 48Vin 4.8A Full Load, Phase Margin of 63.6 deg, Gain Margin of 20.1dB.

6.6 Bypass



Bypass operation at 67Vin. Ch1-Vin, Ch2-Vout, Ch3-Vsw Master.

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