

TI Designs: TIDEP-0070

DDR ECC Reference Design to Improve Memory Reliability in 66AK2Gx-Based Systems



TI Designs

This reference design describes system considerations for the DDR-SDRAM memory interface with Error Correcting Code (ECC) support in high-reliability applications based on the 66AK2Gx Multicore DSP + ARM® System-on-Chip (SoC). System interfaces, board hardware, software, throughput performance, and diagnostic procedures, are discussed. Detailed description about the DDR interface is available in the device Technical Reference Manual (TRM).

Design Resources

TIDEP0070	Design Folder
66AK2G02	Product Folder
66AK2G12	Product Folder
K2G General Purpose EVM	EVM Tool Folder
Processor SDK for K2G	Download Software

Features

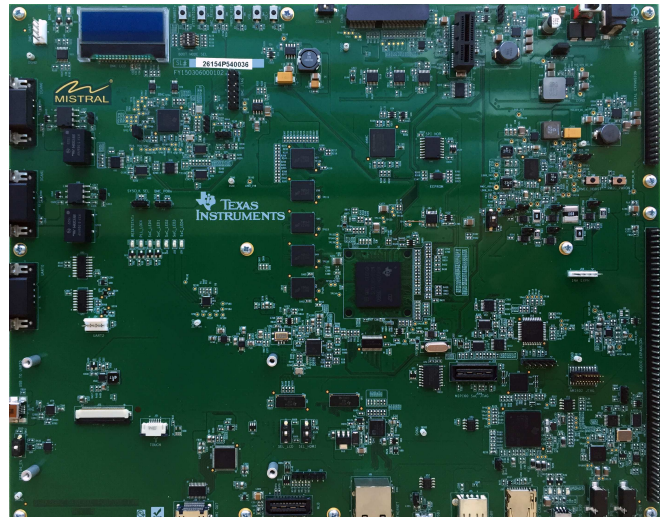
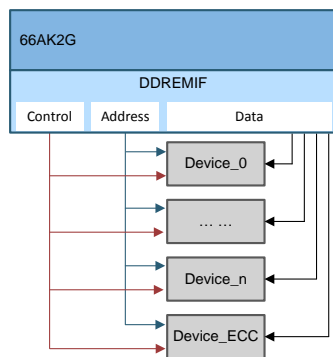
- 32-bit DDR3L Interface With Optional 4-bit ECC for High-Reliability System Designs
- Flexible System Configurations With DDR ECC
- Built-In Read-Modify-Write (RMW) Hardware Supporting ECC Operation With Non-Aligned Access
- Minimum Performance Impact
- Implemented and tested on EVMK2G Hardware and Supported in Processor SDK for K2G

Applications

- Automotive Audio Amplifiers
- Home Audio
- Professional Audio
- Power Protection
- Industrial Communications and Controls



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1 Introduction

The 66AK2Gx SoC supports the following features:

- **Processor Cores and Memory**
 - Arm® Cortex-A15 up to 1000 MHz
 - 32 KB L1D, 32 KB L1P, 512 KB L2 cache
 - C66x DSP up to 1000 MHz
 - 32 KB L1D, 32 KB L1P, 1 MB L2 cache or RAM
 - 1MB of Shared L2 MSMC SRAM
 - ECC on all memory
- **Industrial and Control Peripherals**
 - 2 Industrial Communication Subsystems enable cut through, real-time and low-latency Industrial Ethernet protocols
 - Programmable real-time I/O enables versatile field bus and control interfaces
 - PCIe for connection to an FPGA or ASIC that provides industrial network connections, backplane communication or connection to another 66AK2Gx device
- **Security and Crypto**
 - Standard secure boot with customer programmable OTP keys
 - Crypto Engine hardware accelerator and TRNG
- **Package**
 - 21 x 21 mm, 0.8 mm pitch BGA 625 pins

The 66AK2Gx SoC is suited for applications such as Industrial PLC and Protection Relay as shown in [Figure 1](#) and [Figure 2](#). In these systems ECC on the memory is required for achieving reliability requirements. Device reliability requires managing failures that can cause the device not to function correctly at any point during its expected lifetime.

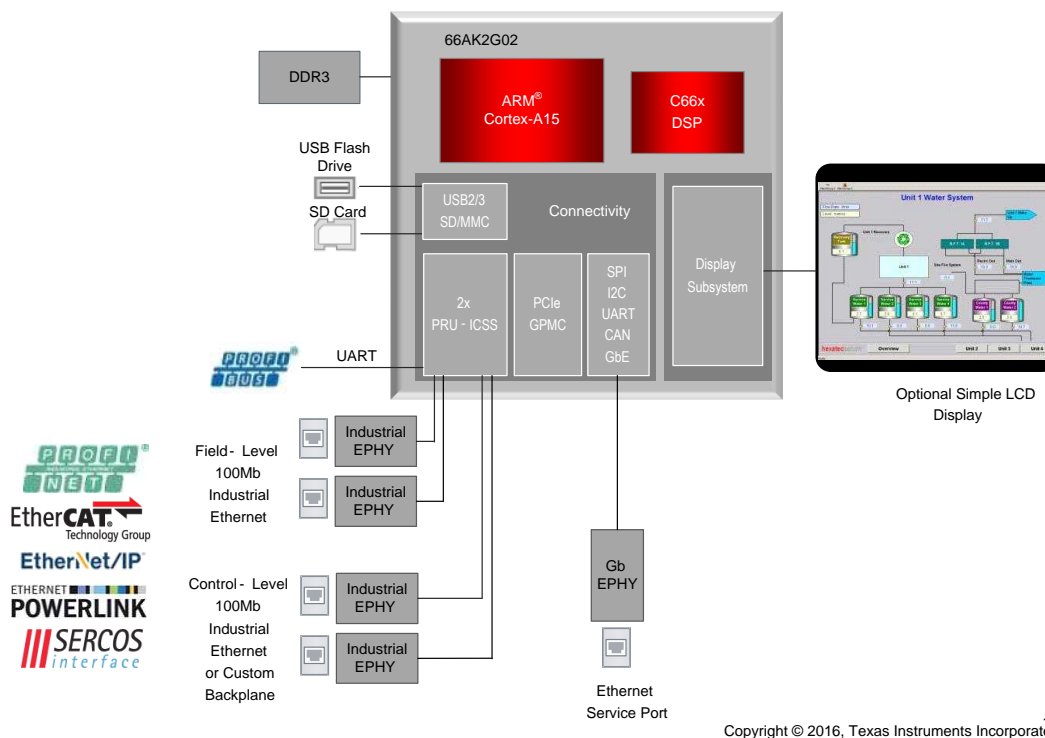
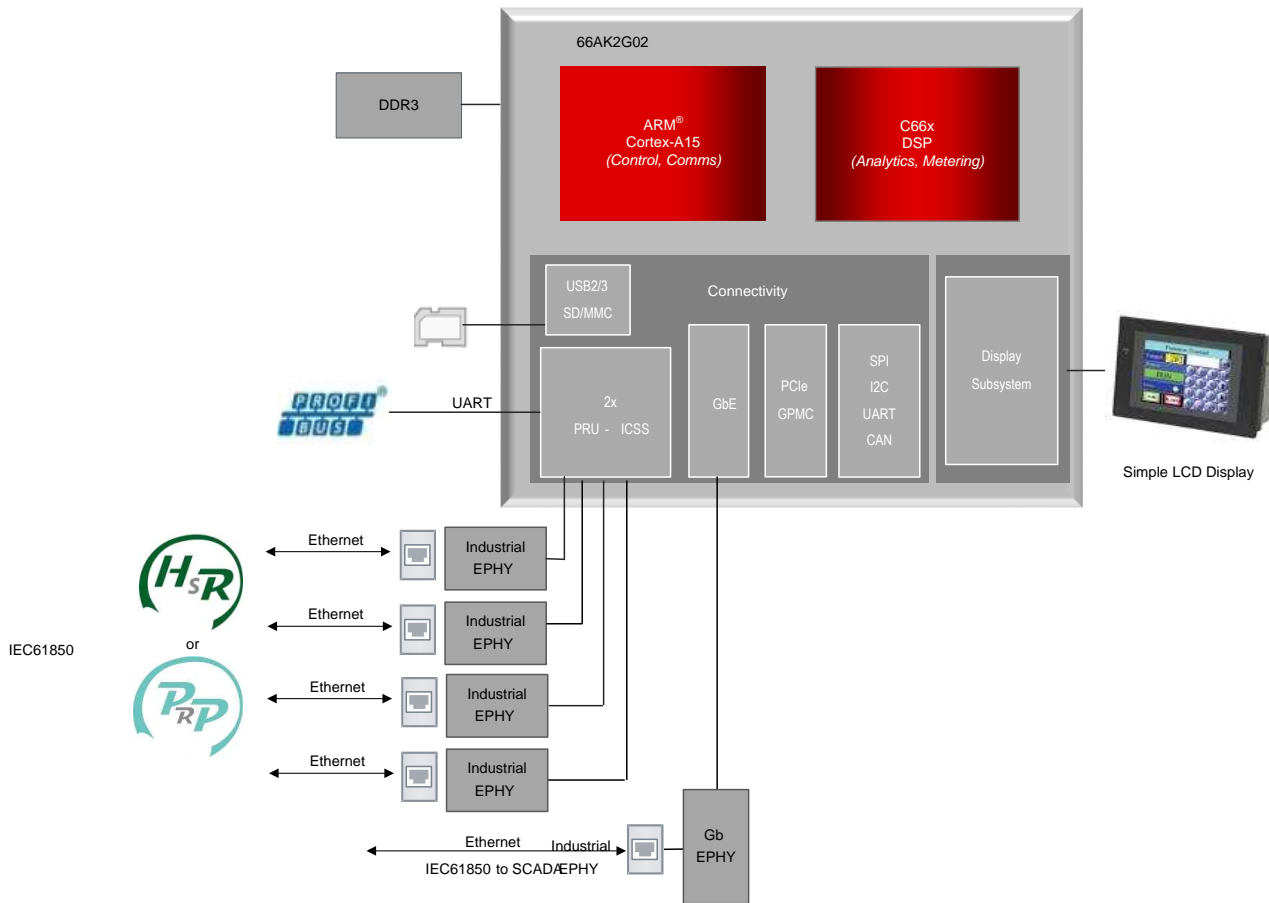


Figure 1. Industrial PLC System Block Diagram



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Figure 2. Protection Relay System Block Diagram

Error Correcting Code (ECC) memory is commonly used in server and communications infrastructure systems today and has significantly improved system reliability. In embedded systems, a similar trend is observed, where ECC memory is required for a variety of applications, such as:

- Safety-critical industrial and factory automation systems
- Harsh operating environment such as extreme temperature, pressure or radiation environment
- Always-on systems with extended duty hours

Figure 3 shows the relative failure rate reduction when ECC is used.

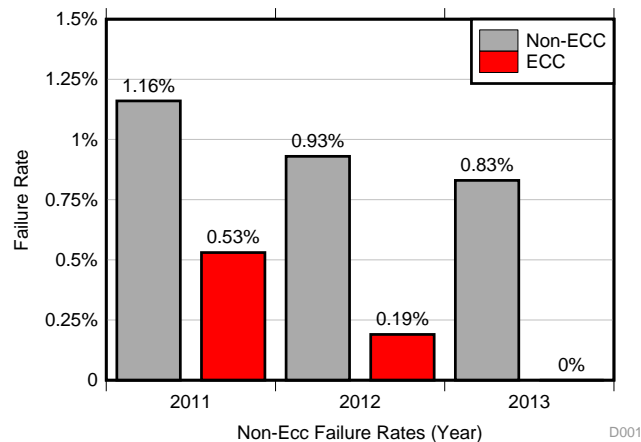


Figure 3. Memory Failure Rate Reduction With ECC

The 66AK2Gx SoC supports various methods of ECC in its internal memory and external memory interfaces. Namely, ECC is supported on:

- Processor core memory blocks
- Internal Multicore Shared Memory Controller (MSMC) SRAM
- Embedded SRAM memory blocks in other subsystems
- DDR3L memory interface

Except for the L1P in the A15 processor core, all ECC functions listed above implement Single Error Correction and Double Error Detection (SECCDED) method using Hamming Code.

This design guide focuses on the DDR interface design with ECC in systems where high reliability is required. The DDR3L memory interface supports standard 32-bit DDR3L interface up to 800MT/s. Additional 4-bit data is available to support optional Error Correcting Code (ECC). ECC is performed on 32-bit quanta based on the SECCDED algorithm. When the DDREMIF is used as 16-bit interface, no ECC is supported.

2 System Overview

The DDR3L interface consists of the following subsystems:

- DDREMIF controller — digital interface, FIFOs, and ECC module
- DDR3LPHY — consists of DDR3L PHY macros and system interface logic

Figure 4 shows the interconnect of the sub-modules in the 66AK2Gx SoC.

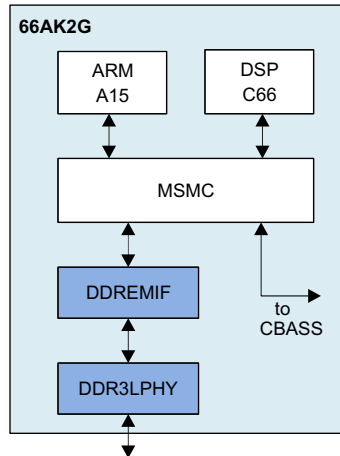
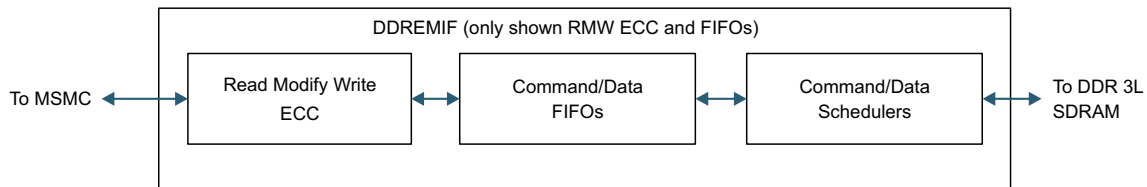


Figure 4. DDREMIF and DDR3L PHY Subsystems in 66AK2Gx Devices

The ECC block is connected in front of the data and command FIFOs within the DDREMIF controller, as shown in Figure 5. The ECC block enables the Read-Modify-Write (RMW) feature that is not available in some earlier KeyStone™ II devices. The RMW block allows data write that is not aligned to a 32-bit boundary, by first read, the full quanta data from the DDR device merges with the non-aligned data, recalculates ECC, and writes back to DDR. This procedure incurs extra write latency.



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Figure 5. ECC Block With RMW in DDREMIF Controller

3 System Specifications

Table 1 lists different DDR configurations depending on the required DDR interface for the device.

NOTE: The 4-bit devices are not supported unless the device is used as an ECC device.

Table 1. DDR Configurations for 66AK2Gx-Based Systems

CONFIGURATION	DDR WIDTH	DDR DEVICES	ECC
1	16-bit DDR3L with no ECC	2 × 8b	–
2	16-bit DDR3L with no ECC	1 × 16b	–
3	32-bit DDR3L with no ECC	4 × 8b	–
4	32-bit DDR3L with no ECC	2 × 16b	–
5	32-bit DDR3L with 4-bit ECC	4 × 8b	1 × 4b
6	32-bit DDR3L with 4-bit ECC	4 × 8b	1 × 8b (tie-off upper 4-bit)
7	32-bit DDR3L with 4-bit ECC	2 × 16b	1 × 4b
8	32-bit DDR3L with 4-bit ECC	2 × 16b	1x8b (tie-off upper 4-bit)
9	No DDR	–	–

Figure 6 shows an example system interconnection between 66AK2Gx and five 8-bit external devices.

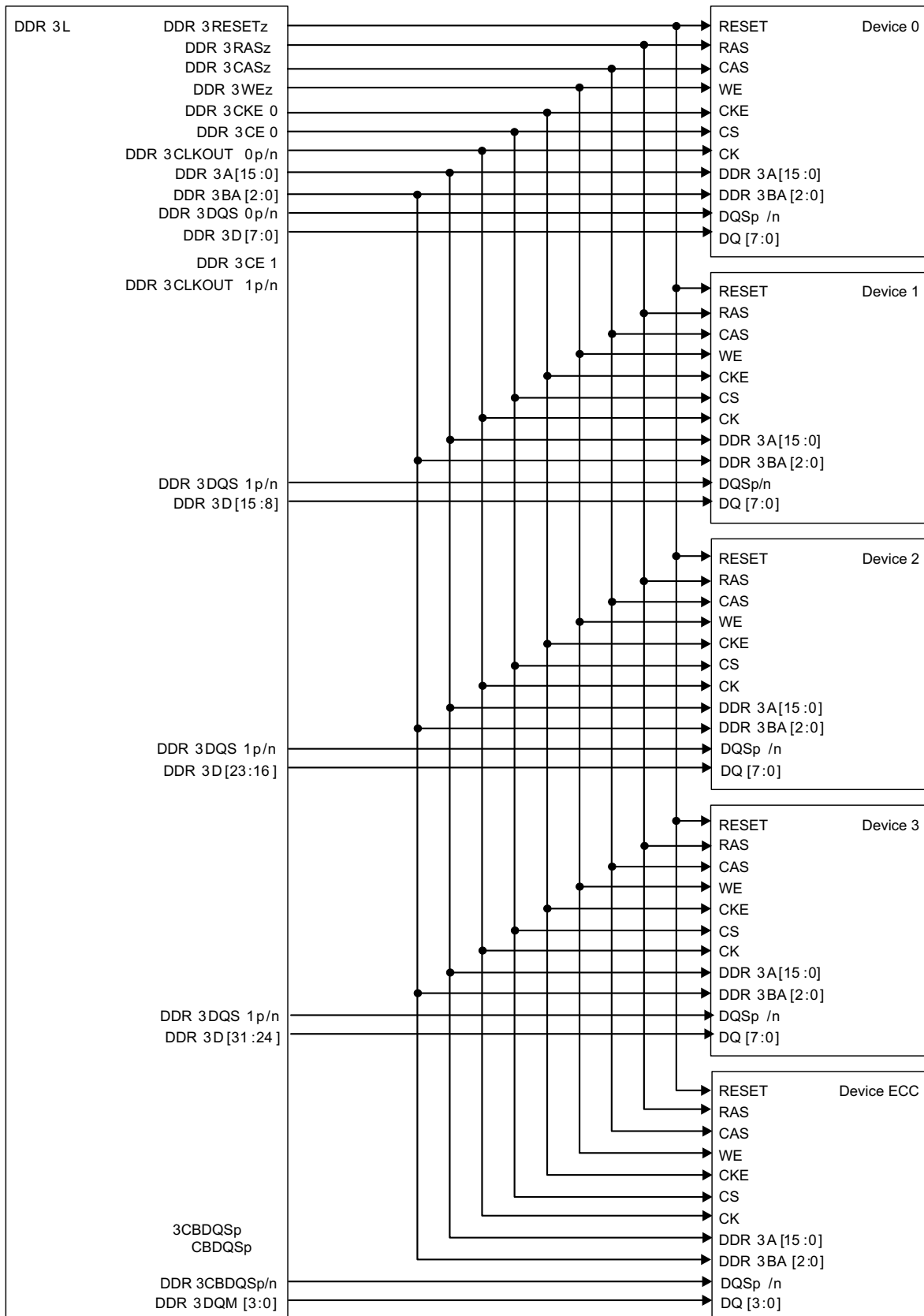


Figure 6. Signal Interconnect of 4 × 8 + 1 × 8 32-bit DDR configuration with ECC

Figure 7 shows the DDR3L device placement relative to the 66AK2Gx device on the EVMK2G board.

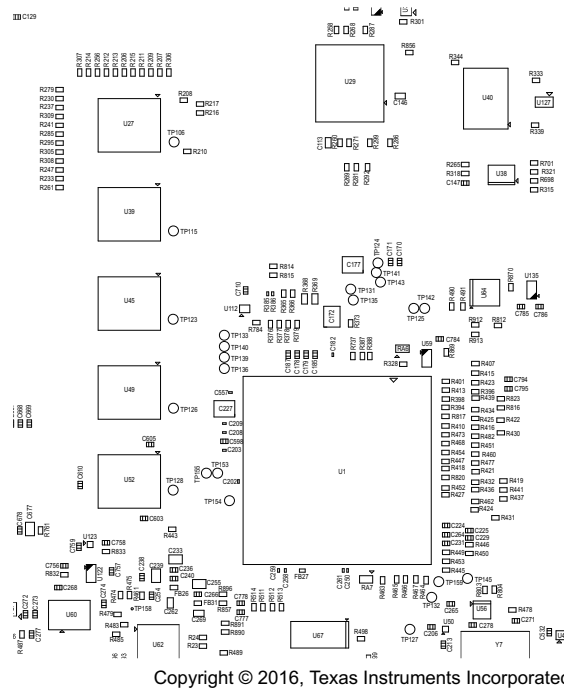


Figure 7. DDR3L Device Placement near the 66AK2Gx Device on the EVMK2G Board

Figure 8 shows the DDR devices on the EVMK2G.

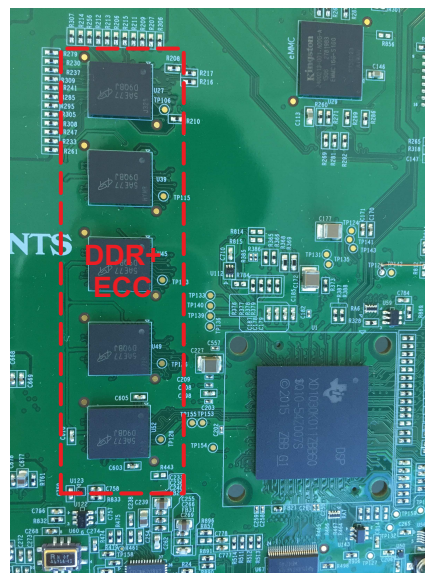


Figure 8. DDR Devices on the EVMK2G

4 Software

The processor SDK supports configuration, initialization, and testing on the DDR ECC, for systems using the feature.

4.1 Initialization

ECC and RMW options are controlled by memory mapped registers. Refer to the device datasheet ([SPRSP07](#)) for the exact register address and assignment. The RMW feature is always enabled whenever ECC is enabled. The following steps are involved to enable ECC:

1. Enable bit[35:32] of the PHY macro (including leveling and training)
2. Enable ECC + RMW
3. Read back control register and verify ECC+RMW is enabled
4. Initialize DDR memory to validate ECC syndrome

NOTE: The entire ECC enabled DDR space must be initialized before any of the ECC memory region is used. Otherwise, due to RMW operations, a non-aligned write operation may invoke the DDREMIF to read back an incorrect ECC syndrome and thus cause ECC error.

Figure 9 shows an example GEL script to enable ECC.

```

ddr3A_setup(int ECC_Enable, int DUAL_RANK)
{
    ... ..

    if(ECC_Enable == 0)
    {
        read_val = DDR3A_DATX8_4;
        DDR3A_DATX8_4 = read_val & 0xFFFFFFFF; //Disable ECC byte lane
    }
    ... ..

    if(ECC_Enable==1)
    {
        //Enable ECC
        //0xB0000000: ECC_EN=1, ECC_VERIFY_EN=1, RMW_EN=1
        //0x50000000: ECC_EN=1, ECC_VERIFY_EN=0, RMW_EN=1
        DDR3A_ECC_CTRL = 0xB0000000;
        read_val = DDR3A_ECC_CTRL;
        if(read_val!=0xB0000000){
            GEL_TextOut("\nIncorrect data written to DDR3A_ECC_CTRL..");
        }
    }
}

```

Figure 9. GEL Script to Enable ECC and RMW

4.2 Verification and Diagnostics

Frequently, it may be required to verify the proper operation of the ECC, especially when the final product is presented to an independent safety compliance assessment body. A simple technique to prove out the proper operation of ECC may be:

1. Enable ECC, write a set of data to DDR. The data could be a combination of aligned and non-aligned bytes.
2. Read and verify these data matched to originals.
3. Disable the ECC by changing the control register.
4. Write a modified data set to the same address, modified means some data has 1 bit errors and some data has 2 or more bits of errors.
5. Reenable ECC.
6. Read back these data and compare with original, verify that single bit error counter increased when accessing single bit modified data, and a kernel panic happened when more than one bit modified data is accessed.

This procedure must be performed to ensure that no other DDR access is present. A real-life random memory bit error may be generated in a laboratory where the device is running under bombardment of high-energy particles such as a high-energy physics accelerator facility.

4.3 ECC Error Handling

Kernels of operating systems typically handle ECC error interrupts. Single-bit errors are automatically corrected when the data is presented to the host, however, data stored in the memory is not corrected. To reduce the probability of another single-bit error from happening in the same quanta block, perform software scrubbing where a scrubbing software performs periodic access to ECC-protected DDR space. When a single-bit error occurs, the scrubbing software first reads, and then writes back the correct data so the memory content is correct. Current K2G Processor SDK Linux® kernel does not perform scrubbing. For a 1-bit ECC error, no direct interrupt will be generated, instead the EMIF can be programmed with a threshold to its ECC Error Count Register. An interrupt will be generated so the host software can re-write memory addresses containing error bits.

The 2-bit ECC will immediately trigger an interrupt to the host, typically causes a kernel panic and subsequently causes a device reset.

4.4 Processor SDK Software Support

Both Linux and RTOS branch of the Processor SDK support initialization, verification and error handling of the ECC. Table II lists sub-modules in each branch related to ECC functions.

ECC and RMW are enabled by default in both Processor SDK Linux and Processor SDK TI-RTOS to match to K2G GP EVM hardware. But can be disabled if not required by customer systems.

Table 2 lists software support for DDR ECC.

Table 2. Software Support for DDR ECC

OPERATIONS	DESCRIPTION	PROCSDK-RTOS	PROCSDK-Linux
Enablement / Initialization	Enable data macros, leveling and training	GEL file scripts	u-boot
Memory Initialization	Initialize memory for correct syndrome	Yes	u-boot
Kernel Handling – Scrubbing	Frequently scrub memory to correct single-bit errors in memory device	No (user software)	No (user software)
Kernel Handling – Unrecoverable	Cause kernel panic if double-bit error is encountered	Not supported (user software)	Kernel Panic
Verification / Diagnostics	Utility or example to verify ECC support	Example code (user software)	Linux Utility (user software)

5 Test Data

For DDR access 8-byte aligned addresses, the ECC is transparently read and verified by the hardware controller. Therefore no impact on latency or memory throughput is expected. Table 3 lists measured block data transfers from the C66x L2 memory to the DDR space, with- and without- ECC enabled in the controller.

Table 3. Throughput Comparison of DDR ECC With and Without ECC Enabled

TEST	SOURCE	DESTINATION	ACNT	BCNT	BIT LENGTH	THROUGHPUT
1	DSP L2	DDR3L	16384	1	131072	98.27%
2	DSP L2	DDR3L	32768	1	262144	99.13%
3	DSP L2	DDR3L	1	32768	262144	99.19%
5	DSP L2	DDR3L	2	32768	524288	99.59%
6	DSP L2	DDR3L	4	32768	1048576	99.65%
7	DSP L2	DDR3L	8	32768	131072	98.27%

In cases where non-aligned write access made to the DDR, the RMW procedure will be performed, where the DDREMIF controller first read the aligned data from the DDR, merge with requested write bytes, re-calculate ECC error correction code, then write to the DDR memory. Latency due to RMW operation is dependent on the background simultaneous access to the DDR, and the DDR command and data FIFO fill levels.

6 Design Files

The design files for the K2G General Purpose EVM may be found at <http://www.ti.com/tool/evmk2gx>.

7 Related Documentation

1. *Keystone II Architecture DDR3 Memory Controller User's Guide* ([SPRUHN7](#))
2. *Hardware Design Guide for KeyStone II Devices* ([SPRABV0](#))
3. *DDR3 Design Requirements for KeyStone Devices* ([SPRABI1](#))
4. *Advantages of ECC Memory*, <https://www.pugetsystems.com/labs/articles/Advantages-of-ECC-Memory-520/>
5. *66AK2Gx Multicore DSP + ARM KeyStone II System-on-Chip (SoC) Technical Reference Manual* ([SPRUHY8](#))

7.1 Trademarks

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8 About the Author

DR. JIAN WANG is a Chip Architect with the Catalog Processor Group. Dr. Wang joined TI in 2006 as a Video Systems Engineer, working on Davinci family of digital media processors. His recent roles focus on SOC system architecture for machine vision and next-generation industrial applications.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to B Revision	Page
• Changed document title to "66AK2Gx"	1
• Added 66AK2G12 Product Folder	1
• Changed EVM Tool Folder to EVMK2G (1GHz version).....	1
• Changed "at 600 MHz" to "up to 1000 MHz" for both Cortex-A15 and C66x	2
• Added MSMC subsystem details.....	2
• Changed datasheet URL to 66AK2G12 version (SPRSP07).....	9

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