TI Designs
CISPR 25 Tested Automotive Tail Light Reference Design for Step-Up and Linear LED Driver-Based Systems

Design Overview

This TI Design details a solution for an automotive LED tail-light application (tail light, stop light, turn signal, and reverse light). This design uses the TPS92630-Q1 linear LED driver powered by an upstream-boost converter (TPS40210-Q1) that is directly supplied through a smart reverse-battery diode off of the automotive-battery voltage. The design guide includes EMI and EMC radiation and pulse tests conducted using CISPR 25 and ISO 7637-2 standards, and highlights potential cost savings and efficiency (power dissipation and system thermals). For a similar design with the TPS92630-Q1 driven by a buck converter, see TIDA-00677. For a similar design with the TPS92630-Q1 driven directly from a car battery, see TIDA-00679.

Design Resources

TIDA-00678	Design Folder
TPS92630-Q1	Product Folder
TPS40210-Q1	Product Folder
LM74610-Q1	Product Folder
TLC555-Q1	Product Folder

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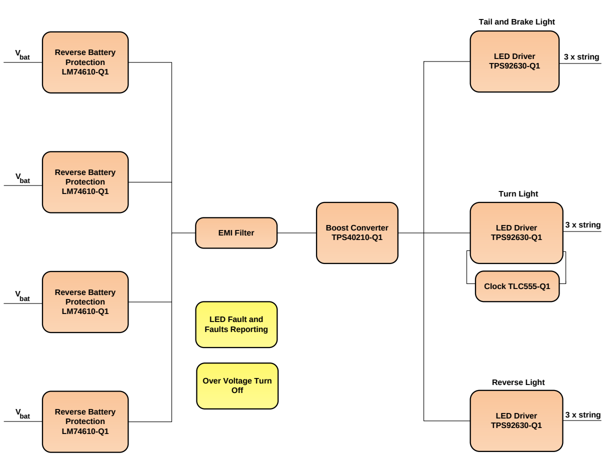
Design Features

- Efficiency-Optimized Design
- CISPR 25 Tested EMI and EMC
- Stays Out of AM Band
- Load-Dump Tolerant
- Operation Through Cold Crank
- Smart Reverse-Battery Protection

Featured Applications

- Automotive Tail Light
- Automotive Front Lighting
- Automotive Interior Lighting



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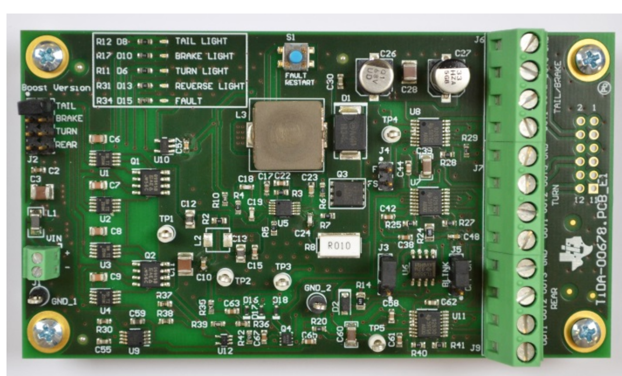

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1 LED Module System Specifications

Table 1 shows the LED system specifications.

Table 1. LED Module System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
System input and output						
V_{IN}	Operating-input voltage	Battery-voltage range. Outputs are functional (DC)	5	13.5	16	V
V_{IN_MAX}	Maximum-input voltage	Maximum-battery voltage on the module without device damage (for example: load dump)			45	V
V_{OUT_MAX}	Output voltage	Maximum output voltage at V_{IN}		16.76		V
V_{TR}	Transient immunity	Load dump (ISO 7637-2)			45	V
V_{IN_MIN}	Minimum input voltage	Cold crank (ISO 7637-2)	5			V
V_{REV}	Reverse voltage	Reverse-polarity protection	–42			V
I_{IN_MAX}	Maximum-input current	All outputs at full load (150mA)		6		A
$I_{OUT\ MaxS}$	Maximum-output current	Maximum current per string			150	mA
V_{OUT_OFF}	Output off	Turn output off at input over voltage		17		V
$LED_{Open\ and\ short\ detect}$		LED open and short detection		Yes		
$LED_{Single\ short\ detect}$		LED single-short detection		No		
Onboard voltages						
V_{Boost_Out}	Output-voltage boost converter	TP3, U5, TPS40210-Q1		17		V
V_{TP1}	Voltage at reverse-battery protection output	TP1, LM74610-Q1		V_{IN}		V
V_{TP2}	Voltage π- filter output	TP2		V_{IN}		V
V_{LDO}	Output-linear regulator	U9, TPS7A1633, comparator and clock supply		3.3		V
f_{OSCB}	Oscillator frequency	Boost converter, U5, TPS40210-Q1		470		kHz
$f_{OSCTurn}$	Oscillator frequency	U6, TLC555-Q1, clock generator		0.5		Hz
Thermal						
TA	Temperature range	Operating-ambient temperature	–40		105	ºC
Pulse tolerance						
Load dump		Thermal shutdown				
Cold crank		Operational				
Jump start		Thermal shutdown				
EMI tolerance						
Meets or exceeds the CISPR 25 class 3 and 5 requirements						
Baseboard						
Number of layers		Two layers, double-side populated				
Form factor		112 mm × 62 mm				

2 System Description

The CISPR 25 system was designed as a complete solution for a TPS92630-Q1 automotive-linear LED driver tail-light application, including key peripherals like voltage conditioning (preboost) and reverse-battery protection. Consider the following points:

- The design is compliant with the CISPR 25 radiated- and conducted-emissions automotive EMI standards.
- Satisfy power requirements for three TPS92630-Q1 devices, each driving three strings of LEDs for tail, brake, turn, and reverse lights.
- Operate over the full range of battery conditions.
  – $V_{IN\ (min)}$ down to 5 V simulating a cold-crank condition (ISO 7637-2:2004 pulse 4)
  – $V_{IN\ (max)}$ up to 16 V simulating the upper range of normal-battery operation
- Survive and continue (or switch off, depending on configuration) operation through:
  – Load dump (ISO 7637-2:2004 pulses 5a)
  – Double-battery condition
- Implement a reverse-battery protection scheme with minimal loss for the system.
  – The system must properly respond to a reverse-battery polarity event and shut down appropriately.
- Protect the output against shorts to the battery and GND voltage.
- Optimize the individual blocks for the lowest power dissipation and the highest efficiency.
- Lay out the board to minimize the footprint of the solution while maintaining high performance.
- Provide a flexible-board interface to mate to a custom board through screw terminals or receptacles (J8).
- Provide power for the TLC555-Q1.
- The system must maintain a constant output voltage over the full DC range of battery conditions specified in OEM or ISO 16750-2 standards.

Many tail-light applications in vehicles may or may not need to maintain operation during cold crank and load dump, have high efficiency, and be CISPR 25 EMI and EMC compliant. Figure 1 is an example block diagram of the tail-light system.

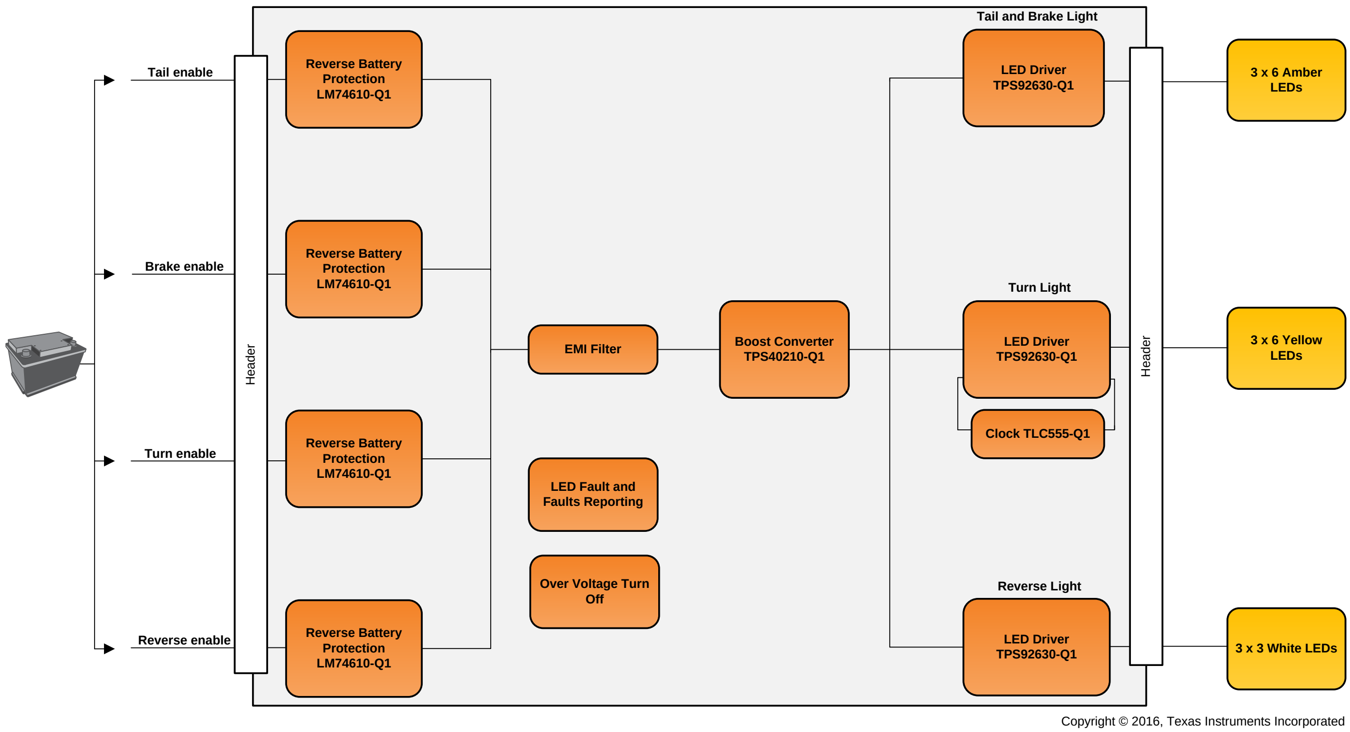


Figure 1. Tail-Light System Driven Off of a Battery

The orange blocks are components found on the TIDA-00678 board. The blocks cover most monitoring and power requirements of Figure 1.

Figure 1 also features reverse-battery protection, EMC filtering, voltage conditioning, and a linear LED driver. Because length of strings vary from application to application, LEDs are not included.

3 Block Diagram

Figure 2 shows the LED block diagram.

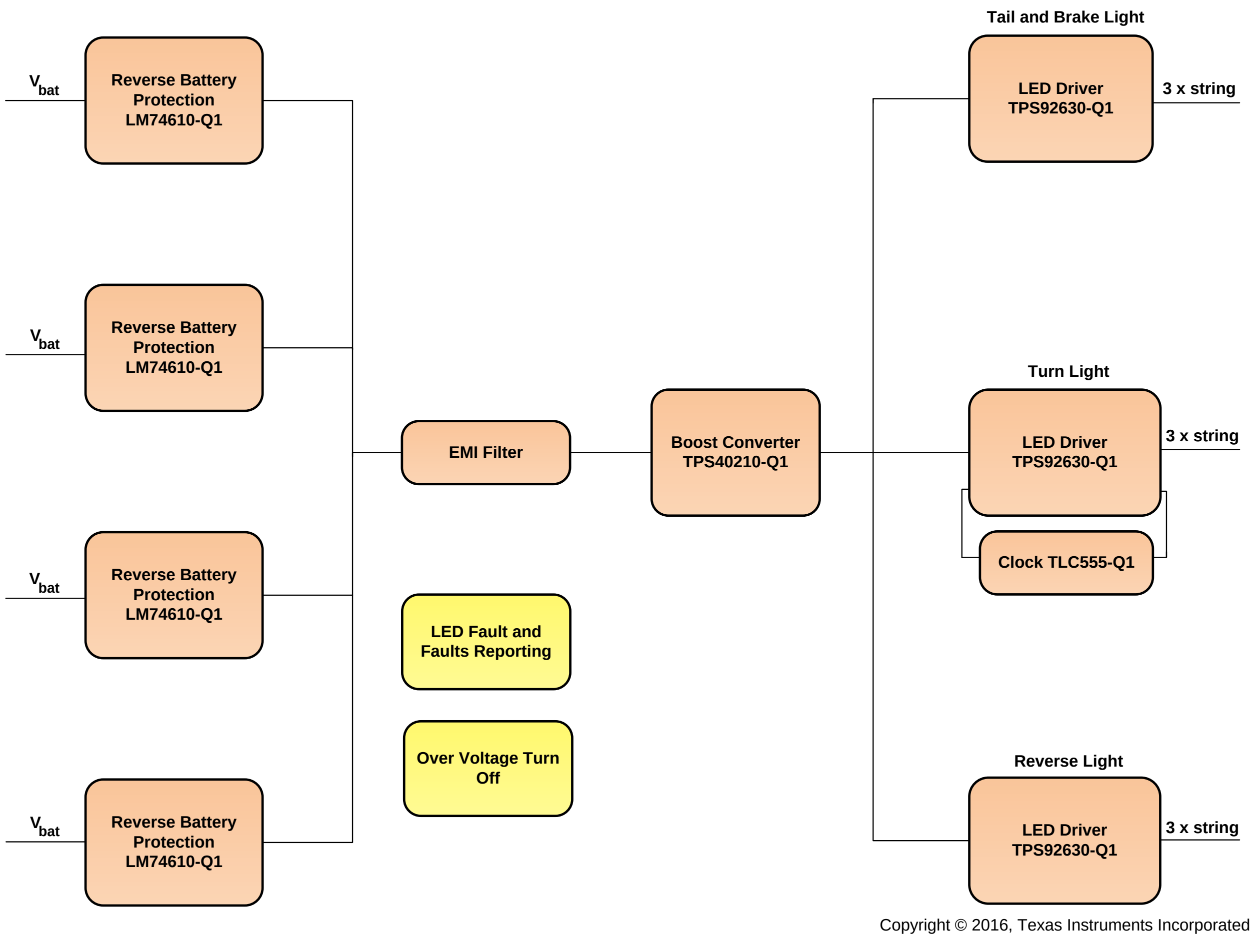


Figure 2. Step-Up and Linear LED Driver Block Diagram

3.1 Highlighted Products

This design uses the TI products in Section 3.1.1, Section 3.1.2, Section 3.1.3, Section 3.1.4, and Section 3.1.5. For more information on each of these devices, see the product folders at www.ti.com.

3.1.1 TPS92630-Q1

The TPS92630-Q1 device is a linear LED driver that has three channels, analog, and PWM dimming controls. Because the TPS92630-Q1 has full-diagnostic and built-in protection capabilities, it is the ideal device for lighting applications with variable-intensity LEDs up to a medium-power range. Figure 3 is a block diagram of the TPS92630-Q1.

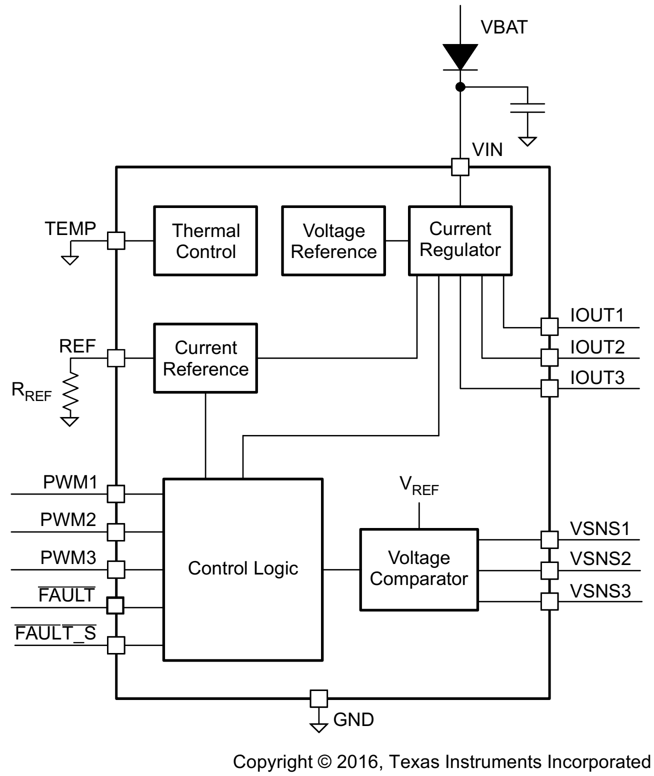


Figure 3. TPS92630-Q1 Linear LED Block Diagram

- The TPS92630-Q1 has a 450-mA maximum-output current (150 mA per channel). This design uses a maximum of 100 mA per channel (for IOUT1, IOUT2, IOUT3). If the brake light is turned on, the IOU1 channel delivers 150 mA.
- The PWM1, PWM2, PWM3 inputs for the tail, brake, turn, and reverse lights are tied together and connected to the VIN pin to make the device operate at 100% duty cycle.
- The PWM inputs are tied together for the turn indicator and can be connected through jumper J5 to the LDO output to enable 100% duty cycle, or to the TLC555-Q1 clock device to enable blinking operation.
- The REF pin is tied through a 1.21-kΩ resistor to GND to set a 100-mA output current per LED string. If the brake light is turned on, a 2.43-kΩ resistor is paralleled to move the current to 150 mA.
- The $\overline{\text{FAULT}}$ pin is used to report general faults as open, short, and thermal shutdown.
- The $\overline{\text{FAULT\_S}}$ pin is not used.
- The TEMP pin is not used and is tied to GND.
- VSNS1, VSNS2, VSNS3 are not used due to long strings.
- Wide-input voltage range (5 V to 16 V and 45-V transients) is required to operate directly off of the battery to withstand load dump and operate through cold-crank and start-stop conditions.

3.1.2 TPS40210-Q1

The TPS40210-Q1 and TPS40211-Q1 devices are boost controllers that use a wide-input voltage (4.5 V to 52 V) and are nonsynchronous. The boost controllers are suitable for topologies that require a grounded source N-channel field-effect transistor (FET) including boost, flyback, SEPIC, and various LED-driver applications. The device features include programmable-soft start, overcurrent protection with automatic retry, and a programmable-oscillator frequency. Current-mode control provides improved-transient response and simplified-loop compensation. Figure 4 shows the wide-input boost controller.

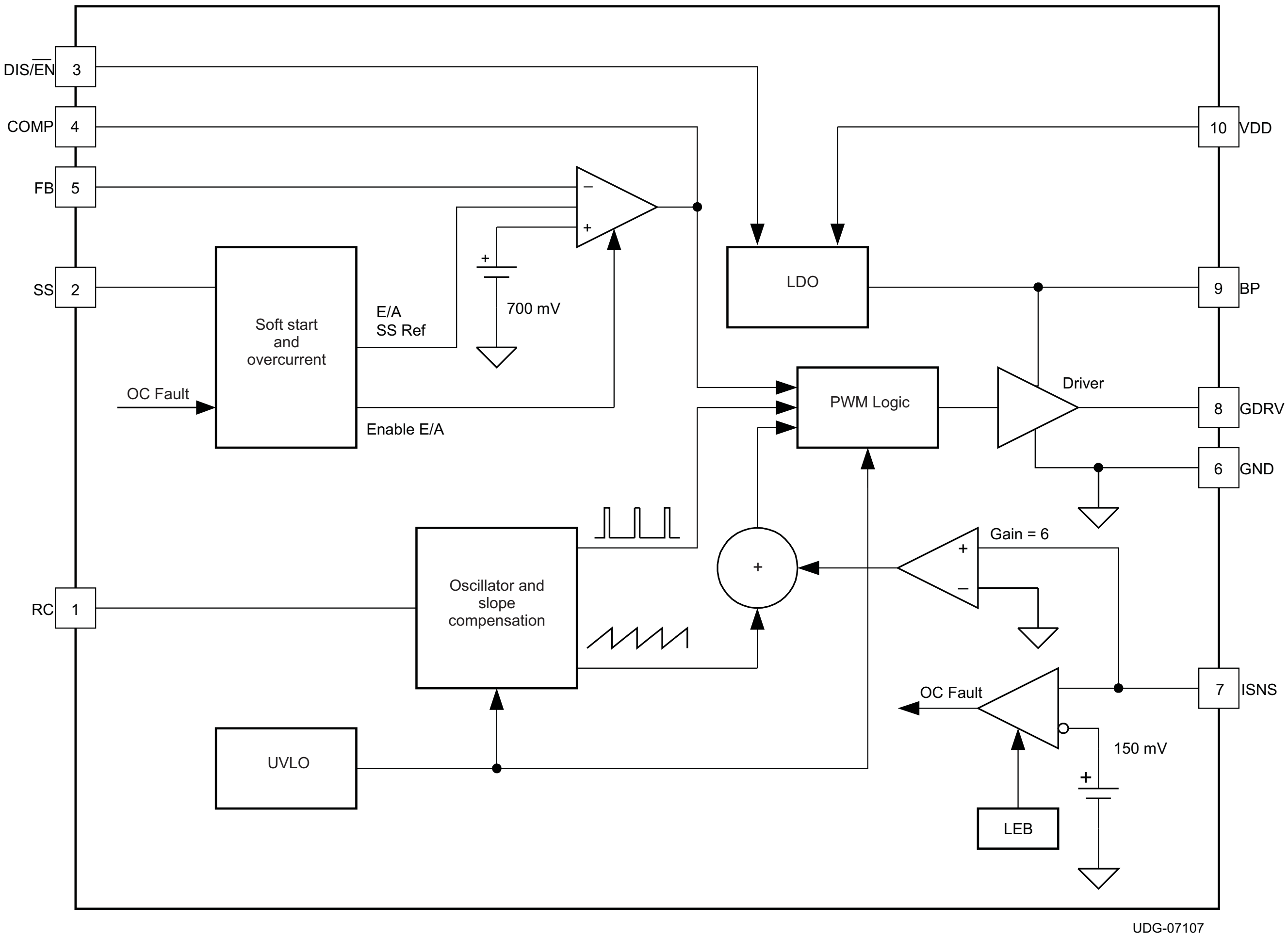


Figure 4. 4.5- to 52-V Input, Current-Mode Boost Controller

- A wide input-voltage range is required to operate directly off of the battery to withstand load dump and operate through cold-crank and start-stop conditions.
- The TPS40210-Q1 switches nominally at 470 kHz (RC pin configuration) below the AM-radio band. Automotive designs require DC-DC converters to switch outside of the AM-radio band.
- The TPS40210-Q1 is dimensioned to deliver 2 A of output current. The design uses a maximum of approximately 1.05 A to provide headroom.
- A 2.2-nF soft-start capacitor is added for the initial start-up time and recovery from a short circuit.
- The DIS/$\overline{\text{EN}}$ pin is connected through a momentary switch to V_{IN} to reset the circuit.
- A resistor (R6) is added for the GDRV gate-driver output to shape the switching waveform for EMC reasons.
- ISNS is through a 1-kΩ, 100-pF snubber network connected to a 0.1-Ω, 1% current-sense resistor for EMC reasons.

- To make the device work at lower input voltages (for example: 3 V), V_{DD} can be supplied through a diode from the output (split-rail supply, not shown in Figure 4).
- Small 5.05 mm × 3.1 mm MSOP power packages, inductors, FETs, sense resistors, diodes, and input and output capacitors are required components.
- A high level of integration (MSOP package) is crucial in applications that are space constrained.

3.1.3 LM74610-Q1

The LM74610-Q1 is a controller device that can be used with an N-Channel MOSFET in protection circuitry with reverse polarity (see Figure 5). The LM74610-Q1 is designed to drive an external MOSFET to emulate an ideal-diode rectifier when connected in series with a power source. A unique advantage of this scheme is that it is not referenced to the ground and has zero quiescent current (I_Q).

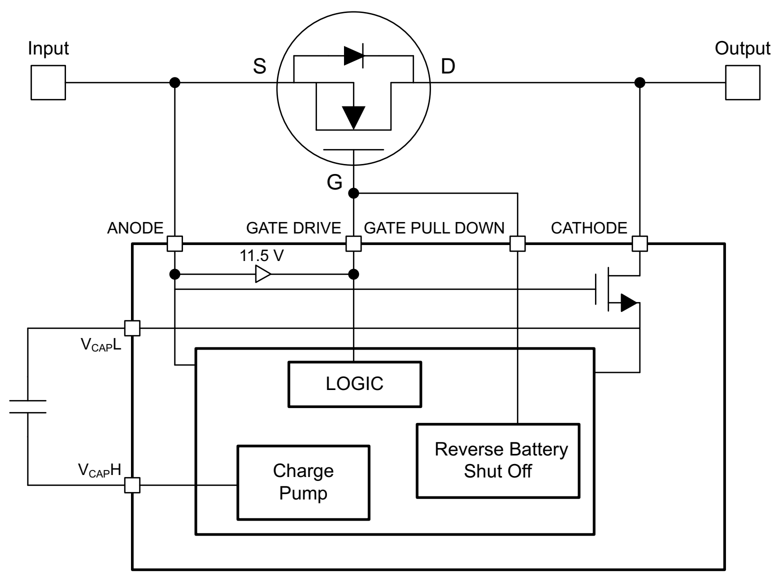


Figure 5. LM74610-Q1 Zero I_Q Reverse-Polarity Protection Smart-Diode Controller

The LM74610-Q1:

- Controls an external NFET in series with the battery-supply input to act as an ideal diode, reducing voltage drop and power loss as opposed to a discrete-diode solution
- Quickly turns off the FET when a reverse-battery condition is detected, isolating and protecting downstream circuitry
- Satisfies the requirement for reverse-battery protection down to –42 V
- Has no ground reference, leading to almost a zero I_Q operation. This helps the subsystem draw less standby current from the battery.

The small voltage drop across the FET provides more input-voltage headroom for the wide-V_{IN} boost converter and reduced power dissipation.

3.1.4 TLC555-Q1

The TLC555-Q1 is a monolithic timing circuit fabricated using the TI LinCMOS™ process. The timer, shown in Figure 6, is fully compatible with CMOS, TTL, and MOS logic and operates at frequencies of up to 2 MHz. This device uses smaller timing capacitors than the NE555 because it has high-input impedance; more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage.

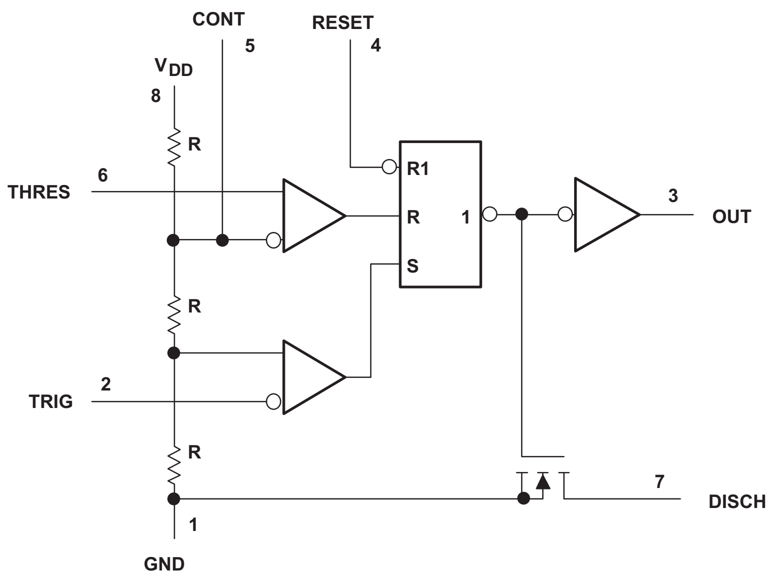


Figure 6. LinCMOS™ Timer

The TLC555-Q1:

- Generates a 0.5-Hz clock signal for the turn-indicator LED string
- Has an operating voltage range of 2 V to 15 V
- Is supplied by the 3.3-V LDO to generate a 3.3-V square-wave output.
- Is attached to the PWM input pins of the U7 turn-indicator (TPS92630-Q1)
- Has low power consumption
- Has low supply currents that reduce spikes during output transitions

The TLC555-Q1 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by using the control-voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level it sets the flip-flop and the output goes high. Having TRIG above the trigger level and the threshold input (THRES) above the threshold level resets the flip-flop, and the output is low. The reset input (RESET) can override all other inputs, and a possible use is to initiate a new timing cycle. RESET going low resets the flip-flop, and the output is low. When the output is low, a low-impedance path exists between the discharge terminal (DISCH) and GND.

3.1.5 TPS7A1633-Q1

Figure 7 shows the TPS711633-Q1 LDO voltage regulator.

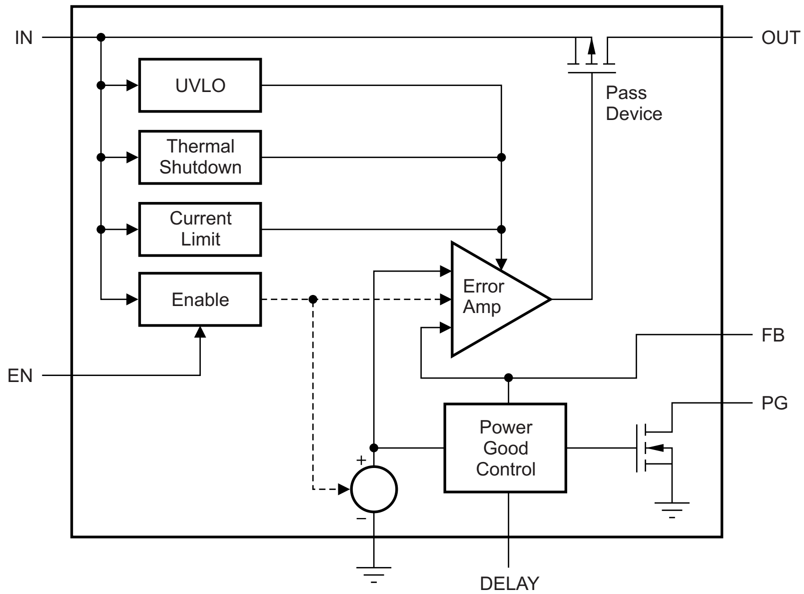


Figure 7. Low-Dropout Voltage Regulator

- The TPS7A1633-Q1 is a wide-V_{IN} linear regulator used to produce a supply voltage of 3.3 V for the overvoltage-turnoff comparator, clock generator, and the fault LED.
- This device is operable because of the low drop-out capability in cold-crank conditions (5 V).
- A 22-µF capacitor is added to the output for stability.
- EN (enable) is tied through a 10-kΩ resistor to IN.
- PG (power good) is not used in this design.

4 Automotive EMC and EMI Standards

This TI Design is compliant with EMC and EMI standards that are important to automotive customers. There are many important standards and tests, but the focus is on the standards and tests that are most applicable to off-battery power supplies: ISO 7637-2, ISO 16750-2, and CISPR25. Auto manufacturers have internal standards for EMC, but these are often based on international ISO and IEC standards. Usually, only a few parameters of different tests or limits are changed, but the essence of the requirements are the same.

4.1 ISO 7637-2

ISO 7637 is titled “*Road vehicles – Electrical disturbances from conduction and coupling*,” and part two is “*Electrical transient conduction along supply lines only*.” Because the design is a subsystem where power comes directly from the supply lines (car battery), ISO 7637 part two is relevant. The standard defines a test procedure, including the description of test pulses, to test the susceptibility of an electrical subsystem to transients that could be harmful to its operation. More details about the pulses used in this design are provided in the following sections.

4.1.1 ISO 7637-2 Pulse 5a (Load Dump)

This section is based on the standard, “This test is a simulation of load dump transient, occurring in the event of a discharged battery being disconnected while the alternator is generating charging current and with other loads remaining on the alternator circuit at this moment … Load dump may occur on account of a battery being disconnected as a result of cable corrosion, poor connection or of intentional disconnection with the engine running.” This pulse was moved from ISO 7637 to ISO 16750 (detailed in Section 4.2), but for historical reasons it is still grouped with the ISO 7637-2 pulses (see Figure 8).

NOTE: The control unit must be able to withstand the high energy and high voltage of the load-dump event.

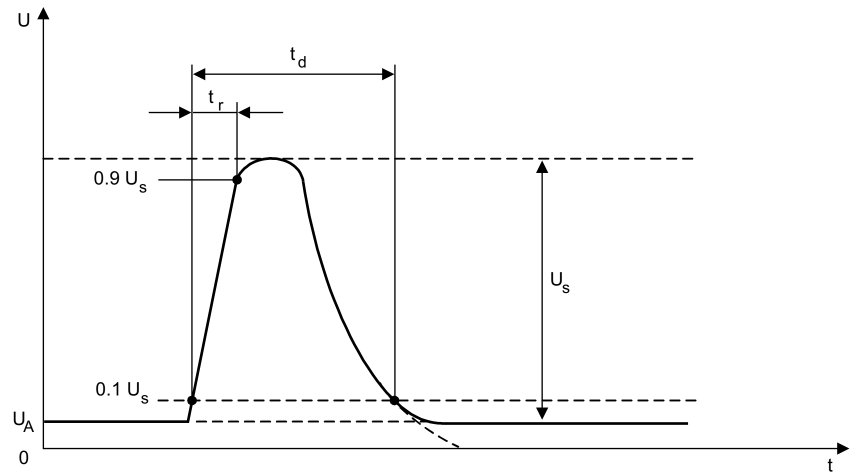


Figure 8. Load-Dump Pulse

4.1.2 Related Standards

As detailed in Section 4, OEMs (and other standards organizations) maintain versions of these pulses in their standards. Usually, the pulses have different parameters depending on the OEM, but they can be the same.

4.2 ISO 16750-2

ISO 16750 is titled "*Road vehicles – Environmental conditions and testing for electrical and electronic equipment*," and part 2 is "*Electrical loads*." One way to think of this standard is that it defines a series of supply-voltage quality events—variations of the battery-supply voltage under various conditions. These conditions, for the most part, are not harmful to the electrical subsystem, but can affect the state of operation. The tests in this standard are designed to see how the subsystem behaves before, during, and after these events. The required behavior can be classified into multiple functional classes.

- **Functional Class A**
  - All functions of the device or the system perform as designed during and after the test.
- **Functional Class B**
  - All functions of the device or the system perform as designed during the test. However, one or more functions may go beyond the specified tolerance. All functions automatically return within normal limits after the test. Memory functions shall remain Class A.
- **Functional Class C**
  - One or more functions of the device or the system do not perform as designed during the test, but automatically return to normal operation after the test.
- **Functional Class D**
  - One or more functions of the device or the system do not perform as designed during the test and do not return to normal operation after the test until the device or the system is reset by a "operator or use" action.
- **Functional Class E**
  - One or more functions of the device or the system do not perform as designed during and after the test and cannot be returned to proper operation without repairing or replacing the device or the system.

The standards define different tests, but only a small subset of the tests apply to this design. Only the cold-crank, reverse-battery, jump-start, and load-dump results are shown in this document.

4.2.1 ISO 16750-2: 4.3.1.2 Jump Start

Figure 9 shows the supply that went through the subsystem during the jump start, where two 12-V batteries are connected to the supply lines in a series. This is an overvoltage condition that is sustained for a period of time.

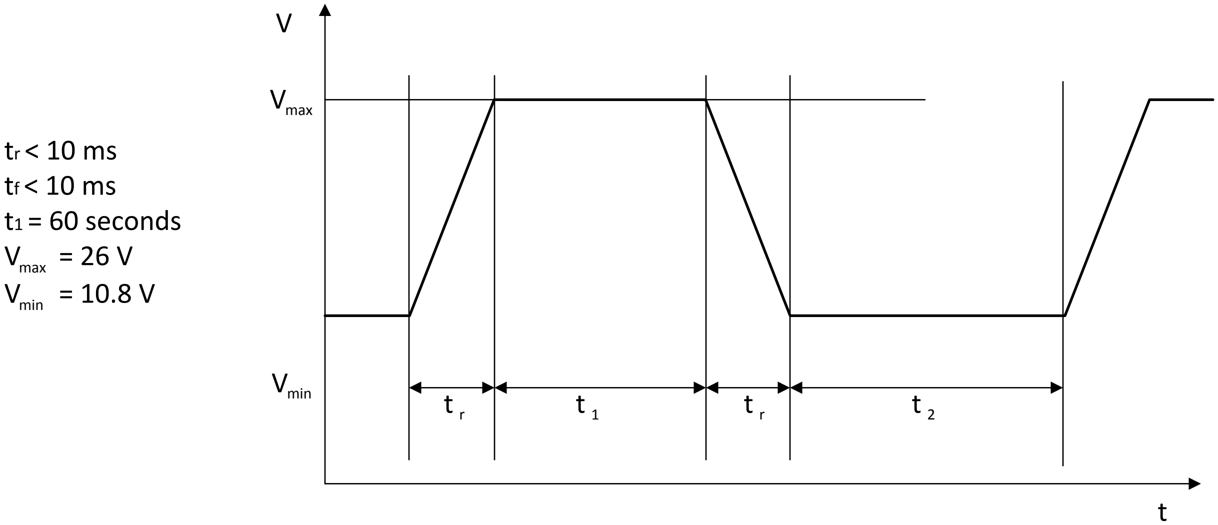


Figure 9. Jump-Start Profile

Functional Class C is the requirement for this test.

4.2.2 ISO 16750-2: 4.7 Reversed Voltage

This section is based on the standard, “This test checks the ability of a DUT to withstand against the connection of a reversed battery in case of using an auxiliary starting device.” Figure 10 shows the reverse-battery pulse referenced in this section.

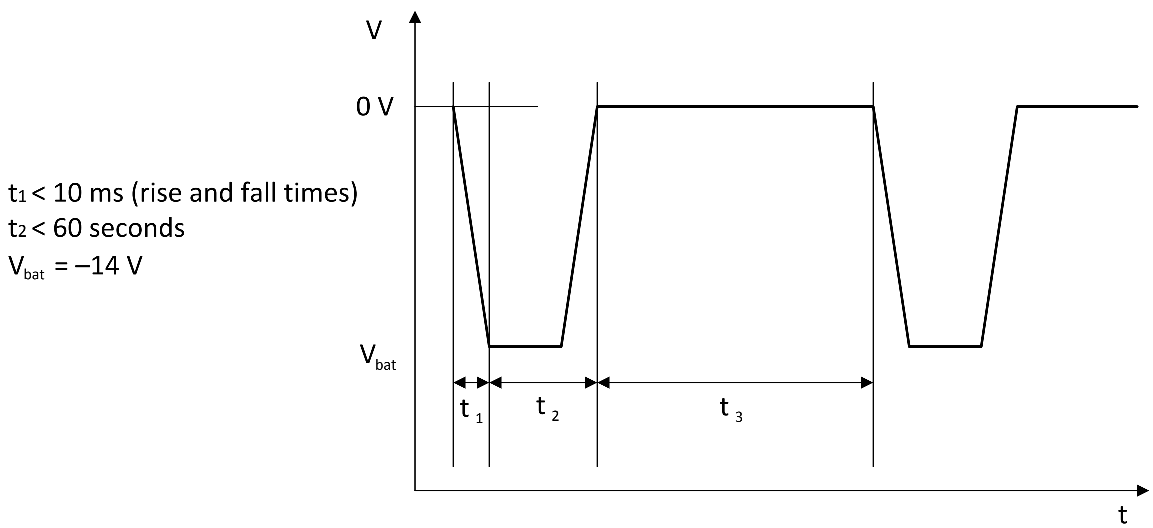


Figure 10. Reverse-Battery Pulse

The subsystem does not need to operate during this event, but upon removing the reverse-polarity and re-establishing the normal supply voltage (12 V), the subsystem can satisfy Functional Class A.

4.2.3 Cranking Profiles

Cranking tests simulate the drop in supply voltage when the engine is started due to the large current draw of the starter motor. The voltage levels are dependent on the temperature of the car during start-up, with severe cold leading to the largest drop in voltage (*cold crank*). Though the profile looks similar for all OEMs, the voltage levels can vary from standard to standard. Figure 11 shows an example of a cold start, and Table 2 shows the parameters for a cold start.

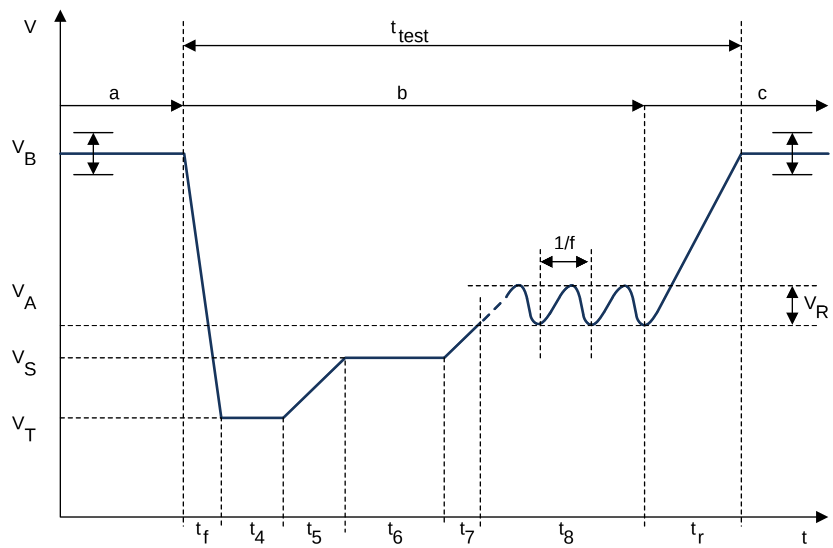


Figure 11. Example of Cold Start

Table 2. Example Parameters for Cold Start

PARAMETER	NORMAL TEST PULSE	SEVERE TEST PULSE
V_B	11.0 V	11.0 V
V_T	4.5 V (0%, –4%)	3.2 V $^{+0.2\ V}$
V_S	4.5 V (0%, –4%)	5.0 V (0%, –4%)
V_A	6.5 V (0%, –4%)	6.0 V (0%, –4%)
V_R	2 V	2 V
t_f	≤ 1 ms	≤ 1 ms
t_4	0 ms	19 ms
t_5	0 ms	≤ 1 ms
t_6	19 ms	329 ms
t_7	50 ms	50 ms
t_8	10 s	10 s
t_r	100 ms	100 ms
f	2 Hz	2 Hz

4.3 CISPR 25

CISPR 25 is the automotive EMI standard that most OEMs reference for requirements. The title of the standard is, "*Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers*." The purpose of the standard is to limit the amount of emissions from a subsystem in several frequency bands to ensure it does not interfere with other systems that intentionally operate in those bands.

For example, an AM radio receiver is tuned to a specific frequency (for example 710 kHz), picking up the signal of a radio station on that frequency. The radio receives and amplifies the signals intended for AM radio broadcast on that frequency. However, if another system on the car is unintentionally emitting large quantities of energy (noise) at that frequency, it impedes the ability of the radio to cleanly resolve the signal of the radio station, and the user may hear noise in the signal, or obscure the intentional signal altogether. Standards like CISPR 25 are specifically designed to avoid this by setting acceptable limits on these systems. OEMs will define limits, but CISPR 25 contains examples.

The testing and limits are split into two separate types of emissions: conducted and radiated. Conducted emissions are coupled onto supply lines directly through conductors (such as traces or wires), and radiated emissions are emitted as EM waves and can be picked up by intentional and unintentional antennas on other systems.

The test procedures, relevant-frequency bands, and limits are different for both types of emissions, but the basics are similar: the device under test (DUT) is placed in an isolated room or chamber and set up in a well-defined, reproducible-electrical setup. All other possible emitters are removed from the chamber and the DUT is turned on and then allowed to operate normally. The DUT is powered through an artificial network (LISN) and loaded through its normal operation. A spectrum analyzer is used to measure the DUT emissions across different frequencies (through the LISN or from an antenna) and compares the emissions against the CISPR 25 limits. Both the peak and average values of the emissions are measured, and both must pass. Finally, the level of passing falls into several categories, or classes, that have different limits. OEMs define which class a specific subsystem must satisfy.

4.3.1 Conducted Emissions

The test setup is outlined in the official CISPR 25 documentation (see the figured titled *Conductied emissions – Test layout for ignition system components* in [9]).

See the official documentation for further information about the test setup. Conducted-emissions testing is done only in the lower-frequency bands for the standard. The limits are defined in the CISPR 25 documentation shown in Table 3 and Table 4.

Table 3. Peak and Quasi Peak Limits

SERVICE OR BRAND	FREQUENCY (MHz)	LEVELS IN dV (µV)									
		CLASS 1		CLASS 2		CLASS 3		CLASS 4		Class 5	
		PEAK	QUASI PEAK	PEAK	QUASI PEAK	PEAK	QUASI PEAK	PEAK	QUASI PEAK	PEAK	QUASI PEAK
Broadcast											
LW	0.15 to 0.30	110	97	100	87	90	77	80	67	70	57
MW	0.53 to 1.8	86	73	78	65	70	57	62	49	54	41
SW	5.9 to 6.2	77	64	71	58	65	52	59	46	53	40
FM	76 to 108	62	49	56	43	50	37	44	31	38	25
TV Band 1	41 to 88	58		52		46		40		34	
TV Band 3	174 to 230	Conducted emission. Voltage method is not applicable.									
DAB 3	171 to 245										
TV Band 4 and 5	468 to 944										
DTTV	470 to 770										
DAB L Band	1447 to 1494										
SDARS	2320 to 2345										
Mobile services											
CB	26 to 28	68	55	62	49	56	43	50	37	44	31
VHF	30 to 54	68	56	62	49	56	43	50	37	44	31
VHF	68 to 87	62	49	56	43	50	37	44	31	38	25

Table 4. Average Limits

SERVICE OR BAND	FREQUENCY (MHz)	LEVELS IN dV (µV)				
		CLASS 1	CLASS 2	CLASS 3	CLASS 4	CLASS 5
		AVERAGE	AVERAGE	AVERAGE	AVERAGE	AVERAGE
Broadcast						
LW	0.15 to 0.30	90	80	70	60	50
MW	0.53 to 1.8	66	58	50	42	34
SW	5.9 to 6.2	57	51	45	39	33
FM	76 to 108	42	36	30	24	18
TV Band 1	41 to 88	48	42	36	30	24
TV Band 3	174 to 230	Conducted emission. Voltage method is not applicable.				
DAB 3	171 to 245					
TV Band 4 and 5	468 to 944					
DTTV	470 to 770					
DAB L Band	1447 to 1494					
SDARS	2320 to 2345					
Mobile services						
CB	26 to 28	48	42	36	30	24
VHF	30 to 54	48	42	36	30	24
VHF	68 to 87	42	36	30	24	18

The DC-DC regulator in the system is the main source of conducted emissions. The switching action of the input-current waveform emits energy back onto the supply lines, and this must be filtered. The supply lines emit at their fundamental-switching frequency and harmonics.

4.3.2 Radiated Emissions

The test setup is outlined in the official CISPR 25 documentation. Three different antennas are used to measure over the full frequency range of the testing, and three different test setups are required (see the figure titled *Example of test set-up – rod antenna* in [9]).

See the official documentation for more information about the other test setups. The limits are defined in the CISPR 25 documentation, and cover a wider band than the conducted emissions test. Table 5 and Table 6 show the peak, quasi-peak, and average limits for radiated emissions testing.

Table 5. Peak and Quasi-Peak Limits for Radiated Emissions Testing

SERVICE OR BAND	FREQUENCY (MHz)	LEVELS IN dV (μV per m)									
		CLASS 1		CLASS 2		CLASS 3		CLASS 4		CLASS 5	
		PEAK	QUASI PEAK	PEAK	QUASI PEAK	PEAK	QUASI PEAK	PEAK	QUASI PEAK	PEAK	QUASI PEAK
Broadcast											
LW	0.15 to 0.30	86	73	76	63	66	53	56	43	46	33
MW	0.53 to 1.8	72	59	64	51	56	43	48	35	40	27
SW	5.9 to 6.2	64	51	58	45	52	39	46	33	40	27
FM	76 to 108	62	49	56	43	50	37	44	31	38	25
TV Band 1	41 to 88	52		46		40		34		28	
TV Band 3	174 to 230	56		50		44		38		32	
DAB 3	171 to 245	50		44		38		32		26	
TV Band 4 and 5	468 to 944	65		59		53		47		41	
DTTV	470 to 770	69		63		57		51		45	
DAB L Band	1447 to 1494	52		46		40		34		28	
SDARS	2320 to 2345	58		52		46		40		34	
Mobile services											
CB	26 to 28	64	51	58	45	52	39	46	33	40	27
VHF	30 to 54	64	51	58	45	52	39	46	33	40	27
VHF	68 to 87	59	46	53	40	47	34	41	28	35	22
VHF	142 to 175	59	46	53	40	47	34	41	28	35	22
Analog UHF	380 to 512	62	49	56	43	50	37	44	31	38	25
RKE	300 to 330	56		50		44		38		32	
RKE	420 to 450	56		50		44		38		32	
Analog UHF	820 to 960	68	55	62	49	56	43	50	37	44	31
GSM 800	860 to 895	68		62		56		50		44	
EGSM and GSM 900	925 to 960	68		62		56		50		44	
GPS L1 civil	1567 to 1583										
GSM 1800 (PCN)	1803 to 1882	68		62		56		50		44	
GSM 1900	1850 to 1990	68		62		56		50		44	
3G and IMT 2000	1900 to 1992	68		62		56		50		44	
3G and IMT 2000	2010 to 2025	68		62		56		50		44	
3G and IMT 2000	2108 to 2172	68		62		56		50		44	
Bluetooth and 802.11	2400 to 2500	68		62		56		50		44	

Table 6. Average Limits for Radiated Emissions Testing

SERVICE OR BAND	FREQUENCY (MHz)	LEVELS IN dV (μV per m)				
		CLASS 1	CLASS 2	CLASS 3	CLASS 4	CLASS 5
		AVERAGE	AVERAGE	AVERAGE	AVERAGE	AVERAGE
Broadcast						
LW	0.15 to 0.30	66	56	46	36	26
MW	0.53 to 1.8	52	44	36	28	20
SW	5.9 to 6.2	44	38	32	26	20
FM	76 to 108	42	36	30	24	18
TV Band 1	41 to 88	42	36	30	24	18
TV Band 3	174 to 230	46	40	34	28	22
DAB 3	171 to 245	40	34	28	22	16
TV Band 4 and 5	468 to 944	55	49	43	37	31
DTTV	470 to 770	59	53	47	41	35
DAB L Band	1447 to 1494	42	36	30	24	18
SDARS	2320 to 2345	48	42	36	30	24
Mobile services						
CB	26 to 28	44	38	32	26	20
VHF	30 to 54	44	38	32	26	20
VHF	68 to 87	39	33	27	21	15
VHF	142 to 175	39	33	27	21	15
Analog UHF	380 to 512	42	36	30	24	18
RKE	300 to 330	42	36	30	24	18
RKE	420 to 450	42	36	30	24	18
Analog UHF	820 to 960	48	42	36	30	24
GSM 800	860 to 895	48	42	36	30	24
EGSM and GSM 900	925 to 960	48	42	36	30	24
GPS L1 civil	1567 to 1583	34	28	22	16	10
GSM 1800 (PCN)	1803 to 1882	48	42	36	30	24
GSM 1900	1850 to 1990	48	42	36	30	24
3G and IMT 2000	1900 to 1992	48	42	36	30	24
3G and IMT 2000	2010 to 2025	48	42	36	30	24
3G and IMT 2000	2108 to 2172	48	42	36	30	24
Bluetooth and 802.11	2400 to 2500	48	42	36	30	24

5 System Design Theory

5.1 PCB and Form Factor

This design is not intended to fit any particular form factor. The only goal of the design with regards to the PCB is to make a solution that is compact, while still providing a way to test the performance of the board. Figure 12 is a 3D rendering of the board.

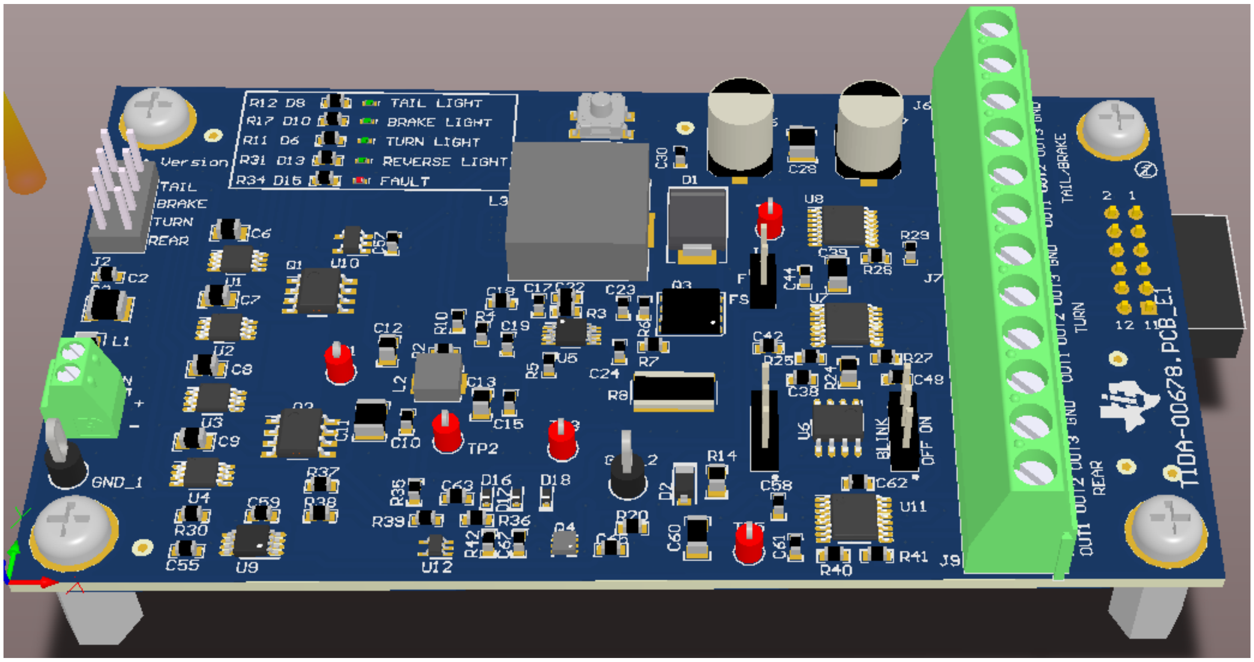


Figure 12. 3D Render of the TIDA-00678 Board

In a final-production version of this design, several techniques may reduce the size of the solution.

- Test points, headers, sockets, standoffs, and banana plugs can be removed.
- The overvoltage-turnoff block can be removed if this function is not required in an application. These blocks can be removed because they do not service a direct function for the board.
- The number, size, and value of capacitors in the system can be optimized.
- Four times a reverse-battery ORing controller might not be needed in the application.

5.2 Input Protection and Wide-V_{IN} DC-DC

5.2.1 Reverse-Battery Protection

Reverse-battery protection is required in nearly every electronic subsystem of a vehicle following OEM and ISO 16750-2 standards. The goal is to prevent reverse-biasing components that are sensitive to polarity, such as polarized capacitors and integrated circuits. Figure 13 shows reverse-battery protection with the LM74610-Q1.

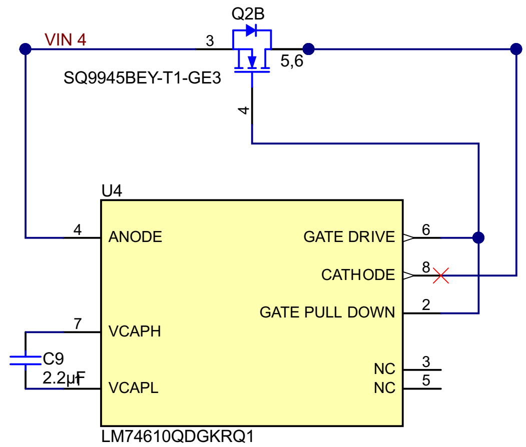


Figure 13. Reverse-Battery Protection Using the LM74610-Q1

Instead of using a traditional-diode rectifier for reverse-battery protection, Figure 13 uses an N-channel MOSFET driven by the LM74610-Q1 smart-diode controller. The power dissipation of the traditional-diode solution can be significant because of the 600- to 700-mV forward drop (P = I × V). Using an N-channel MOSFET results in loss because of the $R_{DS(ON)}$ of the FET, but results in greater efficiency and requires less thermal dissipation.

The LM74610-Q1 team provides recommendations and a tool that can be used to help select a FET for the application. Important considerations follow:

- Ensure that the continuous-current rating is sufficient for the application.
- The V_{GS} threshold should be 2.5-V maximum.
- The V_{DS} should be at least 0.48 V at 6 A and 125°C (in off-state of the FET).

For this design, the FET must be rated at least as high as the clamped-input voltage. A 45-V FET is acceptable, but a 60-V FET allows for additional headroom.

The hiccup behavior of the LM74610-Q1 causes the voltage to drop by approximately 0.5 V every few seconds. Picking a 2.2-µF capacitor for C9 allows for an approximate FET turnon time of 2 s.

5.2.2 Input Capacitors Exposed to Battery Inputs

A final consideration for the front-end protection is the input capacitor. Because of the flexion of the PCB, it is possible for a ceramic capacitor to mechanically fail short. If this happens to an input capacitor that is connected directly to the battery, a hard short may occur at the battery terminals. To avoid a ceramic capacitor failing short, two ceramic capacitors are used in series – if one fails, there is another to avoid a short. Align the capacitors at 90° with respect to each other on the layout to provide a chance that a flexion in one direction may only affect the capacitor aligned in that direction. Because of EMI suppression on this board, additional footprints for capacitors (C1, C2, C3, C4, C5) and a ferrite bead (L1) were added, which can be optionally placed. If the capacitors and a ferrite bead are used in the real application, arrange the capacitors as described in the previous sentence.

5.3 Wide-V_{IN} Boost Converter

The TPS40210-Q1 is an AECQ100 qualified, wide-V_{IN} current-mode boost regulator used as a front-end supply to provide a 17-V system voltage (see Figure 14). With an input voltage range of 4.5 V to 52 V, the device can continue to operate through most battery conditions (start-stop, cold crank, and load dump).

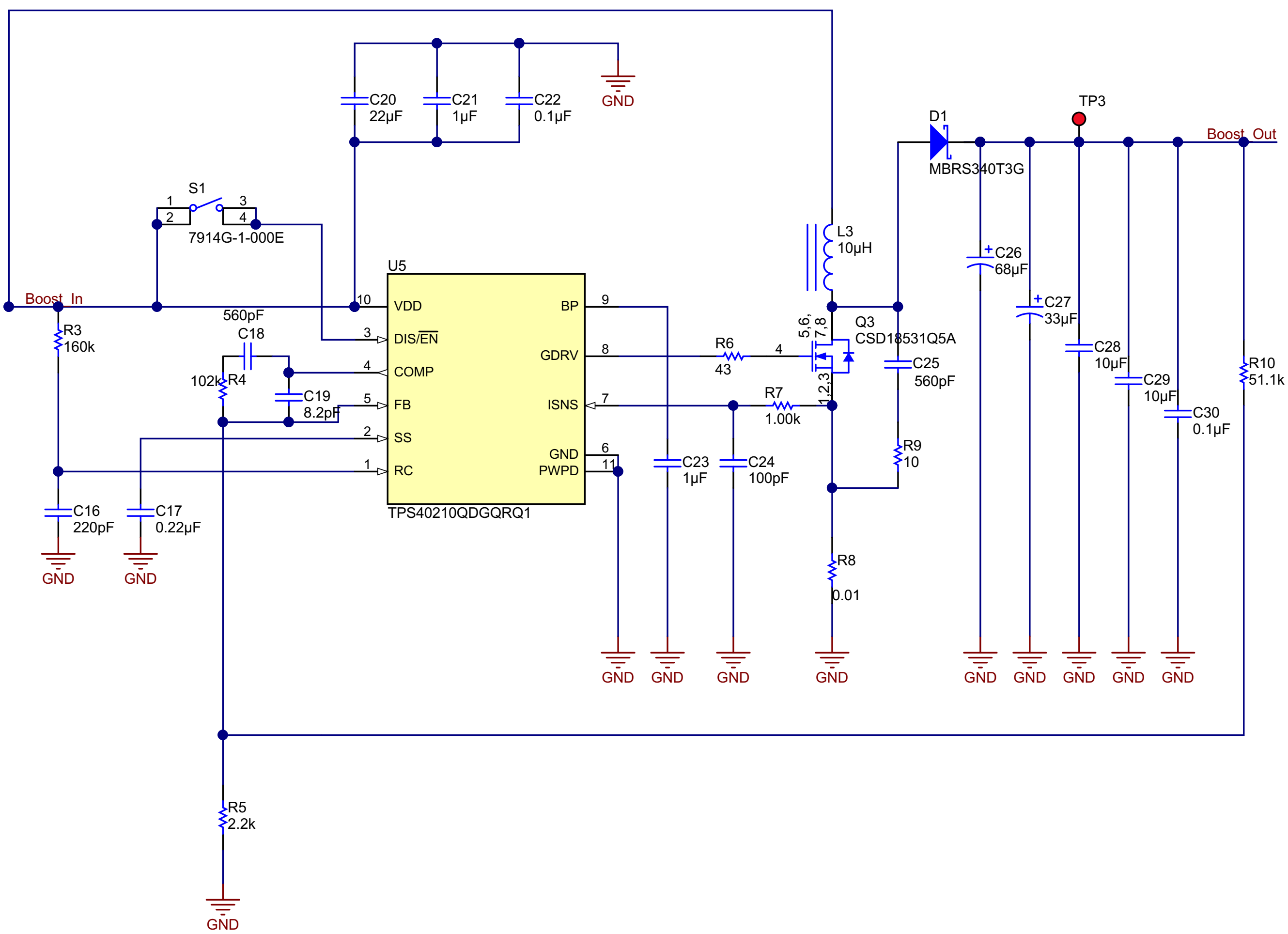


Figure 14. TPS40210-Q1 4.5-V to 52-V Input, Current-Mode Boost Controller

A boost converter is sometimes included in an off-battery power supply to extend the operating range of the subsystem to low values (5 V). This allows the subsystem to continue operation through conditions such as a cold crank.

The boost only operates in the input voltage range from 5 V to 17.5 V and helps sustain a high-output voltage for the LED driver to maintain regulation of the system voltage. When the system voltage is adequately high (greater than 17.5 V), the boost acts in bypass mode, allowing the input voltage to the system to pass directly through to the linear-LED drivers.

Consider whether to choose a synchronous or asynchronous solution when choosing a boost converter. A synchronous solution is more efficient, especially during normal operation when the boost is in bypass mode. During bypass mode, the boost is essentially idle, but the high-side rectifier is still in the main-conduction path. A diode rectifier drops to within the range of 0.5 V to 0.7 V, leading to significant power loss (and voltage headroom loss). A FET only has a loss proportional to its $R_{DS(ON)}$, which is smaller. An asynchronous boost has a simpler control circuitry, and is typically significantly cheaper to design.

5.3.1 Duty Cycle Estimation

Using Equation 1 and Equation 2 to estimate a forward drop of 0.5 V for a Schottky diode, the approximate duty cycle is 8.6% (minimum) to 77.1% (maximum).

$$D_{MIN} \approx \frac{V_{OUT} - V_{IN\_MAX} + V_{FD}}{V_{OUT} + V_{FD}} = \frac{17\text{ V} - 16\text{ V} + 0.5\text{ V}}{17\text{ V} + 0.5\text{ V}} = 8.6\ \% \tag{1}$$

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN\_MAX} + V_{FD}}{V_{OUT} + V_{FD}} = \frac{17\text{ V} - 4\text{ V} + 0.5\text{ V}}{17\text{ V} + 0.5\text{ V}} = 77.1\ \% \tag{2}$$

5.3.2 Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. TI recommends a 1.5-A maximum-output current (see Equation 3).

$$I_{LRIP\_MAX} = \frac{0.3 \times I_{OUT\_MAX}}{1 - D_{MIN}} = \frac{0.3 \times 1.5\text{ A}}{1 - 0.086} = 0.492\text{ A} \tag{3}$$

The minimum inductor size can be estimated using Equation 4 (TI recommends a 17-V maximum-input voltage because the device stops switching above that voltage).

$$L_{MIN} >> \frac{V_{IN\_MAX}}{I_{LRIP\_MAX}} \times D_{MIN} \times \left(\frac{1}{f_{SW}}\right) = \frac{17\text{ V}}{0.492\text{ A}} \times 0.086 \times \frac{1}{470\text{ kHz}} = 6.3\ \mu\text{H} \tag{4}$$

Select the next higher standard inductor value of 10 µH.

5.3.3 Inductor Currents

The ripple current is estimated by using Equation 5 and Equation 6:

$$I_{RIPPLE} \approx \frac{V_{IN}}{L} \times D \times \frac{1}{f_{SW}} = \frac{8.5\text{ V}}{10\ \mu\text{H}} \times 0.5 \times \frac{1}{470\text{ kHz}} = 0.90\text{ A} \tag{5}$$

$$I_{RIPPLE(V_{IN\_MIN})} \approx \frac{V_{IN}}{L} \times D \times \frac{1}{f_{SW}} = \frac{5\text{ V}}{10\ \mu\text{H}} \times 0.771 \times \frac{1}{470\text{ kHz}} = 0.82\text{ A} \tag{6}$$

The worst-case peak-to-peak ripple current occurs at 50% duty cycle and is 0.90 A.

The worst-case RMS current through the inductor is approximated by using Equation 7:

$$I_{L_{RMS}} = \sqrt{\left(I_{L\_AVG}\right)^2 + \left(\frac{1}{12} I_{RIPPLE}\right)^2} \approx \sqrt{\left(\frac{I_{OUT\_MAX}}{1 - D_{MAX}}\right)^2 + \left(\frac{1}{12} I_{RIPPLE(V_{IN\_MIN})}\right)^2} = \sqrt{\left(\frac{1.5\text{ A}}{1 - 0.77}\right)^2 + \left(\frac{1}{12} \times 0.82\text{ A}\right)^2} = 6.52\text{ A}_{RMS} \tag{7}$$

The peak inductor current is estimated by using Equation 8:

$$I_{L\_PEAK} \approx \frac{I_{OUT\_MAX}}{1 - D_{MAX}} + 0.5 \times I_{RIPPLE(V_{IN\_MIN})} = \frac{1.5\text{ A}}{1 - 0.77} + 0.5 \times 0.82 = 6.93\text{ A} \tag{8}$$

A 10-µH inductor with a minimum RMS current rating of 6.52 A and a minimum-saturation current rating of 6.93 A must be selected. Select a BOURNS SRP1250-100M 10-A, 0.0255-mΩ, 10-µH inductor.

5.3.4 Inductor Power Dissipation

The inductor power dissipation is estimated by using Equation 9:

$$P_L \approx \left(I_{L_{RMS}}\right)^2 \times DCR = (6.52\text{ A})^2 \times 0.0255\ \Omega = 1.08\text{ W} \tag{9}$$

5.3.5 Rectifier Diode Selection

A Schottky diode with a low-forward voltage drop is used as a rectifier diode to reduce its power dissipation and improve efficiency. Using 80% derating on V_{OUT} for ringing on the switch node, the rectifier diode minimum reverse break-down voltage is given by using Equation 10:

$$V_{(BR)R\_MIN} \geq \frac{V_{OUT}}{0.8} = \frac{17}{0.8} = 21.25\ V \tag{10}$$

The diode must have a reverse-breakdown voltage greater than 30 V.

The rectifier diode peak and average currents are estimated by using Equation 11 and Equation 12:

$$I_{D\_AVG} \approx I_{OUT\_MAX} = 1.5\ A \tag{11}$$

$$I_{D\_PEAK} \approx I_{L\_PEAK} = 6.93\ A \tag{12}$$

The power dissipation in the diode is estimated by using Equation 13:

$$P_{D\_MAX} \approx V_F \times I_{OUT\_MAX} = 0.5\ V \times 1.5\ A = 0.75\ W \tag{13}$$

The maximum power dissipation is estimated as 0.75 W. Review 30-V and 40-V Schottky diodes and select the MBRS340T3G 40-V 3-A diode in an SMC package. This diode has a forward voltage drop of 0.5 V at 3 A. The conduction power dissipation is approximately 750 mW.

5.3.6 Output Capacitor Selection

Output capacitors must be selected to meet the required-output ripple and transient specifications, calculated using Equation 14 and Equation 15.

$$C_{OUT} = \left(8 \times I_{OUT} \times \frac{D}{V_{OUT\_RIPPLE}}\right) \times \frac{1}{f_{SW}} = 8 \times 1.5\ A \times \frac{0.771}{200\ mV} \times \frac{1}{470\ kHz} = 98\ \mu F \tag{14}$$

$$ESR = \frac{7}{8} \times \frac{V_{OUT\_RIPPLE}}{I_{L\_PEAK} - I_{OUT}} = \frac{7}{8} \times \frac{200\ mV}{6.93\ A - 1.5\ A} = 32\ m\Omega \tag{15}$$

A Nichicon-UUD1V680MCL1GS 35-V, 68-uF, 340-mΩ bulk capacitor and two Murrata-GRM32ER71H106KA12L 10-µF ceramic capacitors are selected to provide the required capacitance and ESR at the switching frequency. The combined capacitances of 120 µF and 60 mΩ are used in compensation calculations.

5.3.7 Input Capacitor Selection

Because a boost converter has continuous-input current, the input capacitor only senses the inductor ripple current. The input capacitor value can be calculated by using Equation 16 and Equation 17:

$$C_{IN} > \frac{I_{RIPPLE}}{4 \times V_{IN\_RIPPLE} \times f_{SW}} = \frac{0.9\ A}{4 \times 20\ mV \times 470\ kHz} = 23.9\ \mu F \tag{16}$$

$$ESR > \frac{V_{IN\_RIPPLE}}{2 \times I_{RIPPLE}} = \frac{20\ mV}{2 \times 0.9\ A} = 11\ m\Omega \tag{17}$$

To meet a maximum-input ripple of 20 mV, a minimum 23.9-µF input capacitor with ESR less than 11 mΩ is needed. Select a 22-µF X7R in parallel with a 1-µF and a 100-nF ceramic capacitor to account for the EMC and EMI.

5.3.8 Current Sense and Current Limit

The maximum-current sense resistor value is limited by both the current limit and subharmonic stability. These two limitations are given by using Equation 18 and Equation 19:

$$R_{ISNS} < \frac{V_{OCP\_MIN}}{1.1 \times \left(I_{L\_PEAK} + I_{DRIVE}\right)} = \frac{100\ \text{mV}}{1.1 \times (6.93\ \text{A} + 0.5\ \text{A})} 12.3\ \text{m}\Omega \tag{18}$$

$$R_{ISNS} < \frac{VDD_{MAX} \times L \times f_{SW}}{60 \times \left(V_{OUT} + V_{fd} - V_{IN}\right)} = \frac{16\ \text{V} \times 10\ \mu\text{H} \times 470\ \text{kHz}}{60 \times (17\ \text{V} + 0.48\ \text{V} - 16\ \text{V})} = 847\ \text{m}\Omega \tag{19}$$

The current limit requires a resistor less than 12.3 mΩ, and stability requires a sense resistor less than 847 mΩ. Select a 10-mΩ resistor. Approximately 2 mΩ of routing resistance is added in compensation calculations.

5.3.9 Current-Sense Filter

To remove switching noise from the current sense, place an R-C filter between the current-sense resistor and the ISNS pin. A resistor with a value between 1 kΩ and 5 kΩ is selected, and a capacitor value is calculated by using Equation 20:

$$C_{IFLT} = \frac{0.1 \times D_{MIN}}{f_{SW} \times R_{IFLT}} = \frac{0.1 \times 0.086}{(470\ \text{kHz} \times 1\ \text{k}\Omega)} = 18.3\ \text{pF} \tag{20}$$

Select a 100-pF capacitor for a 1-kΩ filter resistor after 18.3 pF is calculated.

5.3.10 Switching MOSFET Selection

The TPS40210-Q1 device drives a ground referenced N-channel FET. The R_{DS_ON} and gate charge are estimated based on the desired efficiency target. For a target of 95% efficiency with a 17-V output voltage at 1.5 A, maximum power dissipation is limited to 1.34 W (see Equation 21).

$$P_{DISS(total)} \approx P_{OUT} \times \left(\left(\frac{1}{n}\right) - 1\right) = V_{OUT} \times I_{OUT} \times \left(\left(\frac{1}{n}\right) - 1\right) = 17\ \text{V} \times 1.5\ \text{A} \times \left(\left(\frac{1}{0.95}\right) - 1\right) = 1.34\ \text{W} \tag{21}$$

The main power-dissipating devices are the MOSFET, inductor, diode, current sense resistor, and the integrated circuit (TPS40210-Q1 device). See Equation 22.

$$P_{FET} < P_{DISS(total)} - P_L - P_D - P_{R_{ISNS}} - V_{IN\_MAX} - I_{VDD} \tag{22}$$

Assume a constant-input voltage for the MOSFET-power calculation of 13.5 V and an input current of 2.37 A. This leaves approximately 500 mW of power dissipation for the MOSFET. Allowing half for conduction and half for switching losses, users can determine a target R_{DS_ON} and Q_{GS} for the MOSFET by using Equation 23:

$$Q_{GS} < \frac{3 \times P_{FET} \times I_{DRIVE}}{2 \times V_{OUT} \times I_{OUT} \times f_{SW}} = \frac{3 \times 0.5\ \text{W} \times 0.5\ \text{A}}{2 \times 17\ \text{V} \times 1.5\ \text{A} \times 470\ \text{kHz}} 31\ \text{nC} \tag{23}$$

A target MOSFET gate-to-source charge of less than 31 nC is calculated to limit the switching losses to less than 250 mW. Calculate a target MOSFET R_{DS_ON} of 7.6 mΩ using Equation 24 to limit the conduction losses to less than 250 mW.

$$R_{DS\_ON} < \frac{P_{FET}}{2 \times I_{RMS}^2 \times D} = \frac{0.5\ \text{W}}{2 \times 6.52^2 \times 0.77} = 7.6\ \text{m}\Omega \tag{24}$$

Reviewing 40-V and 60-V MOSFETs, a CSD18531Q5A 4.4-mΩ MOSFET is selected. For EMI reasons, a 43-Ω resistor was placed in the gate path to shape turnon and turnoff edges.

5.3.11 Feedback-Divider Resistors

The primary-feedback divider resistor (R_{FB}) from V_{OUT} to V_{FB} should be selected between 10 kΩ and 100 kΩ to maintain a balance between power dissipation and noise sensitivity. Select R_{FB} = 51.1 kΩ for a 17-V output because a high-feedback resistance is desirable to limit power dissipation.

Select an R_{BIAS} of 2.2 kΩ (see Equation 25).

$$R_{BIAS} = \frac{V_{FB} \times R_{FB}}{V_{OUT} - V_{FB}} = \frac{0.7\ \text{V} \times 51.1\ \text{k}\Omega}{17\ \text{V} - 0.7\ \text{V}} = 2.19\ \text{k}\Omega \quad (25)$$

5.3.12 Error-Amplifier Compensation

Current-mode control typically requires a Type-II compensation, but it is desirable to layout for Type-III compensation to increase flexibility during design and development. Current-mode control-boost converters have a higher gain with a higher output impedance, so it is necessary to calculate the control-loop gain at the maximum-output impedance, estimated by using Equation 26:

$$R_{OUT(max)} = \frac{V_{OUT}}{I_{OUT(min)}} = \frac{17\ \text{V}}{0.165\ \text{A}} = 103\ \Omega \quad (26)$$

The transconductance of the TPS40210-Q1 current-mode control can be estimated by using Equation 27:

$$g_m = \frac{0.13 \times \sqrt{L \times \left(\frac{f_{SW}}{R_{OUT}}\right)}}{(R_{ISNS})^2 \times (120 \times R_{ISNS} + L \times f_{SW})} = \frac{0.13 \times \sqrt{10\ \mu\text{H} \times \left(\frac{470\ \text{kHz}}{R_{OUT}}\right)}}{(12\ \text{m}\Omega)^2 \times (120 \times 12\ \text{m}\Omega + 10\ \mu\text{H} \times 470\ \text{kHz})} = 31.41\ \text{s} \quad (27)$$

The maximum-output impedance Z_{OUT} can be estimated by using Equation 28 and Equation 29.

$$\left|Z_{OUT(f)}\right| = R_{OUT} \times \sqrt{\frac{1 + (2\pi \times f \times R_{ESR} \times C_{OUT})^2}{1 + \left((R_{OUT})^2 + 2 \times R_{OUT} \times R_{ESR} + (R_{ESR})^2\right) \times (2\pi \times f \times C)^2}} \quad (28)$$

$$\left|Z_{OUT(f)}\right| = R_{OUT} \times \sqrt{\frac{1 + (2\pi \times 47\ \text{kHz} \times 60\ \text{m}\Omega \times 120\ \mu\text{F})^2}{1 + \left((103\ \Omega)^2 + 2 \times 103\ \Omega \times 60\ \text{m}\Omega + (60\ \text{m}\Omega)^2\right) \times (2\pi \times 47\ \text{kHz} \times 120\ \mu\text{F})^2}} = 66.2\ \text{m}\Omega \quad (29)$$

The modulator gain at the desired crossover can be estimated by using Equation 30.

$$\left|K_{CO}\right| = g_m \times \left|Z_{OUT}(f_{CO})\right| = 31.41\ \text{S} \times 66\ \text{m}\Omega = 2.08 \quad (30)$$

The feedback compensation network must be designed to provide an inverse gain at the crossover frequency for unit-loop gain. This sets the compensation mid-band gain at a value that is calculated by using Equation 31:

$$K_{COMP} = \frac{1}{\left|K_{CO}\right|} = \frac{1}{2.08} = 0.48 \quad (31)$$

Use Equation 32 to set the mid-band gain of the error amplifier to K_{COMP}:

$$R4 = R7 \times K_{COMP} = \frac{R7}{\left|K_{CO}\right|} = \frac{51.1\ \text{k}\Omega}{0.0974} = 106.5\ \text{k}\Omega \quad (32)$$

Select a 102-kΩ resistor.

Place the zero at one 10th of the desired crossover frequency.

C18 = 331 pF is calculated using Equation 33. However, select C18 = 560 pF for this design.

$$C18 = \frac{10}{2\pi \times f_L \times R4} = \frac{10}{2\pi \times 47\ \text{kHz} \times 102\ \text{k}\Omega} = 331\ \text{pF} \quad (33)$$

Place a high-frequency pole at approximately five times the desired crossover frequency and less than one-half of the unity-gain bandwidth of the error amplifier. See Equation 34 and Equation 35.

$$C19 \approx \frac{1}{10\pi \times f_L \times R4} = \frac{1}{10\pi \times 47\text{ kHz} \times 102\text{ k}\Omega} = 6.7\text{ pF} \tag{34}$$

$$C19 > \frac{1}{\pi \times GBW \times R4} = \frac{1}{10\pi \times 1.5\text{ MHz} \times 102\text{ k}\Omega} = 0.2\text{ pF} \tag{35}$$

C19 = 8.2 pF is selected.

5.3.13 R-C Oscillator

The required resistor for a given oscillator frequency can be found by using Equation 36 or by viewing Figure 15.

$$R_T = \frac{1}{5.8 \times 10^{-8} \times f_{SW} \times C_T + 8 \times 10^{-10} \times f^2{}_{SW} + 1.4 \times 10^{-7} \times f_{SW} - 1.5 \times 10^{-4} + 1.7 \times 10^{-6} \times C_T - 4 \times 10^{-9} \times C_T} \tag{36}$$

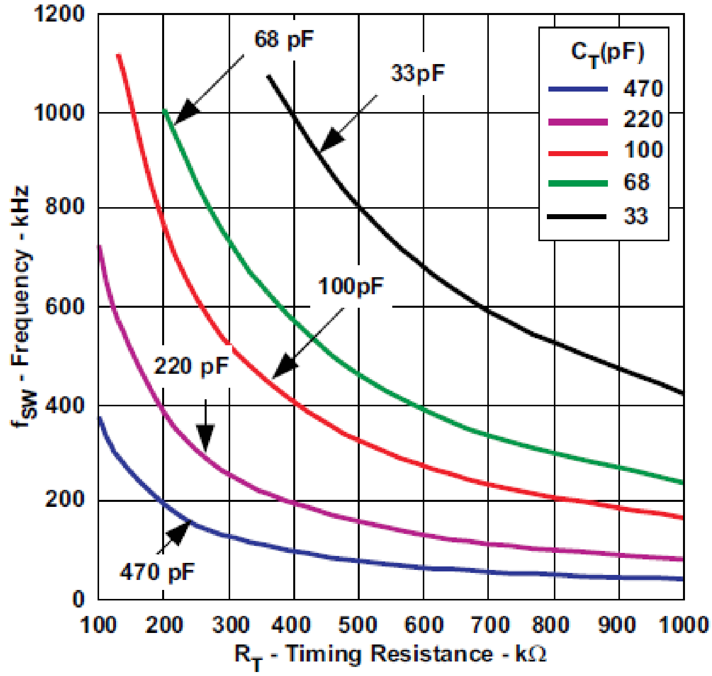


Figure 15. Switching Frequency versus Timing Resistance

Use a 220-pF capacitor (C16) and a 160-kΩ resistor (R3) for a switching frequency of 470 kHz.

5.3.14 Soft-Start Capacitor

Because V_{DD} is greater than 8 V, select the soft-start capacitor by using Equation 37:

$$C_{SS} = 20 \times T_{SS} \times 10^{-6} \tag{37}$$

For T_{SS} = 11 ms and C_{SS} = 220 nF, select a 220-nF capacitor for C17.

5.3.15 Regulator Bypass

As a regulator-bypass capacitor, a minimum of 1.0 μF is required. To improve EMI and EMC, C20 = 22 μF and C22 = 100 nF can be added.

5.3.16 General Power-Supply Design Considerations

Choose inductors for DC-DC converters so:

- The ripple current is between 20% and 40% of the load current I_{LOAD} (with the given F_{SW}, V_{IN}, and V_{OUT}).
- The temperature ratings are appropriate for an automotive application, typically 40°C to 105°C for lighting applications.

The saturation current is chosen using Equation 38 for peak current and additional margin:

$$I_{SAT} \geq \left(I_{LOAD} + \frac{1}{2} I_{RIPPLE} \right) \times 1.2 \quad (38)$$

Use X7R-dielectric material for lighting applications to ensure a minimum-capacitance variation over the full-temperature range. The voltage rating of the capacitors should be greater than the maximum-possible voltage, and two times the voltage to avoid DC-bias effects. The amount of output capacitance used depends on output ripple and transient-response requirements.

Use low-ESR ceramic capacitors and aluminum ELKOs to reduce ripple. See the device-specific data sheets for internally-compensated supplies because of the limitations on acceptable LC-output filter values. ICs should always be qualified according to AECQ100 standards. The part numbers of TI parts that are qualified typically end with “Q1”. FB-resistor dividers should have components with a 1% or higher tolerance for improved accuracy.

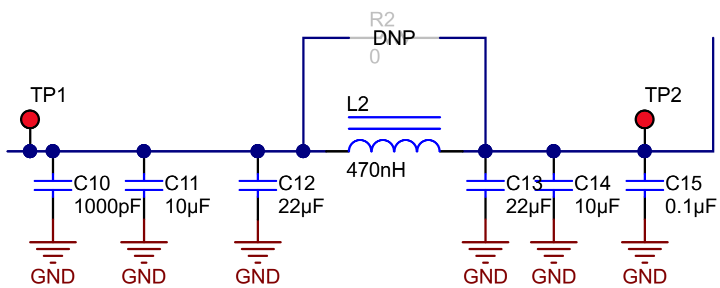


Figure 16. Input Voltage-Noise Filtering (R2 is Optional)

As detailed in Section 4.3.1, DC-DC converters can couple large amounts of energy (especially at the fundamental switching frequency) back through the battery inputs and into the remainder of the vehicle. This energy is produced because of the switching action of the input-current waveform that is translated into voltage noise by the ESR of the input capacitors that carry most of this current. A low-pass filter, placed between the input of the module and the DC-DC converters, can attenuate this noise. The low-pass filter also filters incoming noise that enters the system.

The low-pass filter can be designed empirically or theoretically (by calculation and simulation). The empirical approach is to design the system without the EMI filter, measure the conducted emissions with a spectrum analyzer, and compare it to the standard that must be passed. Next, calculate the attenuation needed to pass at certain frequencies and place the corner frequency of the filter low enough to achieve the desired attenuation.

NOTE: This method requires waiting on hardware to begin the design, gaining access to a testing lab, then modifying the hardware and retesting. Most designers will not have immediate access to a testing chamber, and want to pass the desired standard on the first try, or with minor adjustments.

The theoretical approach is more complicated. Ensure the assumption is that the boost converter is the problem, and that the noise generated by the downstream circuitry will be filtered by the boost inductor or capacitors.

NOTE: The main sources of noise are fundamental at the switching frequency of the boost (470 kHz) and the harmonics. If the amplitude of the noise at that frequency can be estimated and attenuated appropriately, the harmonics will be attenuated as well.

Figure 17 shows the input-current waveform.

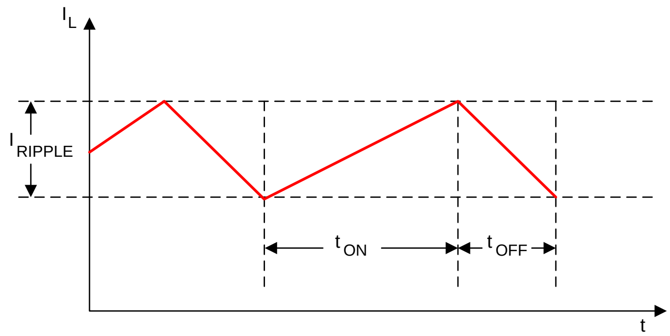


Figure 17. Input-Current Waveform

The input voltage is the voltage generated by the ripple current through the ESR of the input capacitors. Because ceramic capacitors are used, this ESR is very low (approximately 3 mΩ). The peak amplitude of the input voltage ripple is approximately 2.7 mV (see Equation 39). The concern is the frequency content at 470 kHz, not the time domain.

$$3\ \text{m}\Omega \times 0.9\ \text{A} = 2.7\ \text{mV} \quad (39)$$

Use the Fourier transform of this asymmetric-triangle waveform to find the coefficients and amplitudes of each component frequency.

The coefficient of the fundamental for this type of waveform is 0.8. Multiply the coefficient times the time-domain amplitude to find the energy at 470 kHz (see Equation 40).

$$0.8 \times 2.7\ \text{mV} = 2.16\ \text{mV} \quad (40)$$

Using Equation 41, convert the product of Equation 40 to dBµV to make analyzing it based on the CISPR 25 standards easier.

$$20 \times \log(2.16\ \text{mV} / 1\ \mu\text{V}) \approx 67\ \text{dB}\mu\text{V} \quad (41)$$

Compare the 67 dBµV to the CISPR 25 specification and calculate how much to attenuate. The CISPR 25 specification does not define a limit at 470 kHz, but the limit at 530 kHz for Class 5 conducted emissions is 54 dBµV (peak). An attenuation of at least 13 dB is required. Make the goal 40-dB attenuation at the switching frequency.

Calculate where to place the corner frequency of the filter when attenuation at 470 kHz is known. The ssecond-order low-pass filter has a rolloff of –40 dB per decade. Place the corner frequency at 47 kHz to attain 40 dB of attenuation at 470 kHz. The corner frequency is related to the values of the filter inductor and capacitor, calculated by using Equation 42.

$$2\pi \times f_C = \frac{1}{\sqrt{L \times C}} \quad (42)$$

Choose an L of 470 nH. There is approximately 25 µF, calculating out for C. This is not a standard value. To keep the ESR low, put two capacitors in parallel, and choose 22 µF for C12 and 10 µF for C11. Choosing a larger value lowers the corner frequency of the filter, providing more attenuation at 470 kHz. Also, ceramic capacitors suffer from DC bias effects and operate at a capacitance that is less than their rating. To filter the high-frequency noise content, 1-nF and 100-nF capacitors are added.

5.4 Three-Channel Linear LED Driver

5.4.1 Tail Light and Brake Light

Figure 18 shows the schematic for the tail light and the brake light, and shows the 2-level brightness adjustment.

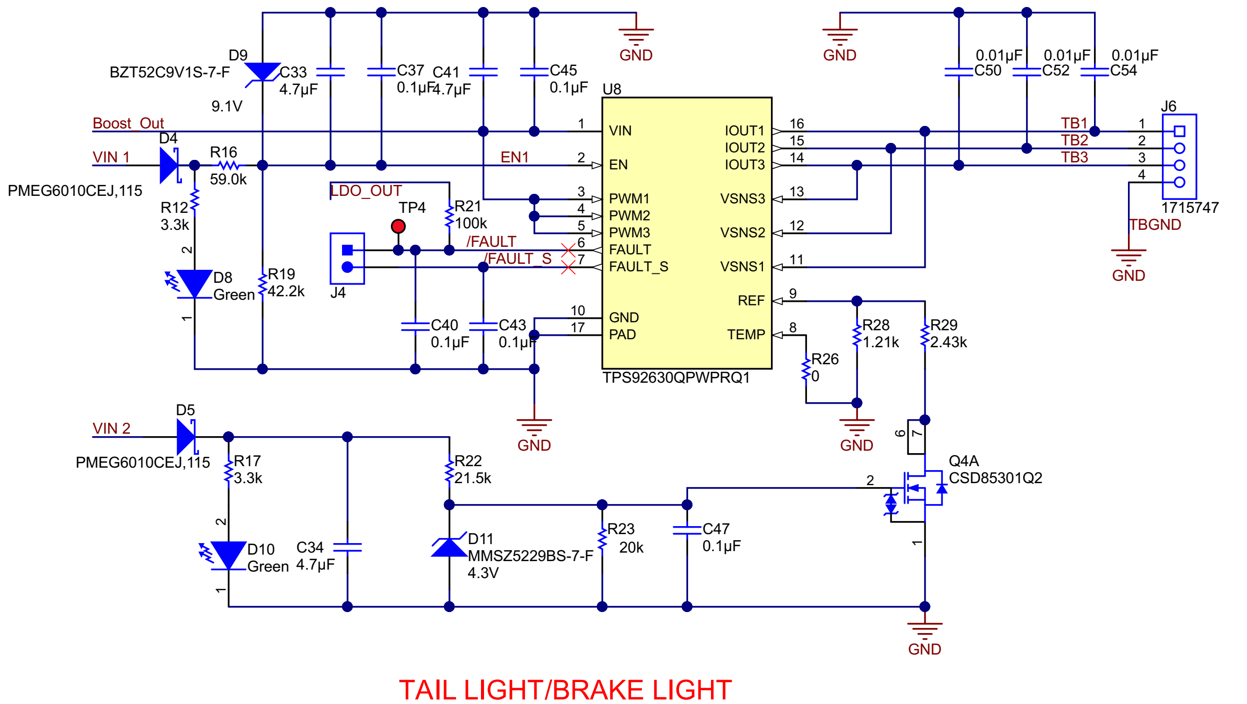


Figure 18. TPS92630-Q1 3-Channel LED Driver

Dim the pulse-width modulation (PWM) to achieve different brightness. Dimming the PWM has switching currents as the LEDs are turned on and off, causing electromagnetic interference.

Dim the PWM linearly to operate at a constant 100% duty cycle, and the maximum current adjusts to the brightness that is required. TI recommends this approach to have the application EMI as quiet as possible. The maximum current that passes through the LEDs is programmable by the sense resistor $R_{(REF)}$ (R28, R29). This design has a 100-mA current ($I_{(tail)}$) per LED string for the tail ight, turn indicator, and the reverse light. See Equation 43 for the $R_{(REF)}$ calculation.

$$R_{REF} = \frac{V_{REF} \times K_{(I)}}{I_{tail}} = \frac{1.22\text{ V} \times 100}{0.1\text{ A}} \times 1.222\text{ k}\Omega$$

Where:

- V_{REF} = 1.222 V and $K_{(1)}$= 100 (both V_{REF} and $K_{(1)}$ are data sheet values) (43)

For many automobiles, the same set of LEDs illuminates both tail lights and stop lights. Thus, the LEDs must operate at two different brightness levels. The dimming level is set with a parallel resistor in REF through an external MOS (Q4A). See Equation 44.

$$R_{tail} = \left(\frac{I_{stop}}{V_{REF} \times K_{(I)}} - 1/R_{stop} \right)^{-1} = \left(\frac{0.15}{1.22\ V \times 100} - 1/1.21\,k\Omega \right)^{-1} = 2.49\ k\Omega \tag{44}$$

A 2.49-kΩ resistor is ideal, but this design uses a 2.43-kΩ resistor. VSNS1 to VSNS3 are not used in this design and are tied to OUT1 to OUT3 per the data sheet recommendation. Because the gate of the brake-light MOSFET Q4A is directly attached to jumper J2 through the net VIN2, which is connected directly to the car-battery input voltage, the brake light must be protected against the highest voltage the input can conduct. In this design the load-dump voltage is 45 V.

A resistor divider (R22 and R23) in combination with a 4.3-V Zener diode is used to prevent the gate from high voltage transients. Two debounce capacitors (C34 and C47) are also used. Additional reverse-battery protection is required for the gate of FET Q4A and the EN path of the device because the nets VIN 1 and VIN 2 are directly connected to the car battery.

Two LEDs (green) indicate the operating mode of the device. If the device is in the tail-light operating mode, diode D8 turns on (see D8 Green in Figure 18). If the device is in the brake-light operating mode, diode D10 turns on (see D10 Green in Figure 18). R12 and R17 limit the current of the indicator LEDs. The maximum-input voltage of R16 and R19 is divided down, helping D9 and the 9.1-V Zener protect the EN pin from external disturbances.

The included temperature monitor reduces the LED drive current if the IC junction temperature exceeds a thermal threshold. Users can program the temperature threshold through an external resistor. Users can disable the thermal current-monitor feature by connecting the TEMP pin to ground.

The TPS92630-Q1 device monitors fault conditions on the output and reports the status on the $\overline{\text{FAULT}}$ and FAULT_S pins. The device features single-shorted-LED detection, output short-to-ground detection, open-load detection, and thermal shutdown. Two separate fault pins allow maximum flexibility of fault-mode reporting to the MCU in case of an error.

The TPS92630-Q1 device has two fault pins, $\overline{\text{FAULT}}$ and $\overline{\text{FAULT\_S}}$. $\overline{\text{FAULT\_S}}$ is a dedicated fault pin for single-LED short failure, and $\overline{\text{FAULT}}$ is for general faults (for example: short, open, and thermal shutdown). The dual pins allow maximum flexibility based on all requirements and application conditions. The device fault pins can be connected to an MCU for fault reporting. Both fault pins are open-drain transistors with a weak internal pullup. In this design, the $\overline{\text{FAULT}}$ pin is tied with a 100-kΩ resistor to the 3.3-V output of the LDO to have a defined state. $\overline{\text{FAULT\_S}}$ can also be connected through a jumper to $\overline{\text{FAULT}}$. Both pins feature a capacitor-debounce protection (C43 and C40) at 100 nF each. Input VIN is decoupled with a 4.7-uF and 100-nF capacitor (C41 and C45).

The outputs IOUT1 to IOUT3 are connected to a header to allow different lengths of LED strings to be attached per channel. C50, C52, and C54 are ESD capacitors for protection of the device from high-voltage transients generated by people touching the connector interface.

5.4.2 Reverse Light

The reverse light is set up the same as the tail and brake light. However, the outputs are not dimmable. The REF input is only tied to GND through the 1.21-kΩ resistor and the parallel path is omitted in Figure 19. Refer to Section 5.4.1 for a detailed description of the device dimensioning and features of the reverse light.

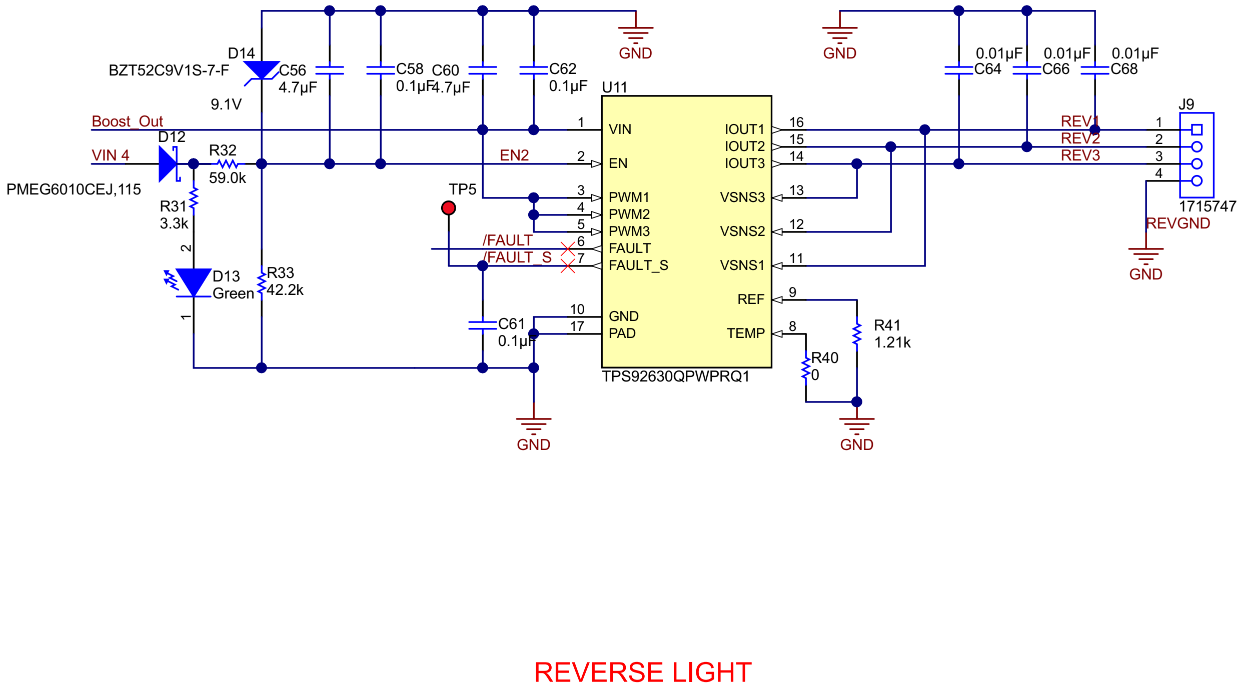


Figure 19. TPS92630-Q1 3-Channel LED Driver

5.4.3 Turn Light

In Figure 20, the PWM1 to PWM3 inputs are tied together and connected to jumper J5, which allows the user to select between permanent on or the LED-blinking function. Setting jumper J3 enables and disables the TLC555-Q1 oscillation.

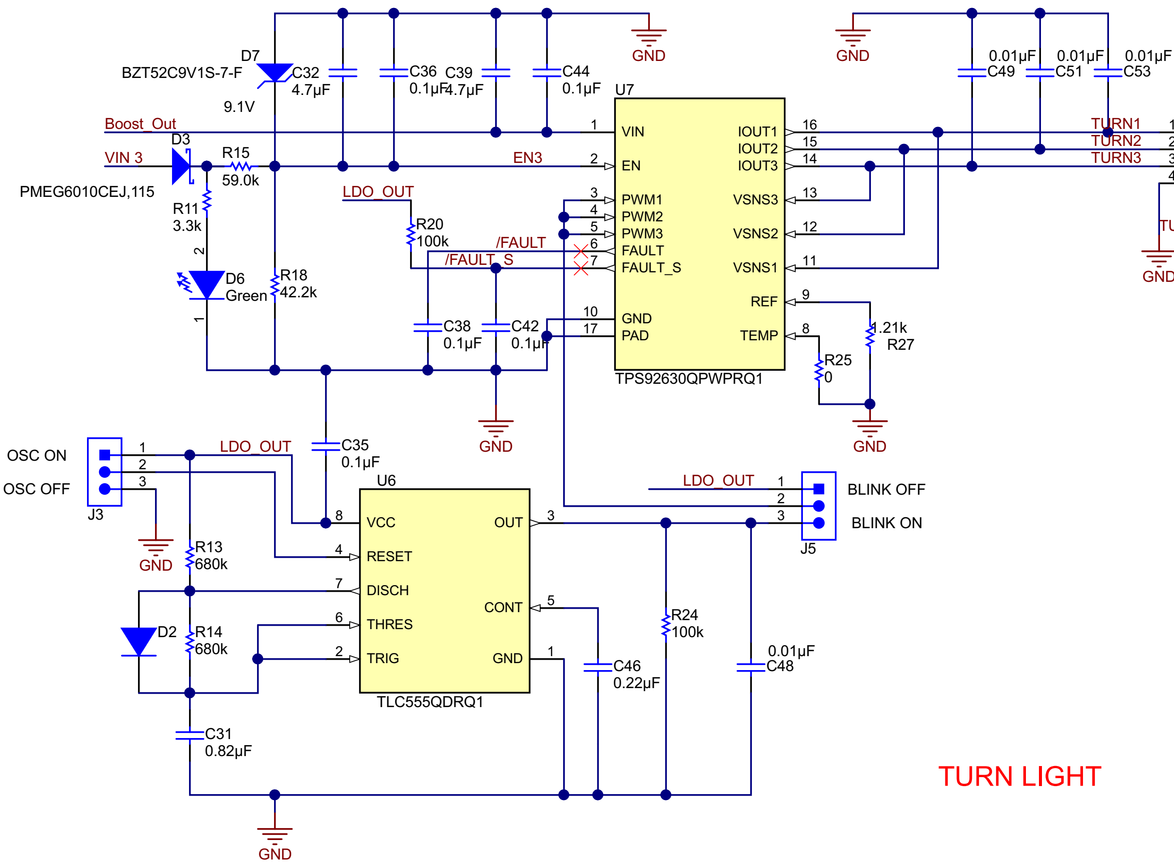


Figure 20. TPS92630-Q1 3-Channel LED Driver

In Figure 20, connecting TRIG to THRES of the TLC555-Q1 causes the timer to run as a multivibrator, generating a square-wave output voltage. Capacitor C31 charges through R13 and R14 to the threshold-voltage level (approximately 0.67 V_{DD}), then discharges through R14 to the value of the trigger-voltage level (approximately 0.33 V_{DD}). The output is high during the charging cycle ($t_{C(H)}$) and low during the discharge cycle ($t_{C(L)}$). The values of R13, R14, and C31 control the duty cycle as shown in Equation 45 and Equation 46.

$$t_{C(H)} \approx C_T \left(R13 + R14\right) \times \ln 2 \approx 0.82\ \mu F \times \left(680\ k\Omega + 680\ k\Omega\right) \times \ln 2 \approx 0.77\ s \tag{45}$$

$$t_{C(L)} \approx C_T \times R14 \times \mathrm{Ln}2 \approx 0.82\ \mu F \times 680\ k\Omega \times \mathrm{Ln}2 \approx 0.4\ s \tag{46}$$

In the previous two equations, use R13 and R14 = 680 kΩ. To get a symmetric duty cycle, diode D2 is paralleled to R14. This approach helps to eliminate one resistor during the charging phase. The capacitors at CONT, C46, and C48 are used for debouncing reasons.

5.4.4 Voltage Supervision

Figure 21 shows a supporting block. The circuitry in this block turns off the LED drivers if the battery voltage exceeds 17 V and it will signal open and short failures by turning on the red LED (D15) under normal- and high-voltage conditions.

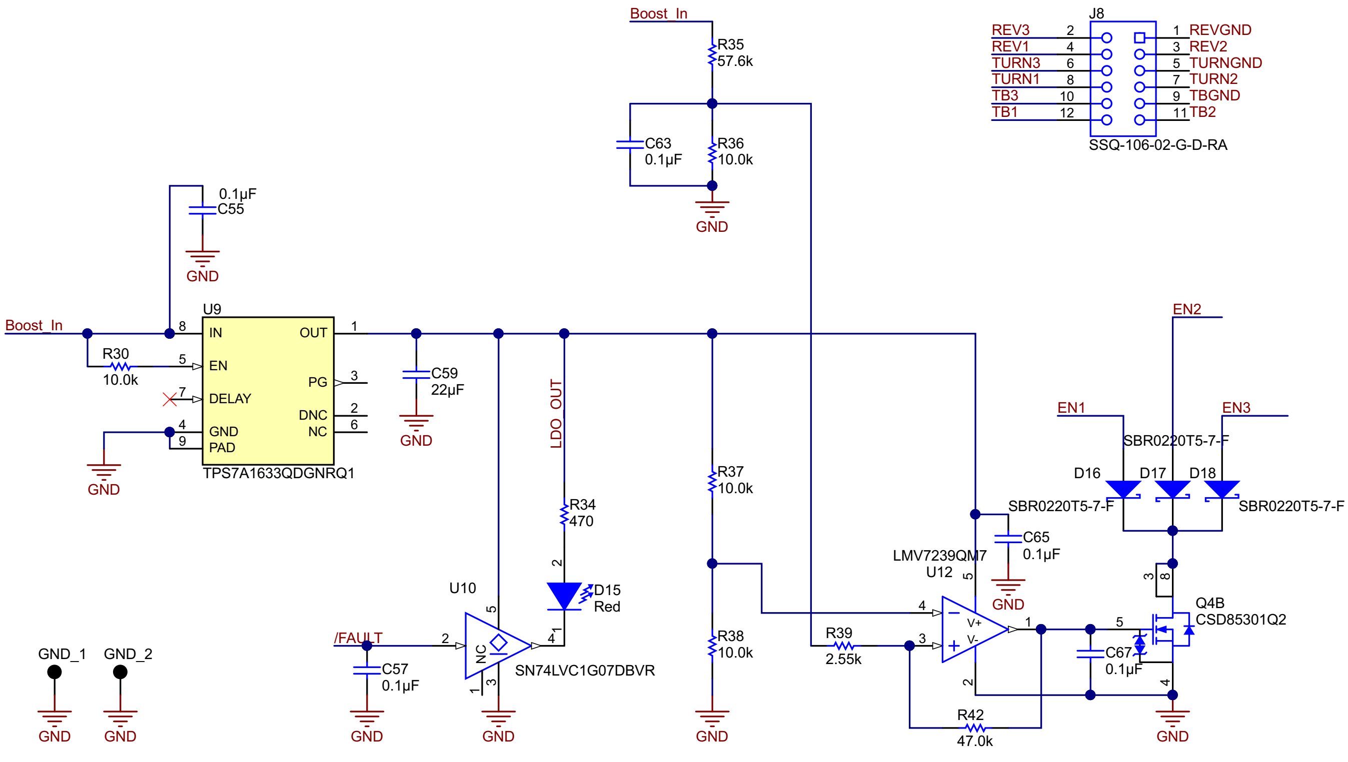


Figure 21. Voltage Supervision

Two 3.3-V linear regulators (LDO and U9) supply the little-logic buffer SN74LVC1G07 (U10). If the $\overline{\text{FAULT}}$ signal from the LED drivers is pulled low, the output of the SN74 is also pulled low and enables the red LED. R34 limits the current through the LED. C57 is a debounce capacitor. C59 at the LDO is used for stability, and a 22-µF capacitor is used according to the data sheet recommendation. EN is pulled high with a 10-k resistor so it remains on. For the overvoltage turnoff, an op amp noninverting circuitry is used. This circuitry activates a FET that pulls the cathode of the three diodes (D16, D17, D18) low, disabling the three LED drivers through the signals EN1, EN2, and EN3.

To set the threshold for the >17-V turnoff, R37 and R38 provide a 1.65-V reverence (50% of the 3.3-V LDO) to the negative input of the op amp. If the voltage at the signal Boost_In exceeds 17 V, the resistor dividers (R35 and R36) are dimensioned so the output of the comparator goes high and activates the downstream FET. C67 is used as a debounce capacitor, and C65 is the decoupling capacitor for the op amp. R39 and R42 are set according to the data sheet recommendation.

6 Getting Started Hardware

Connect the desired number of LEDs per string at the output screw terminals or at the receptacle to get started with the TIDA-00678 board. The ouputs are grouped in four terminals according to the type of light. Group 1 is labeled with TAIL/BRAKE for the tail light and brake light function. Group 2 is labeled TURN for the turn light. The third group is labeled REAR, and is for the reverse light. All outputs are labeled OUT1, OUT2, OUT3, and GND per group. One string of LEDs can be connected for every output. The maximum output voltage the board supports is approximately 16.5 V. Nine strings of LEDs up to this voltage can be connected for all terminals. As detailed in Section 5.4.1, the output current is set to 100 mA nominal. The appropriate jumper setting is 150 mA for the brake light. The turn and rear light is 100 mA and cannot be dimmed.

Loads can be connected to each output through the screw terminals along the bottom of the board, labeled in Figure 22.

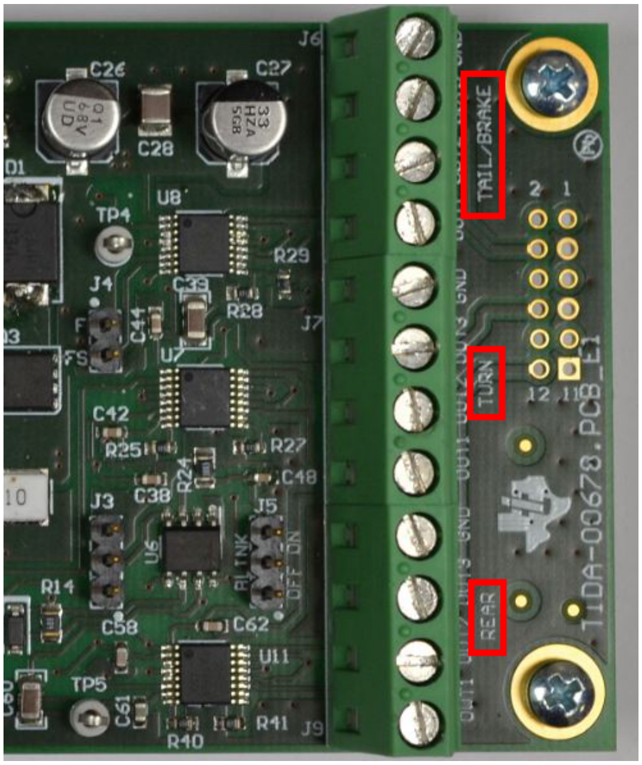


Figure 22. Screw Terminals for LED-String Outputs (100 mA and 150 mA, Maximum of 9 Strings, Maximum Output Voltage of 16.5 V)

Set the header on jumper J2 in Figure 23 for the desired type of light (tail, brake, turn, or reverse light).

Figure 23. Jumper J2 for Setting the Type of Light

To enable an active turn light (blinking), set jumpers J3 and J5 as shown in Figure 24.

Figure 24. Turn-Indicator Setting

Connect the leads displayed in Figure 25 (a minimum of 15 AWG is recommended) to the 2-port screw terminal on the left side of the board. The screw terminal is labeled VIN (+) and (–) to indicate the proper polarity of the supply.

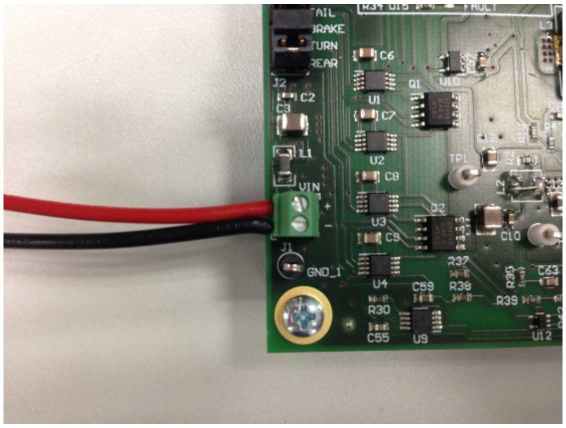


Figure 25. Board Supply-Input Terminal

Connect a power supply capable of at least 12 V and 7 A to the leads, then turn it on.

Figure 26 shows the LEDs that indicate on lights and failures.

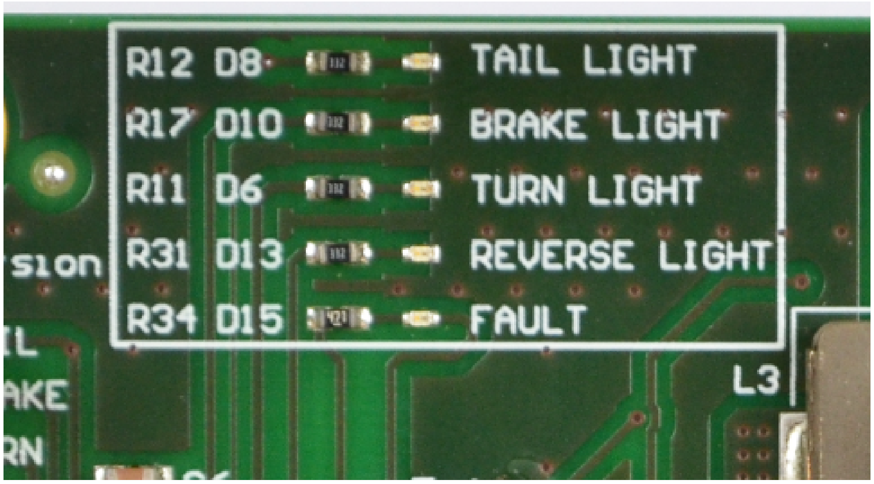


Figure 26. LEDs Indicating Failures and On Lights

A 0-Ω resistor (R2) is available on the board to bridge the input filter if desired. To disable the overvoltage-turnoff function, remove resistor R35 (see Figure 27).

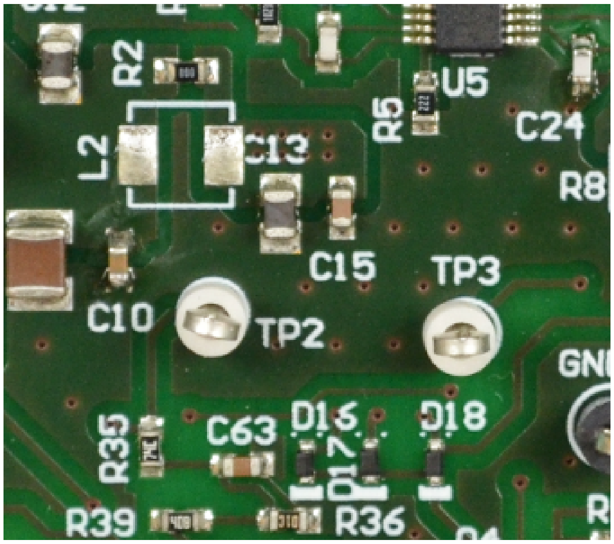


Figure 27. Resistors R2 and R35

7 Test Setup

Figure 28, Figure 29, Figure 30, and Figure 31 show how to set up for various tests.

7.1 Load-Transient Test Setup

Figure 28 shows the test setup for load dump, cold crank, jump start, and reverse battery.

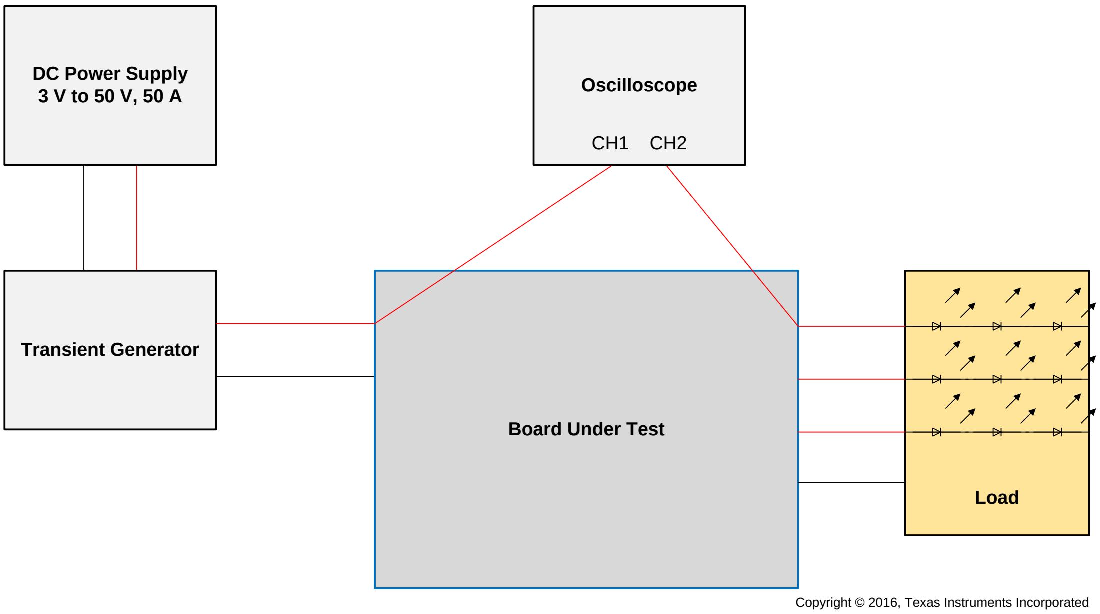


Figure 28. Test Setup for Load Dump, Cold Crank, Jump Start, and Reverse Battery

The NSG is used for transient generation. Users need the Teseq AutoStar software to work with the NSG 5500. The software has predefined pulses that the user can adjust to meet specific requirements. See Figure 29.

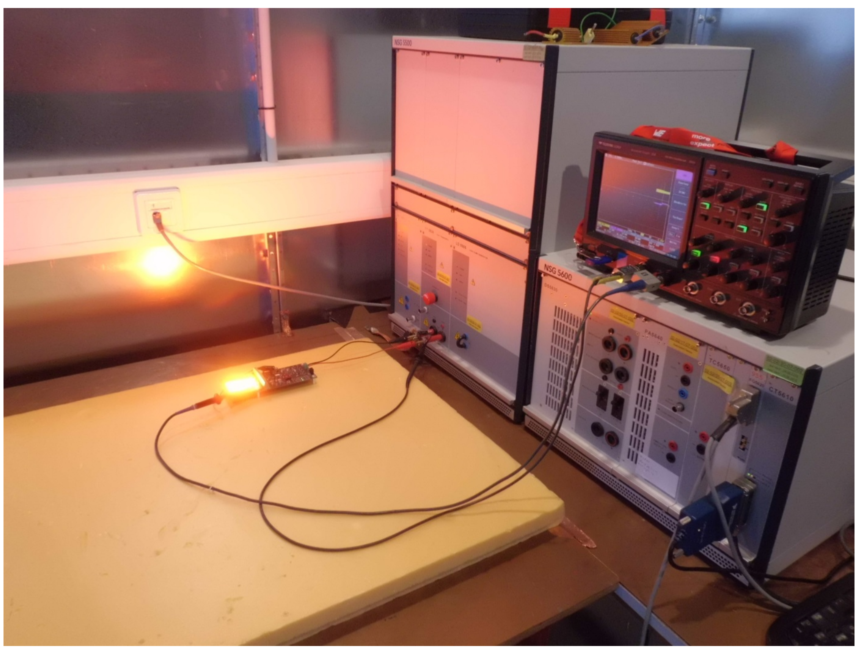


Figure 29. Setup for Transient Tests With LED Board and NSG 5500 Transient Generator

7.2 Thermal Image-Test Setup

The diagram in Figure 30 shows the setup to measure thermal behavior.

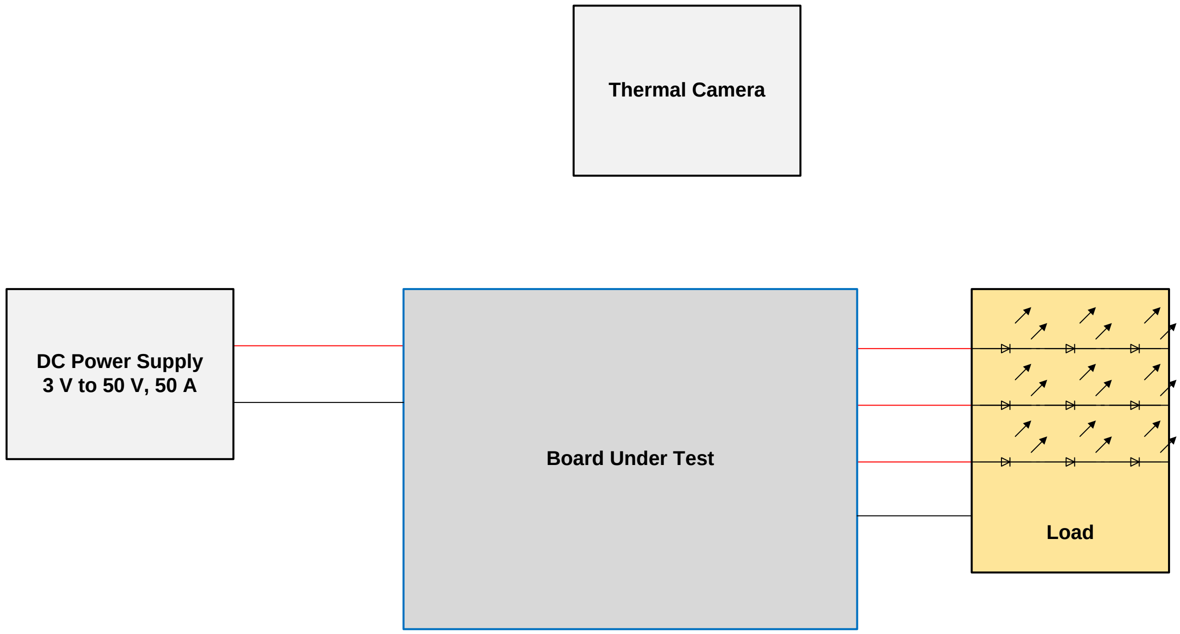


Figure 30. Setup to Measure Thermal Behavior of the Board

7.3 Efficiency-Measurement Setup

The diagram in Figure 31 shows how to set up an efficiency test.

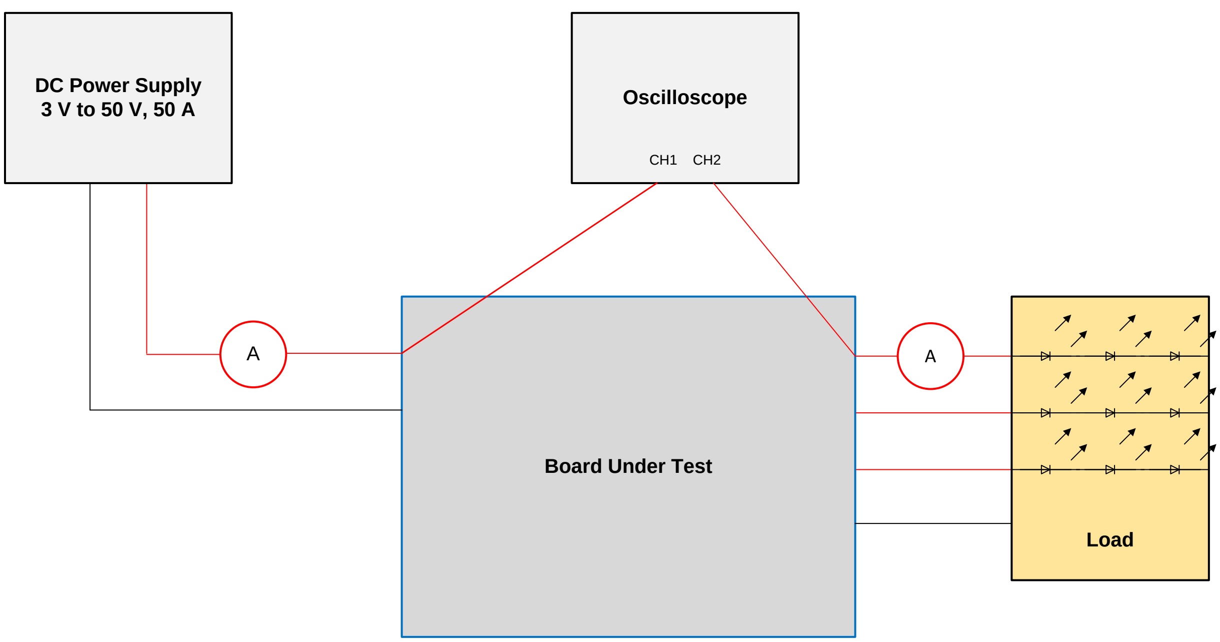


Figure 31. Efficiency-Test Setup

8 Test Data

The following subsections show data from Section 7.

8.1 Thermal Images

Figure 32, Figure 33, and Figure 34 show the temperature rise of the different components at room temperature.

Figure 32. TPS92630-Q1 Linear LED Driver-Temperature at Three Strings of 100-mA LEDs

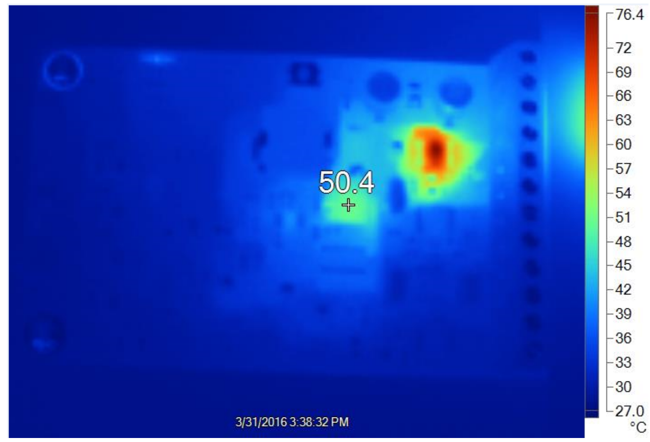


Figure 33. TPS40210-Q1 Boost-Converter Temperature Above 50°C at Three Strings of LEDs at 100 mA

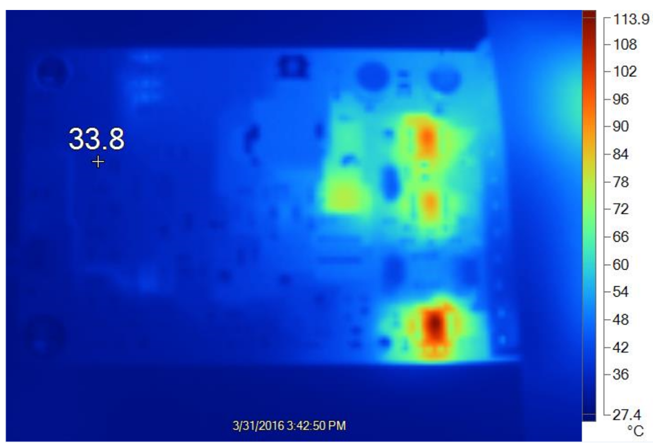


Figure 34. LM74610-Q1 Smart-Reverse Battery-Diode Temperature at 13.5-V Input Voltage

8.2 Efficiency Testing

Figure 35 shows the results of the efficiency test on the system. The V_{IN} that is given is what is applied to the board inputs, not the voltage at the input of the linear LED driver. This implies that this is a measure of the total-system efficiency taking all losses into account, and not simply that of the TPS92630-Q1 LED driver.

8.3 Electrical-Transient Testing

Four electrical transient tests were performed with standardized pulses to show the behavior of the LED driver-boost combination during tests, shown in Figure 36, Figure 37, Figure 38, and Figure 39. Pulses from ISO 7637-2:2004 Pulse 4, 5a (cold crank and load dump), jump start, and reverse battery were used. The test voltage is 13.5 V. On the LED board there is turnoff circuitry with overvoltage that can turn off the LED driver once the input voltage exceeds 17 V. All tests were conducted twice: once without high-voltage turnoff and once with high-voltage turnoff.

8.3.1 Load Dump

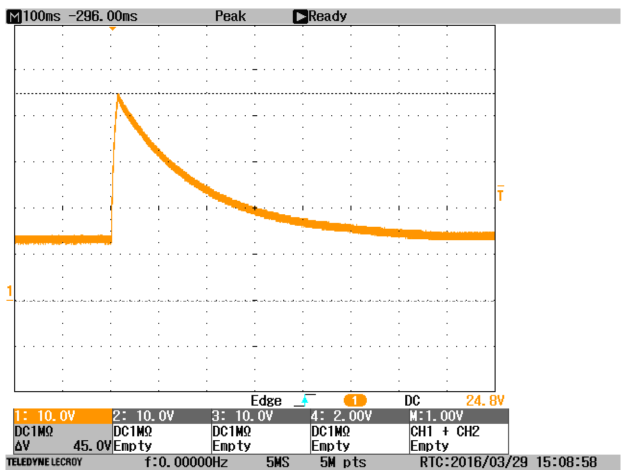


Figure 36. ISO 7637-2:2004 Pulse 4 Load Dump

The pulse was verified open circuit. The following parameters were used:

- V_{min} = 45 V
- R_{source} = 2 Ω
- T_{rise} = 10 ms
- $T_{duration}$ = 400 ms

The circuit was subjected to the pulse, and the disturbance to the output of the TPS92630-Q1 was measured.

Figure 37, Figure 38, and Figure 39 show the remaining three electrical transient tests that were performed with standardized pulses to show the behavior of the LED driver-boost combination.

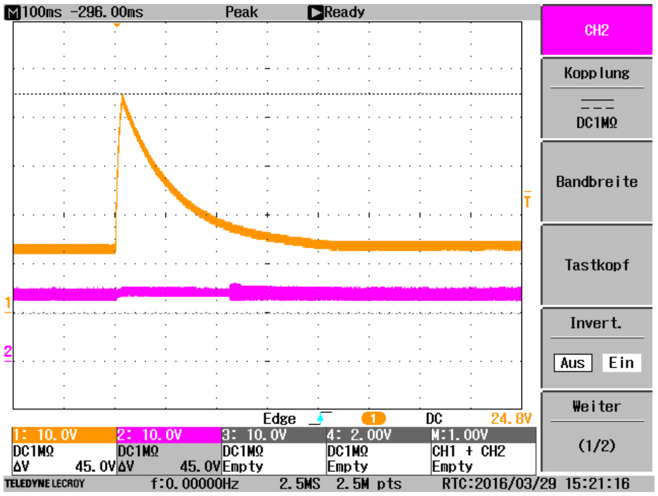


Figure 37. Load Dump (Orange) and Output (Pink) of TPS92630-Q1: No Turnoff

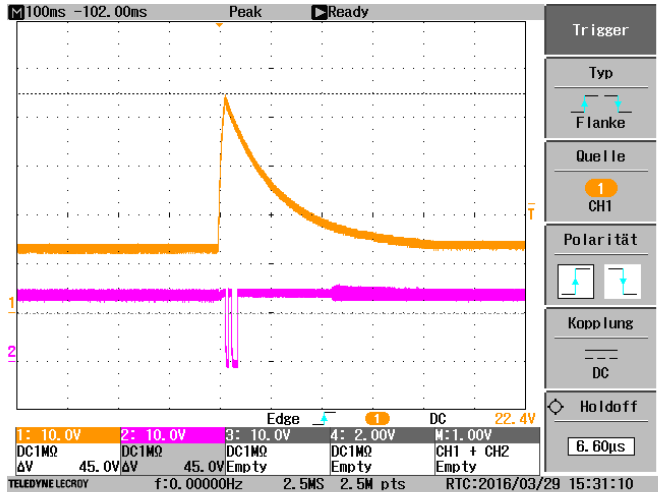


Figure 38. Load Dump and Output of TPS92630-Q1: With Thermal Toggling and No Turnoff

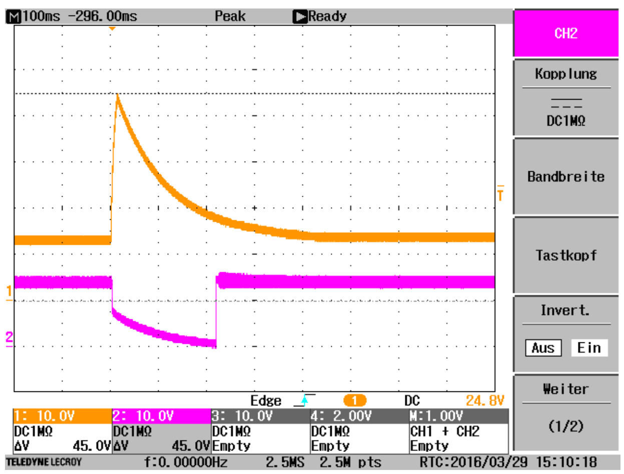


Figure 39. Load Dump and Output of TPS92630-Q1: Turned Off at > 17 V then Turned On

8.3.2 Reverse Battery

Reference the brown trace in Figure 40 on reversing the input voltage. The blue trace decays to 0 V and does not harm any device. The LM74610-Q1 disconnects the circuit from the input within a few µs.

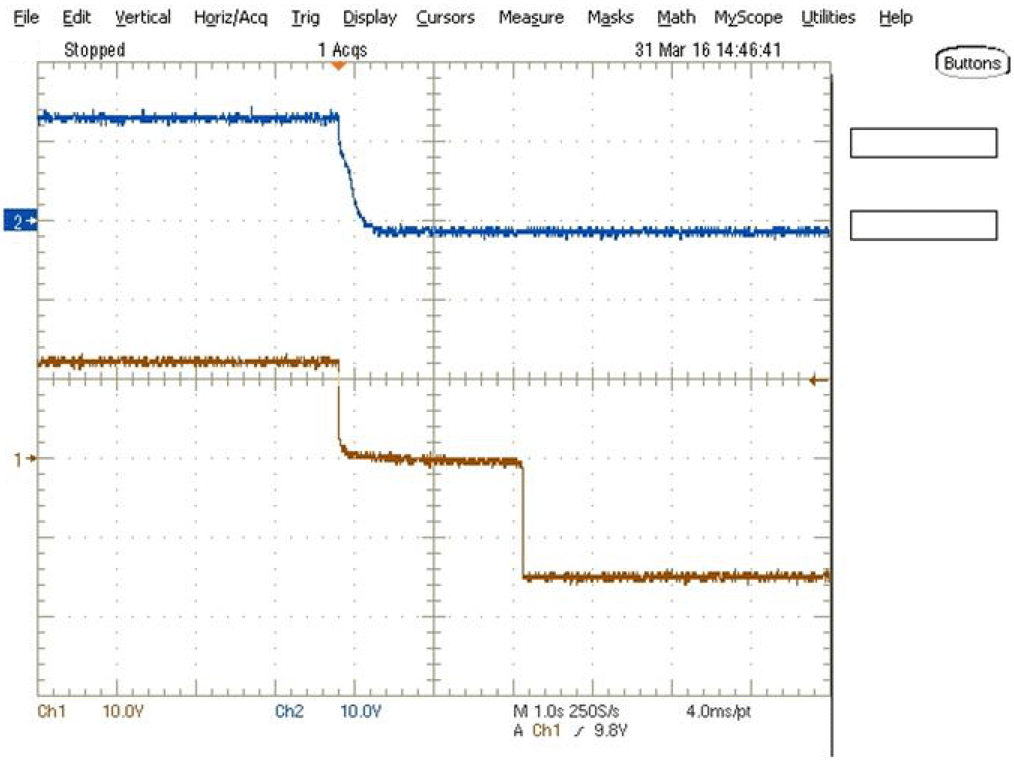


Figure 40. Reversing the Voltage to 13.5 V

The brown trace is the voltage at the board input (V_{IN}), and the blue trace is the voltage at the LED driver output (OUT1).

8.3.3 Double Battery and Jump Start

Figure 41 shows the jump-start test with the output-turnoff > 17 V feature enabled. The input voltage of the device rose from 13.5 to 26 V in 60 seconds (orange). The pink line is the output voltage on OUT1. LEDs turn off at > 17 V.

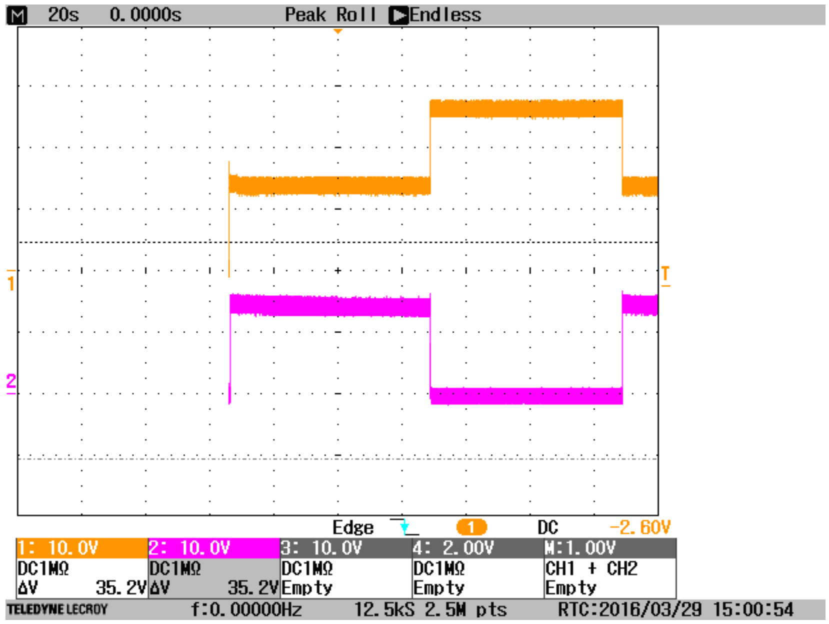


Figure 41. Jump-Start Condition

In Figure 42, the circuit was subjected to the pulse and the disturbance output of the TPS92630-Q1 was measured with the output turnoff at high-voltage feature disabled. The input voltage rose from 13.5 to 26 V in 60 seconds (orange). The pink lines is the output voltage on OUT1. The TPS92630-Q1 starts to terminally toggle. The high-voltage turnoff feature is disabled (> 17 V).

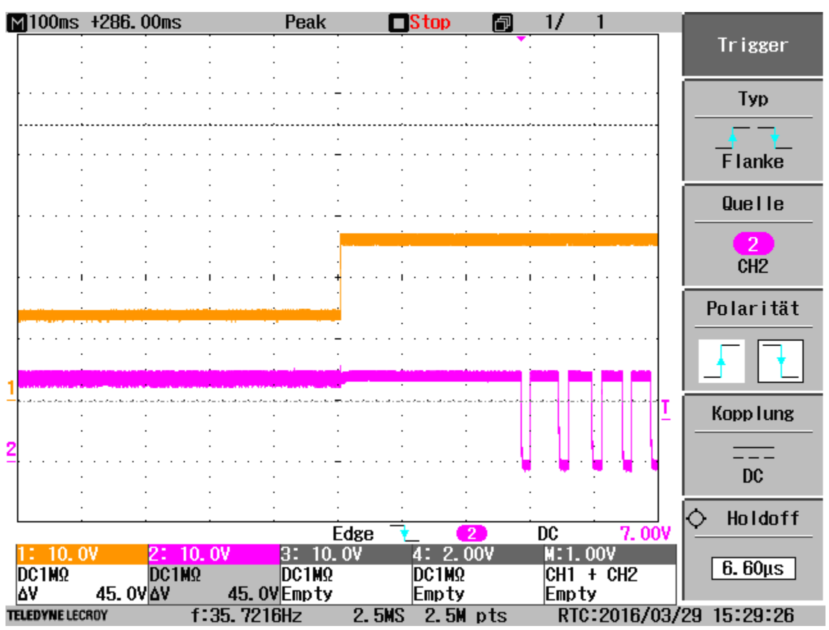


Figure 42. Jump-Start Condition 2

8.4 Cold-Crank Test

Testing the design for operation during a severe cold-crank pulse was an objective of this design. Figure 43 shows the parameters used for this test (only the *Severe* pulse was tested).

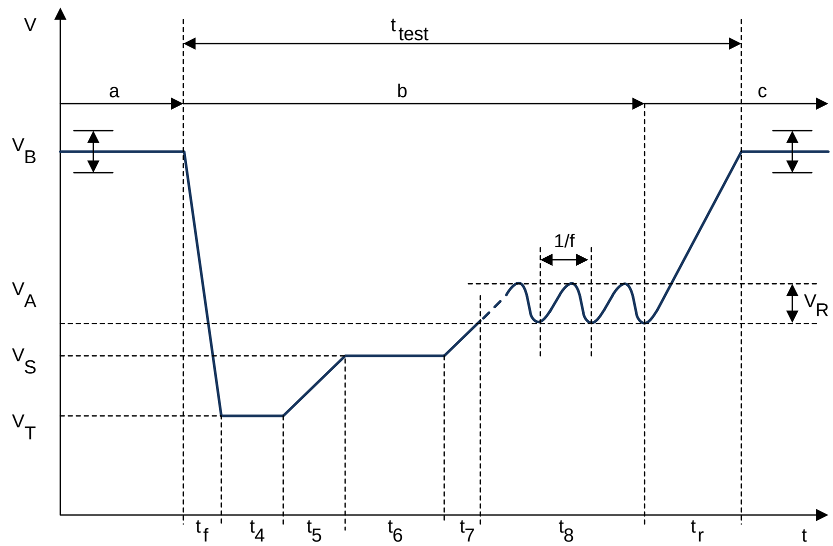


Figure 43. Cold-Crank Wave Shape

The lowest voltage (V_T) used in Figure 44 is 5 V. In Figure 44, the output (pink) stays high during the voltage drop (orange); the LEDs will stay on during the voltage dip.

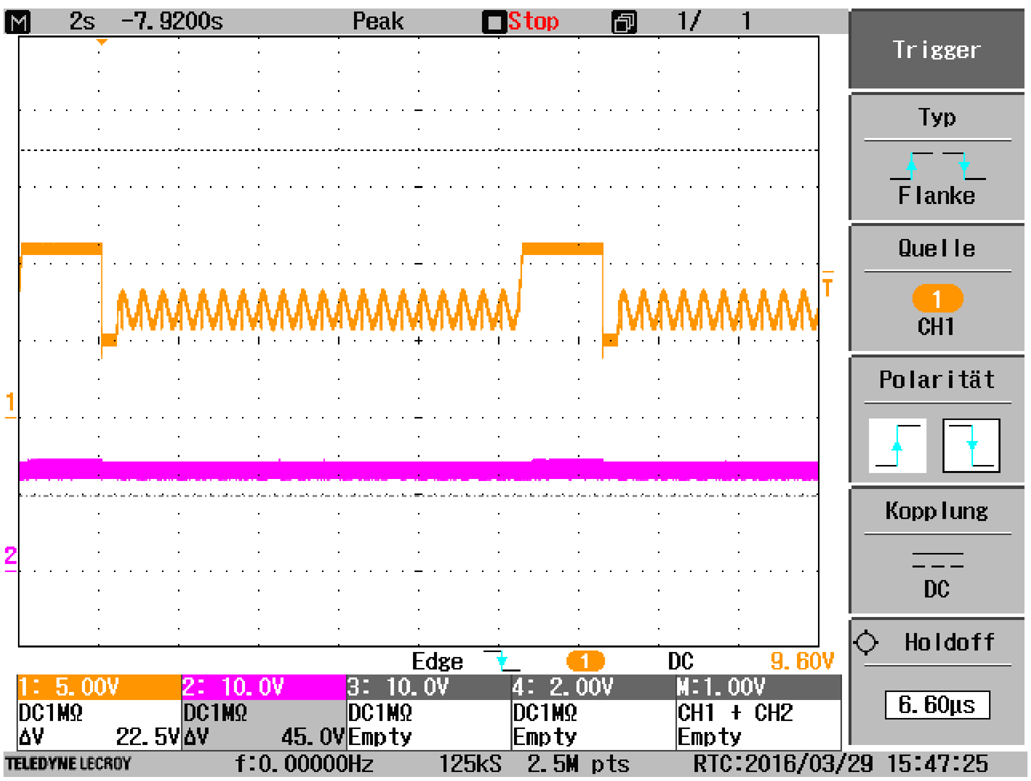


Figure 44. Cold-Crank Test

The boost responded quickly to compensate for the voltage dip to sustain the output voltage, allowing the TPS92630-Q1 to operate without any disturbance to the output.

8.5 CISPR 25-Emissions Testing

CISPR 25-EMI testing was completed at a third-party facility with compliant ALSE chambers used for emissions testing. Both Conducted and Radiated emissions tests were completed. Background on the standard and the test setup can be found in Section 4.3. When viewing the results, the red lines are Class 5 limits for average emissions, and the blue lines are the peak-emission limits. A table of measurements is available upon request. This report only shows the graphs.

8.5.1 Conducted Emissions

The conducted-emissions setup is shown in Figure 45 (power cable not attached). The LISNs are the gray boxes on the left side, the car battery is behind them, and the DUT is on the insulating material to the right. To test at 13.5 V, a variable voltage supply was fed through the bulkhead from outside of the chamber.

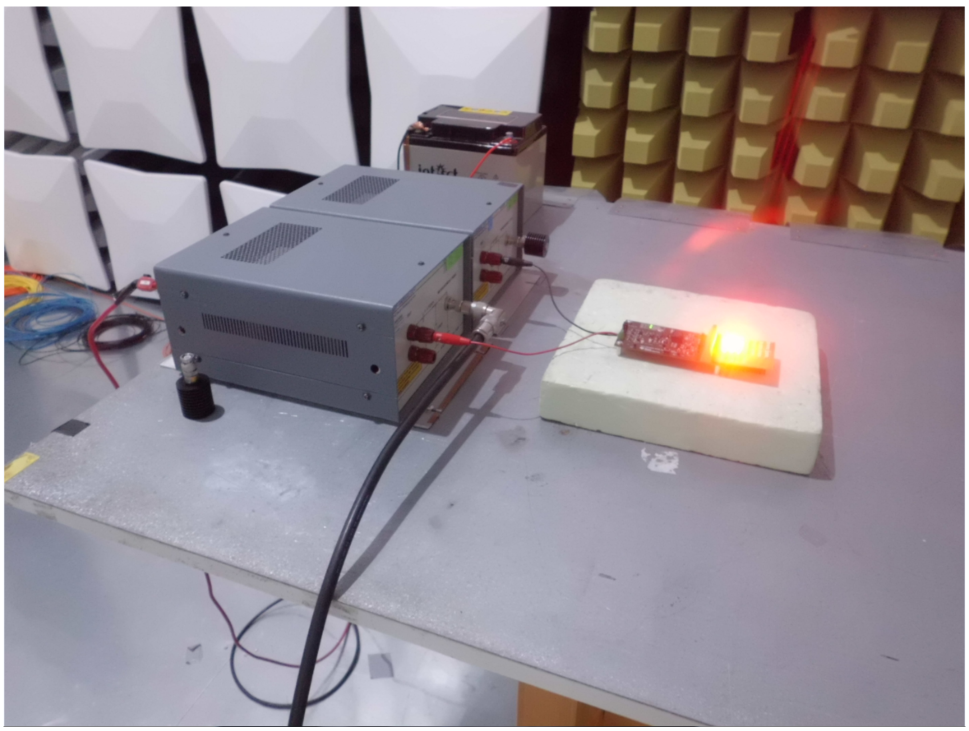


Figure 45. Conducted-Emissions Setup

The results are taken on both the return (ground) and line (hot) side through their respective LISNs. The test was conducted at 13.5 V (with the car battery). A load-LED board was connected during operation. Before testing, the noise floor was measured by conducting an ambient measurement with the DUT disconnected. The measurement technique changes above 30 MHz, resulting in the raise of the noise floor, shown in Figure 46 and Figure 47.

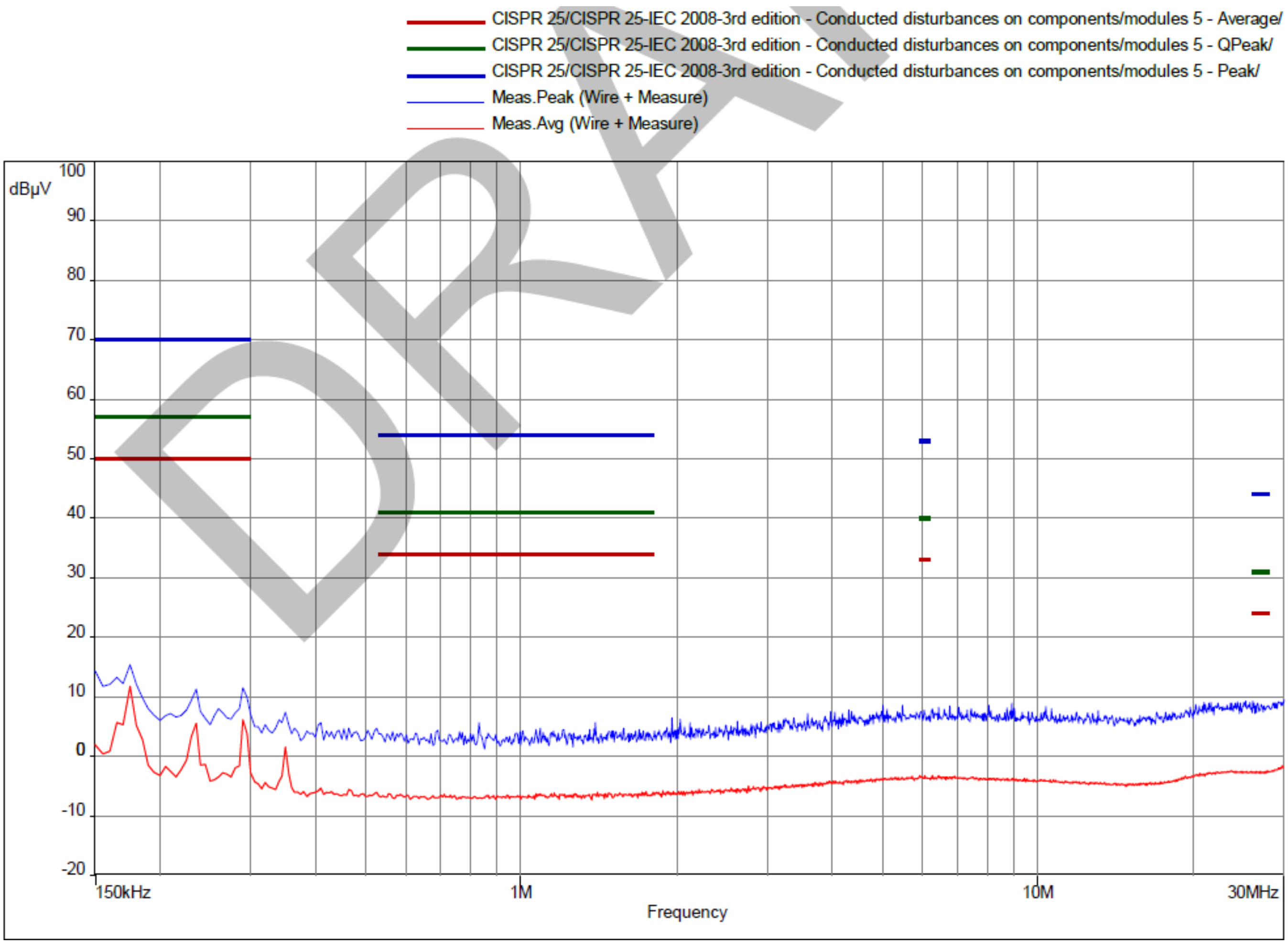


Figure 46. Ambient-Noise Level: Line Side 150 kHz to 30 MHz

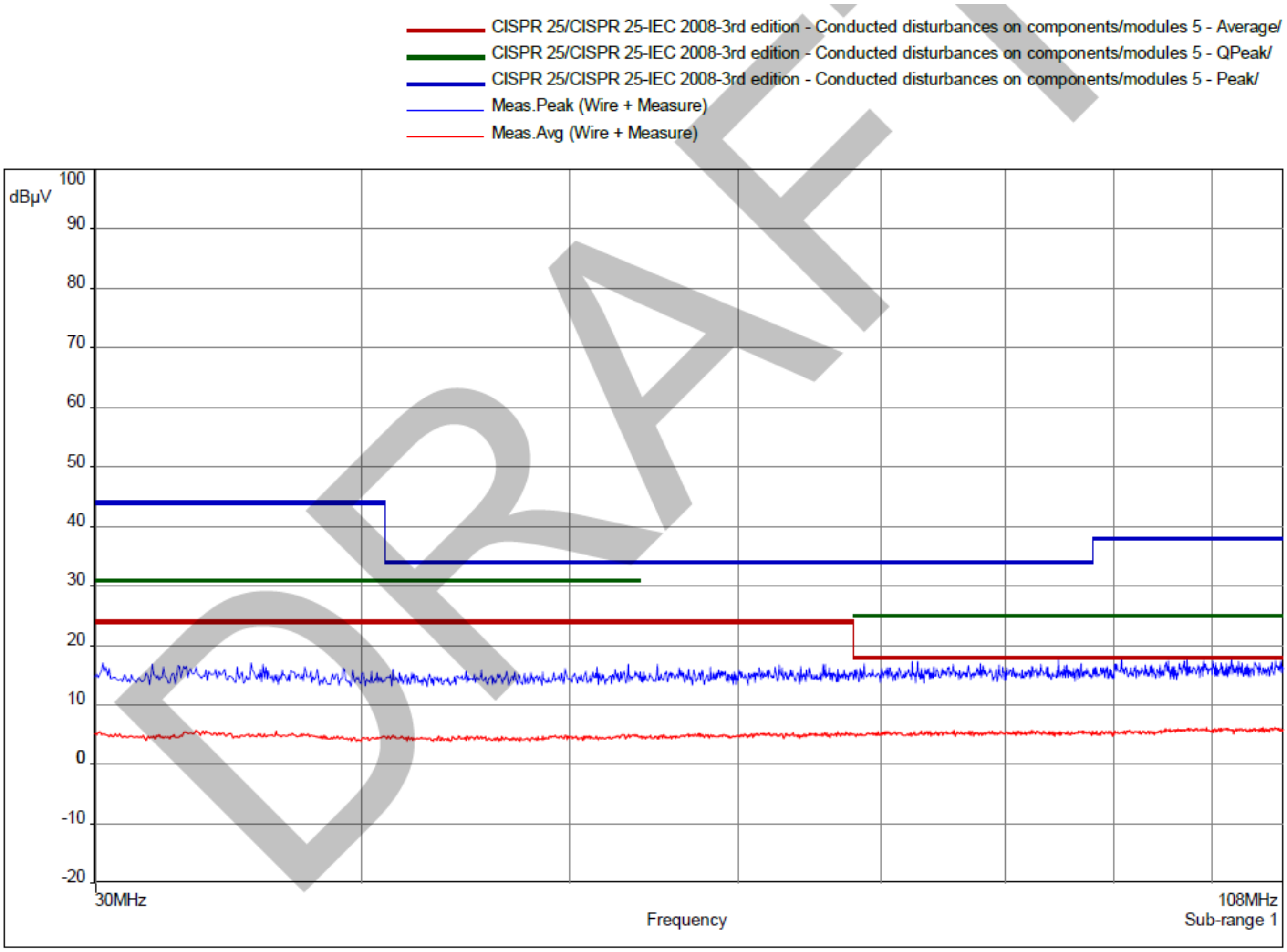


Figure 47. Ambient-Noise Level 2: Line Side 150 kHz to 30 MHz

The remainder of the results are shown in Figure 48 and Figure 49 at V_{IN} = 13.5 V. Only the graphs from the line side are shown because the graphs from the return (GND) side are identical.

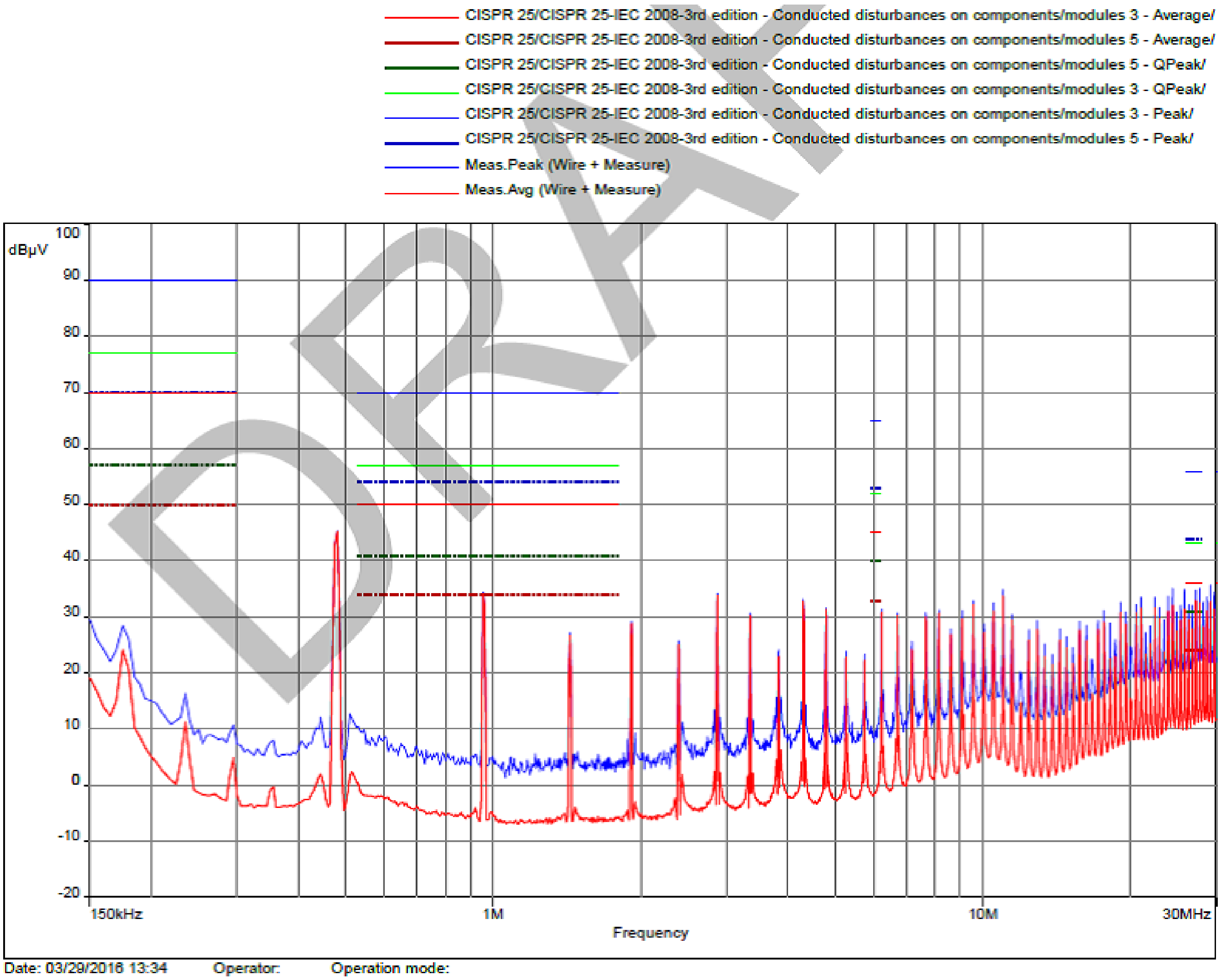


Figure 48. Conducted Emissions: Line Side 150 kHz to 30 MHz

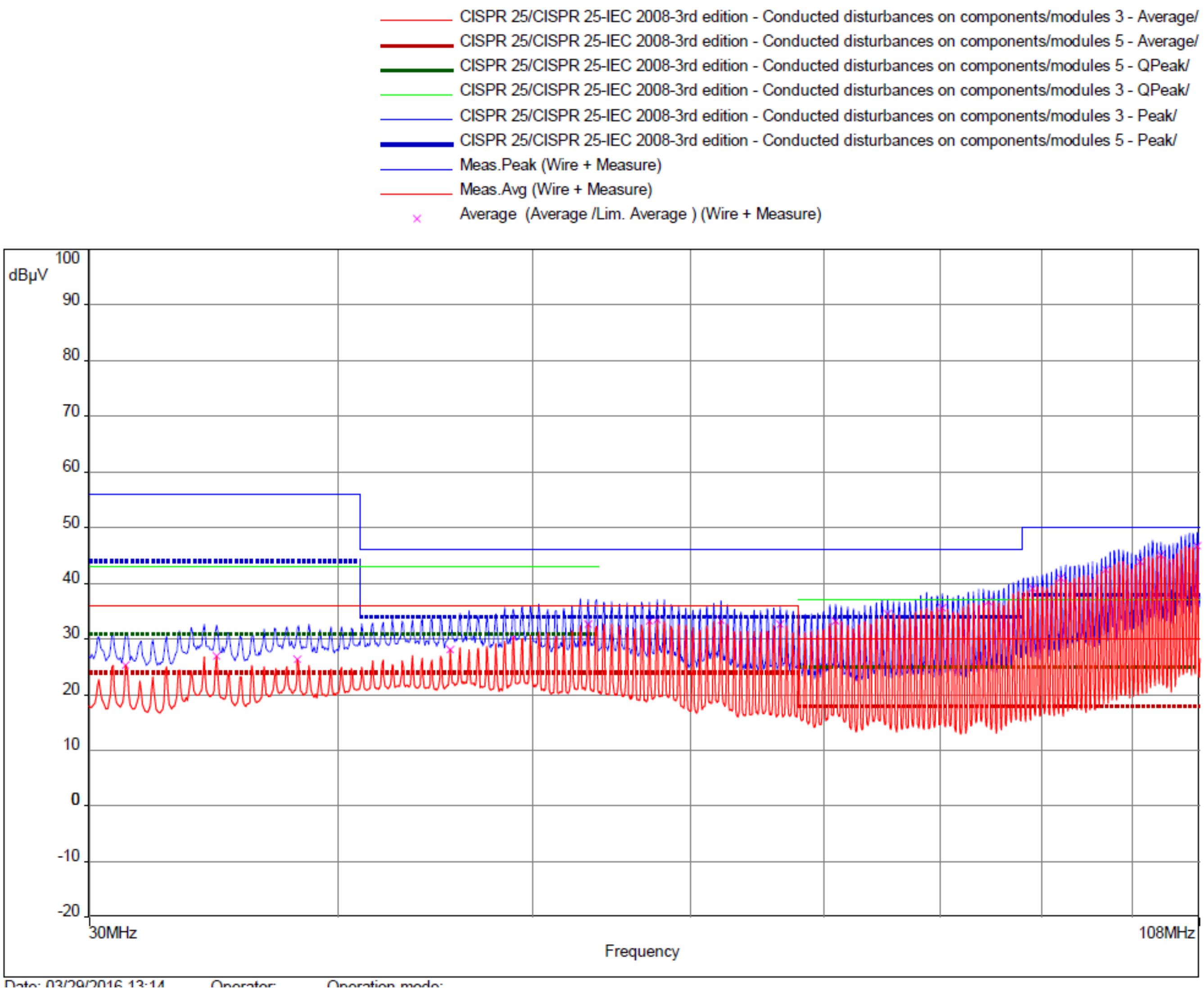


Figure 49. Conducted Emissions 2: Line Side 150 kHz to 30 MHz

In Figure 48, the conducted emissions in the range of 150 kHz to 30 MHz meet the requirements of CISPR 25 Class 5 for the peak measurement (blue). The average measurement (red) at 26 MHz meets Class 3.

In Figure 49, the conducted emissions in the range of 30 MHz to 108 MHz meet the 30 MHz to 67 MHz requirements of CISPR25 Class 3 for the average and peak measurement. Class 3 is still met for the peak (blue) measurement. The average (red) from 67 MHz to approximately 87 MHZ in Class 2 is met, and above that only Class 1 requirements are met.

8.5.2 Radiated Emissions

The radiated emissions setup is shown in Figure 50 and Figure 51. The LISNs are the gray boxes on the left side, the car battery is behind them, and the DUT is sitting on the insulating material to the right. To test at 13.5 V, a variable voltage supply was fed through the bulkhead from outside of the chamber. Unlike conducted emissions, the measurements must be divided into different sections, each section tested with a different type of antenna appropriate for that band.

Due to the limitations of the testing facility, the test was only to 1 GHz (a low enough noise floor could not be achieved above this level). There is some ambiguity in the CISPR25 requirement. It is unclear whether the DUT should be grounded to the test-ground plane. The DUT should be connected only if it would be connected in the car. Because the design is not a complete module and is somewhat generic, this connection option was available. This connection will often improve results by several dBµV.

Figure 50 and Figure 51 are images of the test setup for Radiated Emissions. A logarithmic antenna was used to test the lower frequencies.

Figure 50. Radiated Emissions Setup With a Logarithmic Antenna: 30 MHz to 2.5 GHz

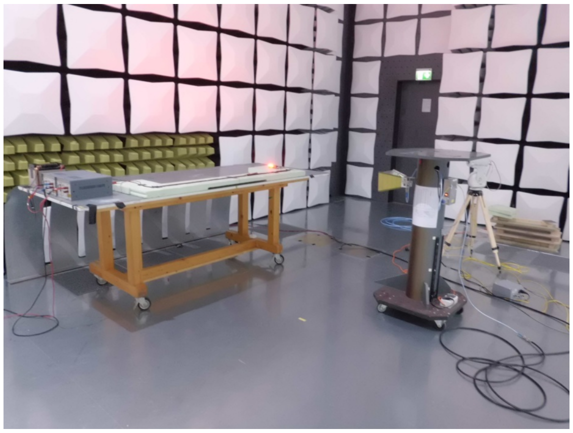


Figure 51. Radiated Emissions Setup With a Horn Antenna: 1.447 GHz to 1 GHz

Figure 52, Figure 53, and Figure 54 show the results when testing at 13.5 V.

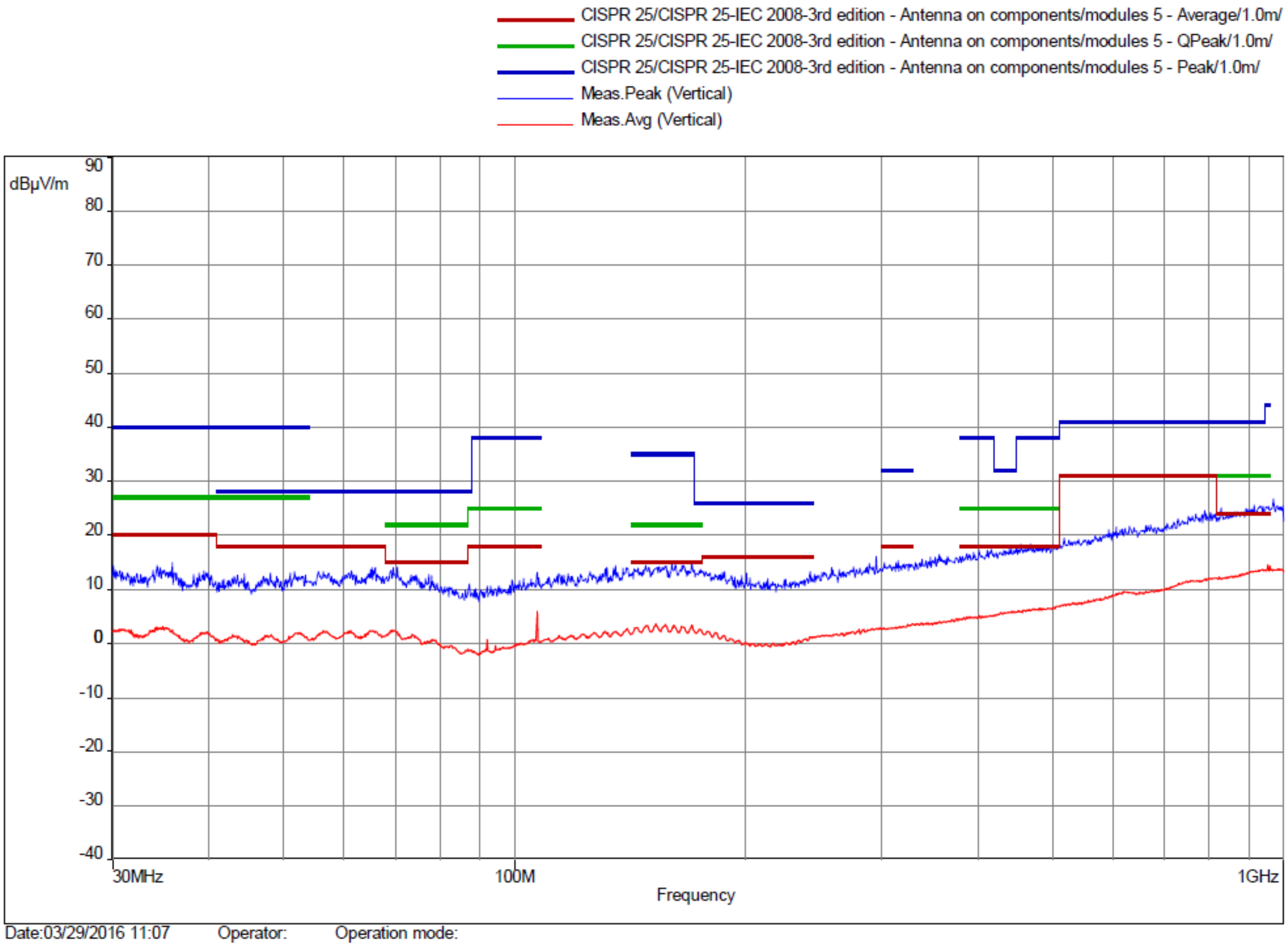


Figure 52. Ambient-Noise Level of Radiated Emissions: Line Side 30 MHz to 1 GHz

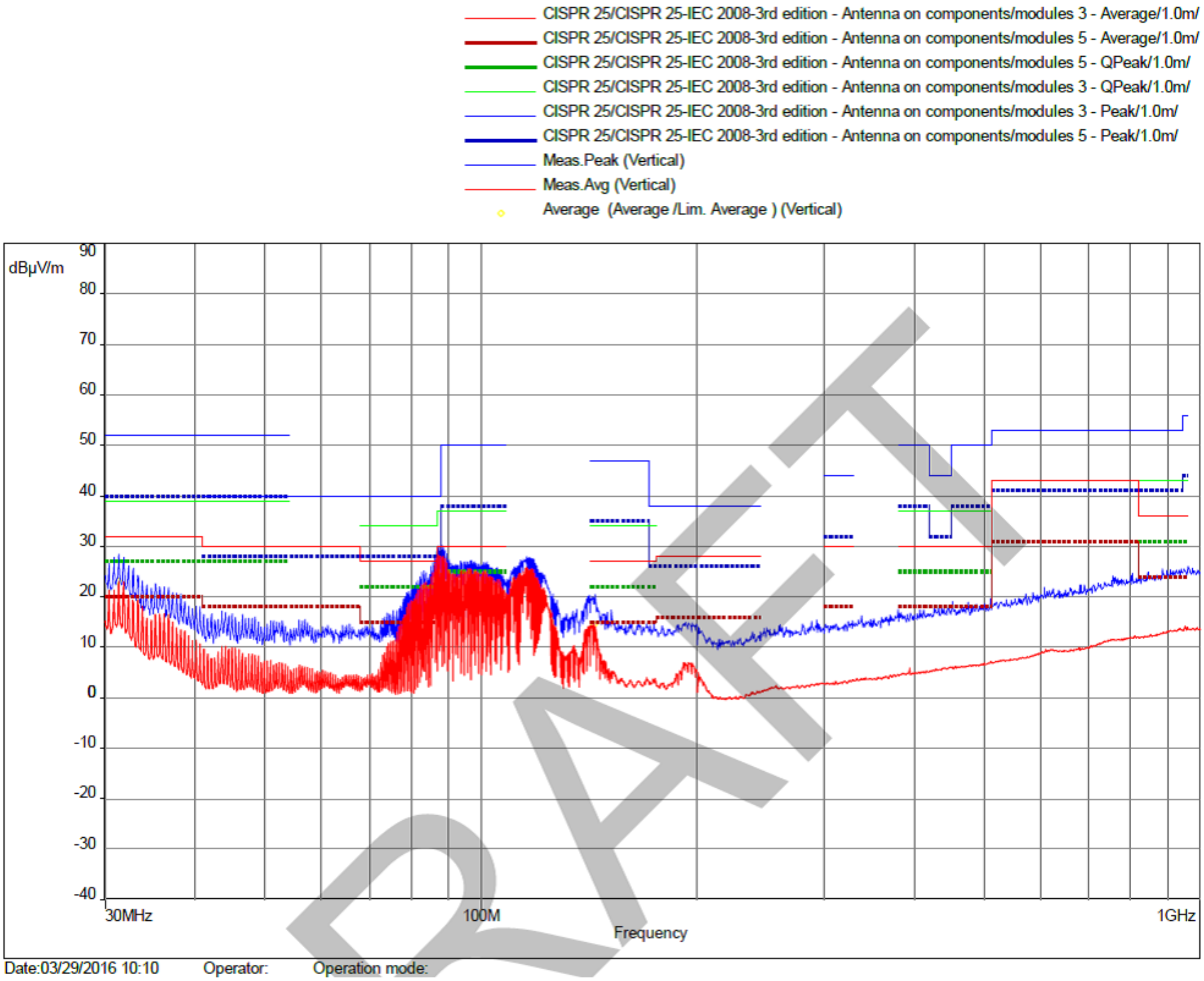


Figure 53. Radiated Emissions: Line Side 30 MHz to 1 GHz

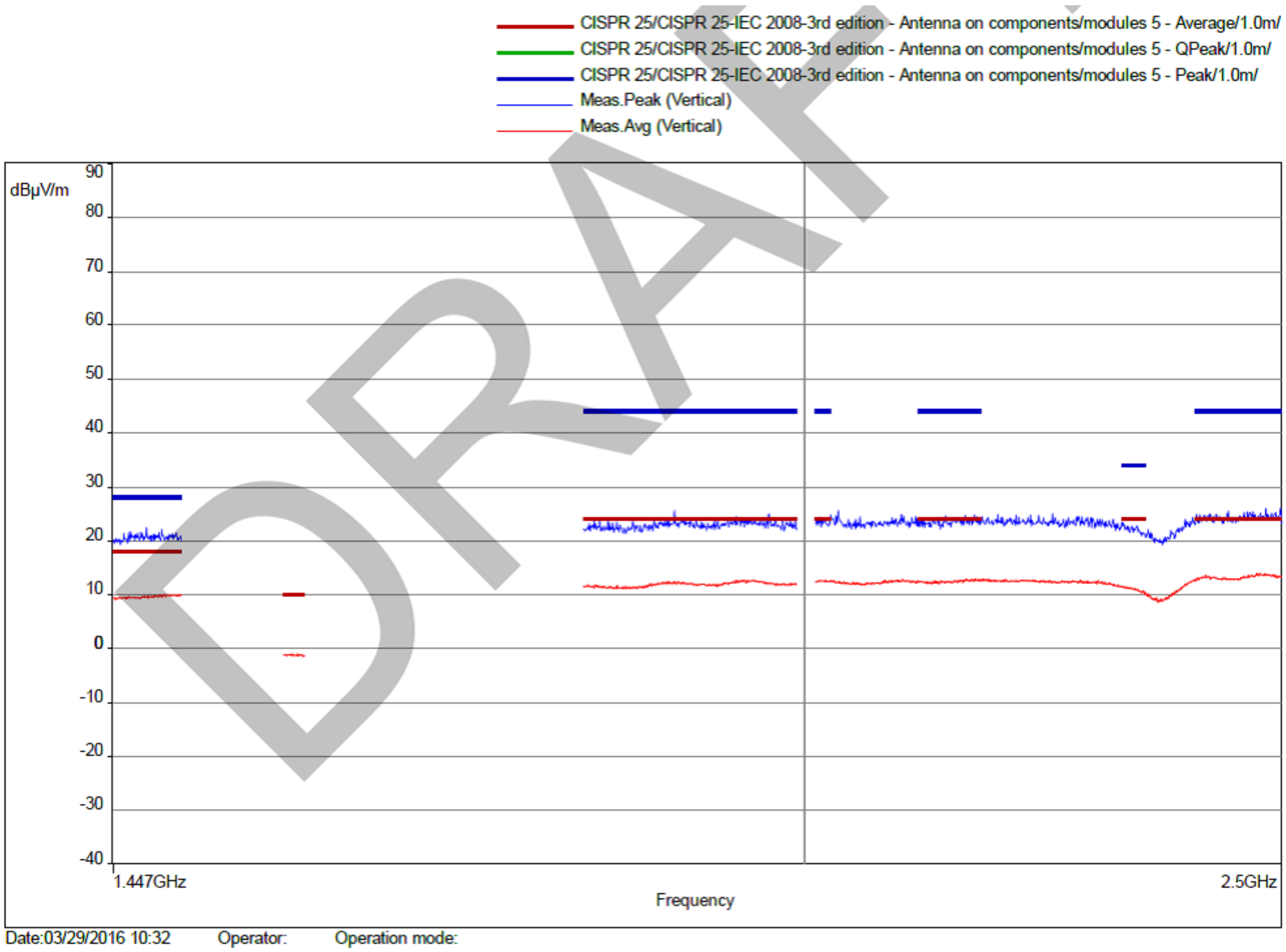


Figure 54. Radiated Emissions with a Horizontally-Oriented Antenna: 1.44 GHz to 2.5 GHz

The radiated emissions in the range of 30 MHz to 1 GHz meet the CISPR25 Class-3 requirements from 30 MHz to 32 MHz for the average and Class 5 for the peak measurement. Approximately 76 MHz requirement is met for peak and average Class 5 requirements. From 76 MHz to 108 MHz, only Class 3 is passed for both types of measurements. From approximately 125 MHz to 1 GHz, class 5 is met again for both measurements. In the upper range from 1.44 GHz to 2.5 GHz, the Class 5 standard can also be fulfilled.

8.5.3 Summary of Results

Table 7 shows the summarized results of both the Conducted and Radiated portions of the tests across different operating points and test conditions.

Table 7. Summary of Results

Conducted Emissions	Conducted Emissions	Class
150 kHz to 25 MHz	Peak	Class 5
	Average	Class 5
26 MHz to 30 MHz	Peak	Class 5
	Average	Class 3
30 MHz to 67 MHz	Peak	Class 3
	Average	Class 3
68 MHz to 87 MHz	Peak	Class 3
	Average	Class 2
88 MHz to 108 MHz	Peak	Class 3
	Average	Class 1
Radiated emissions		
30 MHz to 32 MHz	Peak	Class 5
	Average	Class 3
33 MHz to 76 MHz	Peak	Class 5
	Average	Class 5
77 MHz to 108 MHz	Peak	Class 3
	Average	Class 3
1.44 GHz to 2.5 GHz	Peak	Class 5
	Average	Class 5

Based on the results in Table 7, 13.5-V operation peak and average results do not always meet the highest CISPR 25 class level requirement. However, with some additional effort in filtering, such as tweaking the input filter, shaping the wave of the boost converter, or using a higher series resistor in the gate path, significant improvements can be achieved. Reviewing the layout and with an enclosure or shielding, this could be brought into compliance. Testing with the board grounded to the test-ground plane could improve results across all frequency ranges.

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00678.

9.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00678.

9.3 PCB Layout Recommendations

9.3.1 TPS92630-Q1 LED Driver

Figure 55 shows the thermal vias under the LED driver.

To download the layer plots, see the design files at TIDA-00678.

To prevent thermal shutdown of the TPS92630-Q1, T_J must be less than 150°C. If the input voltage is high, the power dissipation might be large. The devices are currently available in the TSSOP-EP package, which has good thermal impedance. However, the PCB layout is very important. A good PCB design can optimize heat transfer, which is essential for the long-term reliability of the device.

Maximize the copper coverage on the PCB to increase the thermal conductivity of the board because the major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is important when the design does not include heat sinks attached to the PCB on the other side of the package.

Add as many thermal vias as possible directly under the package-ground pad to optimize the thermal conductivity of the board.

All thermal vias should be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85 percent.

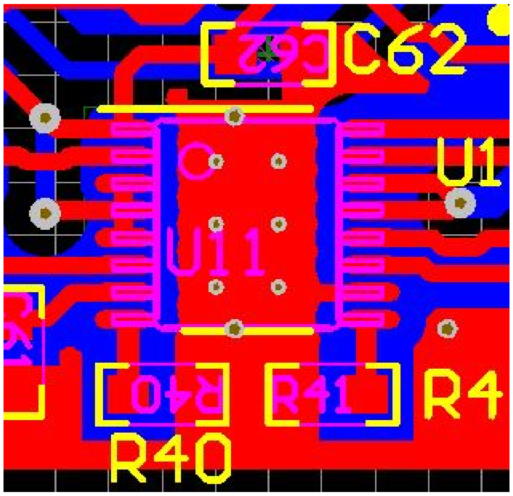


Figure 55. TPS92630-Q1 Thermal Vias Under LED Driver

9.3.2 LM74610-Q1 Layout Tips

Figure 56 shows the smart-reverse battery-diode layout. The following list contains recommended information about the layout of the LM74610-Q1.

- The VIN terminal must be tied to the source of the MOSFET using a thick trace or polygon.
- Connect the ANODE pin of the LM74610-Q1 to the source of the MOSFET for sensing.
- Connect the CATHODE pin of the LM74610-Q1 to the drain of the MOSFET for sensing.
- The high current path of this design is through the MOSFET, and it is important to use thick traces for source and drain of the MOSFET.
- The charge pump capacitor VCAP must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The GATE DRIVE and GATE PULL DOWN pins of the LM74610-Q1 must be connected to the MOSFET gate without using vias, and the trace to the FET should be as short as possible.
- Obtaining acceptable performance with alternate layout schemes is possible, but this layout has produced good results and is intended as a guideline.

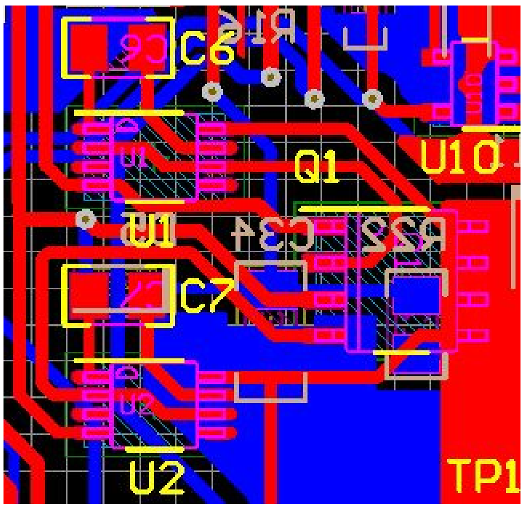


Figure 56. LM74610-Q1 Smart-Reverse Battery-Diode Layout

9.3.3 TPS40210-Q1 Layout Tips

Route voltage-feedback (FB) traces away from other noisy traces or components.. Avoid routing things under the switch node of a power inductor if possible.

FB nodes are high-impedance lines that are sensitive to disturbances. The switch node can radiate a significant amount of energy and could couple noise into FB traces or other sensitive lines. Placing these traces on the other side of the device (see the green square in Figure 57) helps mitigate noise-coupling effects. It is critical to place analog and control-loop components such that their trace lengths back to the IC are minimized.

The FB and COMP nodes are high impedance and susceptible to picking up noise. Because these nodes are critical in the operation of the device control loop, poor placement and routing of these components and traces can affect the performance of the device by enabling unwanted parasitic inductances and capacitances.

The boost converter (U5) is a controller (external FET) and therefore gate drive signals must be routed between the IC and the FETs. These nodes switch very quickly, so the distance and inductance they travel should be minimized. It is important to use the fewest number of vias as possible. Two vias are required in this design (see the purple square in Figure 57).

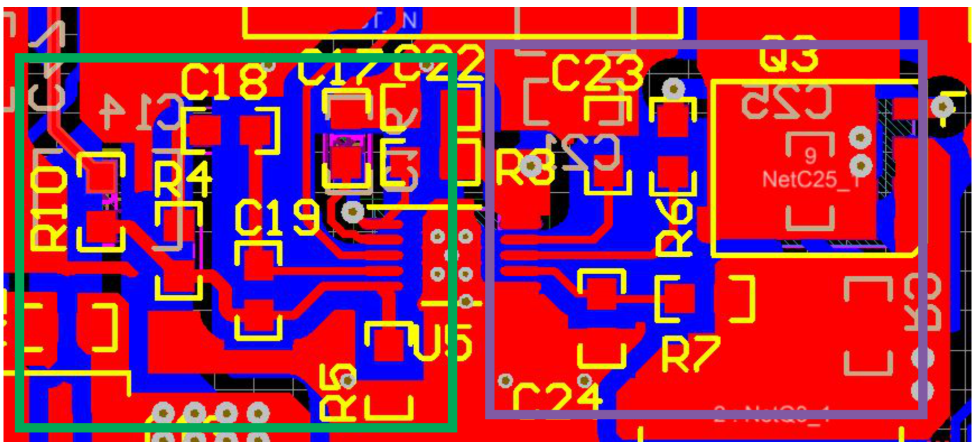
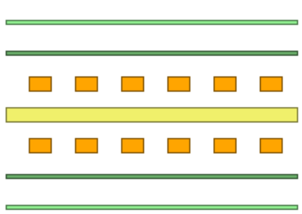


Figure 57. Switching-Converter Routing

9.3.4 PCB Layering Recommendations for 2-Layer Boards

Most LED driver boards in practice are 2-layer boards because of cost. Figure 58 is the stackup used in this board. TI recommends a 1.5-mm 2-layer FR4.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation
Top Overlay	Overlay						
Top Solder	Solder Mask/...	Surface Mat...	0.4	Solder Resist	3.5		
Top Layer	Signal	Copper	1.4				Top
Dielectric1	Dielectric	Core	59.2	FR-4	4.8		
Bottom Layer	Signal	Copper	1.4				Bottom
Bottom Solder	Solder Mask/...	Surface Mat...	0.4	Solder Resist	3.5		
Bottom Over...	Overlay						

Figure 58. Layer Stackup of the LED Board

9.3.5 General Power-Supply Considerations

Input capacitors should be placed as close to the IC as possible to reduce the parasitic-series inductance from the capacitor to the device it is supplying. Place the input capacitors in order of ascending size and value, with the smallest capacitor closest to the device input pin (see C44 and C39 in Figure 59.

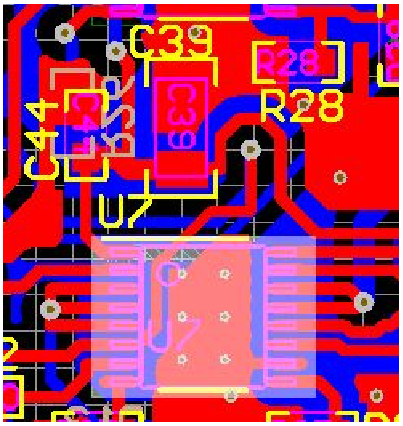


Figure 59. Input and Output Capacitor Placement

9.3.6 GND Pour and Via Stitching

Use a solid GND fill at the top and bottom layer with via stitching to keep current loops as short as possible and to improve thermals (see Figure 60).

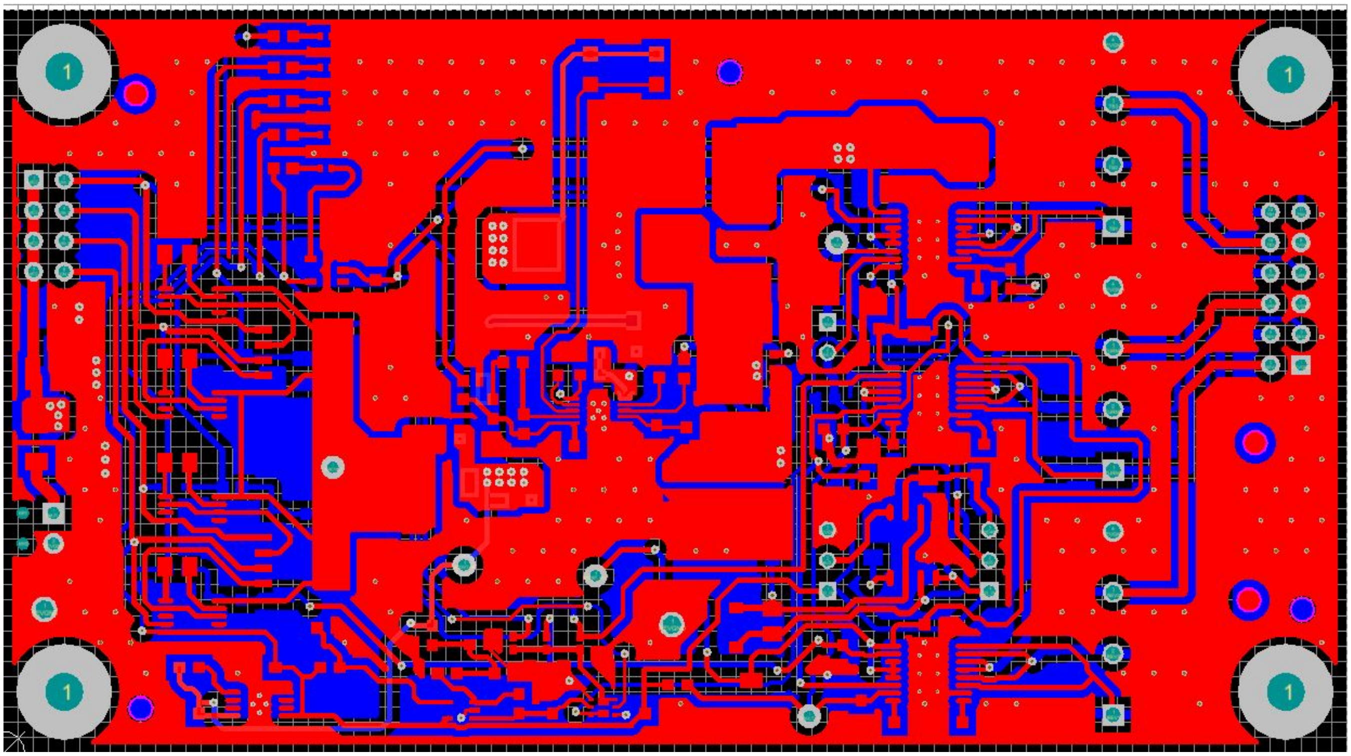
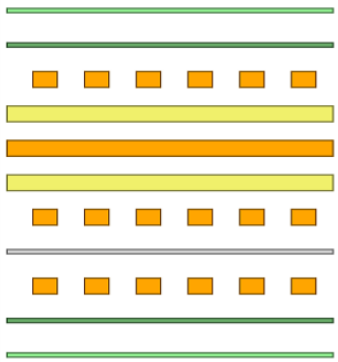


Figure 60. Solid GND Fill

9.3.7 PCB Layering Recommendations for 4-Layer Boards

If a 4-layer board is used, layer two should be a ground plane. Because most of the components and switching currents are on the top layer, the inductive effect of the vias is reduced when currents are returned through the plane. Figure 61 shows the layer stackup of a 4-layer board.



Layer Name	Type	Material	Thickness (mil)
Top Overlay	Overlay		
Top Solder	Solder Mask/...	Surface Mat...	0.4
Top Layer	Signal	Copper	1.4
Dielectric1	Dielectric	Core	59.2
Internal Plan...	Internal Plane	Copper	1.417
Dielectric 2	Dielectric	Core	10
Signal Layer 1	Signal	Copper	1.417
Dielectric 3	Dielectric	Prepreg	5
Bottom Layer	Signal	Copper	1.4
Bottom Solder	Solder Mask/...	Surface Mat...	0.4
Bottom Over...	Overlay		

Figure 61. Layer Stackup

9.4 *Layout Prints*

To download the layout prints for each board, see the design files at TIDA-00678.

9.5 *Altium Project*

To download the Altium project files, see the design files at TIDA-00678.

9.6 *Gerber Files*

To download the Gerber files, see the design files at TIDA-00678.

10 Software Files

To download the software files, see the design files at TIDA-00678.

11 References

1. CISPR 25, Edition 3.0 2008-03, *Vehicles, Boats and Internal Combustion Engines – Radio Disturbance Characteristics – Limits and Methods of Measurement for the Protection of On-Board Receivers*
2. ISO 16750-2:2010 *Road Vehicles – Environmental Conditions and Testing for Electrical and Electronic Equipment – Part 2: Electrical Loads*, section 4.6
3. ISO 7637-2:2004 *Road Vehicles – Electrical Disturbances From Conduction and Coupling – Part 2: Electrical Transient Conduction Along Supply Lines Only*, section 5.6
4. Texas Instruments, *Automotive Three-Channel Linear LED Driver with Analog and PWM Dimming*, Data sheet (SLVSC76)
5. Texas Instruments, *TPS4021x-Q1 4.5-V to 52-V Input, Current-Mode Boost Controllers*, Data sheet (SLVS861)
6. Texas Instruments, *LM74610-Q1 Zero IQ Reverse Polarity Protection Smart Diode Controller*, Data sheet (SNOSCZ1)
7. Texas Instruments, *TLC555-Q1 LinCMOS™ TIMER*, Data sheet (SLFS078)
8. Texas Instruments, *CSD18531Q5A 60 V N-Channel NexFET™ Power MOSFET*, Data sheet (SLPS321)
9. Texas Instruments, *TPS7A16xx-Q1 60-V, 5-μA I Q , 100-mA, Low-Dropout Voltage Regulator With Enable and Power-Good*, Data sheet (SBVS188)
10. Texas Instruments, *AN-2155 Layout Tips for EMI Reduction in DC / DC Converters*, Application note (SNVA638)
11. Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*, Application note (SNVA489)
12. Texas Instruments, *Automotive Wide Vin power frontend with cold crank operation, transient protection, and EMI filter*, Application note (TIDUB49)

12 About the Author

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2016) to A Revision	Page
• Updated product-folder links	1
• Updated TPS92630-Q1 3-Channel LED Driver schematic	33

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