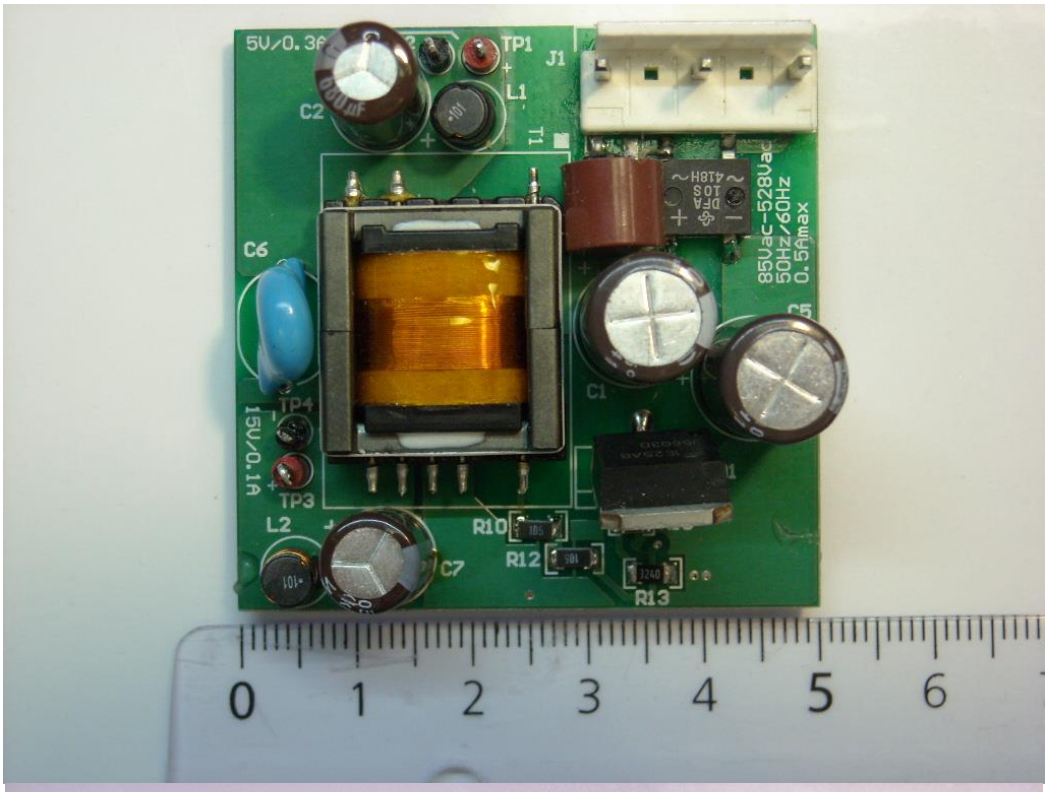
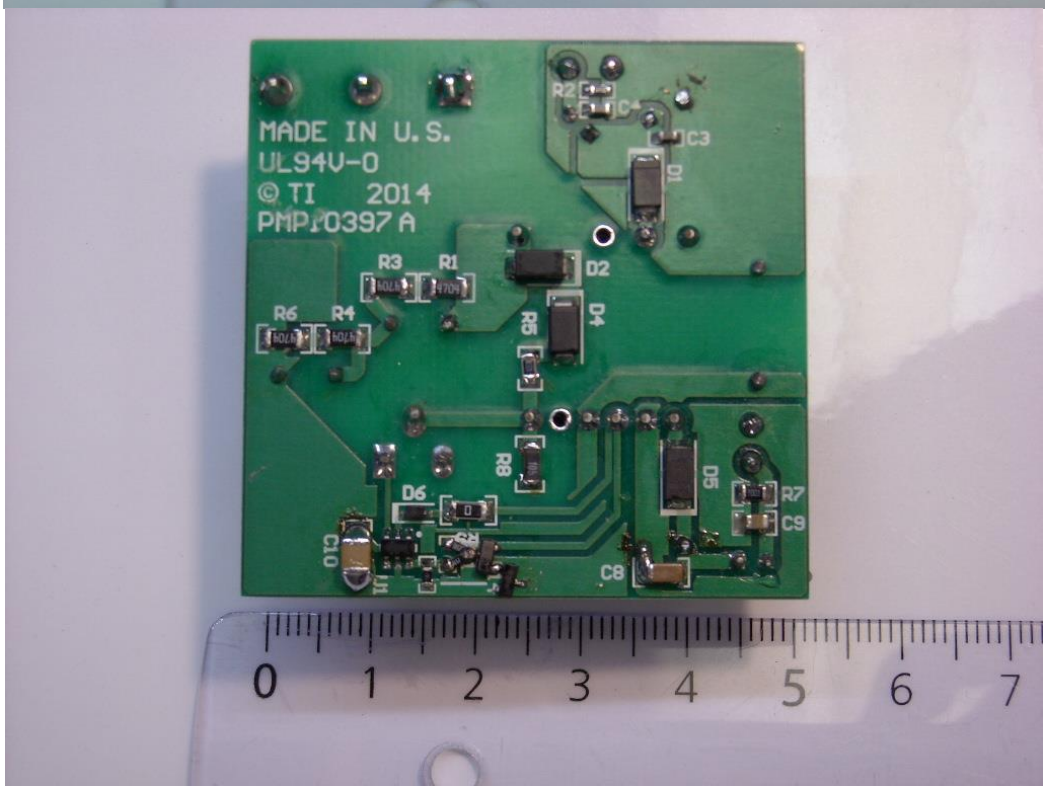
1 Photo of the prototype: the PCB used for this design is the same as the PCB of PMP10397 Rev_A

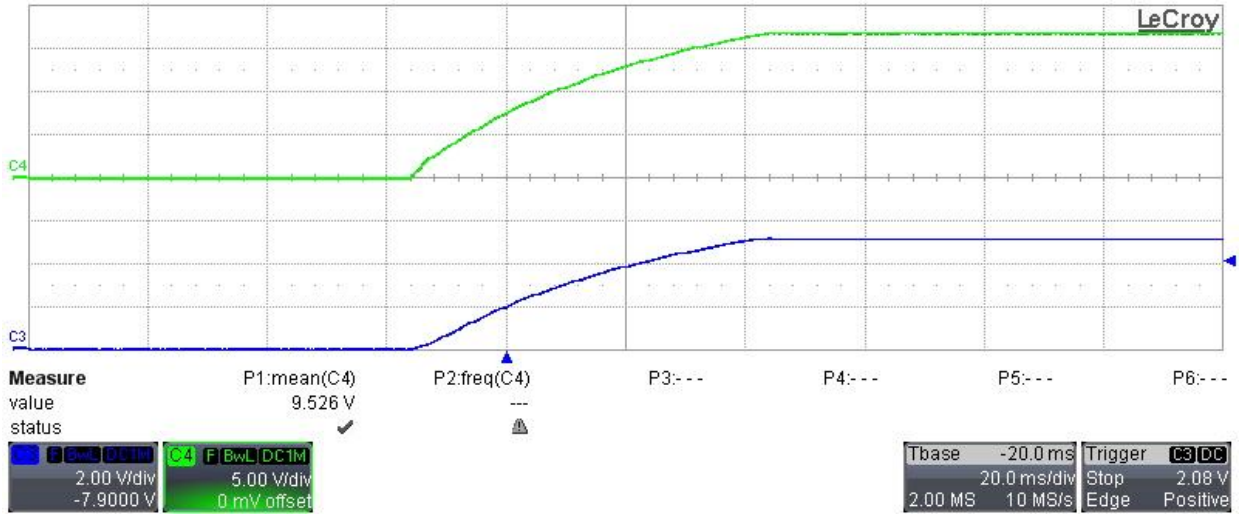


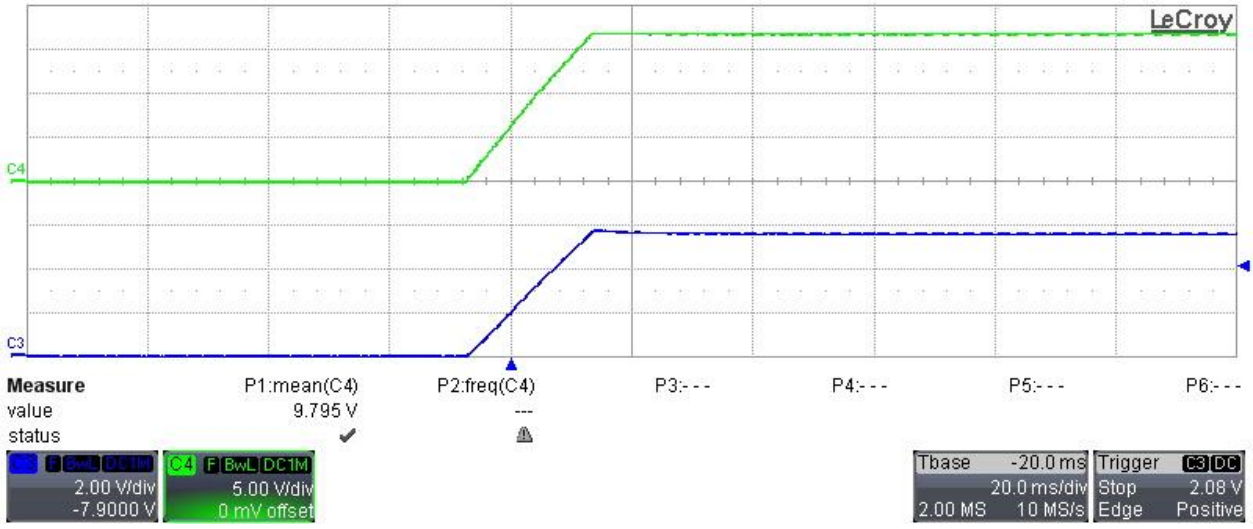


2 Startup

The output voltage behavior for 5V and 15V outputs is shown in the images below. The input voltage was set to 325Vdc. The outputs were fully loaded for the upper picture and unloaded for the bottom one.

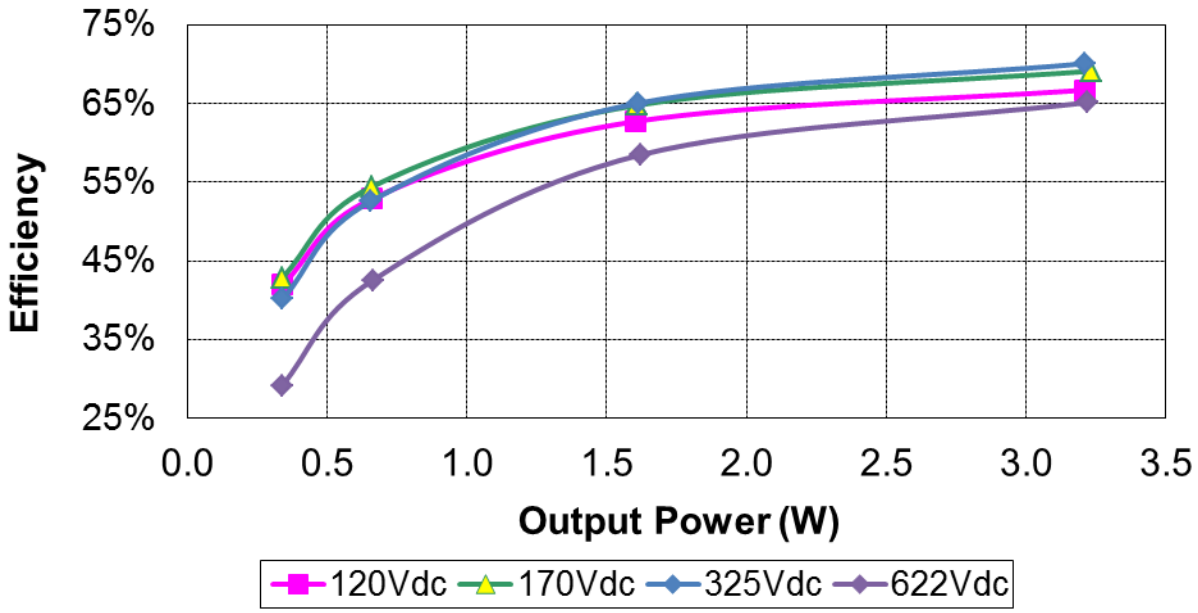
Ch.3: 5V Output (2V/div, 20ms/div, 20MHz BWL)
Ch.4: 15V Output (5V/div, 20MHz BWL)





3 Efficiency

The efficiency data are shown in the tables and graphs below.
The input voltage has been set to DC peak value of 85Vac, 120Vac, 230Vac and 440Vac, respectively equivalent to 120Vdc, 170Vdc, 325Vdc and 622Vdc. Both outputs have been loaded from 0 to full load proportionally.



Vin (V)	Iin (mA)	V5 (V)	I5 (mA)	V15 (V)	I15(mA)	Pout (W)	Pin (W)	Eff. (%)
120	2.46	5.495	0.0	16.74	0.0	0.00	0.30	0.0%
120	6.79	5.287	32.4	16.73	10.2	0.34	0.81	42.0%
120	10.39	5.228	61.8	16.71	20.1	0.66	1.25	52.9%
120	21.31	5.139	150.0	16.66	50.0	1.60	2.56	62.7%
120	40.09	5.072	302.3	16.64	100.7	3.21	4.81	66.7%

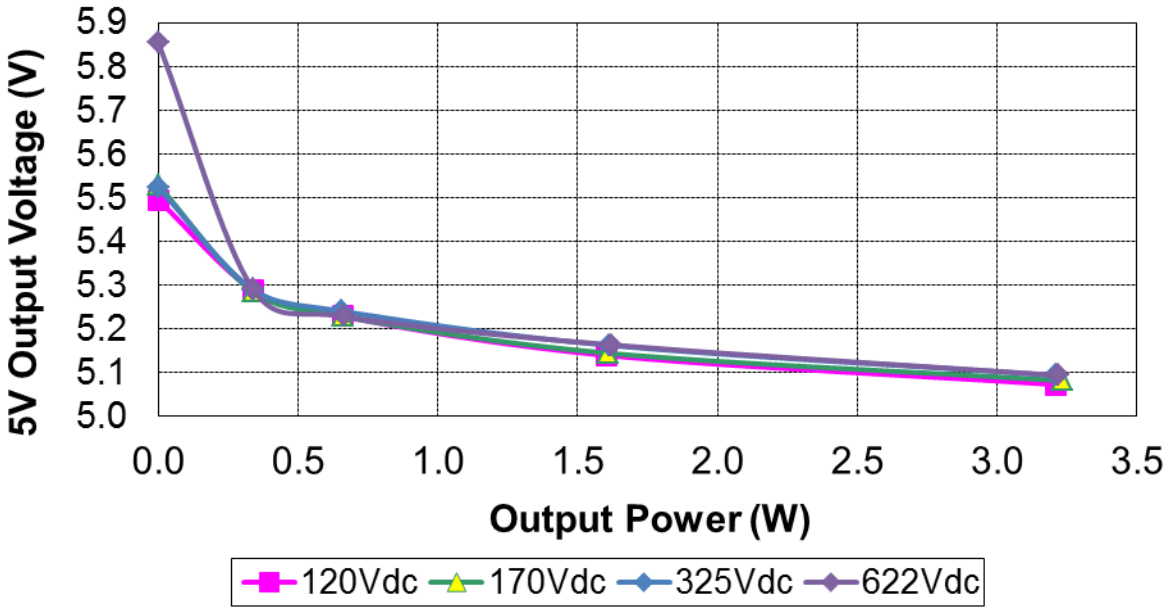
Vin (V)	Iin (mA)	V5 (V)	I5 (mA)	V15 (V)	I15(mA)	Pout (W)	Pin (W)	Eff. (%)
170	1.76	5.529	0.0	16.78	0.0	0.00	0.30	0.0%
170	4.65	5.285	32.4	16.72	10.0	0.34	0.79	42.8%
170	7.14	5.228	61.8	16.70	20.2	0.66	1.21	54.4%
170	14.62	5.144	150.0	16.67	50.3	1.61	2.49	64.8%
170	27.52	5.081	302.4	16.66	101.9	3.23	4.68	69.1%

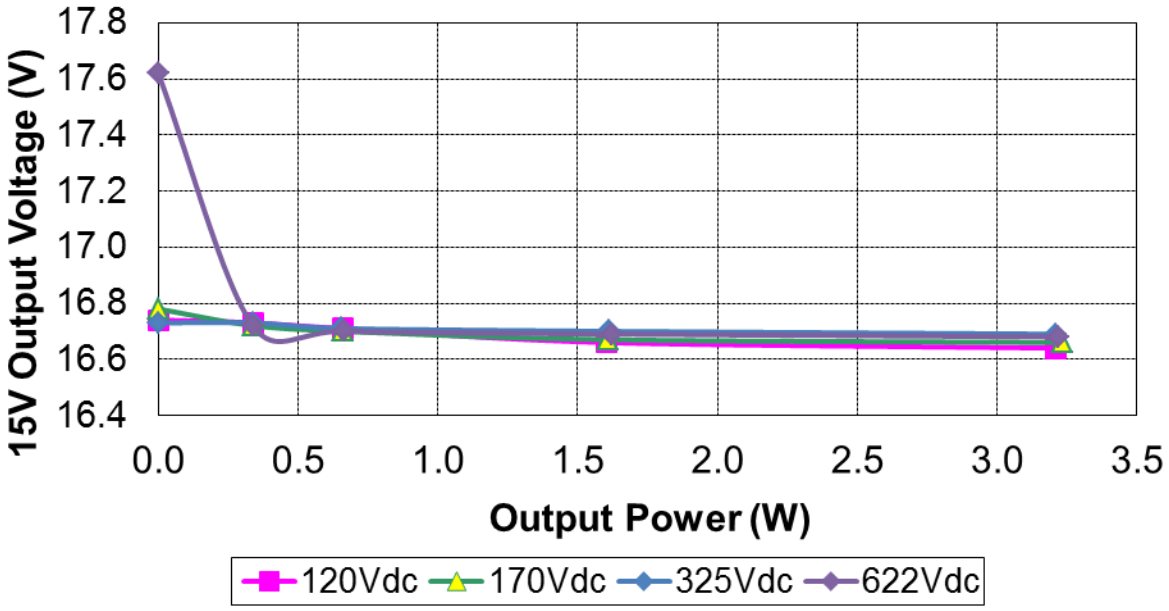
Vin (V)	Iin (mA)	V5 (V)	I5 (mA)	V15 (V)	I15(mA)	Pout (W)	Pin (W)	Eff. (%)
325	1.03	5.523	0.0	16.73	0.0	0.00	0.33	0.0%
325	2.61	5.289	32.4	16.73	10.1	0.34	0.85	40.1%
325	3.85	5.240	61.8	16.71	20.0	0.66	1.25	52.6%
325	7.63	5.162	150.0	16.70	50.2	1.61	2.48	65.0%
325	14.09	5.093	302.3	16.69	100.0	3.21	4.58	70.1%

Vin (V)	Iin (mA)	V5 (V)	I5 (mA)	V15 (V)	I15(mA)	Pout (W)	Pin (W)	Eff. (%)
622	0.922	5.855	0.0	17.62	0.0	0.00	0.57	0.0%
622	1.87	5.291	32.4	16.72	10.0	0.34	1.16	29.1%
622	2.51	5.228	61.8	16.70	20.4	0.66	1.56	42.5%
622	4.46	5.163	150.0	16.69	50.8	1.62	2.77	58.5%
622	7.95	5.093	302.3	16.68	100.8	3.22	4.94	65.1%

4 Output Voltage Regulation versus Output Power

The output voltage variation versus total load, for the four input voltages, is plotted below.





5 Cross Regulation

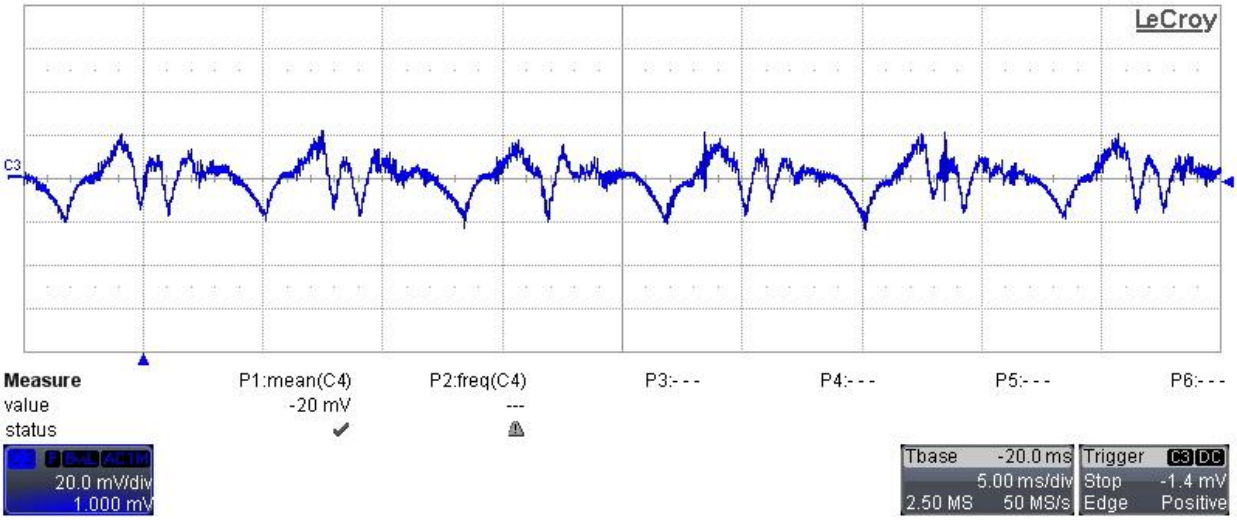
The output voltage variation, by unbalancing the outputs, has been measured with the converter supplied at 325Vdc. The results are shown in the table below:

5V Current	15V Current	5V Voltage	15V Voltage
50mA	0	5.099V	16.88V
300mA	100mA	5.093V	16.69V
300mA	0	5.046V	18.38V
50mA	100mA	6.057V	16.67V

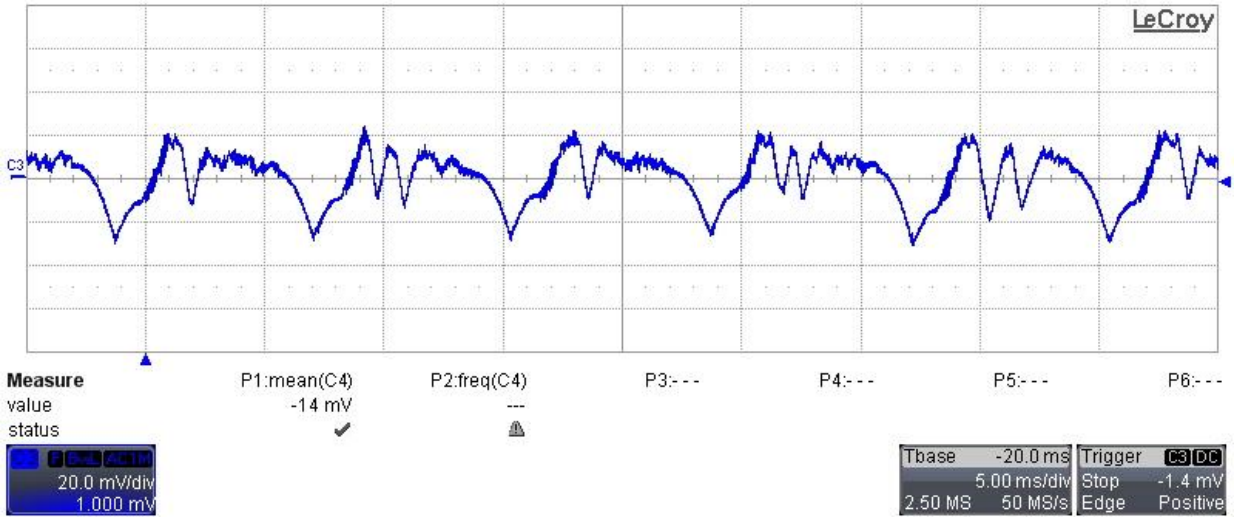
6 Output Ripple Voltage

The output ripple voltage on both outputs have been measured by supplying the converter @ 85Vac, 60Hz (worst case) and 325Vdc with both outputs fully loaded (20MHz BWL for all waveforms).

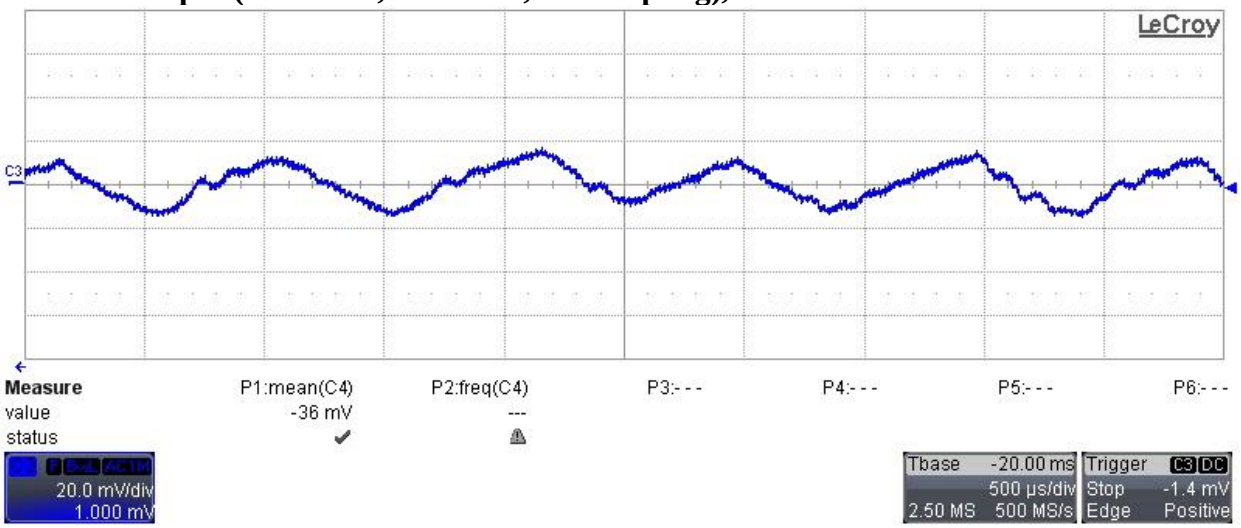
Ch.3: 5V Output (20mV/div, 5ms/div, AC coupling), Vin = 85Vac, 60Hz



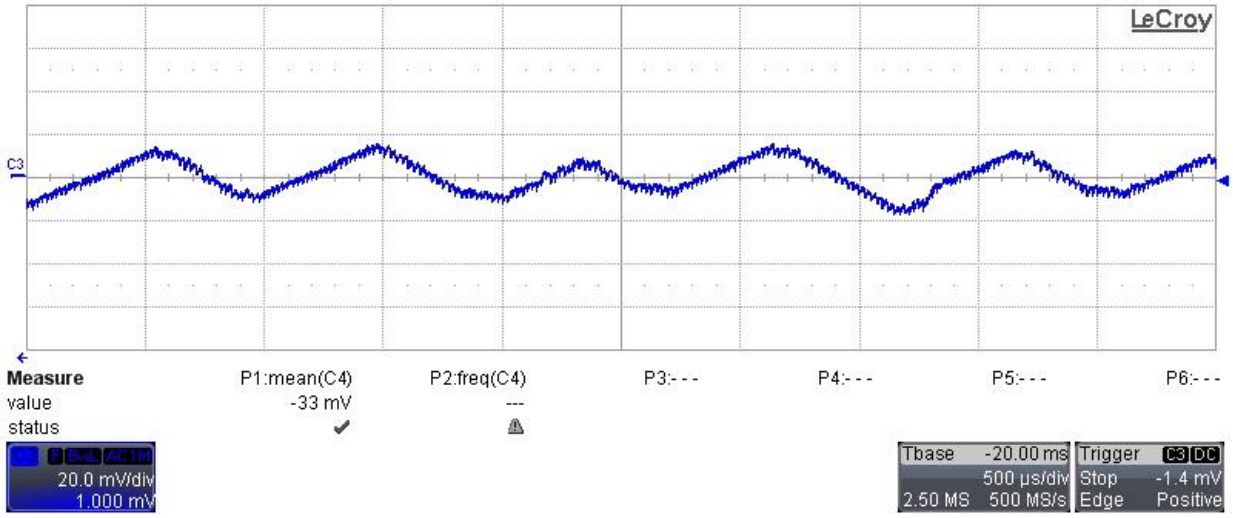
Ch.3: 15V Output (20mV/div, 5ms/div, AC coupling), Vin = 85Vac, 60Hz



Ch.3: 5V Output (20mV/div, 500us/div, AC coupling), Vin = 325Vdc



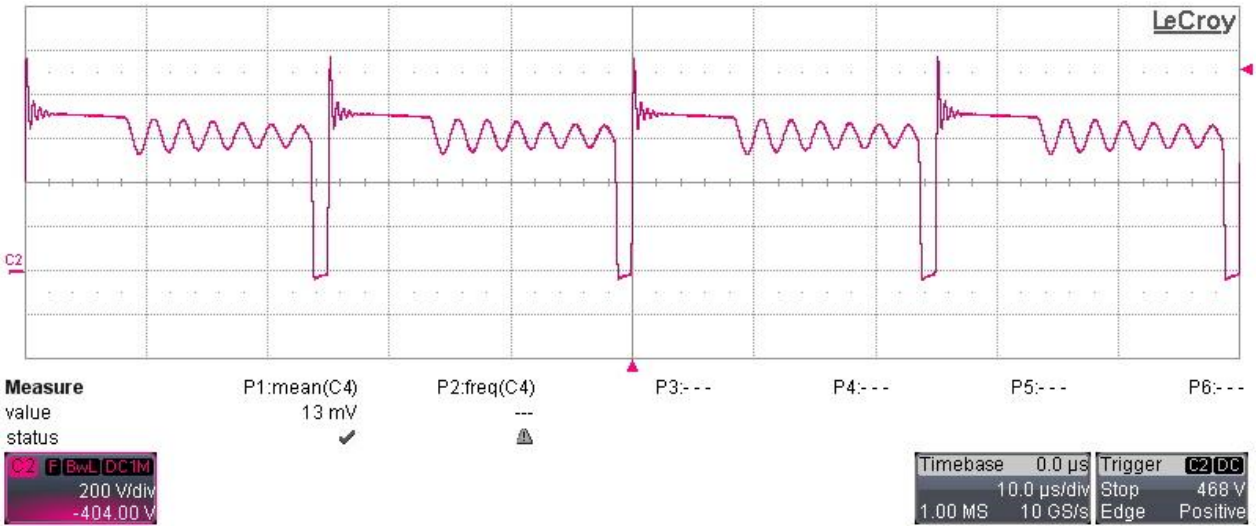
Ch.3: 15V Output (20mV/div, 500us/div, AC coupling), Vin = 325Vdc



7 Switch-node

The image below shows the collector voltage of Q1, taken at 622Vdc input and full load on both outputs.

Ch.2: Q1 Collector Voltage (200V/div, 10us/div, DC coupling, 200MHz BWL)



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