PMP10733 Test Results

Test Data

PMP10733

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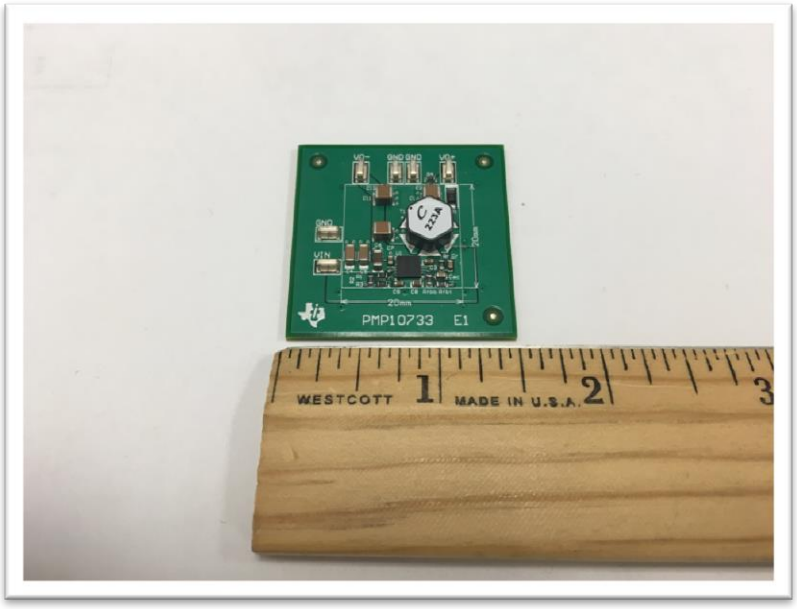
Circuit Description

PMP10733 uses the LM5160 in a Fly-Buck-Boost topology with the primary set as to a negative voltage. Setting the primary side to a negative voltage reduces the turn's ratio of the transformer and yield better line and load regulation as a result. The primary and secondary voltages are set to negative 15V and positive 15V respectively. The maximum operating current on the primary and secondary rails are set to 150mA. The switching frequency is set to 200 kHz.

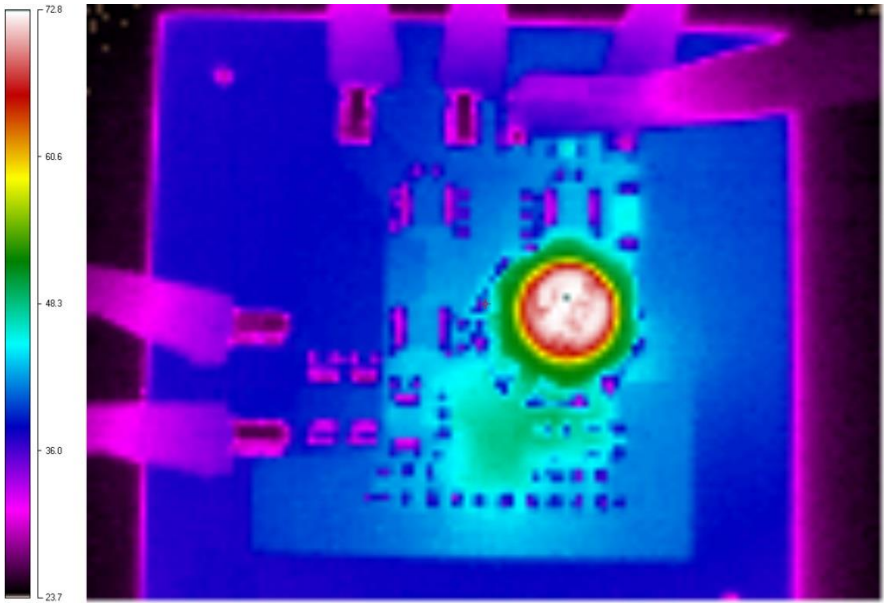
Power Specification

VIN Min.	**5-V**
VIN Max.	**20-V**
$V_{OUT,PRI}$	**-15-V**
$V_{OUT,SEC}$	**15-V**
$I_{OUT,PRI}$	**0-A-0.15-A**
$I_{OUT,SEC}$	**0-A-0.15-A**
Approximate Switching Frequency	**≈200 KHz**

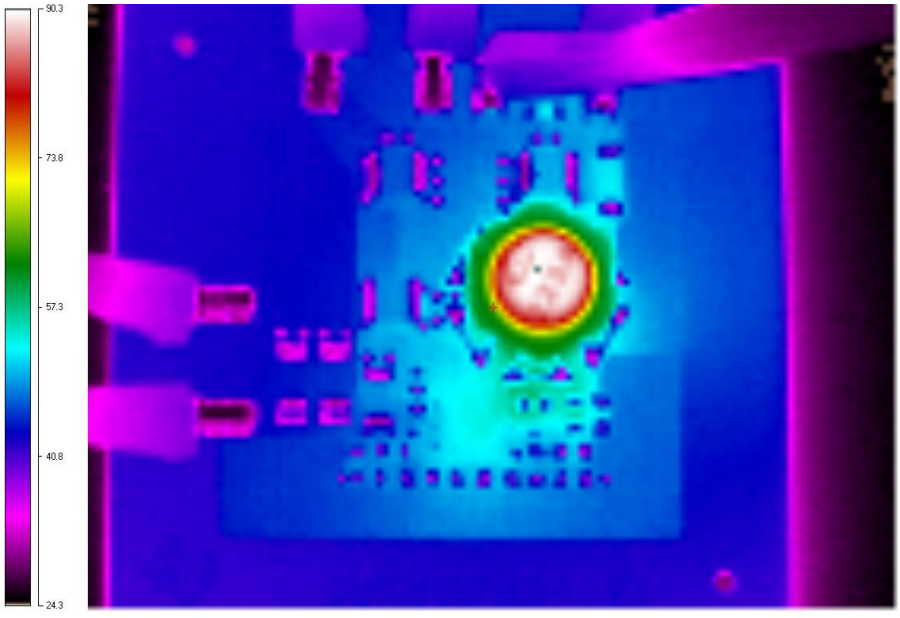
Board Photo (with LM5160)



Thermal Image of the EVM at 12VIN &I_{PRI}=I_{SEC}=0.15A



Thermal Image of the EVM at 20VIN &I_{PRI}=I_{SEC}=0.15A



Efficiency Data

The efficiency is calculated here for both outputs.

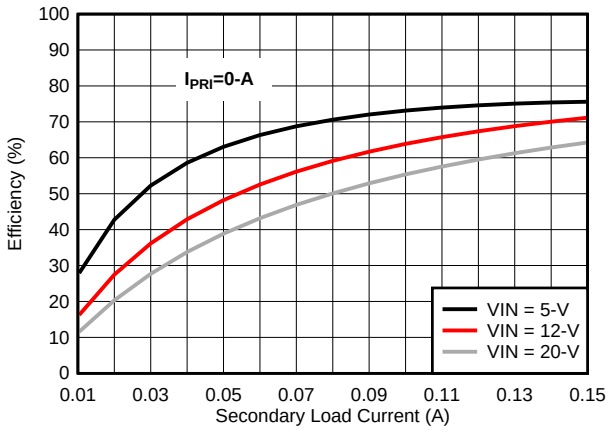


Figure 1. Efficiency with I_{PRI} set at 0A load and I_{SEC} increasing from 0A to 150mA

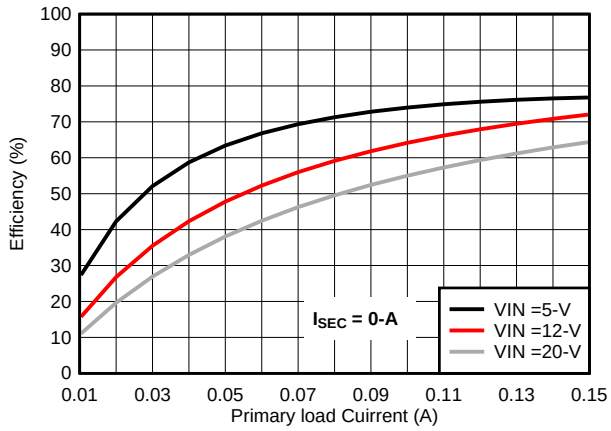


Figure 2. Efficiency with I_{SEC} set at 0A load and I_{PRI} increasing from 0A to 150mA

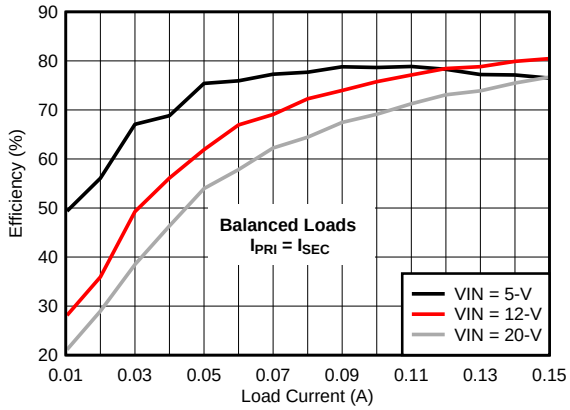


Figure 3. Efficiency with I_{PRI} = I_{SEC} = Load Current increased from 0A to 0.15A on each rail

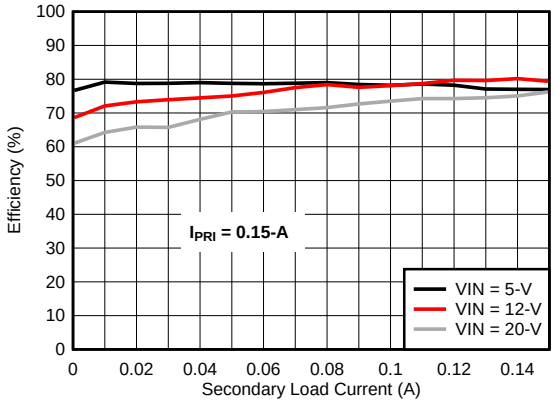


Figure 4. Efficiency with I_{PRI} set at 150mA load and I_{SEC} increasing from 0A to 150mA

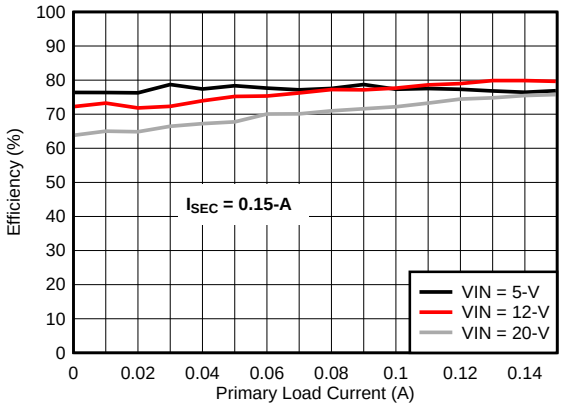


Figure 5. Efficiency with I_{SEC} set at 150mA load and I_{PRI} increasing from 0A to 150mA

Load Regulation Data

Dotted line plots (- - - -) show **modulus V_{PRI}** and the solid line plots show **V_{SEC} (unless specified).**

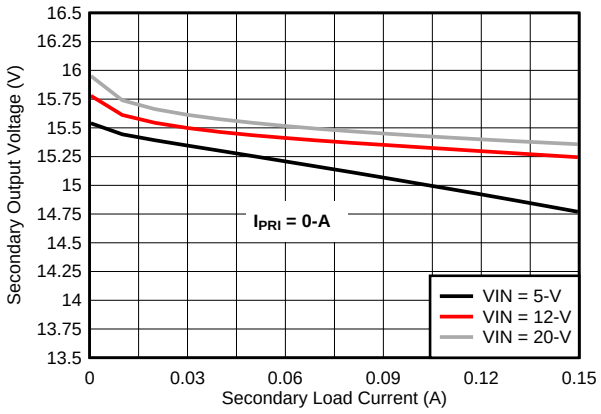


Figure 6. Load Regulation with I_{PRI} set at 0A and I_{SEC} increasing from 0A to 150mA

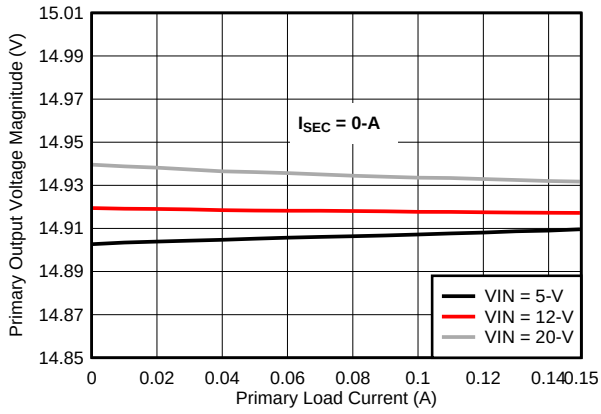


Figure 7. Load Regulation with I_{SEC} set at 0A and I_{PRI} increasing from 0A to 150mA

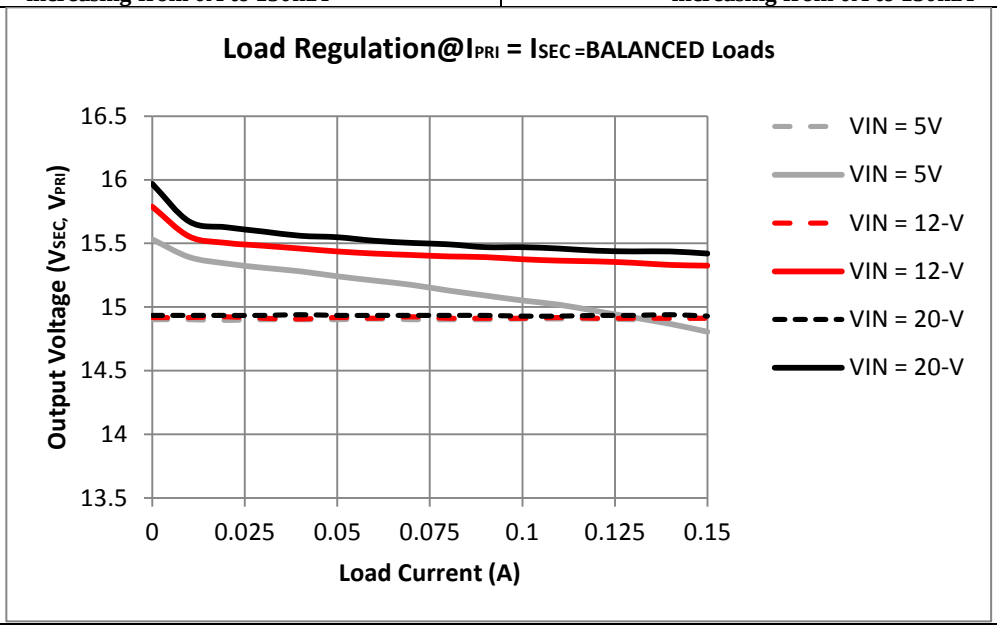


Figure 8. Load Regulation with I_{PRI} = I_{SEC} = Load Current increased from 0A to 0.15A on each rail

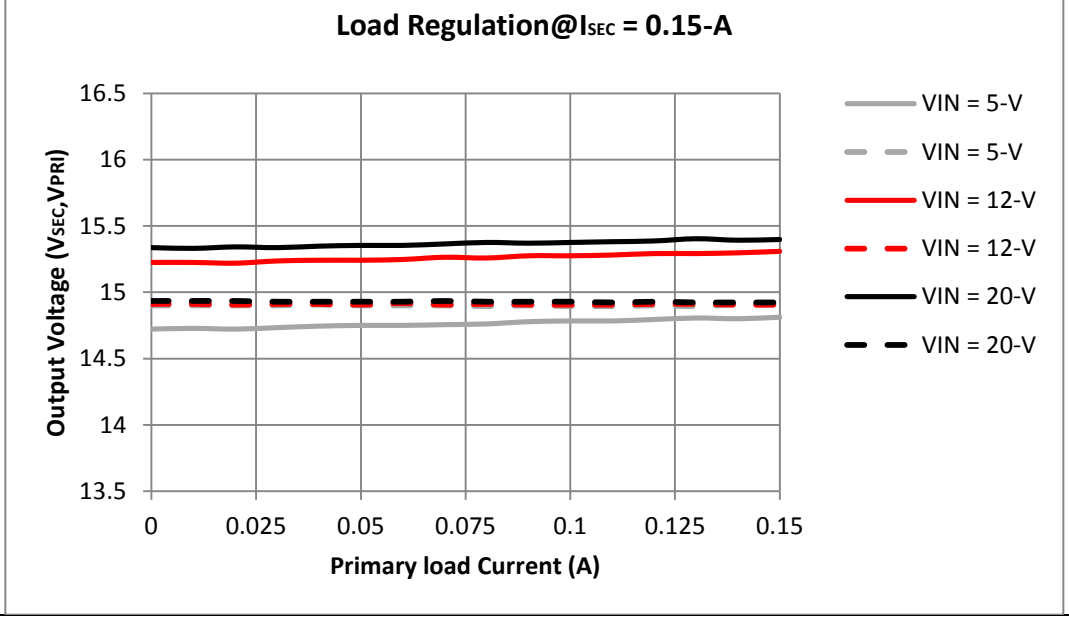


Figure 9. Load Regulation with I_{SEC} set at 150mA load and I_{PRI} increasing from 0A to 150mA

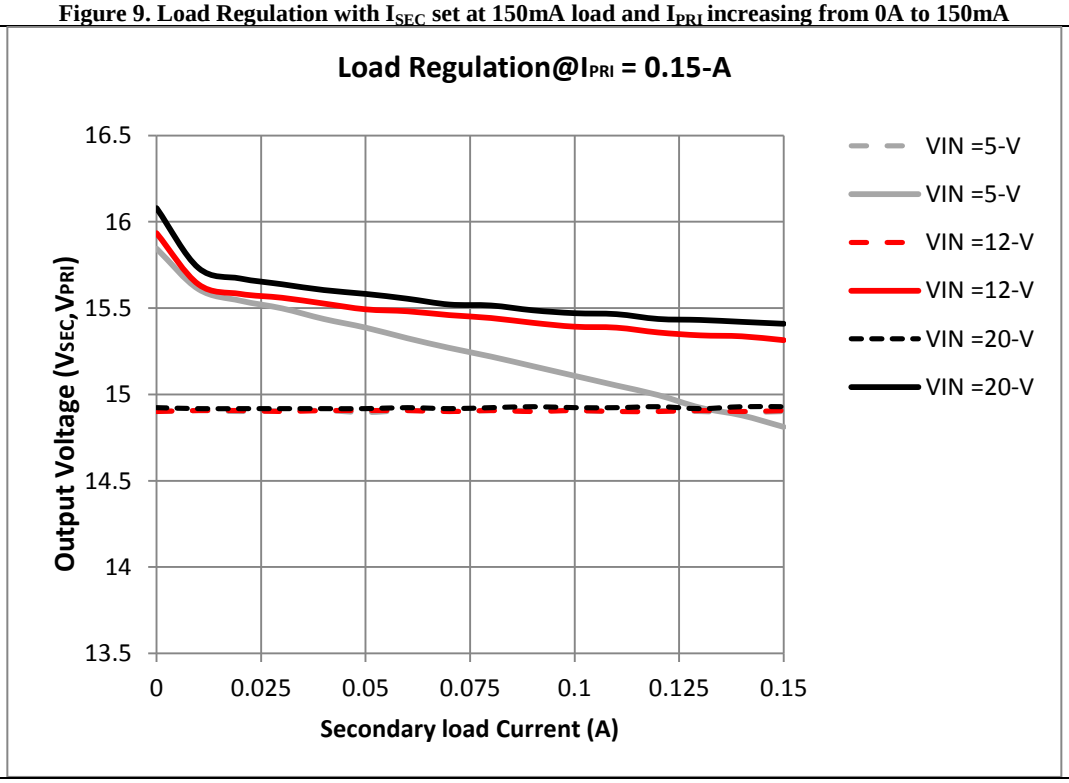
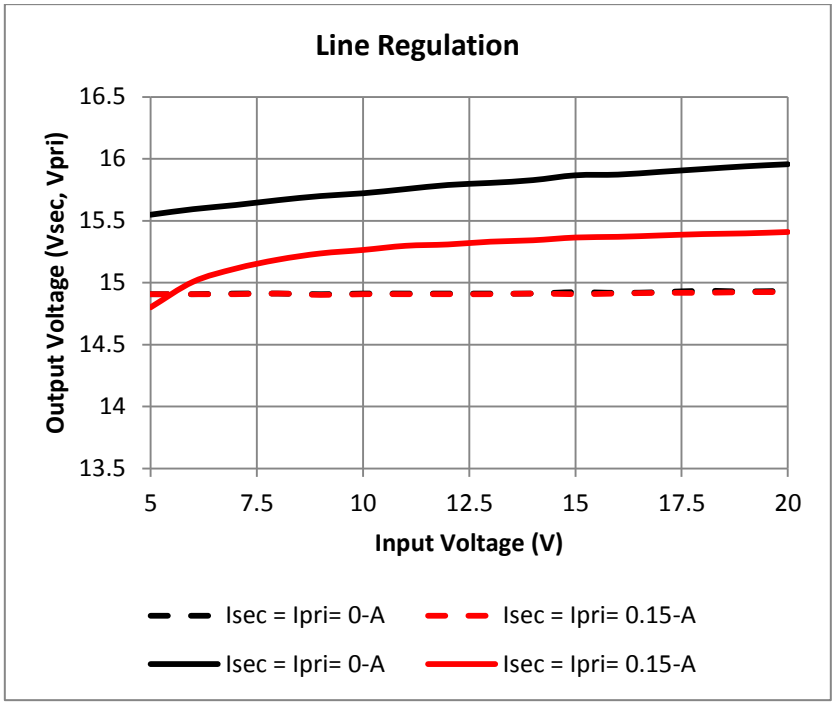
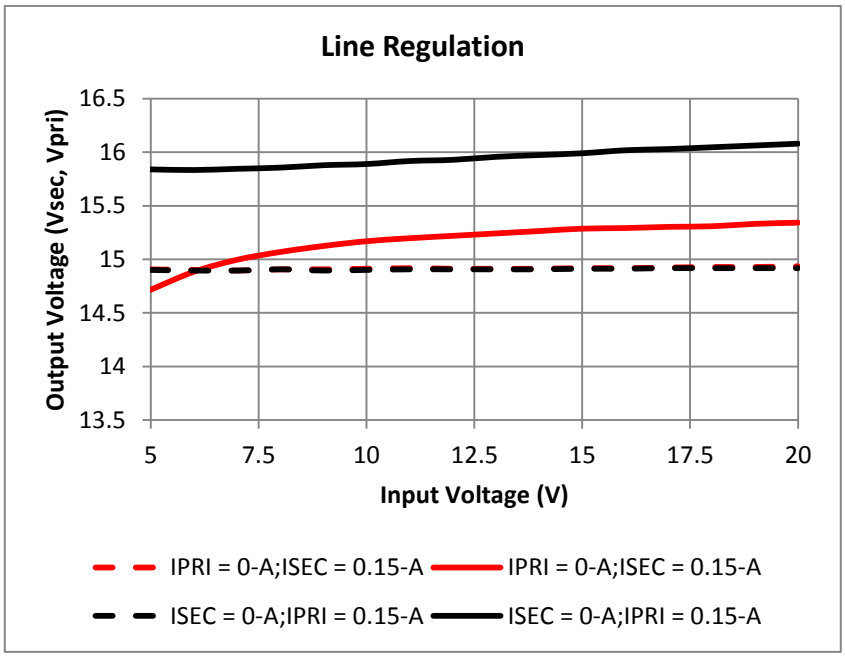


Figure 10. Load Regulation with I_{PRI} set at 150mA load and I_{SEC} increasing from 0A to 150mA

Line Regulation Data

Dotted line plots (- - - -) = **modulus V_{PRI}** and the solid line plots = **V_{SEC} (unless specified).**



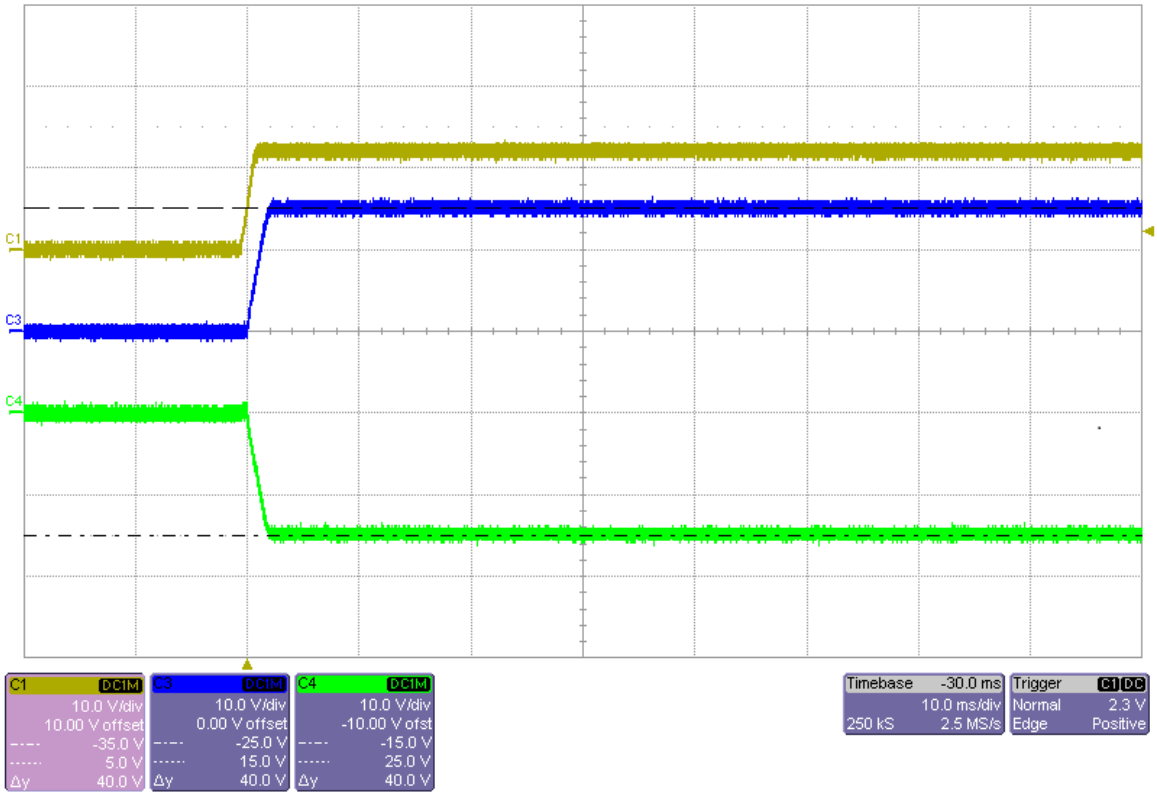


Start Up

Test condition: VIN = 12V, and both outputs were set to full load (150mA on Primary and Secondary).
C1 (Yellow) - VIN

C3 (Blue) –V_{SEC}

C4 (Green) –V_{PRI}



Load Transients

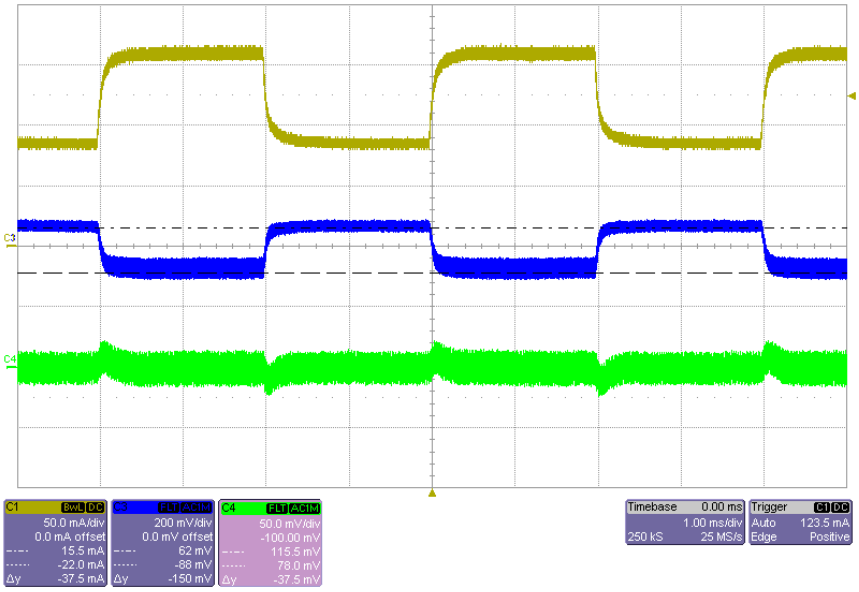
V_{SEC} Load Step

Test condition: VIN = 12V with I_{PRI} set to 0A.

CH1 (Yellow) - I_{SEC} = load step from 75mA to 150mA with slew rate set to 500mA/us

CH3 (Blue) - V_{SEC} (AC coupled); ΔV_{SEC} = 150mV peak to peak

CH4 (Green) - V_{PRI} (AC coupled); ΔV_{PRI} = 25mV peak to peak



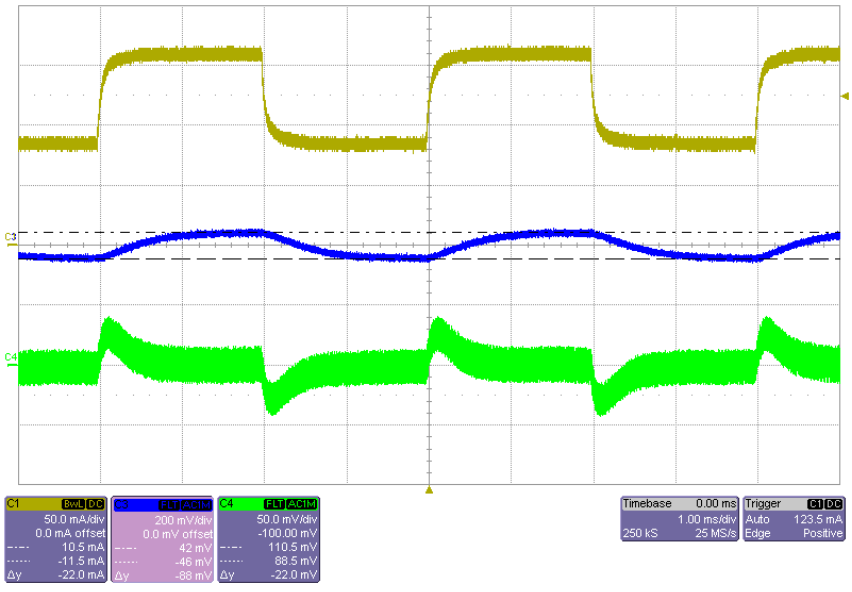
V_{PRI} Load Step

Test condition: VIN = 12V with I_{SEC} set to 0A

CH1 (Yellow) - I_{PRI} = 75mA to 150mA with slew rate set to 500mA/us

CH3 (Blue) - V_{SEC} **(AC coupled);** ΔV_{SEC} = 88mV peak to peak

CH4 (Green) - V_{PRI} **(AC coupled);** ΔV_{PRI} = 50mV peak to peak



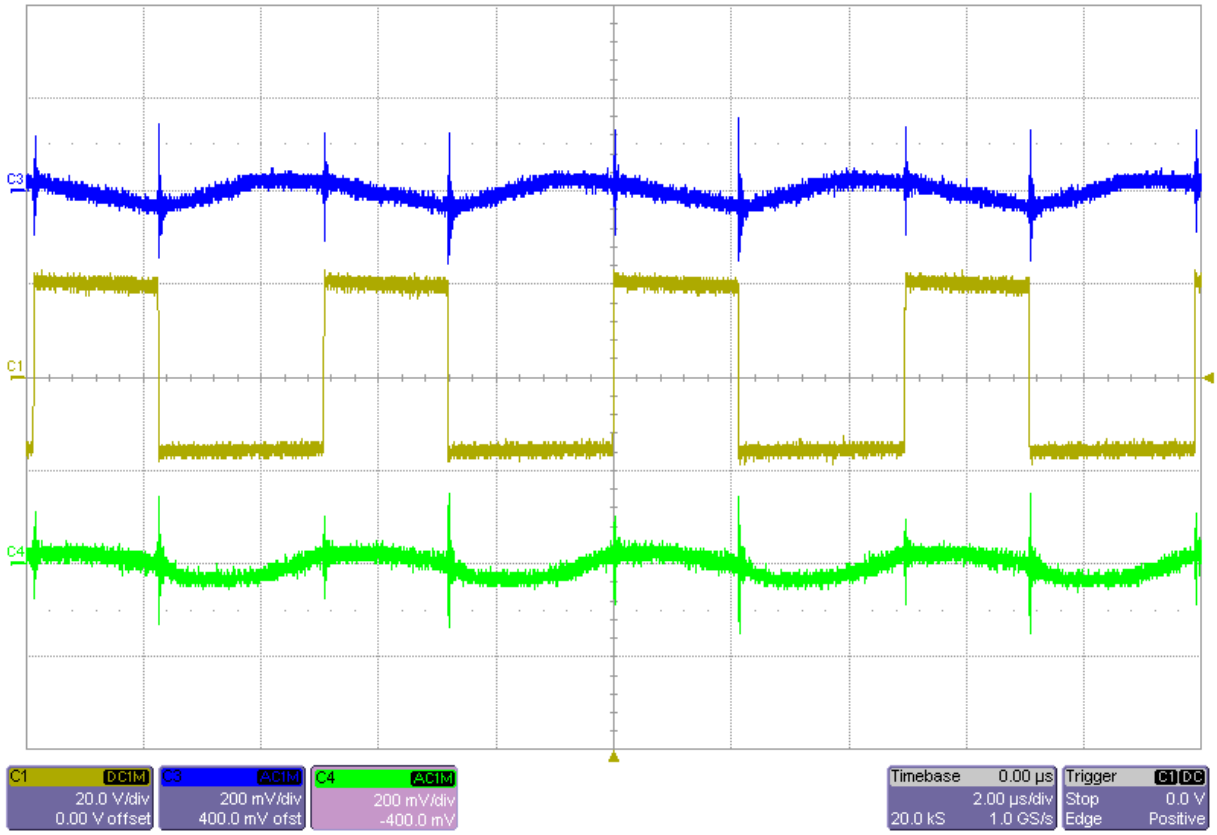
SW Node waveforms and Output Voltage Ripple Waveforms

Test condition: VIN = 20V, and both outputs were set to full load (150mA on Primary and Secondary).

C1 (Yellow) - Switch node

C3 (Blue) - V_{SEC} (AC coupled): ΔV_{SEC} = 100mV peak to peak

C4 (Green)- V_{PRI} (AC coupled): ΔV_{PRI} = 100mV peak to peak



Short Circuit Test

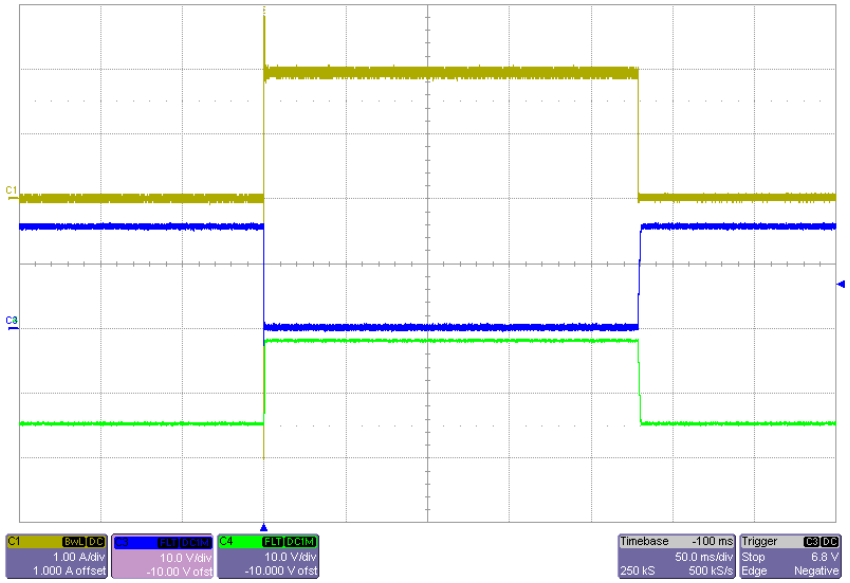
Secondary Side Short Circuit Test

Test condition: VIN = 12V, and both outputs were set to no load (0A on Primary and Secondary).

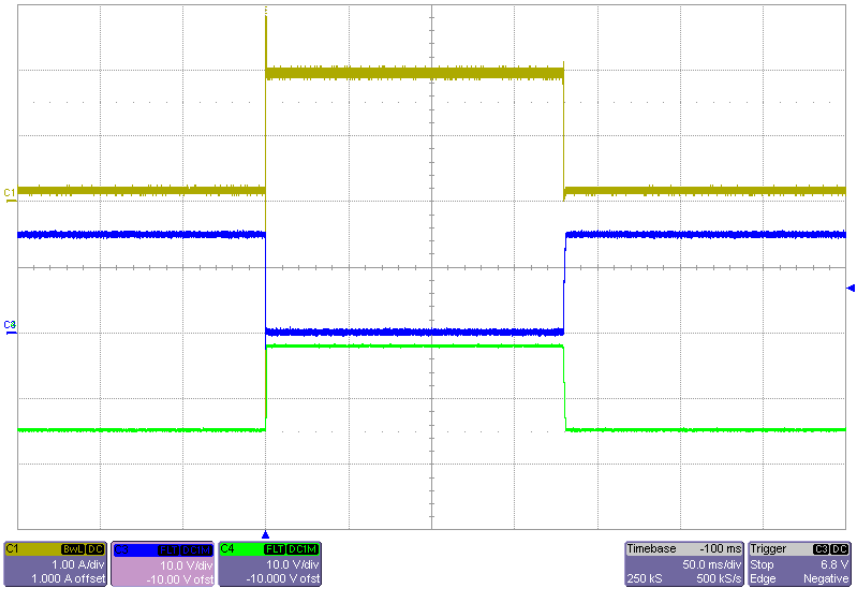
C1 (Yellow) - I_{SEC}

C3 (Blue) - V_{SEC}

C4 (Green) - V_{PRI}



Test condition: VIN = 12V, with I_{SEC} set to 150mA and the I_{PRI} set to 0A.



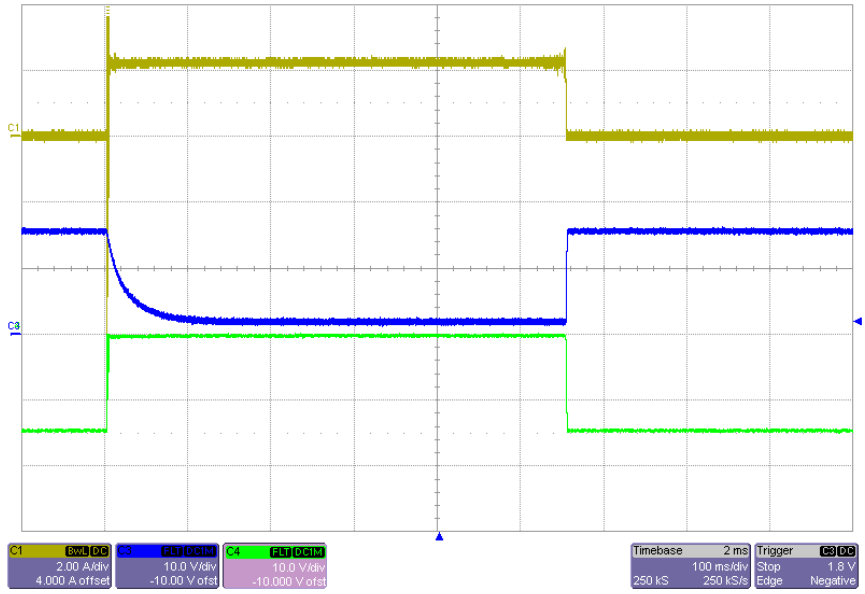
Primary Side Short Circuit Test

Test condition: VIN = 12V, and both outputs were set to no load (0A on Primary and Secondary).

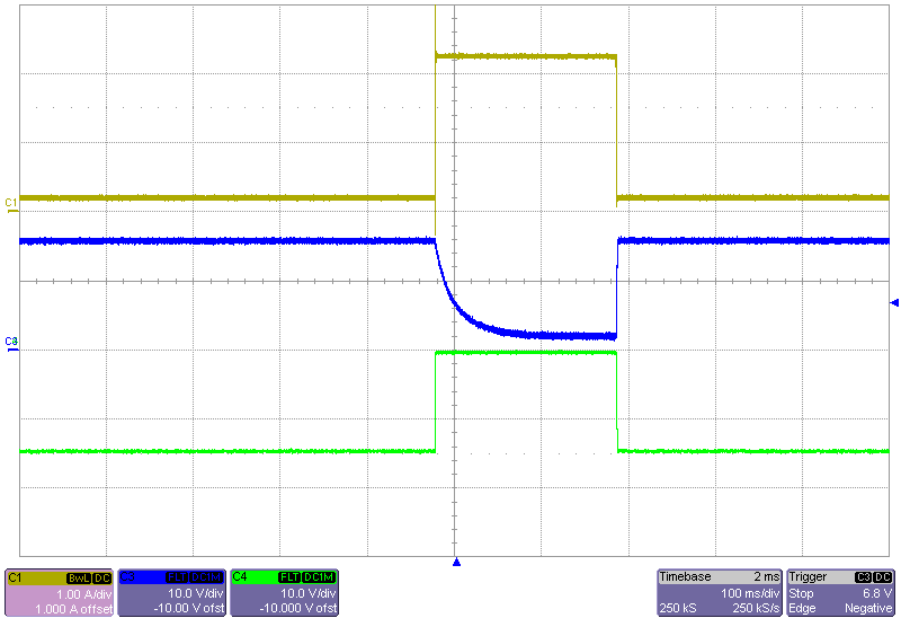
C1 (Yellow) – I_{PRI}

C3 (Blue) - V_{SEC}

C4 (Green) - V_{PRI}



Test condition: VIN = 12V, with I_{PRI} set to 150mA and the I_{SEC} set to 0A.



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