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# *Dynamic Voltage Scaling Power Solution for MSP430™ FRAM Devices With Single Channel LDO Reference Design*

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This TI Design enables power savings for MSP430 FRAM devices or other systems that utilizes a power-on hysteresis. The design uses an adjustable LDO and a RC time delay to switch from a higher start-up voltage to the final low power operating voltage.

## Design Resources

| | |
|---|---|
| TIDA-01172 | Design Folder |
| LP3982 | Product Folder |
| MSP430FR5969 | Product Folder |

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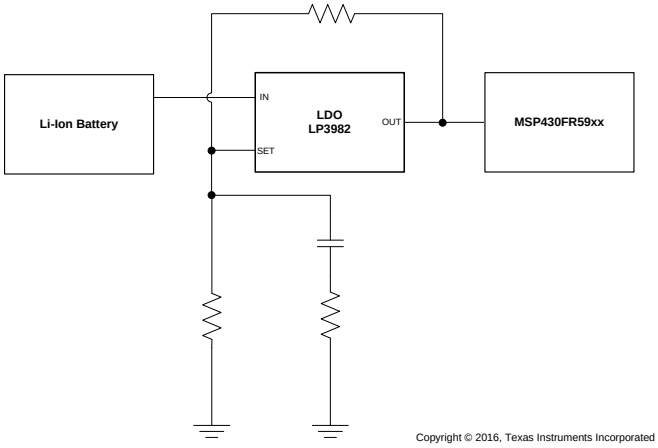
## Design Features

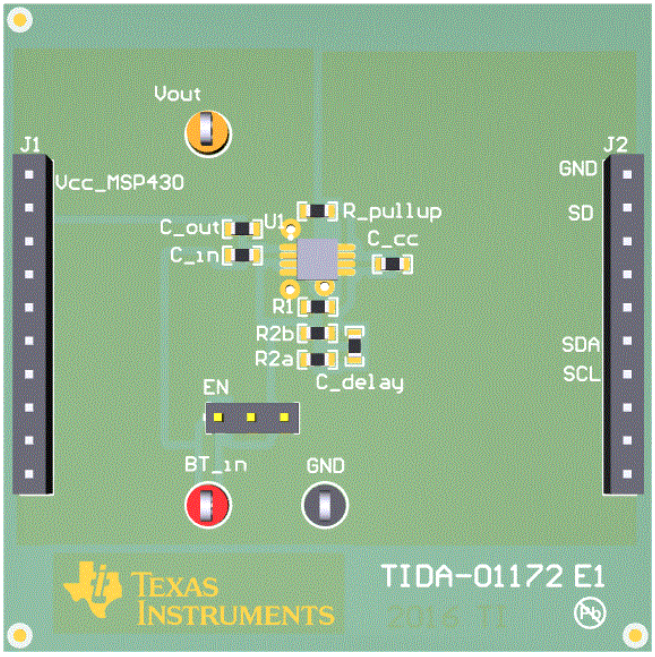
- Low Power Dissipation
- No Additional Active Components Required
- Small Solution Size
- Cost-Optimized Solution
- Ripple-Free and Low-Noise Solution
- TIDA-01172 Provides Design Guide and Design Files of Power Solution

## Featured Applications

- Single Li-Ion Battery Applications
  - Power Supplies of MSP430 FRAM Devices
  - Personal Electronics
  - E-Meter Power Supplies
  - DSP and FPGA Power Supplies
  - Home or Office Security Monitoring



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# 1 Key System Specifications

This TI Design uses the LP3982 to power MSP430 FRAM devices, and Table 1 describes the recommended operating conditions specific to power with which to configure the LP3982 device to supply power to MSP430 FRAM devices. Table 2 describes the characteristics of the LP3982 that are relevant to power MSP430 FRAM devices.

**Table 1. Recommended Operating Conditions for MSP430FR59XX**

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage applied at all DVCC and AVCC pins(1)(2)(3) | 1.8(4) | | 3.6 | V |
| $V_{SS}$ | Supply voltage applied at all DVSS and AVSS pins | | 0 | | V |

(1) TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in the *Absolute Maximum Ratings* table of the MSP430FR5969 data sheet. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

(2) See Table 5-1 in the MSP430FR5969 data sheet for additional important information.

(3) Modules may have a different supply voltage range specification. Refer to the specification of the respective module in the MSP430FR5969 data sheet.

(4) The minimum supply voltage is defined by the supervisor SVS levels. See Table 5 for the exact values.

**Table 2. Design Parameters for LP3982**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Minimum input voltage | $V_{OUT}$ + 0.5 V |
| Nominal output voltage | 3.3 V |
| Maximum output current | 300 mA |
| RMS noise, 10 Hz to 100 kHz | 37 $\mu V_{RMS}$ |
| PSRR at 1 kHz | 60 dB |

This design is specifically targeted to be used for MSP430 FRAM devices that must operate at the lowest operating voltage range. With adjustments to the design voltage levels, this design can also be applied to other MSP430 family devices that may require similar voltage sequences in order to operate at their lowest operating voltages. Refer to the MSP430F5xxx/6xxx, MSP430G2xxx, and MSP430F4xx data sheets to see if this design is applicable and what voltage options are necessary to operate the MSP430 family devices at the lowest operating voltages.

## 2 System Description

This TI Design focuses on the voltage sequence required to operate MSP430 FRAM devices at their lowest operating voltage. This design is not required for general operation of MSP430 FRAM devices or any other MSP430 devices. Figure 1 shows the current required to toggle a single pin on MSP430 FRAM devices on and off and an exponential curve of the current required based on the $V_{CC}$ of the MSP430. This TI design leverages power savings by running MSP430 FRAM devices at the lowest voltage required. However, MSP430 FRAM devices contain a hysteresis feature, which requires it to start up with a higher voltage. Therefore, this design explains how to start the output voltage of the LDO with a higher voltage and switch to a lower voltage to ensure maximum power savings.

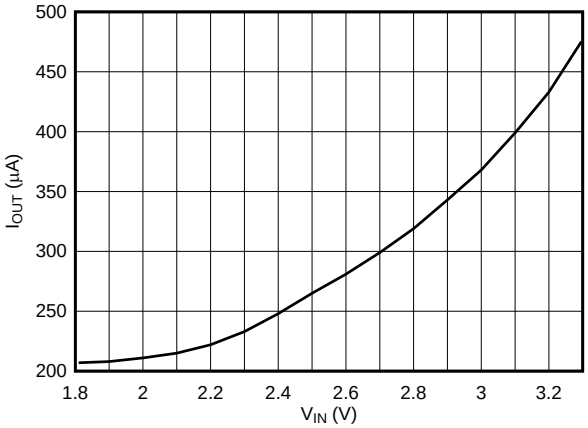


**Figure 1. MSP430 Current Consumption Based on $V_{CC}$**

### 2.1 TI MSP430FR5969

The MSP430 is an ultra-low-power microcontroller that utilizes uniquely embedded FRAM. This is allows users the speed, flexibility, and endurance of SRAM with the stability and reliability of flash at a much lower power. Some of the unique features of the MSP430FR5969 are listed below and a block diagram of these features is shown in Figure 2:

- 16-Bit RISC architecture up to 16-MHz clock
- 64 KB of non-volatile memory
- 66 KB of RAM
- 40 GPIO
- 1 I2C
- 3 SPI
- 2 UART
- 3 DMA
- 12-bit analog-to-digital converter with up to 16 external input channels
- 5 16-bit timers
- Capacitive touch I/O

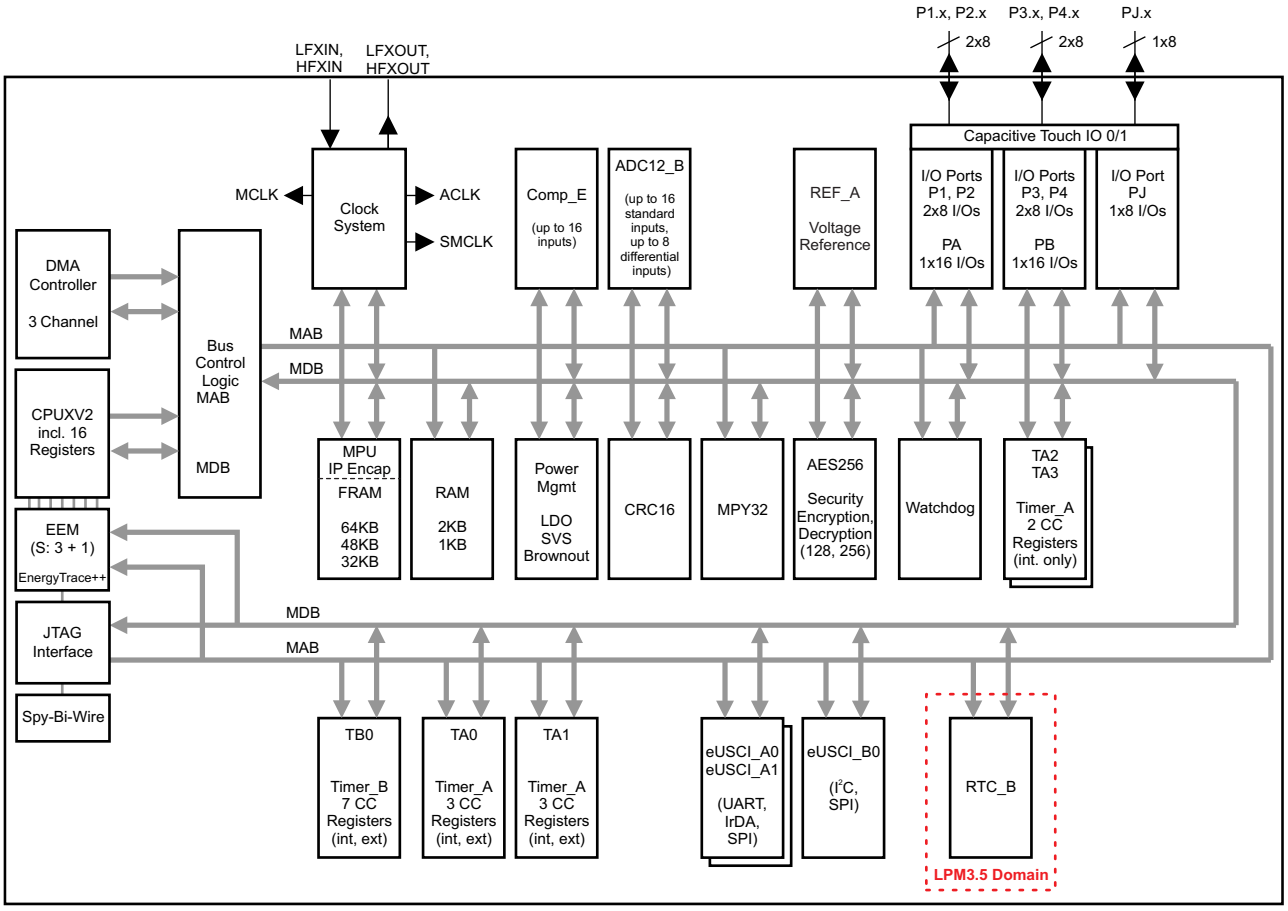




**Figure 2. Block Diagram of MSP430FR5969**

Even with all these features, MSP430 FRAM devices allow a wide supply voltage range from 1.8 V to 3.6 V and requires approximately 100 µA/MHz in active mode. Table 3 describes the required current in detail and provides visual representation.

**Table 3. Active Mode Supply Current Into $V_{CC}$ Excluding External Current for the MSP430™ (1)(2)**

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | FREQUENCY ($f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 MHz 0 wait states (NWAITSx = 0) | | 4 MHz 0 wait states (NWAITSx = 0) | | 8 MHz 0 wait states (NWAITSx = 0) | | 12 MHz 1 wait states (NWAITSx = 1) | | 16 MHz 1 wait states (NWAITSx = 1) | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM,\ FRAM\_UNI}$ (Unified memory) (3) | FRAM | 3 V | 210 | | 640 | | 1220 | | 1475 | | 1845 | | µA |
| $I_{AM,\ FRAM}$(0%) (4)(5) | FRAM 0% cache hit ratio | 3 V | 370 | | 1280 | | 2510 | | 2080 | | 2650 | | µA |
| $I_{AM,\ FRAM}$(50%) (4)(5) | FRAM 50% cache hit ratio | 3 V | 240 | | 745 | | 1440 | | 1575 | | 1990 | | µA |
| $I_{AM,\ FRAM}$(66%) (4)(5) | FRAM 66% cache hit ratio | 3 V | 200 | | 560 | | 1070 | | 1300 | | 1620 | | µA |
| $I_{AM,\ FRAM}$(75%) (4)(5) | FRAM 75% cache hit ratio | 3 V | 170 | 255 | 480 | | 890 | 1085 | 1155 | 1310 | 1420 | 1620 | µA |
| $I_{AM,\ FRAM}$(100%) (4)(5) | FRAM 100% cache hit ratio | 3 V | 110 | | 235 | | 420 | | 640 | | 730 | | µA |
| $I_{AM,\ RAM}$ (6) | RAM | 3 V | 130 | | 320 | | 585 | | 890 | | 1070 | | µA |
| $I_{AM,\ RAM\ only}$ (5)(7) | RAM | 3 V | 100 | 180 | 290 | | 555 | | 860 | | 1040 | 1300 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.

(2) Characterized with program executing typical data processing.
$f_{ACLK}$ = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency, except for 12 MHz. For 12 MHz, $f_{DCO}$= 24 MHz and $f_{MCLK} = f_{SMCLK} = f_{DCO} / 2$.
At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency ($f_{MCLK,eff}$) decreases. The effective MCLK frequency also depends on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio.
The following equation can be used to compute $f_{MCLK,eff}$:
$f_{MCLK,eff} = f_{MCLK}$ / [wait states × (1 - cache hit ratio) + 1]
For example, with 1 wait state and 75% cache hit ratio $f_{MCKL,eff} = f_{MCLK} / [1 \times (1 - 0.75) + 1] = f_{MCLK} / 1.25$.

(3) Represents typical program execution. Program and data reside entirely in FRAM. All execution is from FRAM.

(4) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 75% ratio implies three of every four accesses is from cache, and the remaining are FRAM accesses.

(5) See Figure 3 — each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Table 3.

(6) Program and data reside entirely in RAM. All execution is from RAM.

(7) Program and data reside entirely in RAM. All execution is from RAM. FRAM is off.

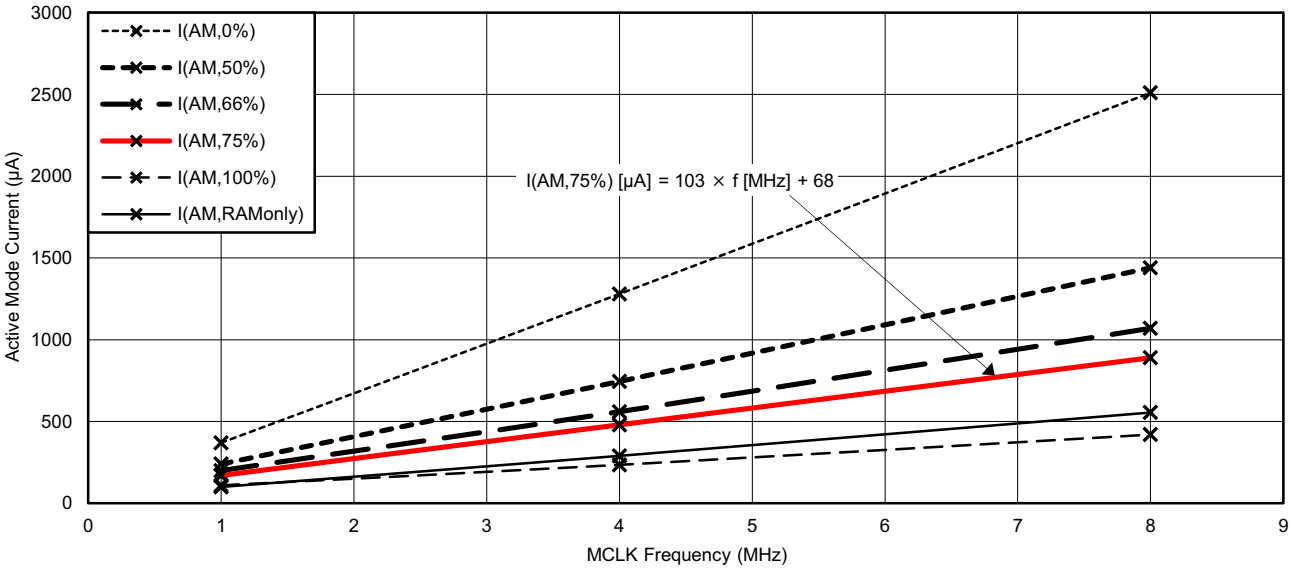


**Figure 3. Typical Characteristics - Active Mode Supply Currents for MSP430**

## 2.2 TI LP3982

The LP3982 device was chosen for its adjustable version with low dropout of 120 mV typical and up to 300 mA of output current. The following features were also put into consideration for this application with the low power MSP430:

- 2.5-V to 6-V input range
- 1-nA typical shutdown mode
- 90-µA typical low quiescent current
- 60-dB typical PSRR
- 37-$\mu V_{RMS}$ output voltage noise
- ±2% output voltage tolerance
- Stable with capacitance Loads of 2.2 µF
- Small package sizes: 2.50 mm × 3.00 mm (WSON) and 3.00 mm × 3.00 mm (VSSOP)

Table 4 provides a more detailed description of the operating characteristics of the LP3982, and Figure 4 shows the functional block diagram of the LP3982 to show how the LDO operates internally.

**Table 4. Operating Characteristics of LP3982**

| PARAMETER | | TEST CONDITIONS | MIN(1) | TYP(2) | MAX(1) | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | For operating temperature extremes: −40°C to 85°C | 2.5 | | 6 | V |
| $\Delta V_{OUT}$ | Output voltage tolerance | 100 µA ≤ $I_{OUT}$ ≤ 300 mA<br>$V_{IN}$ = $V_{OUT}$ + 0.5 V(3)<br>SET = OUT for the ADJ Versions, $T_J$ = 25°C | −2 | | 2 | % of $V_{OUT}$ (NOM) |
| | | For operating temperature extremes: −40°C to 85°C | −3 | | 3 | |
| $V_{OUT}$ | Output adjust range | ADJ version only;<br>for operating temperature extremes: −40°C to 85°C | 1.25 | | 6 | V |

(1) All limits are verified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Condition does not apply to input voltages below 2.5 V because this is the minimum input operating voltage.

**Table 4. Operating Characteristics of LP3982 (continued)**

| PARAMETER | | TEST CONDITIONS | MIN[1] | TYP[2] | MAX[1] | UNIT |
|---|---|---|---|---|---|---|
| $I_{OUT}$ | Maximum output current | Average DC current rating; For operating temperature extremes: −40°C and 85°C | 300 | | | mA |
| $I_{LIMIT}$ | Output current limit | $T_J$ = 25°C | | 770 | | mA |
| | | For operating temperature extremes: −40°C to 85°C | 330 | | | |
| $I_Q$ | Supply current | $I_{OUT}$ = 0 mA, $T_J$ = 25°C | | 90 | | µA |
| | | $I_{OUT}$ = 0 mA for operating temperature extremes: −40°C to 85°C | | | 270 | |
| | | $I_{OUT}$ = 300 mA | | 225 | | |
| | Shutdown supply current | $V_O$ = 0 V, $\overline{SHDN}$ = GND, $T_J$ = 25°C | | 0.001 | 1 | µA |
| $V_{DO}$ | Dropout voltage[3][4] | $I_{OUT}$ = 1 mA, $T_J$ = 25°C | | 0.4 | | mV |
| | | $I_{OUT}$ = 200 mA, $T_J$ = 25°C | | 80 | | |
| | | $I_{OUT}$ = 200 mA for operating temperature extremes: −40°C to 85°C | | | 220 | |
| | | $I_{OUT}$ = 300 mA, $T_J$ = 25°C | | 120 | | |
| $\Delta V_{OUT}$ | Line regulation | $I_{OUT}$ = 1 mA, $T_J$ = 25°C $(V_{OUT} + 0.5\ V) \le V_I \le 6\ V$[3] | | 0.01 | | %/V |
| | | $I_{OUT}$ = 1 mA, $(V_{OUT} + 0.5\ V) \le V_I \le 6\ V$[3]; for operating temperature extremes: −40°C to 85°C | −0.1 | | 0.1 | |
| | Load regulation | 100 µA ≤ $I_{OUT}$ ≤ 300 mA, $T_J$ = 25°C | | 0.002 | | %/mA |
| $e_n$ | Output voltage noise | $I_{OUT}$ = 10 mA, 10 Hz ≤ $f$ ≤ 100 kHz, $T_J$ = 25°C | | 37 | | $\mu V_{RMS}$ |
| | Output voltage noise density | 10 Hz ≤ f ≤ 100 kHz, $C_{OUT}$ = 10 µF, $T_J$ = 25°C | | 190 | | $nV/\sqrt{Hz}$ |
| $V_{\overline{SHDN}}$ | $\overline{SHDN}$ input threshold | $V_{IH}$, $(V_{OUT} + 0.5\ V) \le V_{IN} \le 6\ V$[3]; for operating temperature extremes: −40°C to 85°C | 2 | | | V |
| | | $V_{IL}$, $(V_{OUT} + 0.5\ V) \le V_{IN} \le 6\ V$[3]; for operating temperature extremes: −40°C to 85°C | | | 0.4 | |
| $I_{\overline{SHDN}}$ | $\overline{SHDN}$ input bias current | $\overline{SHDN}$ = GND or IN, $T_J$ = 25°C | | 0.1 | 100 | nA |
| $I_{SET}$ | SET input leakage | SET = 1.3 V, ADJ version only[5] | | 0.1 | 2.5 | nA |
| $V_{\overline{FAULT}}$ | $\overline{FAULT}$ detection voltage | $V_O \ge 2.5\ V$, $I_{OUT}$ = 200 mA, $T_J$ = 25°C[6] | | 120 | | mV |
| | | $V_{OUT} \ge 2.5\ V$, $I_{OUT}$ = 200 mA[6]; for operating temperature extremes: −40°C to 85°C | | | 280 | |
| | $\overline{FAULT}$ output low voltage | $I_{SINK}$ = 2 mA, $T_J$ = 25°C | | 0.115 | | V |
| | | $I_{SINK}$ = 2 mA for operating temperature extremes: −40°C to 85°C | | | 0.25 | |
| $I_{\overline{FAULT}}$ | $\overline{FAULT}$ off-leakage current | $\overline{FAULT}$ = 3.6 V, $\overline{SHDN}$ = 0 V, $T_J$ = 25°C | | 0.1 | 100 | nA |
| $T_{SD}$ | Thermal shutdown temperature | $T_J$ = 25°C | | 160 | | °C |
| | Thermal shutdown hysteresis | $T_J$ = 25°C | | 10 | | |
| $T_{ON}$ | Start-up time | $C_{OUT}$ = 10 µF, $V_{OUT}$ at 90% of final value, $T_J$ = 25°C | | 120 | | µs |

(4) Dropout voltage is measured by reducing $V_{IN}$ until $V_{OUT}$ drops 100 mV from its nominal value at $V_{IN} - V_{OUT}$ = 0.5 V. Dropout voltage does not apply to the 1.8-V version.
(5) The SET pin is not externally connected for the fixed versions.
(6) The $\overline{FAULT}$ detection voltage is specified for the input-to-output voltage differential at which the $\overline{FAULT}$ pin goes active low.

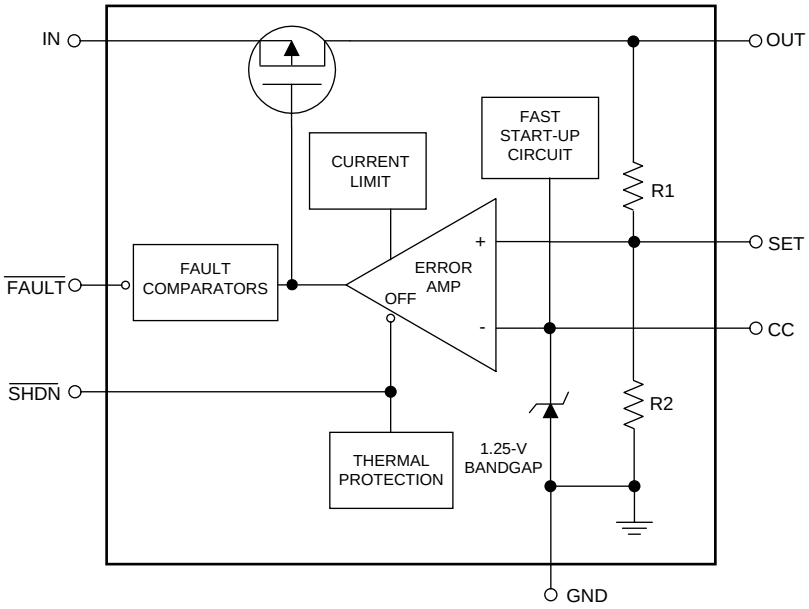




**Figure 4. LP3982 Functional Block Diagram**

## 3 Circuit Diagram

Figure 5 shows the full schematic of the circuit. The power rail or input voltage to the LDO must be equal to, or greater than, the starting output voltage of the LDO with the addition of the dropout voltage. To be more specific within this design, the desired output voltage of the LDO must start equal to or above the power-up voltage of MSP430 FRAM devices. Therefore, the minimum input to the LDO must be the start-up voltage of the MSP430 FRAM device with the addition of the dropout voltage. Numerical details are described in detail in Section 4.

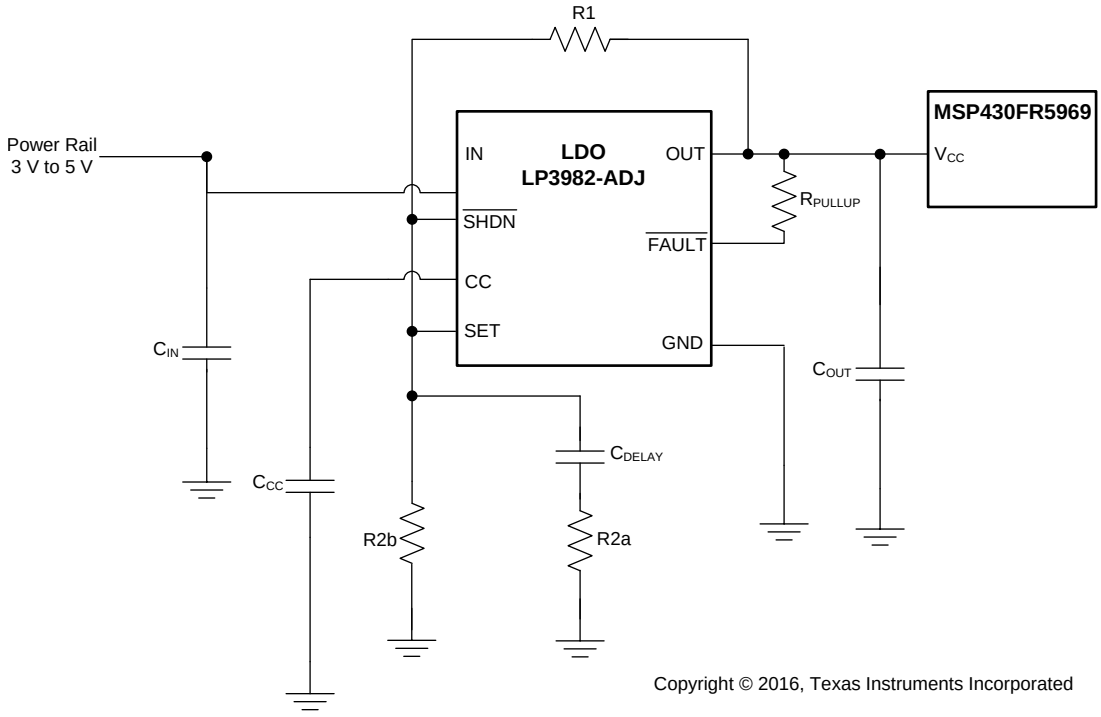


**Figure 5. Full Schematic of the System**

$C_{IN}$ and $C_{OUT}$ are determined based on stability. The LP3982 is stable with a 2.2-µF ceramic output capacitor. The bypass capacitor $C_{CC}$ is in place to reduce the output noise without slowing the transient response. The pullup resistor is in place for the $\overline{\text{FAULT}}$ pin because it is an open-drain circuit. TI recommends a 100-kΩ resistor for most applications. Figure 6 shows a typical application schematic referenced from the LP3982 data sheet with the recommended component values.

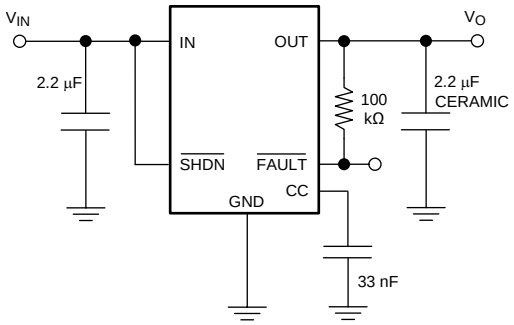


**Figure 6. LP3982 Typical Application (Fixed $V_{OUT}$ Version)**

## 4 Dynamic Voltage Scaling

The TI Design uses the LP3982 adjustable output voltage to switch between the required starting voltage and the final power efficient voltage for MSP430 FRAM devices. The output voltage of the LP3982 is set with the combination of resistors in a negative feedback configuration, shown in Figure 5, and is characterized by Equation 1:

$$V_O = V_{REF}\left[\frac{R_1}{R_2} + 1\right] \quad (1)$$

where

- $R_1$ is the resistor between OUT and and the SET pin
- $R_2$ is connected between the SET pin and GND
- $V_{REF}$ is set to be 1.25 V according to the LP3982 datasheet

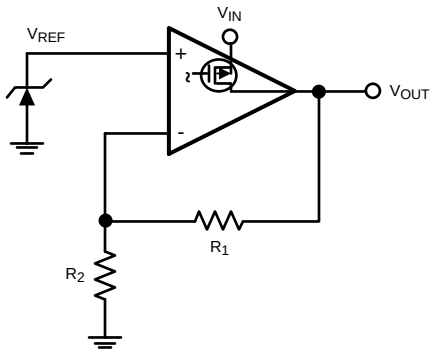


**Figure 7. Simplified Regulator Topology**

The data sheet also suggests setting R2 to be 100 kΩ to optimize accuracy, power supply rejection, noise, and power consumption. Finally, to find out what the appropriate output needs to be, the MSP430FR5969 data sheet is referenced. The recommended operating conditions suggest the supply voltage range $V_{CC}$ to be at least 1.8 V minimum, and 3.6 V maximum, with the system power down level $V_{SVSH-}$ ranging from 1.75 V to 1.85 V with 1.8 V typical. For optimal power efficiency, the MSP430 FRAM device must operate at the voltage just above the shutdown voltage. Table 5 describes the power-on characteristics of the MSP430. The power-up level $V_{SVSH+}$ ranges from 1.77 V to 1.99 V with 1.85 V typical and the hysteresis $V_{SVSH\_hys}$ to be 40 mV minimum, 120 mV maximum. To ensure that the MSP430 FRAM device starts up, output voltage at the beginning must be at least over 1.99 V. Finally, to save power, the final settled value of $V_O$ must be just slightly higher than the voltage at which the MSP430 FRAM device powers down. In this design, the start-up value was chosen to be 2 V, and the operating voltage was chosen to be 1.8 V. Section 4.1 explains in detail the design process.

**Table 5. Hysteresis Design Parameters(1)**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SVSH,LPM}$ | $SVS_H$ current consumption, low power modes | | | 170 | 300 | nA |
| $V_{SVSH-}$ | $SVS_H$ power-down level | | 1.75 | 1.8 | 1.85 | V |
| $V_{SVSH+}$ | $SVS_H$ power-up level | | 1.77 | 1.88 | 1.99 | V |
| $V_{SVSH\_hys}$ | $SVS_H$ hysteresis | | 40 | | 120 | mV |
| $t_{PD,SVSH,\ AM}$ | $SVS_H$ propogation delay, active mode | $dV_{VCC}/dt$ = –10 mV/µs | | | 10 | µs |

(1) Over recommended ranges of supply voltage and operating free-air temperature

### 4.1 Application Notes

To achieve dynamic voltage scaling with a single output LDO, an RC time delay is added to the circuit in parallel with $R_{2a}$ to effectively change the feedback resistance to the SET pin of the LDO, as shown in Figure 4. To evaluate the effects of the time delay, the basic behaviors of a capacitor must first be visited. Ideally, during start-up, there is no charge in the capacitor, and when the LDO powers up to 2 V, the capacitor acts as a short in which case the two resistors are in parallel and can be equivalently combined to form:

$$V_O = V_{REF}\left[\frac{R_1}{R_{2a} \,||\, R_{2b}} + 1\right]$$

or

$$V_O = V_{REF}\left[\frac{R_1}{R_{2a}} + \frac{R_1}{R_{2b}} + 1\right] \quad (2)$$

As the capacitor begins to charge, the current through $R_{2a}$ begins to drop, and the capacitor begins to have an effect on the circuit. This can be characterized with Equation 3:

$$V_O = V_{REF}\left[\frac{R_1}{R_{2b}} + \frac{R_1}{R_{2a}} e^{-t/R_{2a} \times C_{DELAY}} + 1\right] \quad (3)$$

When the capacitor is fully charged at steady state, the capacitor appears to be an open circuit, and there is no current through $R_{2a}$. In this case Equation 3 can be simplified to Equation 4:

$$V_O = V_{REF}\left[\frac{R_1}{R_{2b}} + 1\right] \quad (4)$$

With $V_{REF}$ set at 1.25 V, $R_{2b}$ set as 100 kΩ to optimize for noise and accuracy, and desired output voltage ($V_o$) of 1.8 V, when the capacitor reaches steady state (open circuit), $R_1$ is calculated as 44.2 kΩ. Once $R_1$ is calculated, the start-up short circuit equation, Equation 2, can be used to calculate $R_{2a}$. With output voltage of 2 V during start-up according to the MSP430FR5969 data sheet, $R_{2a}$ was calculated as 274 kΩ.

After trying out the circuit with these calculated values, $R_{2b}$ was readjusted to 100 kΩ so that the start-up voltage is 2.355 V to ensure that the MSP430 starts up regardless of process variation and device tolerances. $C_{DELAY}$ was calculated using Equation 5 as 2.2 µF for the time constant of 220 ms.

$$\tau = R_{2b} \times C_{DELAY} \quad (5)$$

## 4.2 Test Data

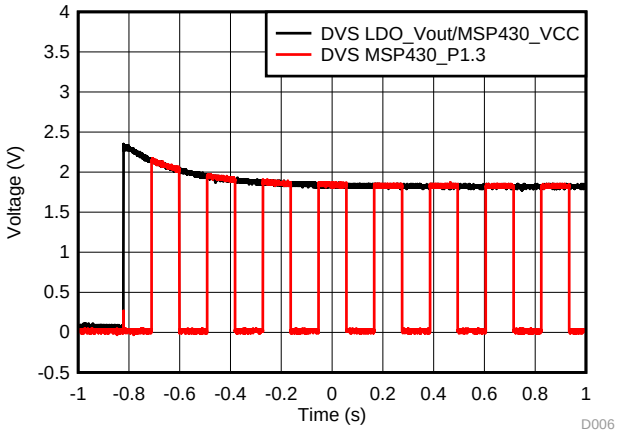


**Figure 8. With Dynamic Voltage Scaling for MSP430RF5969**

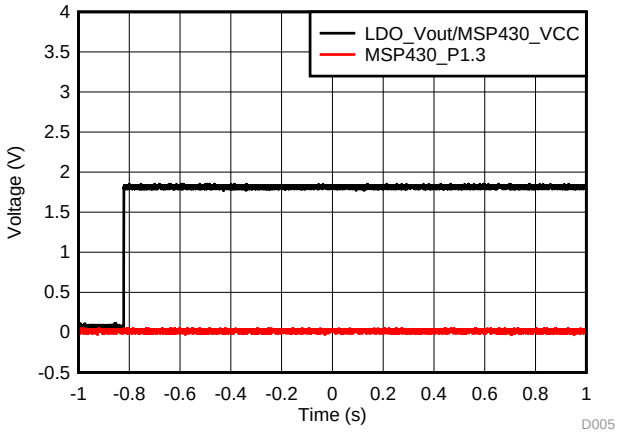


**Figure 9. Without Dynamic Voltage Scaling for MSP430RF5969**

Figure 8 and Figure 9 show the importance of the dynamic voltage scaling. Figure 8 shows the MSP430 FRAM device with the dynamic voltage scaling. The red line shows the MSP430 FRAM device maintaining operation even as $V_{CC}$, shown with the black line, ramps down from 2.3 V to 1.8 V. The black line in Figure 9 shows the MSP430 FRAM device $V_{CC}$ staying consistent at 1.8 V without dynamic voltage scaling. As a result, the corresponding output pin of the MSP430 FRAM device, shown with the red line in Figure 9, is not toggling, which shows that the MSP430 FRAM device is not operating. Figure 8 and Figure 9 are shown side-by-side for a direct comparison.

# 5 Design Files

## 5.1 Schematics

To download the schematics, see the design files at TIDA-01172.

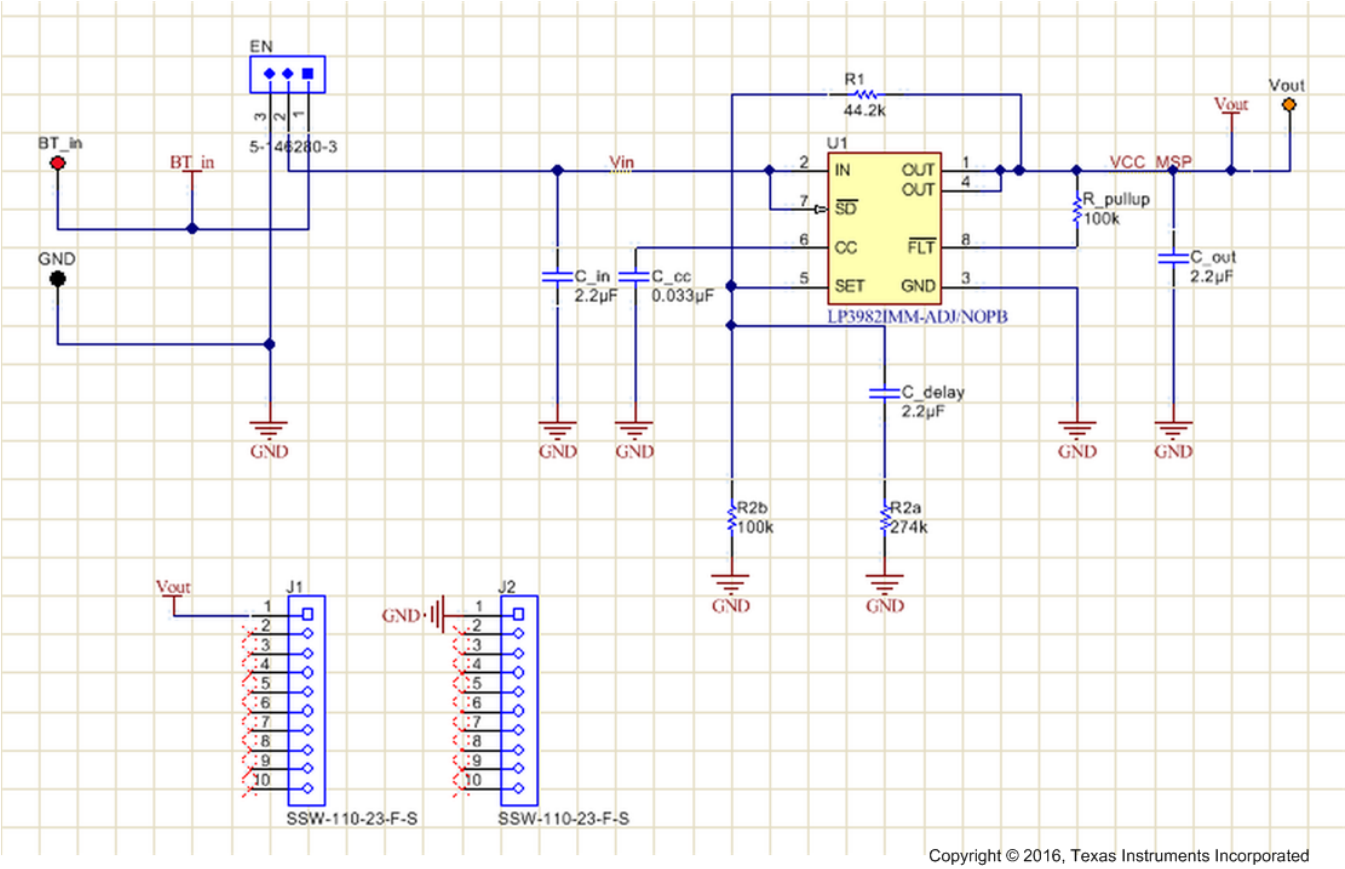


**Figure 10. TIDA-01172 Schematic**

## 5.2 PCB Layout Recommendations

### 5.2.1 Layout Guidelines

For optimal performance, place $C_{IN}$ and $C_{OUT}$ as close as possible to the pins of the LP3982 device. A large area ground plane is also preferred for good heat dissipation. Lastly, avoid long traces and narrow trace widths to prevent parasitic inductances.

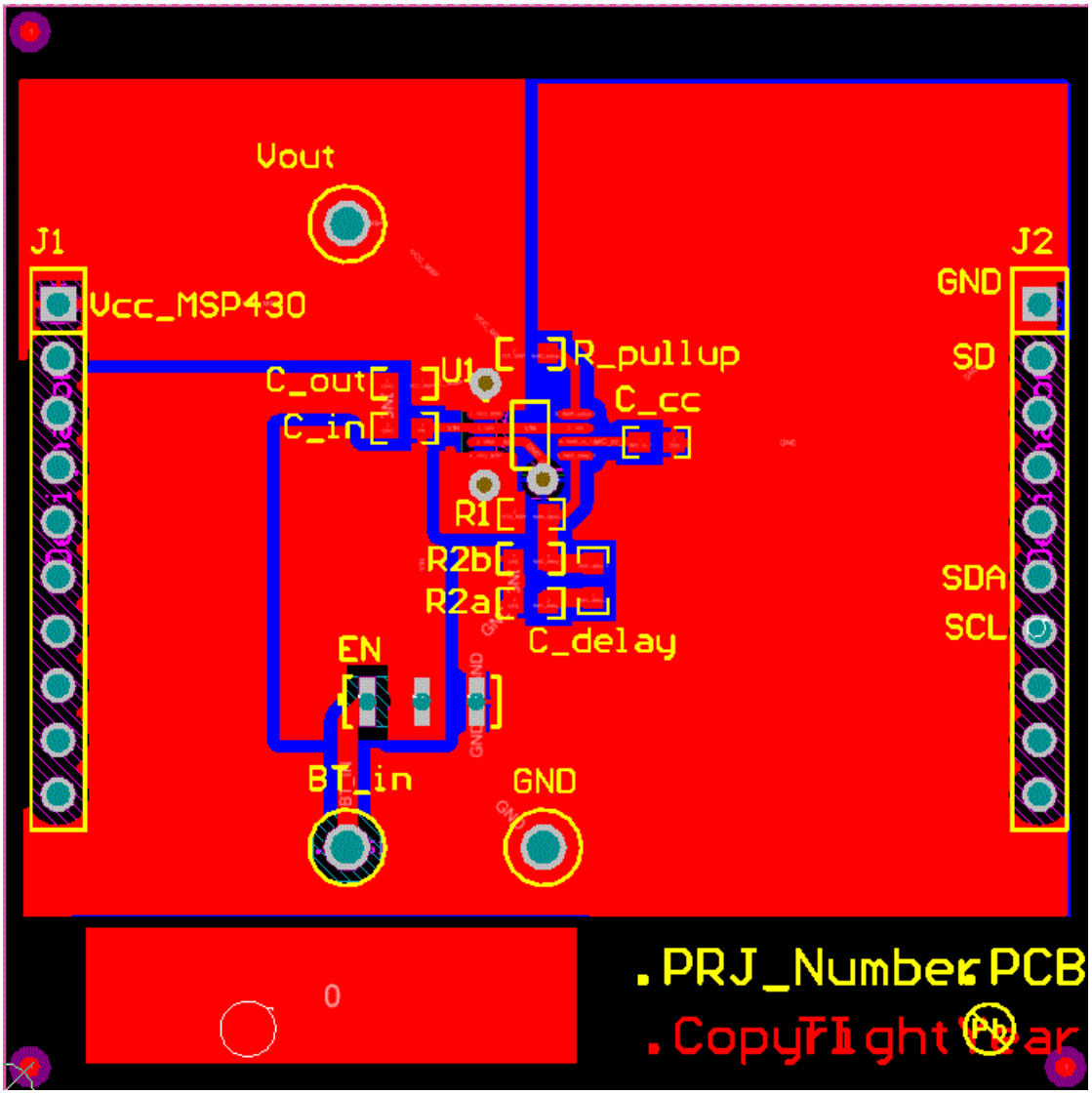


**Figure 11. PCB Layout Guidelines**

### 5.3 Layout Prints

To download the layer plots, see the design files at TIDA-01172.

### 5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01172.

## 6 References

1. MSP430FR59xx Mixed-Signal Microcontrollers data sheet
2. LP3982 Micropower, Ultra-Low-Dropout, Low-Noise, 300-mA CMOS Regulator data sheet

## 7 About the Author

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