TI Designs

CISPR 25 Class 5 USB Type-C™ Port With USB3.0 Data Support Reference Design

Description

The TIDA-00987 is a TI Reference Design for automotive media ports that require data transfers. This TI Design has the capability to support USB2.0 and USB3.0 data through a 15-W USB Type-C™ port. Customers can accelerate their media port systems by taking advantage of a complete reference design comprised of analog AEC-Q100 qualified integrated circuits (ICs) that is CISPR-25 Class-5 [18] tested. This TI Design creates a robust, flexible solution that allows the system to charge both Type-C and legacy devices all within a small 1 × 2.5-inch solution.

Resources

TIDA-00987	Design Folder
LM53635-Q1	Product Folder
TPS25810-Q1	Product Folder
LM74610-Q1	Product Folder
TPD4E05U06-Q1	Product Folder
TLV70033-Q1	Product Folder
TPS254900-Q1	Product Folder
HD3SS3212	Product Folder

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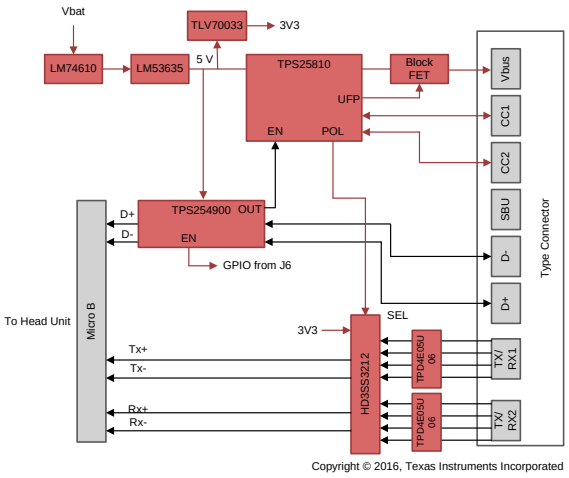
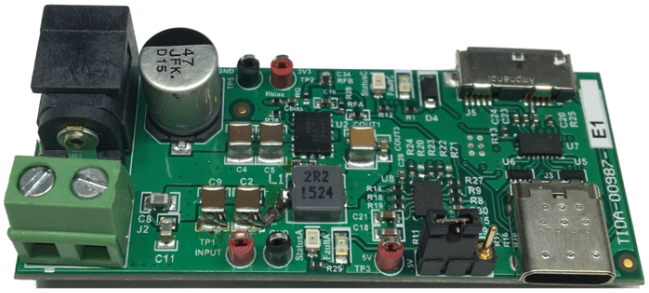
Features

- LM74610-Q1 Smart Diode Emulates Ideal Diode Rectifier and Protects Downstream Devices in Case of Reverse Polarity
- TPS25810-Q1 and TPS254900 Provide Negotiation Over CC1/CC2 and D+/D– Lines, Respectively, to Enable Charging of Either Type-C or Legacy Downstream Devices
- Small Solution Size Based on Typical Media Interface Board Dimensions of 1 inch × 2.5 inch
- Components in This System Provide Short-to-Battery Protection and Load Dump Protection Against Input Transients up to 40 V
- By Combining HD3SS3212 With TPD4E05U06 and Optimized Layout, Demonstrates SuperSpeed Compatibility With Type-C Connector Without Signal Degradation
- Automotive Grade LM53635-Q1 Optimizes Power Supply Through Unique Hotrod Package and Reduces Parasitics to Mitigate EMI Without Interfering With AM or FM Band Frequencies

Applications

- Automotive Head Units With Remote Displays
- Automotive Midrange and High-End Head Units
- Remote Media Hubs





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1 System Overview

1.1 System Description

The TIDA-00987 is a TI Reference Design (Figure 1) for automotive media hubs that have a Type-C port requiring both USB3.0 and USB2.0 data capabilities. Customers can accelerate the design of their media hub systems by taking advantage of a complete reference design comprised of analog AEC-Q100 qualified integrated circuits (ICs) from TI. This TI Design creates a robust, low-cost solution that allows the system to charge both Type-C and legacy devices all within a small 1-inch × 2.5-inch solution.

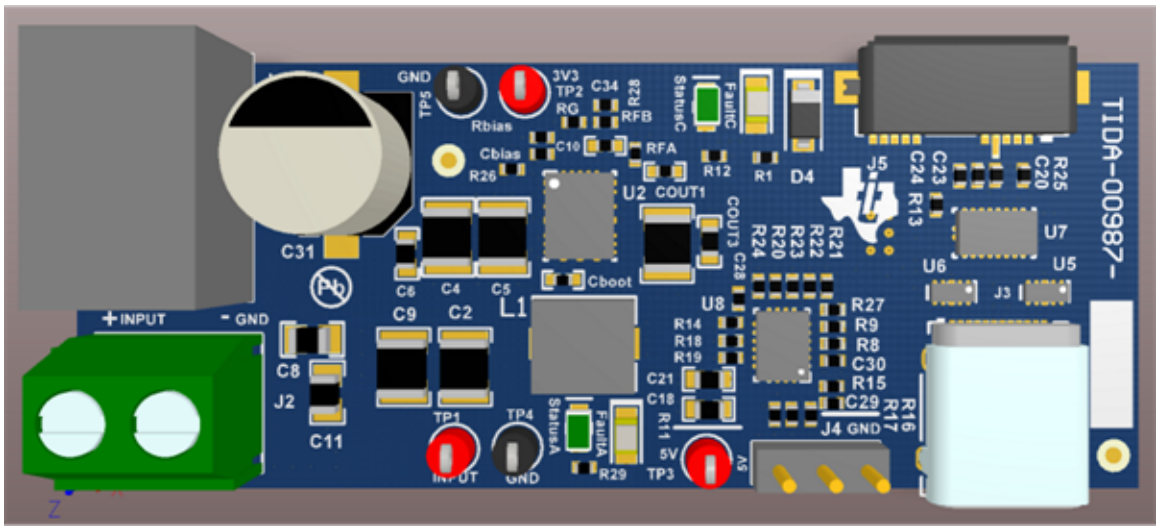

Figure 1. Automotive Type-C With USB3.0 Data Reference Design

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
System operation					
V_{IN}	Input voltage	5.5	12	36	V
F_{SW}	Switching frequency	1.85	2.1	2.35	MHz
$R_{DS(ON)}$	On resistance of power switch		34	46	mΩ
I_{OS}	Short circuit current limit	3.16	3.4	3.64	A
Output voltages					
V_{DC-DC}	DC-DC system output	4.75	5	5.25	V
V_{LDO}	LDO output		3.3		V
Output current					
I_{OUT}	VBUS	0.5	1.5	3	A
Data rates					
D+/D-	High speed		480		Mbps
T_x+/-, R_x+/-	SuperSpeed		5		Gbps

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1.3 Block Diagram

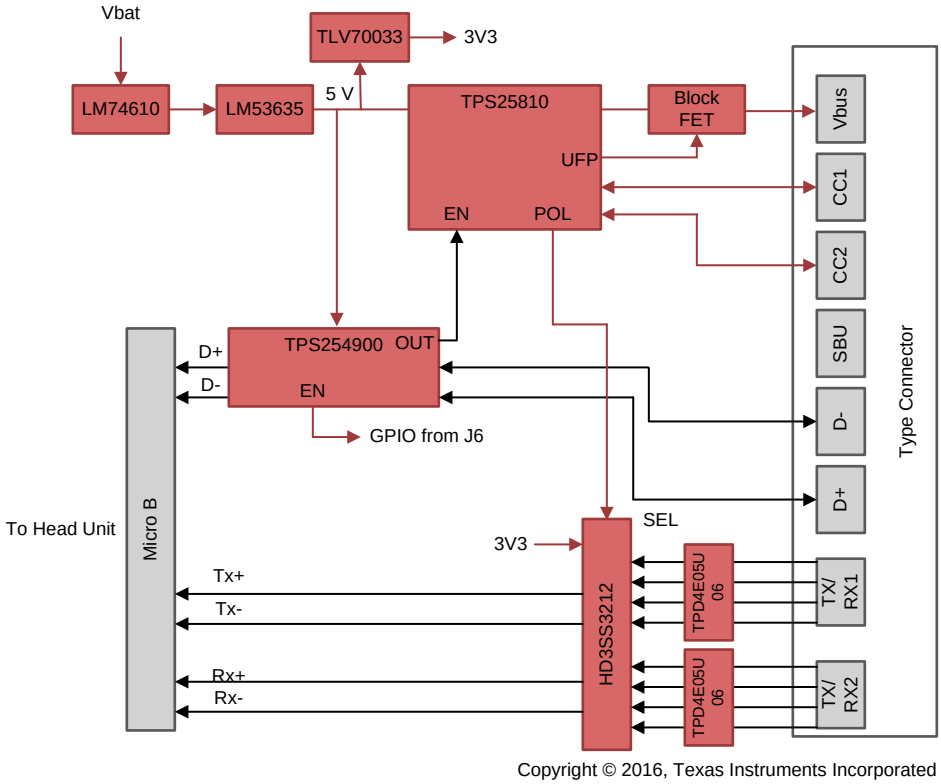

Figure 2. Type-C With Data Block Diagram

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1.4 Highlighted Products

1.4.1 TPS25810-Q1 Type-C USB3.0 Power Supply

The TPS25810 (Figure 3 and Figure 4) is a USB Type-C downstream facing port (DFP) controller with an integrated 3-A rate USB power switch. The TPS25810 monitors the Type-C Configuration Channel (CC) lines to determine when an USB device is attached. If an upstream facing port (UFP) device is attached, the TPS25810 applies power to V_{BUS} current sourcing capability to the UFP through the pass through CC line. If the UFP is attached using an electronically marked cable, the TPS25810 also applies V_{CONN} power to the cable CC pin. The TPS25810 also identifies when Type-C audio or debug accessories are attached.

The TPS25810 draws less than 0.7 µA (typ) when no device is attached. Additional system power saving is achievable in S4/S5 system power states by using the ($\overline{UFP}$) output to disable the high-power 5-V supply when no UFP is attached. In this mode, the device is capable of running from an auxiliary supply (AUX) that can be a lower voltage supply (3.3 V), typically power the system µC in low-power states (S4/S5).

The TPS25810 34-mΩ power switch has two selectable fixed current limits that align with the Type-C current levels. The ($\overline{FAULT}$) output signals when the switch is in an over current or over temperature condition. The ($\overline{LD\_DET}$) output controls power management to multiple high-current Type-C ports in an environment where all ports cannot simultaneously provide high current (3 A).

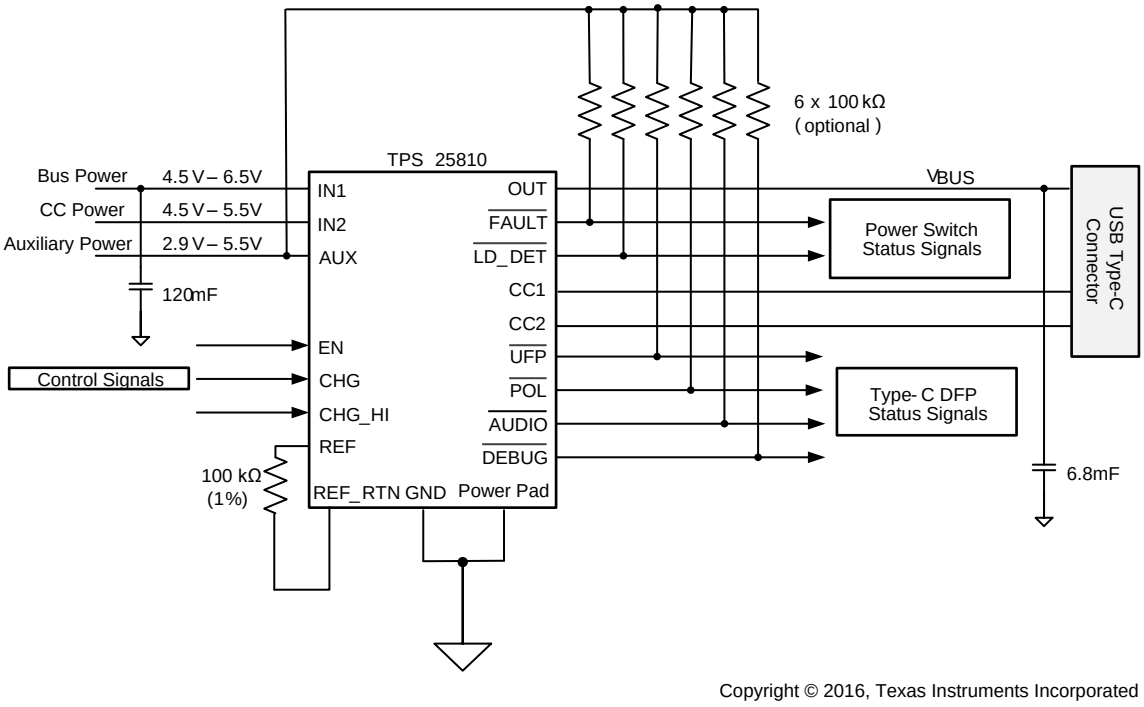

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Figure 3. TPS25810 Simplified Schematic

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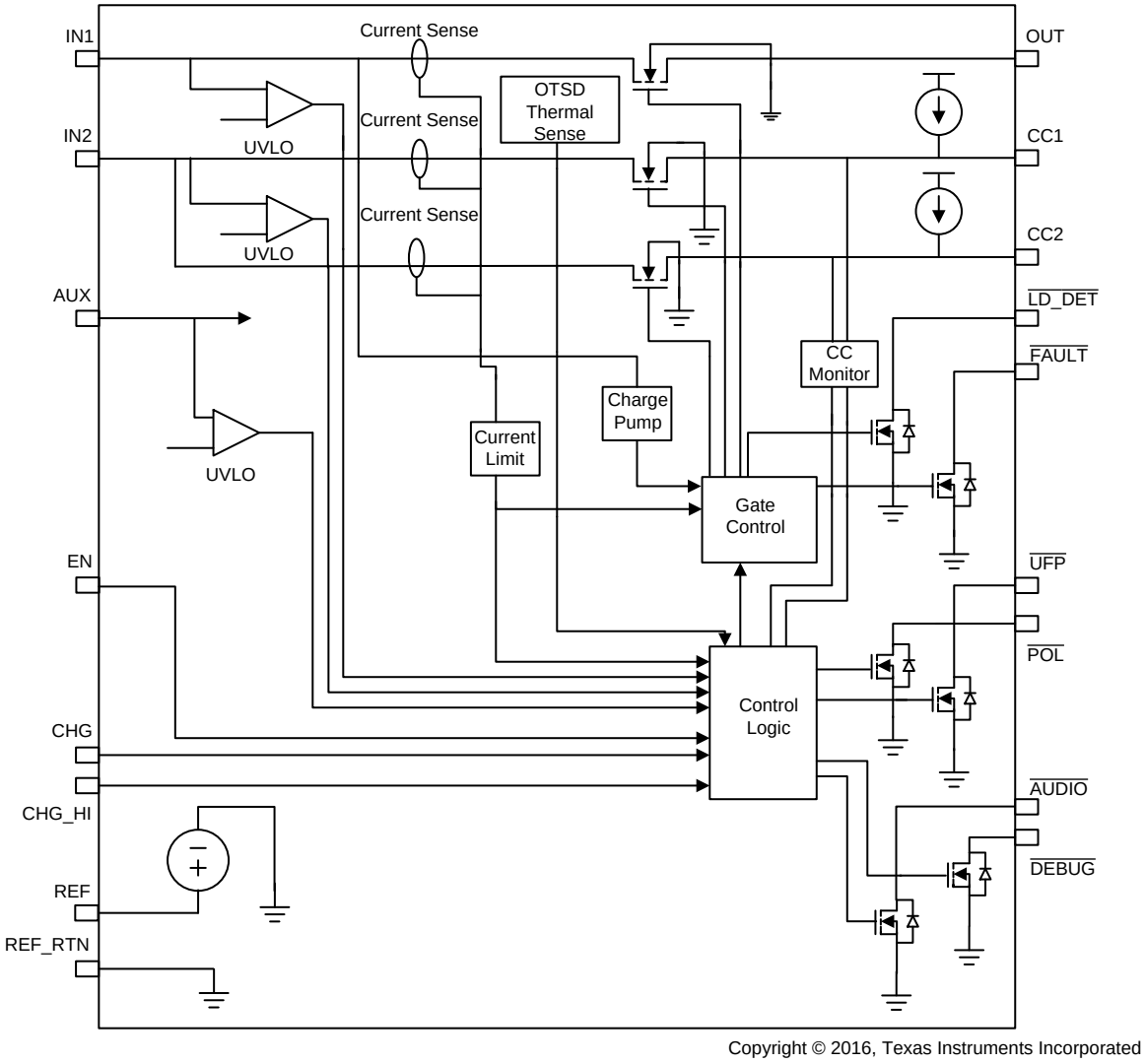

Figure 4. TPS25810 Functional Block Diagram

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Establishing Connection

Unlike traditional Type-A or Type-B ports that physically determine if the hardware is a host or a device, a Type-C port does not have a physical distinction to establish the relationship. Instead, Type-C uses the CC pins to negotiate the initial power and data relationships before the normal USB enumeration occurs.

As defined in the USB Type-C Specification by USB.org, the initial power relationship is either source only, sink only, or dual role power (DRP). Similarly, when a port supports data there are three modes: DFP only, UFP only, or dual role data (DRD), where a port can be configured in either DFP or UFP.

DFPs and DRPs fulfill the role of detecting a valid connection over USB Type-C. Figure 5 shows a DFP to UFP connection made with a Type-C cable. As shown in Figure 5, the detection concept is based on being able to detect terminations in the product that has been attached. A pullup and pulldown termination model is used. A pullup termination can be replaced by a current source.

- In the DFP-UFP connection, the DFP monitors both CC pins for a voltage lower than the unterminated voltage.
- A UFP advertises Rd on both its CC pins (CC1 and CC2).
- A powered cable advertises Ra on the V_{CONN} pin.
- An analog audio device advertises Ra on both the V_{CONN} and CC pins, which identifies it as an analog audio device, and initiates the transfer to the alternative audio mode.

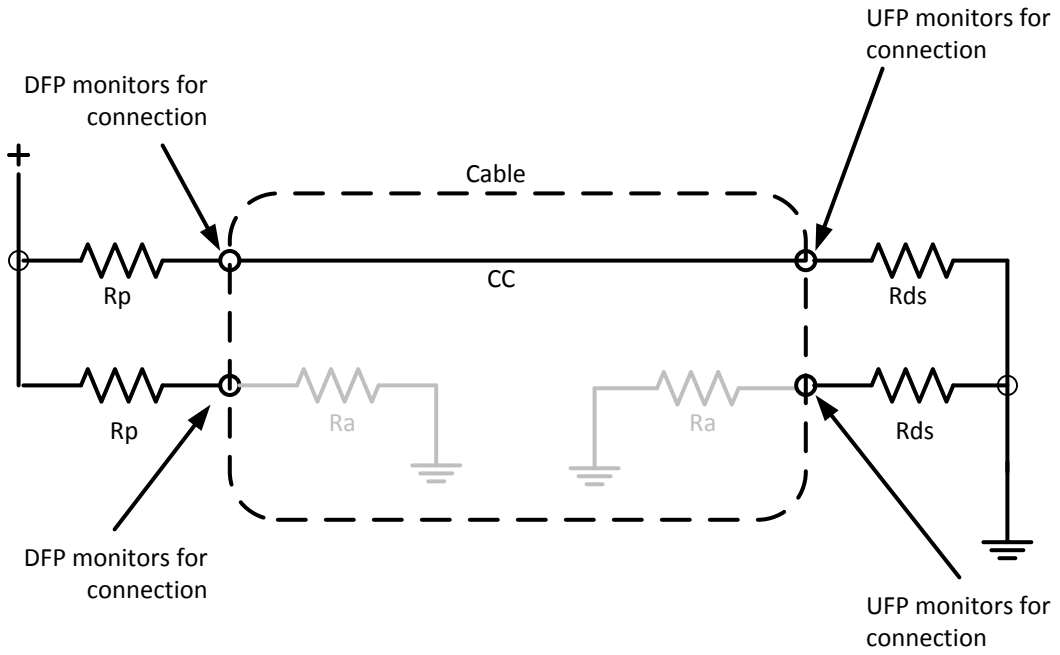

Figure 5. Type-C DFP to UFP Connection

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1.4.2 TPS254900-Q1 Automotive Charging Port Controller and Power Switch With Short-to-Battery Protection

The TPS254900-Q1 (Figure 6 and Figure 7) is a USB charging port controller and power switch with short-to-battery protection. The TPS254900-Q1 provides protection on OUT, DM_IN, and DP_IN. These three pins withstand voltages up to 18 V. Upon a short-to-battery incident, an internal MOSFET quickly disconnects the pin. This provides protection to the TPS254900-Q1's power supply, the upstream processor, or the upstream HUB.

The TPS254900-Q1 50-mΩ power switch has two selectable, programmable current limits that support port power management by providing a lower current limit that can be used when adjacent ports are experiencing heavy loads. This is important in a system with multiple ports and the upstream supply is unable to provide full current to all ports simultaneously.

The TPS254900Q1 has a current-sense output that is able to control an upstream supply. This allows it to maintain 5 V at the USB port even during heavy charging currents. This is important in systems with long USB cables where significant voltage drops can occur while fast-charging portable devices.

The unique IMON feature allows the system to know the load current by monitoring the IMON voltage. This feature is used for dynamic port power management.

To save space in the application, the TPS254900-Q1 also integrates IEC 61000-4-2 compliant ESD protection.

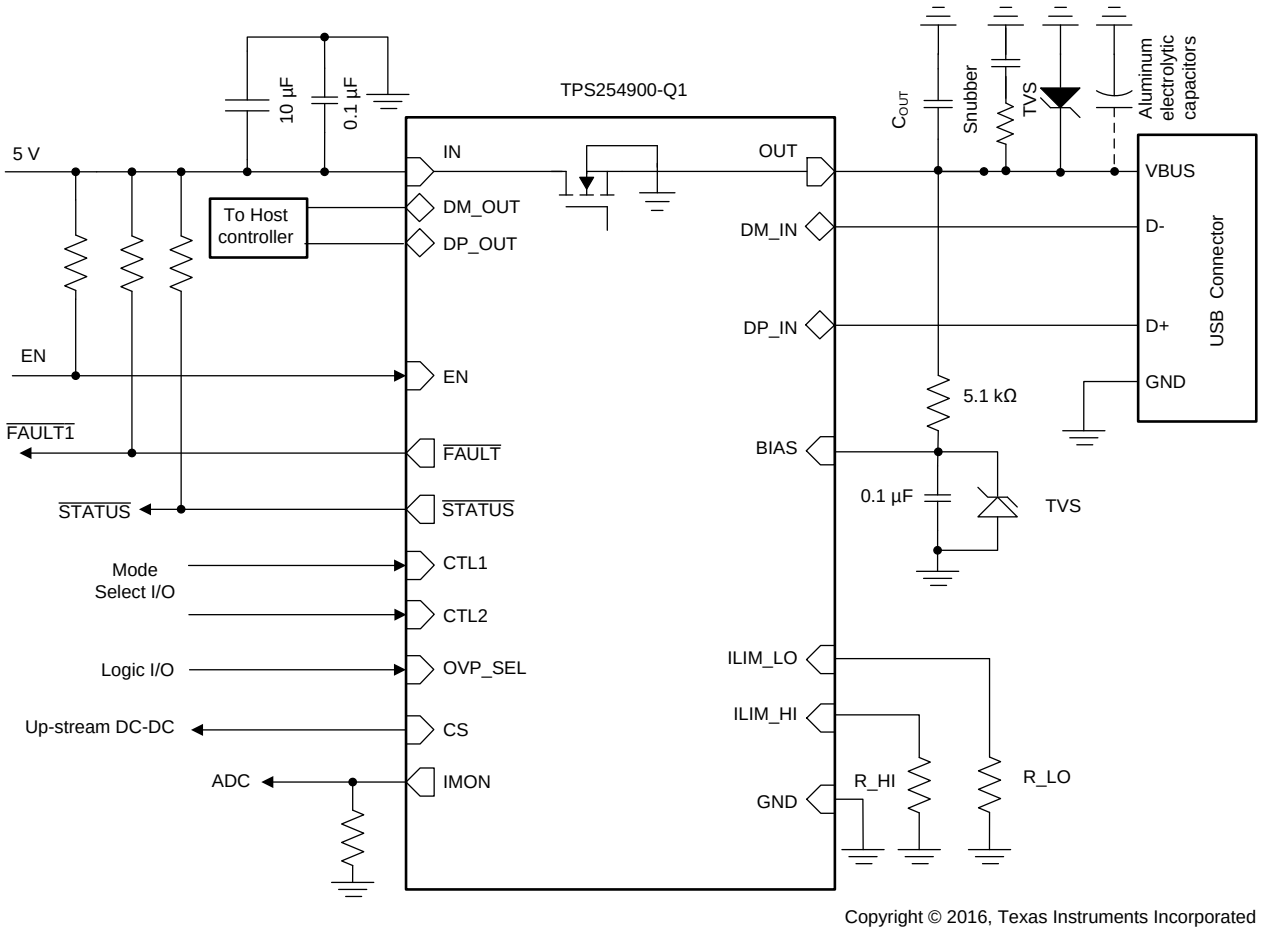

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Figure 6. TPS254900 Simplified Schematic

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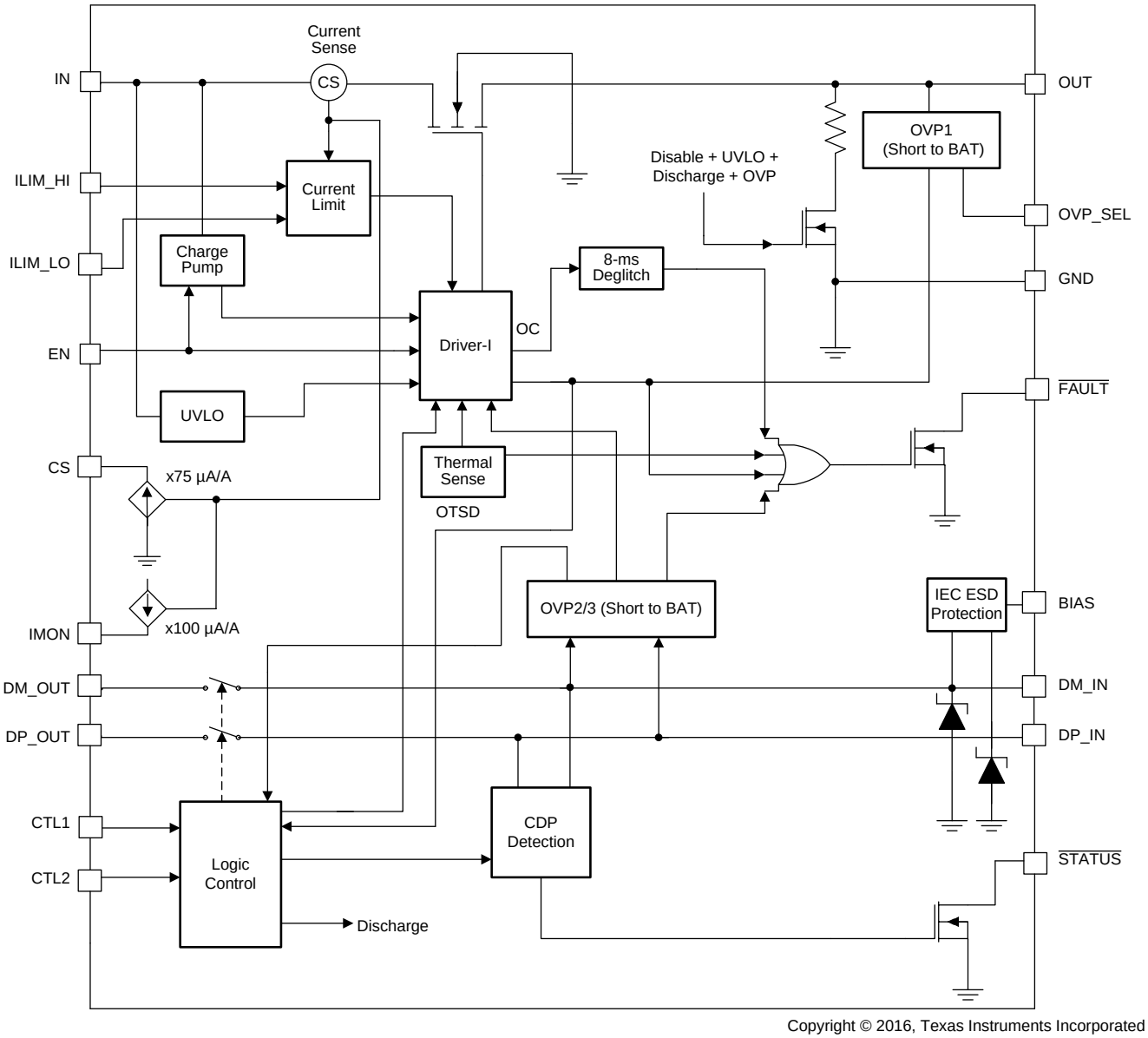

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Figure 7. TPS254900 Functional Block Diagram

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1.4.3 LM74610-Q1 Zero I_Q Reverse Polarity Protection Smart Diode Controller

The LM74610-Q1 (Figure 8 and Figure 9) is a controller device that can be used with an N-channel MOSFET in a reverse-polarity protection circuit. It is designed to drive an external MOSFET to emulate an ideal diode rectifier when connected in series with a power source. A unique advantage of this scheme is that it is not referenced to ground and thus has zero I_Q.

The LM74610-Q1 controller provides a gate drive for an external N-channel MOSFET and a fast response internal comparator to discharge the MOSFET gate in the event of reverse polarity. This fast pulldown feature limits the amount and duration of reverse current flow if opposite polarity is sensed. The device design also meets CISPR25 Class 5 electromagnetic interference (EMI) specifications and automotive ISO7637 transient requirements with a suitable transient voltage suppressor (TVS) diode.

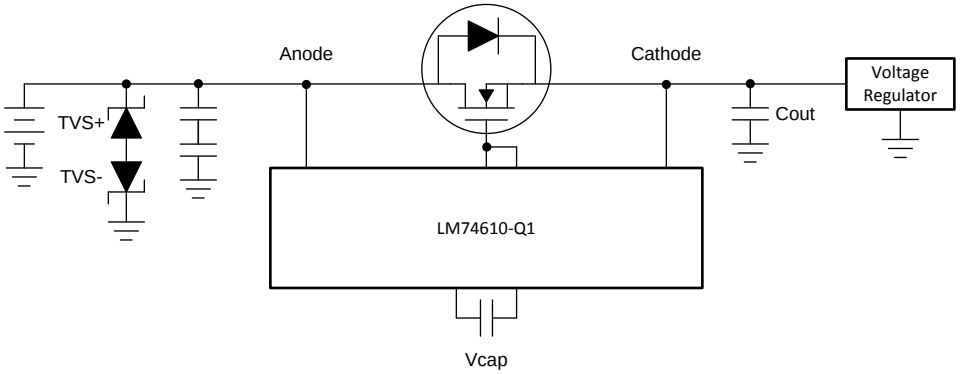

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Figure 8. LM74610 Simplified Schematic

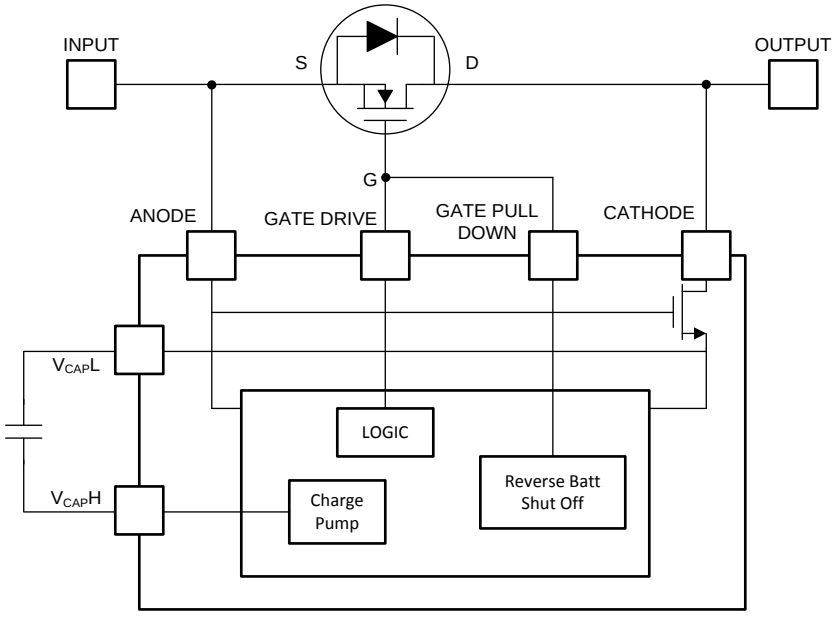

Figure 9. LM74610 Functional Block Diagram

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1.4.4 LM53635 3.5-A, 36-V Synchronous, 2.1-MHz, Step-Down DC-DC Converter

The LM53625-Q1/LM53635-Q1 synchronous buck regulator (Figure 10 and Figure 11) is optimized for automotive applications, providing an output voltage of 5 V, 3.3 V, or an adjustable output. Advanced high-speed circuitry allows the LM53625-Q1/LM53635-Q1 to regulate from an input of 18 V to an output of 3.3 V at a fixed frequency of 2.1 MHz. The innovative architecture allows this device to regulate a 3.3-V output from an input voltage of only 3.55 V. All aspects of the LM53625- Q1/LM53635-Q1 are optimized for automotive and performance-driven industrial customers. An input voltage range up to 36 V, with transient tolerance up to 42 V, eases input surge protection design. The automotive-qualified Hotrod QFN package with wettable flanks reduces parasitic inductance and resistance while increasing efficiency, minimizing switch node ringing, and dramatically lowering EMI. An open-drain reset output, with built-in filtering and delay, provides a true indication of system status. This feature negates the requirement for an additional supervisory component, saving cost and board space. Seamless transition between pulse-width modulation (PWM) and pulse-frequency modulation (PFM) modes and low quiescent current (only 15 µA for the 3.3-V option) ensure high efficiency and superior transient responses at all loads.

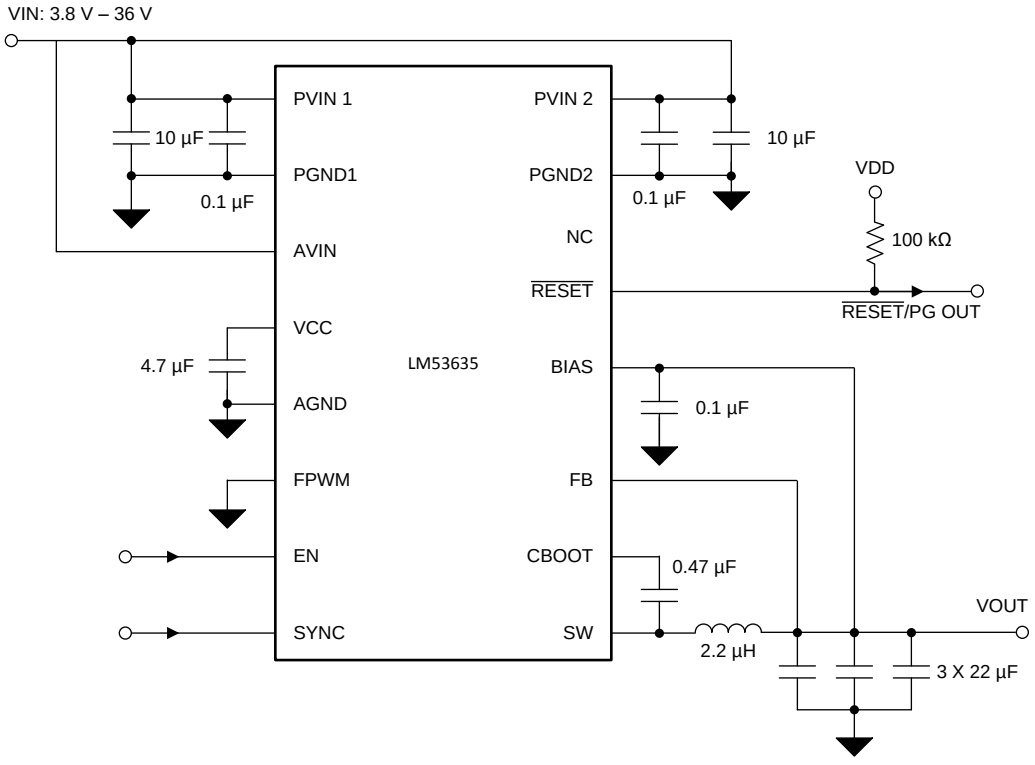

Figure 10. LM53635 Simplified Schematic

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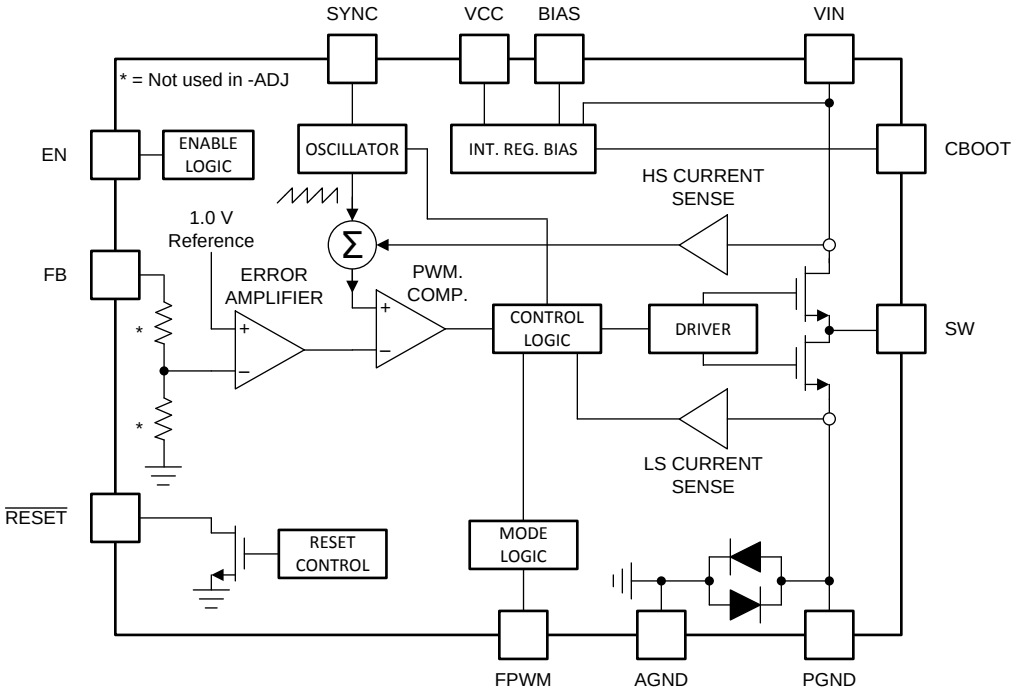

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Figure 11. LM53635 Functional Block Diagram

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1.4.5 TPD4E05U06

The TPD4E05U06-Q1 (Figure 12 and Figure 13) is a unidirectional TVS electrostatic discharge (ESD) protection diode array with ultra-low capacitance. It is rated to dissipate ESD strikes above the maximum level specified in the IED61000-4-2 level 4 international standard. Its ultra-low loading capacitance makes it ideal for protecting any high-speed signal pins.

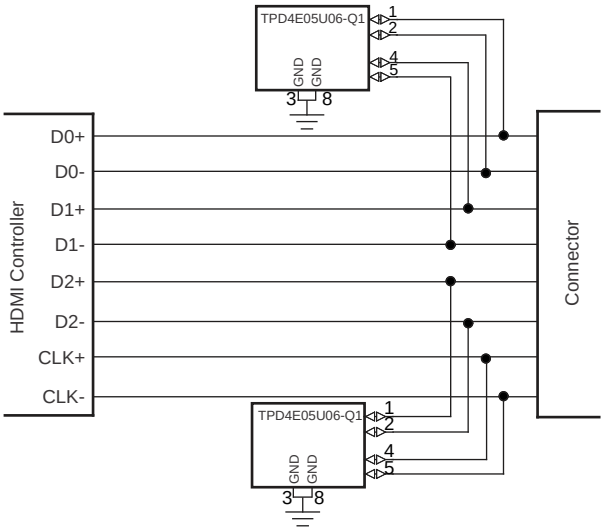

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Figure 12. TPD4E05U06 Simplified Schematic

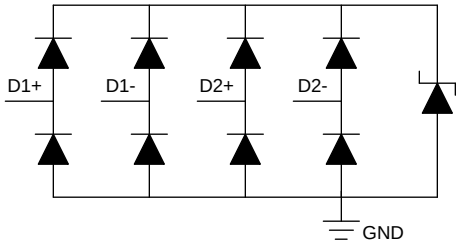

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Figure 13. TPD4E05U06 Functional Block Diagram

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1.4.6 HD3SS3212

The HD3SS3212 (Figure 14 and Figure 15) is a high-speed bidirectional passive switch in MUX or DEMUX configurations suited for USB Type-C application supporting USB3.1 Gen 1 and Gen 2 data rates. Based on control pin SEL, the device provides switching on differential channels between Port B, Port C, or Port A.

The HD3SS3212 is a generic analog differential passive switch that can work for any high-speed interface application requiring a common-mode voltage range of 0 to 2 V and differential signaling with differential amplitude up to 1800 mVpp. It employs adaptive tracking that ensures the channel remains unchanged for the entire common mode voltage range.

Excellent dynamic characteristics of the device allow high-speed switching with minimum attenuation to signal eye diagram with very little added jitter. It consumes < 2 mW of power when operational and has a shutdown mode exercisable by OEn pin resulting < 20 µW.

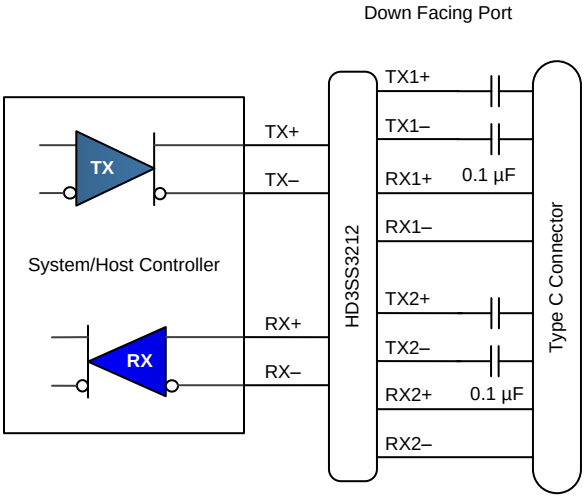

Figure 14. HD3SS3212 Simplified Schematic

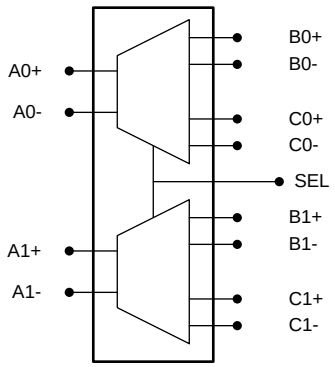

Figure 15. HD3SS3212 Functional Block Diagram

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2 System Design Theory

2.1 Introduction

The TIDA-00987 Reference Design is designed to support Type-C DFP charging and CDP legacy charging in addition to USB2.0 and USB3.0 data. As seen in Figure 16, the TIDA-00987 is a media interface subsystem that could be integrated into a head unit with integrated display. This TI Design can be enabled through the legacy controller by either tying enable (EN) high or through an external application processor such as the Texas Instruments Jacinto 6 family of infotainment processors (DRA7x) allowing simultaneous charge and on-the-go functionality.

This TI Design was done specifically to meet automotive standards and uses parts that are already or planned to be released as automotive Q-100 grade qualified. In designing a subsystem for automotive infotainment, it is important to meet pertinent protection standards as required by automotive OEMs. In this TI Design, parts were selected to support typical protection requirements such as reverse battery protection, current limiting, short-to-battery protection, as well as ESD protection. Additionally, power supplies typically require spread spectrum to mitigate EMI and switching frequency outside of AM band operation while supporting wide input off-battery operation. In the circuit board layout, care was taken to improve thermal dissipation and EMI to ultimately pass CISPR-25 Class 5 Standards [18].

Each system subsection, seen in Figure 17 and Figure 18, is explained in Section 2.2 through Section 2.6.

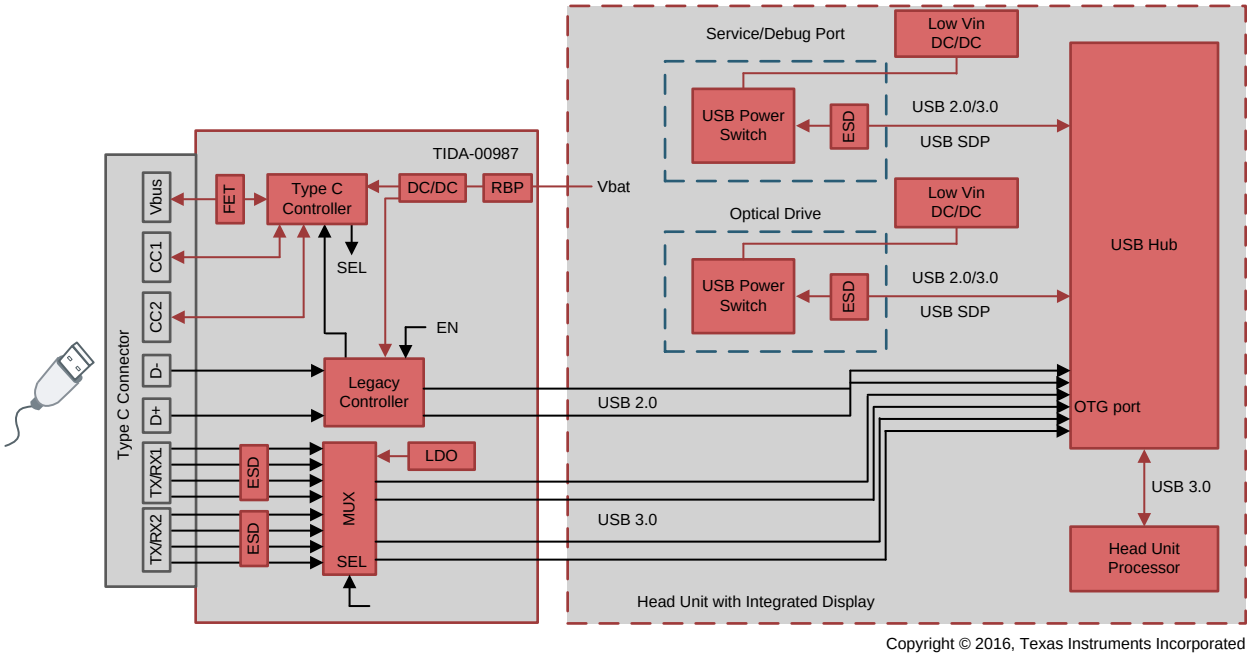

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Figure 16. System Integration Concept

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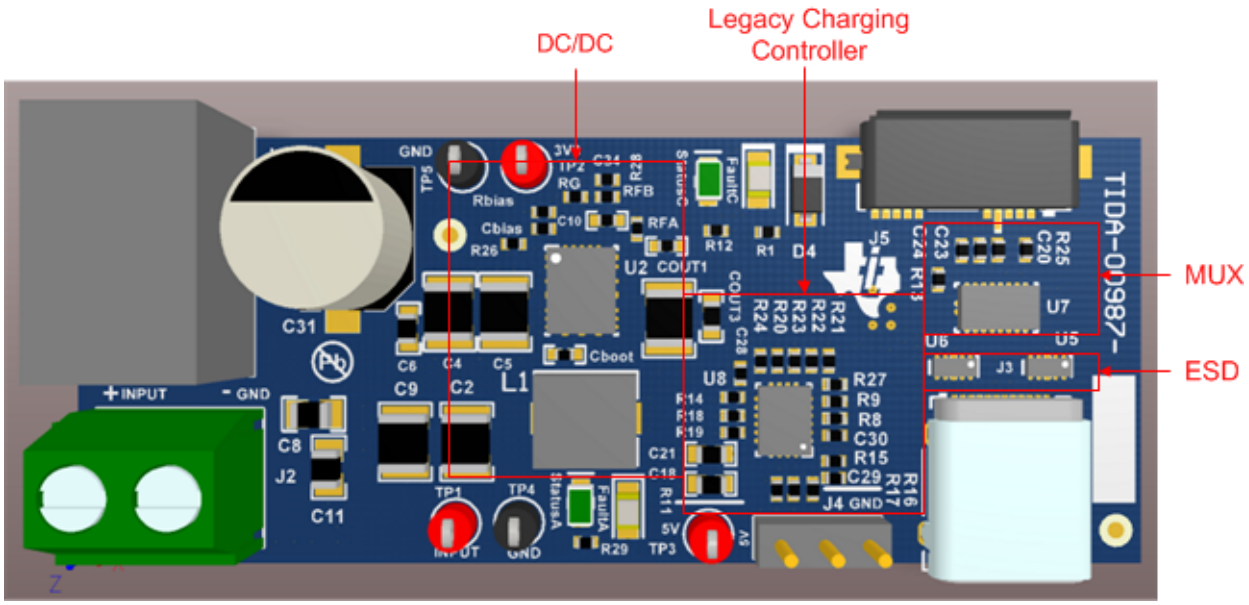

Figure 17. USB Type-C Reference Design Front

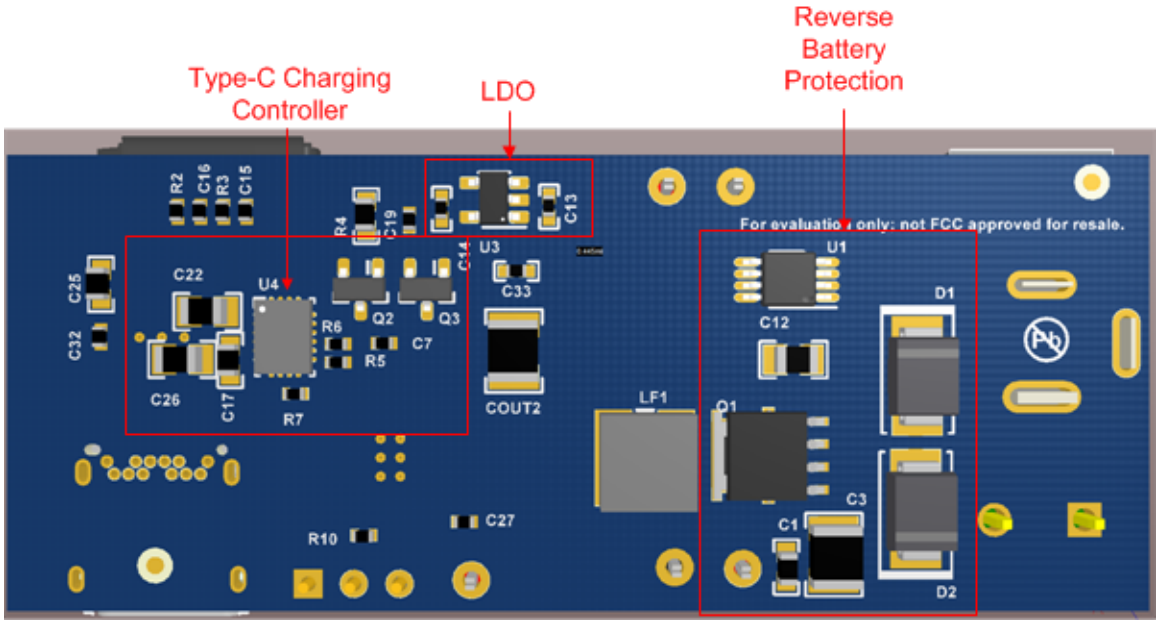

Figure 18. USB Type-C Reference Design Back

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2.1.1 Charging Design Overview

There are many benefits to Type-C connectors including reversible orientation, high-speed data rates, and high-power capabilities. For this particular design, this port is 15-W capable and supports both high-speed and SuperSpeed. The Type-C controller transmits its 3-A current capability over the CC1/CC2 lines and for the cases that a Type-C to Type-C connector is plugged in, the power switch of the Type-C controller will instantiate charging for the UFP device. For situations where a Type-C to legacy connector (Type-A, micro Type-B, and so on), the current capability is not received through the Type-B receptacle device that monitors USB2.0 data line (D+/D-), leading to the device drawing 500-mA maximum defined by USB2.0 or 900 mA for USB3.0 standards. This current level is insufficient for many devices due to higher charging rate requirement. By adding the legacy controller, all the electrical signatures on D+/D– are provided to support charging downstream port (CDP) protocols. This allows host and client devices to acknowledge the protocol handshake and draw additional current beyond the 500-mA or 900-mA maximum defined by USB2.0 and USB3.0, respectively. For more information about the theory behind this configuration, see the *TPS25810 Charging Port Over USB Type-C™* Application Report (SLVA768).

2.1.2 Data Design Overview

As previously mentioned, the flip-ability of the Type-C connector allows the user ease-of-use; however, requires careful design consideration. The Type-C connector supports both USB2.0 and USB 3.0 data. This is possible due to its Row A and Row B mirror image 12 pin-out configuration as seen in Figure 19.

Pins A/B2, A/B3, A/B10, and A/B11 are the eight T_x and R_x high-speed lanes. These lanes are capable of up to 5 Gbps, although the connector itself can handle speeds of up to 20 Gbps per lane for future USB specifications improvements. Because there is a duplicate set of T_x+/T_x– and R_x+/R_x– lines due to the reversible feature of the connector, a multiplexer is needed to pass a single set of T_x and R_x lines. The SEL of the MUX is controlled by the Type-C controller $\overline{\text{POL}}$ pin.

Pins A/B6 and A/B7 have the D+/D– lines, which allow for backwards compatibility with USB2.0 data rates up to 480 Mbps. Pins A/B4 and A/B9 have VBUS, which provides the power lines and supports up to 3 A. Pins A/B8 have the secondary bus (SBU), which allows extra data lines for alternate use; however, extra data lines are not used in this particular design. Pins A/B5 have the channel configuration (CC) lines, which are responsible for cable attachment orientation, role detection, and current mode.

PIN:	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
NAME:	GND	Tx1+	Tx1–	VBUS	CC1	D+	D–	SBU1	VBUS	Rx2–	Rx2+	GND
NAME:	GND	Rx1+	Rx1–	VBUS	SBU2	D–	D+	CC2	VBUS	Tx2–	Tx2+	GND
PIN:	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 19. Pin Out for USB Type-C Connector

2.2 Reverse Battery Protection

Reverse battery protection (Figure 20) is a requirement for every electronic subsystem in a vehicle recognized by OEM standards as well as Load Dump Protection Standards ISO 16750-2. The LM74610 is used to control the NFET to protect the load in a negative polarity condition. This device is used to emulate an ideal diode by using an NFET in series with the battery supply. This has the advantage of a highly effective and efficient substitute for reverse battery protection to the traditional rectifier. The LM74610 has no power pin and no ground reference thus requiring zero I_Q and reducing standby current drawn from the battery. Additionally, the voltage drop across the FET is so inconsequential that it allows the wide V_{IN} Buck Regulator to operate at even lower battery input voltages. This is an advantage for scenarios such as cold crank when the battery voltage temporarily drop to as low as 3.5 V. A traditional diode solution usually has a 700-mV voltage drop, so the buck converter would not be able to maintain the 5-V_{OUT} system voltage. With the smart diode solution, the buck will still receive close to 5 V during this condition and can continue to operate.

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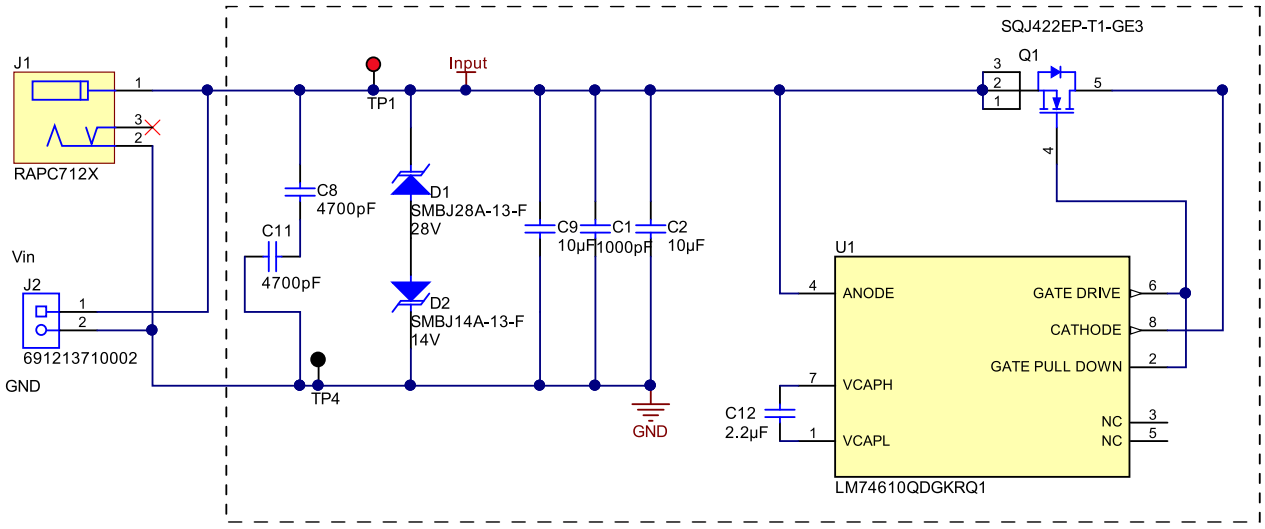

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Figure 20. Reverse Battery Protection Schematic

2.2.1 MOSFET

The LM74610-Q1 product folder has tools to help simulate using the WEBENCH® Design simulator tool. The datasheet also outlines MOSFET selection in the LM74610-Q1 datasheet (SNOSCZ1). Important characteristics it recommends to design around are:

- Continuous drain current (I_D)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Gate-to-source threshold voltage ($V_{GS(TH)}$)
- Drain-to-source on resistance ($R_{DS(ON)}$)

I_D must exceed the load current that in this system is 3 A t ($I_D > I_{LOAD}$) and the body diode maximum current $I_S \geq (I_D$. Also the gate-to-source threshold voltage must be $V_{GS(TH)} \leq 3$ V. The NFET outlined in Table 2 was selected for this application.

Table 2. MOSFET Parameters

Automotive N-Channel 40 V (D-S) 175 °C MOSFET (SQJ422EP)					
PARAMETER	**COMMENTS**	**MIN**	**TYP**	**MAX**	**UNIT**
I_D	Drain-to-source current			75	A
V_{DS}	Drain-to-source voltage			40	V
$V_{GS(TH)}$	Gate-to-source voltage	1.5	2.5	2.5	V
$R_{DS(ON)}$	Drain-to-source on resistance at V_{GS} = 4.5 V		4.3		mΩ

2.2.2 Input Capacitors

Due to the possibility of this subsystem PCB flexing, the likelihood of mechanical short increases. If this were to occur, then there would be a short between the two terminals of the battery. To mitigate this, the two input capacitors are placed in series but rotated 90 degrees to one another in case the vibration in an automotive system causes one capacitor to crack. There are options from some component manufacturers for an integrated solution using automotive grade multilayer ceramic capacitors (MLCC) but for this solution discrete components were used.

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2.2.3 TVS Input Diodes

Although the TVS diodes used in this TI Design are not required by the LM74610-Q1, as outlined in the LM74610-Q1 datasheet (SNOSCZ1), they are used to clamp the positive and negative voltage surges that might occur in the input. These transients are outlines in the ISO specification ISO 7637-2:2004 pulses 1 and 2a. An LC filter is also used downstream. Because this system must remain in operation during such transient conditions, this TI Design focuses on maintaining a fully functional system while transients may be present.

Two specifications that need to be considered are breakdown voltage and clamping voltage:

- Breakdown voltage is the voltage when the TVS diode goes into avalanche similar to a Zener diode and is specified at a low-current value (typically 1 mA).
- Clamping voltage is the voltage the TVS diode clamps to in high current pulse situations.

Table 3 shows these parameters for the selected diodes.

Table 3. TVS Diode Parameters

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
D1: SMBJ28A					
V_{RWM}	Reverse standoff voltage		28.0		V
V_C	Clamping voltage			45.4	V
V_{BR}	Breakdown voltage	31.1		35.8	V
D2: SMBJ14A					
V_{RWM}	Reverse standoff voltage		14.0		V
V_C	Clamping voltage			23.2	V
V_{BR}	Breakdown voltage	15.6		17.9	V

The diode breakdown voltages should be chosen such that transients are clamped at the voltages that will protect the MOSFET/rest of the system. In Figure 21, the positive clamping diode D1 will clamp above double battery (jump-start) and clamped load dump voltages, but lower than the maximum operating voltage of the downstream devices. In this case, it will start to clamp around 28 V but has a maximum clamp voltage just below 40 V. Ideally, somewhere around 36 V, which is why D1 was chosen for its maximum clamping voltage.

The reverse clamping diode D2 should clamp all negative voltages greater than the battery voltage so that it does not short out during a reverse-battery condition. Because the battery voltage is likely to be 14 V, D2 was selected to block all negative voltages greater than this voltage.

In regard to power levels for TVS diodes, the particular package used is SMBJ and supports 600-W peak power levels. This is sufficient for ISO 7637-2 pulses and suppressed load dump case (ISO-16750-2 pulse B). For unsuppressed load dumps (ISO-16750-2 pulse A), higher power TVS diodes such as SMCJ or SMDJ may be required. For more information, see the LM74610-Q1 datasheet (SNOSCZ1) for more information about designing the TVS diodes for this application.

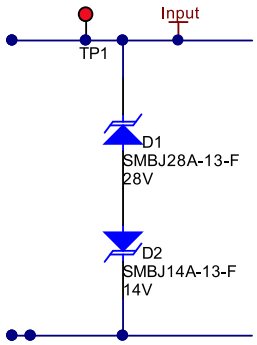

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Figure 21. TVS Input Diodes

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2.2.4 LC Filter and Output Capacitors

After the LM74610, an LC filter was used for two main functions:

1. To prevent EMI
2. To prevent high-frequency voltage on the power line from passing through to the power supply regulator

For EMI filter designs, it is important to determine the attenuation and appropriate cutoff frequency in order to properly calculate the capacitor and inductor values. For further clarification, see the *AN-2162 Simple Success With Conducted EMI From DCDC Converters* Application Report (SNVA489).

Because the regulator is switching at 2.1 MHz, it is recommended to set the cutoff frequency to be approximately 1/10 f_{SW}. The cutoff frequency is set to:

$$f_C = 210\ \text{kHz} = \frac{1}{2\pi\sqrt{LC}}$$

and common values were chosen for C3 and LF1 (10 µF and 100 nH, respectively).

The cutoff frequency as a result is shown in Figure 22.

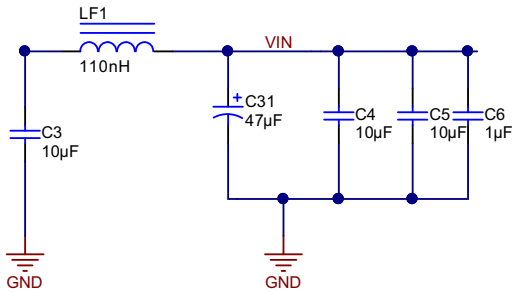

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Figure 22. LC Filter

2.3 Power Supply

The LM53635 was chosen for its optimization for automotive applications. The LM53635 meets many of the requirements needed for automotive applications such as:

- Wide V_{IN} operation with transient tolerance up to 42 V
- Wettable flanks
- Spread spectrum
- Switching frequency outside AM band (2.1 MHz)
- Low EMI and switch noise
- External frequency synchronization
- AEC-Q100 automotive qualified

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The design parameters used in the LM53635-Q1 DC-DC and TLV70033-Q1 LDO are outlined in the spreadsheet and in Figure 23, Figure 24, and Table 4.

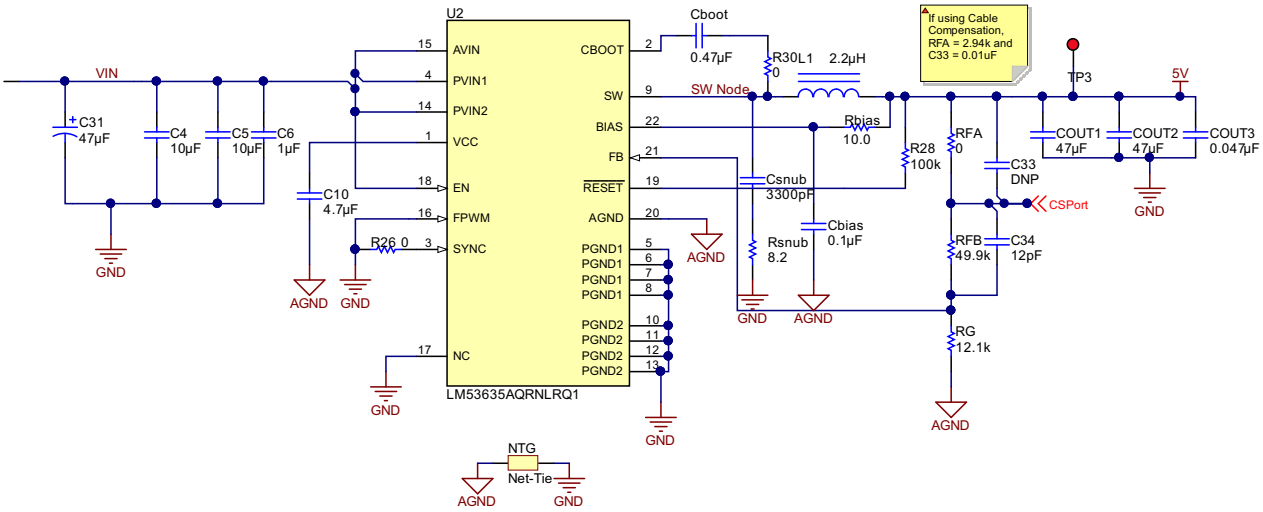

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Figure 23. DC-DC LM53635-Q1 Schematic

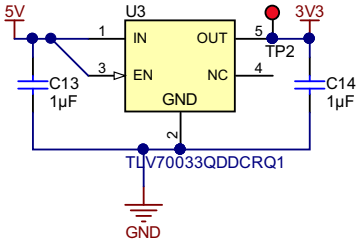

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Figure 24. LDO TLV70033-Q1 Schematic

Table 4. Power Supply Design Spreadsheet Parameters

PARAMETER	COMMENTS	MIN	TYP	MAX	UNIT
System operation					
V_{IN}	Input voltage	5.5	14.5	36	V
F_{SW}	Switching frequency	1.85	2.1	2.35	MHz
Output voltages					
V_{DC-DC}	DC-DC system output voltage	4.8	5	5.2	V
V_{LDO}	LDO output voltage		3.3		V
Output current					
$I_{OUT\ DC-DC}$	DC-DC		3		A
$I_{OUT\ LDO}$	LDO load current		100		mA
Component values					
L1	Inductor		2.2		µH
C_{IN}	Input capacitance		68		µF
C_{OUT}	Output capacitance		94		µF

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2.3.1 Input Capacitor Selection

Typically ceramic capacitors are used at the input of a power supply because they provide a low-impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. Because the input of the regulator could see voltages up to 40 V, the rating of the capacitors needs to accommodate these voltages (see Table 5). Consequently, a bulk capacitor of 47 µF was used to meet the necessary input capacitance for ripple current and switching noise isolation. In addition, small high-frequency bypass capacitors connected directly between the VIN and PGND pins are used to reduce noise spikes and aid in reducing conducted EMI. Additional high-frequency capacitors can be used to help manage conducted EMI or voltage spike issues that may be encountered. The following calculations help determine the right input capacitance to use.

Table 5. Input Capacitor Selection

NOMINAL CAPACITANCE	VOLTAGE RATING	ESR	PART NUMBER
47 µF	63 V	650 mΩ	EEE-FK1J470P
2 × 10 µF	50 V	1 mΩ	GRM32ER71H106KA12L
1 µF	50 V	1 mΩ	UMK107AB7105KA-T

The input capacitors must be able to handle both the RMS current $I_{RMS(CIN)}$ and the dissipated power $P_{D(CIN)}$. The following input capacitor was picked for bulk capacitance.

$I_{RMS(CIN)}$ and $P_{D(CIN)}$ can be calculated as:

$$I_{RMS(CIN)} = I_O \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} = 1.43 \text{ A}$$

$$P_{D(CIN)} = I^2RMS_{CIN}R_{ESR(CIN)} = 3 \text{ mW}$$

where:

- I_O = 3 A
- V_{OUT} = 5 V
- V_{IN} = 14.5 V

and the effective ESR of all the input capacitors is $R_{ESR(CIN)}$ = 1.5 mΩ.

The input ripple voltage can be calculated as:

$$V_{PP(IN)} = \frac{I_{OUT}D}{C_{IN}F_S} + I_{OUT}ESR_{CIN} = 11.7 \text{mV}$$

where:

- Duty cycle D = 0.345
- C_{IN} = 68 µF
- F_S = 2.1 MHz

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2.3.2 DC-DC Inductor Selection

Recommendations are made in the LM53635-Q1 datasheet (SNVSAA7). The optimal inductance for the LM53635-Q1 at a 5-V output is 2.2 µH (see Table 6) because this provides 20% or 30% ripple current at the full load current and keeps the internal compensation stable.

The important parameters that the inductor selection recommends is to make sure the saturation current is at least 7 to 8 A and the parasitic resistance is as low as possible to reduce losses.

The following inductor was chosen for this particular application because it is 2.2 µH, has a sufficient saturation current, low parasitic resistance, and is a small footprint for this small solution size.

Table 6. Inductor Selection

NOMINAL INDUCTANCE	SATURATION CURRENT	DCR	PART NUMBER
2.2 µH	9 A	35 mΩ	SRP5030T-2R2M

2.3.3 Output Voltage and Capacitor Selection

The LM53635-Q1 is optimized to work with low-ESR ceramic capacitors such as X5R or X7R ceramic capacitors. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors, however, have very low ESR, stay capacitive up to high frequencies, and the inductive component can be usually neglected.

Ultimately, the capacitor helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

It is good practice to target output peak-to-peak ripple voltage $V_{OUT\_Ripple\_PP}$ to be within ±5% but adding more output capacitance is used to improve transient performance. It is still important to limit the maximum value of total output capacitance to between 300 and 400 µF because higher capacitance could disrupt the start-up of a regulator or the loop stability. The values for output capacitors can be seen in Table 7.

Table 7. Output Capacitor Selection

NOMINAL CAPACITANCE	VOLTAGE RATING	ESR	PARTNUMBER
2 × 47 µF	10 V	1 mΩ	GRM32ER71A476KE15L
0.047 µF	25 V	1 mΩ	GCM188R71E473KA37D

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2.4 Legacy Charge Controller

The TPS254900-Q1 was chosen for its optimization for automotive applications. The TPS254900 meets many of the requirements needed for automotive applications such as:

- Supports VBUS, D+, D– short-to-battery protection
- Cable compensation (although not used in this TI Design)

The operation of the charging over the Type-C port circuit depends on the TPS254900 presented in Figure 25 for providing the electrical signatures on D+/D– to support BC1.2 CDP compliant charging.

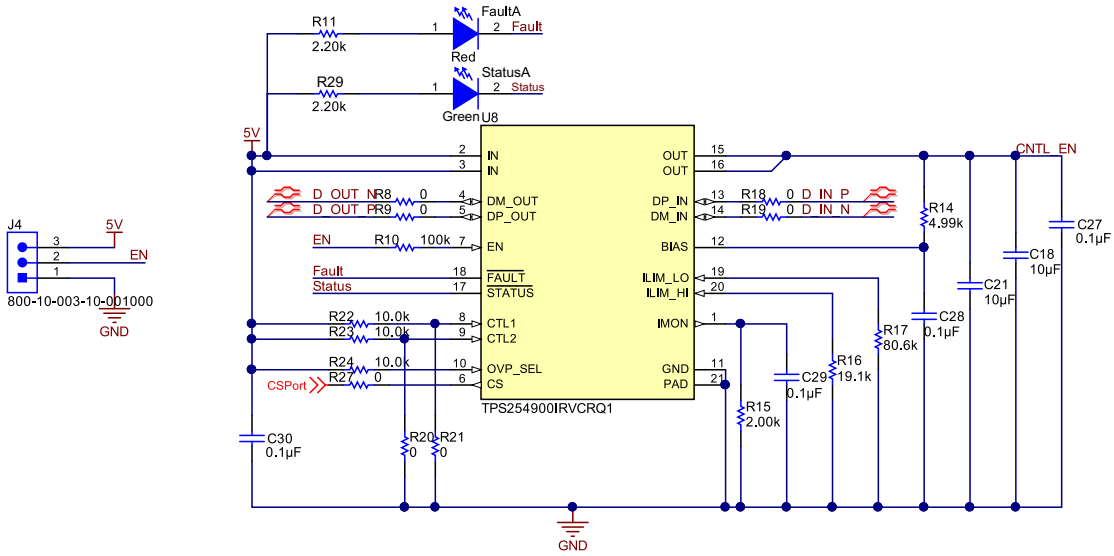

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Figure 25. TPS254900-Q1 Legacy Charge Controller Schematic

The internal switch of the TPS25810 is connected between the 5-V power source and the Type-C connector VBUS, while the TPS254900 internal switch is not connected. The TPS254900 OUT pins are connected to the TPS25810 EN to control the VBUS discharge. A CDP port is a USB port that follows USB BC1.2 requirements and supplies a minimum of 1.5 A per port. It provides power and meets USB2.0 requirements for device enumeration. USB2.0 communication is supported, and the host controller must be active to allow charging. What separates a CDP from an SDP is the host-charge handshaking logic that identifies this port as a CDP. A CDP is identifiable by a compliant BC1.2 client device and allows for additional current draw by the client device.

As noted in Figure 25, CTL1 and CTL2 are connected through R20, R21, R22, and R23 (R20 and R21 are not populated) for the configuration of SDP, SDP1, or CDP mode. See Table 8 for the configurations.

Table 8. CTL1 and CTL2 Configurations

CTL1	CTL2	MODE	$\overline{\text{FAULT}}$ REPORT	NOTES
0	0	Client	OFF	Power switch is disabled, only analog switch is on
0	1	SDP	ON	Standard SDP
1	0	SDP1	ON	No OUT discharge between CDP and SDP1 for port power management (PPM)
1	1	CDP	ON	No OUT discharge when changing between 10 and 11

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2.4.1 Additional Features of TPS254900

This part was particularly chosen for its USB2.0 data support and integrated short-to-battery protection. Additionally, this part can support remote media hubs because of its cable compensation feature through the CS pin. This particular feature was not used in this TI Design because the higher current power switch from the Type-C Controller was used on VBUS instead. In cases where the TPS254900 power switch would be sufficient, the cable compensation feature could be used and the configuration seen in Figure 26 could be implemented.

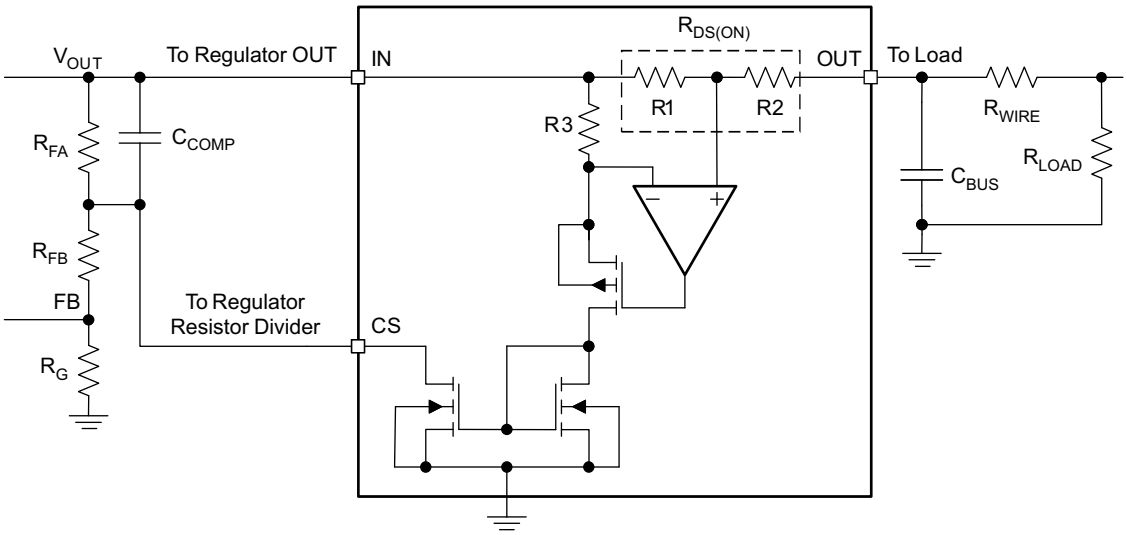

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Figure 26. Cable Compensation Design

2.4.2 Why Cable Compensation?

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. In the vehicle from the voltage regulator 5-V output to the VPD_IN (input voltage of portable device), the total resistance of power switch $R_{DS(ON)}$ and cable resistance causes an IR drop at the PD input. So the charging current of most portable devices is less than their expected maximum charging current.

The TPS254900-Q1 detects the load currents and sets a proportional sink current that can be used to adjust output voltage of the up-stream regulator to compensate the IR drop in the charging path. The gain G_{CS} of sink current proportional to load current is 75 µA/A.

To design the feedback network on the regulator, the following calculations can be used:

- Choose R_G according to the voltage regulator guidelines.
- Calculate R_{FA} as:

$$R_{FA} = \frac{\left(R_{DS(ON)} + R_{WIRE}\right)}{G_{CS}}$$

  where :

  – R_{WIRE} is typically 80 mΩ to 120 mΩ/m, up to 3 m long
  – G_{CS} = 75 µA/A

- Calculate R_{FB} as:

$$R_{FB} = \frac{V_{OUT}}{\left(V_{FB} / R_G\right)} - R_G - R_{FA}$$

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2.5 Type-C Charge Controller

The TPS25810-Q1 (Figure 27) was chosen for meeting key specifications for this TI Design. Important specs include:

- USB Type-C compliant DFP control
- 3-A current advertisement on CC lines
- Programmable 3.4-A I_{LIMIT}
- USB3.0 MUX control

Although there are a variety of features that the TPS25810 is capable of, such as $\overline{\text{LD\_DET}}$, $\overline{\text{DEBUG}}$, and $\overline{\text{AUDIO}}$, the main features that this TI Design uses are:

- REF/REF_RTN
- CHG/CHG_HI
- $\overline{\text{POL}}$
- $\overline{\text{UFP}}$
- $\overline{\text{FAULT}}$

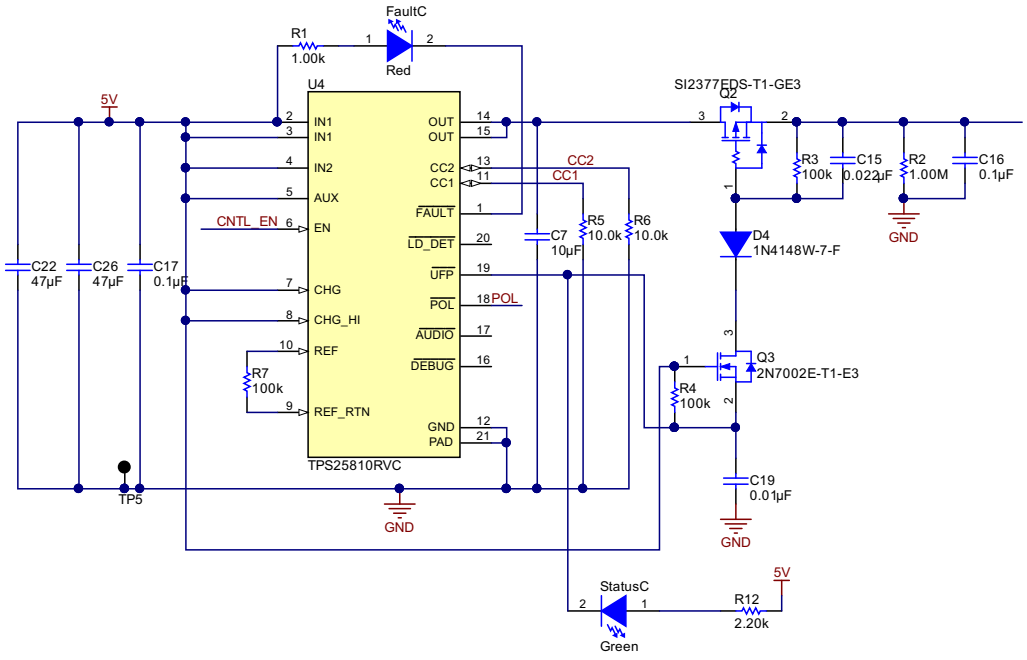

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Figure 27. TPS25810 Type-C Controller Schematic

2.5.1 REF/REF_RTN

A 100-kΩ resistor is connected between the REF and REF_RTN pins. These pins set the reference current required to bias the internal circuitry. The overload current limit tolerance and CC currents depend upon the accuracy of this resistor, so it is important to use an accurate ±1% resistor.

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2.5.2 CHG/CHG_HI

There are three types of Type-C current advertisements defined in the USB Type-C standards and the TPS25810 supports all of them. In this TI Design, both CHG and CHG_HI are set high (see Table 9) meaning that the broadcast capability of the CC lines is 3 A. The load detect threshold associated with this level is 1.95 A; however, the $\overline{\text{LD\_DET}}$ function is not used in this TI Design because it is meant for systems with multiple charging ports. In systems where $\overline{\text{LD\_DET}}$ is not needed, pulling the pin low or leaving it open is sufficient.

Table 9. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

2.5.3 Plug Polarity Detection: $\overline{\text{POL}}$

Reversible Type-C plug orientation is reported by the $\overline{\text{POL}}$ pin when a UFP is connected. However, when no UFP is attached, $\overline{\text{POL}}$ remains de-asserted irrespective of cable plug orientation. Table 10 describes the $\overline{\text{POL}}$ state based on which device CC pin detects V_{RD} from an attached UFP pulldown. In this TI Design, the $\overline{\text{POL}}$ pin is connected to the SEL of the HD3SS3212 to control the multiplexing of the SuperSpeed T_x and R_x lanes.

Table 10. Plug Polarity Detection

CC1	CC2	$\overline{\text{POL}}$	STATE
Rd	Open	High-impedance	UFP connected
Open	Rd	Asserted (pulled low)	UFP connected with reverse plug orientation

2.5.4 Protecting TPS25810 from High-Voltage DFPs

When a UFP device is attached to the port that the TPS25810 is on, the TPS25810 applies power to VBUS. A concern in USB Type-C applications (Figure 28) is that a non-compliant DFP device that disregards the USB Type-C specification can be connected to the port controlled by the TPS25810. Such a device may apply a voltage above the absolute maximum rating of the TPS25810, which could damage the part. The circuit designed for protecting against these types of situations will be discussed in Noncompliant DFP Protection but for more information, see the *Protecting the TPS25810 from High Voltage DFPs* Application Report (SLVA751).

Noncompliant DFP Protection

The circuit in Figure 27 is used to block against noncompliant DFP devices. Its operation depends upon turning on and off the PFET (Q2) using the $\overline{\text{UFP}}$ signal from the TPS25810. When a compliant UFP device is plugged in, the $\overline{\text{UFP}}$ pin on the TPS25810 pulls low that turns on the PFET. However, if a non-compliant DFP device is plugged in that offers > 5 V without first going through the proper power negotiation, $\overline{\text{UFP}}$ stays in high-impedance. Thus, the PFET does not get turned on and the high voltage on the VBUS is not transferred to the OUT pin of the TPS25810. Q3 serves as a cascade device and protects the $\overline{\text{UFP}}$ pin from going above 5 V. This is important because the gate of Q2 is 20 V when 20 V is applied to VBUS, and the absolute maximum of the TPS25810 pins is 7 V. The 1N4148 diode, D4, is used to limit leakage current through Q3 that could result in unwanted voltage on VBUS or the OUT pin. R2 is used to discharge the voltage on the VBUS line when a device is disconnected. This must be done in order to comply with the USB Type-C specification that the voltage must discharge to 0.8 V within 650 ms. C16 is used to prevent the parasitic turn on of the PFET during a hot plug event. C19 is used to suppress transients on the $\overline{\text{UFP}}$ pin of the TPS25810.

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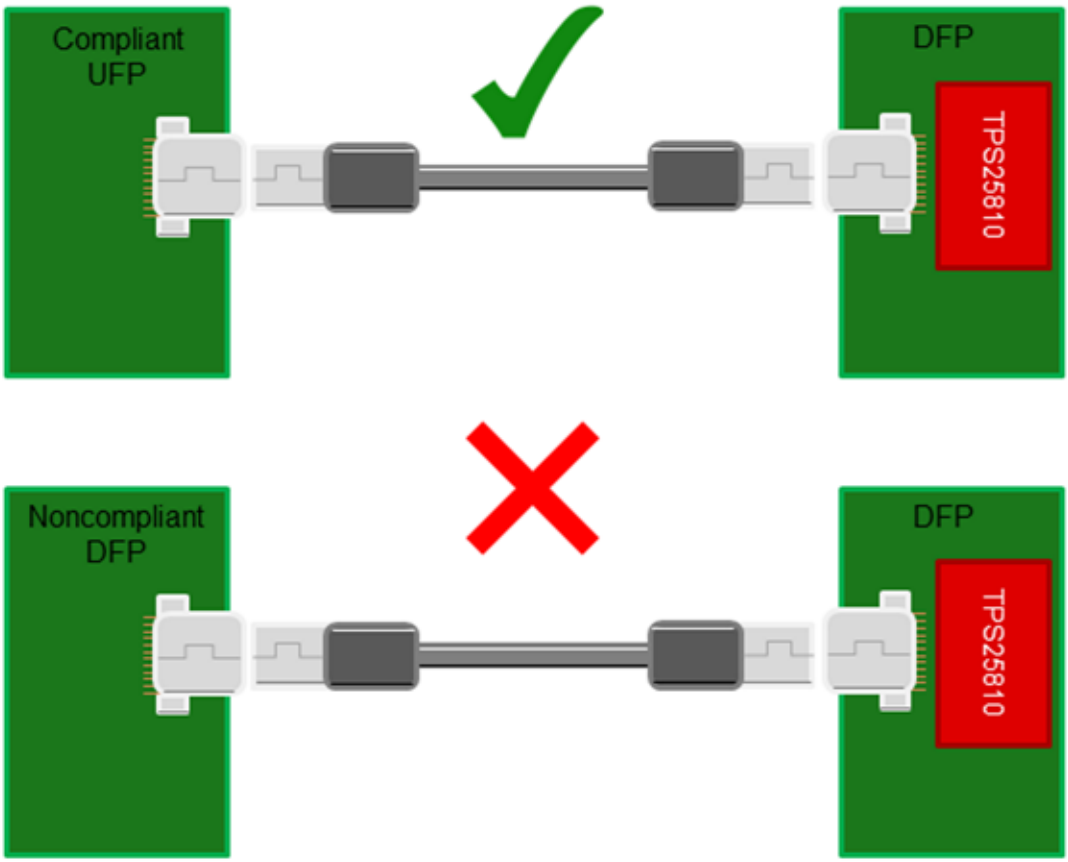

Figure 28. Correct Operational Configuration

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2.6 SuperSpeed MUX

The HD3SS3212 two-channel MUX was chosen for its specific capabilities to multiplex the four T_x and four R_x lines into two T_x and two R_x lines at data rates up to 5 Gbps. Unlike legacy devices that have fewer or slower data lines, the Type-C connector has mirrored data lines in order to maintain the connections flip-ability resulting in eight lanes that need to be consolidated into four T_x+/T_x– and R_x+/R_x– lanes. Figure 29 is a schematic of the MUX.

In Table 11, the polarity of the signals does not match the polarity of the pins. This is to aid in a more streamlined board routing that is discussed further in Section 5.3.6. The HD3SS3212 is able to tolerate polarity inversions for any of the differential signals as long as all of the polarities for A, B, or C ports are also switched. In this TI Design, the B0 and C0 polarities are switched, so the A0 polarities of the output of the MUX are also switched.

For additional design considerations regarding the HD3SS3212, see the HD3SS3212x datasheet (SLASE74).

Table 11. T_x/R_x Signal Pinout

	PIN							
	19	18	17	16	15	14	13	12
PIN NAME	B0p	B0n	B1p	B1n	C0p	C0n	C1p	C1n
SIGNAL NAME	TX2_N	TX2_P	RX2_P	RX2_N	TX1_N	TX1_P	RX1_P	RX1_N

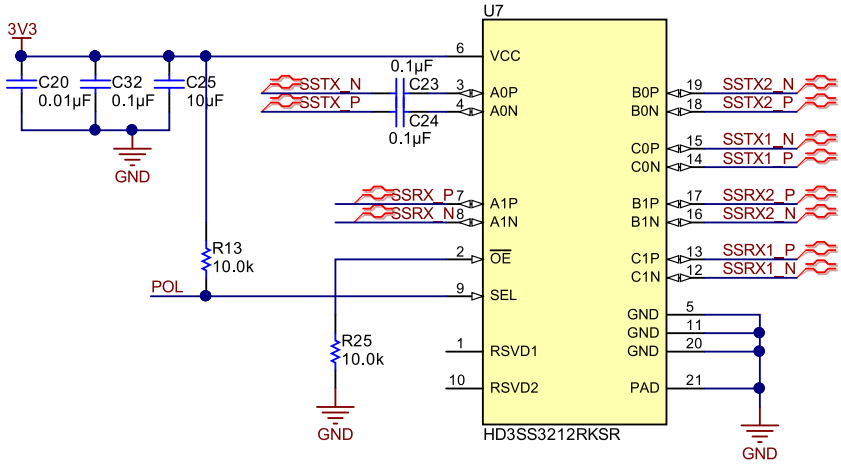

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Figure 29. HD3SS3212 SuperSpeed MUX Schematic

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3 Getting Started

To get started, two options are given to power up the board: the AC adapter barrel connector or the screw terminals. Both connections are capable of powering the board but allow testing flexibility with whatever connection is available.

1. Connect preferred power supply. Input voltage can be 5.5 to 36 V and must be capable of up to 3.0 A.
2. Connect the UFP. This can be using one of two options:
   (a) Type-C to Type-C connector (see Figure 30).
   (b) Type-C to a legacy Type-A/Type-B connector (see Figure 31)
3. Optional: Connect the Micro-B 3.0 to the board and a host such as a computer.
   (a) A host is needed for legacy devices to be charged in CDP mode (see Figure 32); otherwise, they revert to SDP mode and only draw 500 or 900 mA depending on USB2.0 or USB3.0 connection. Note that devices such as Apple® iPhones® will not charge unless in CDP mode due to minimum current draw requirements. A Type-C to Type-C connection does not need a connection to a USB host (see Figure 33).
4. When plugged in, a green LED turns on when a compliant device has been connected. Note that some Type-C to Type-A dongles may initiate the LED even without a device plugged in.

Figure 30. Setup: Type-C to Type-C Connection

Figure 31. Setup: Type-C to Legacy Type-A Connection

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Figure 32. Type-A Needs Host Connection for CDP Mode

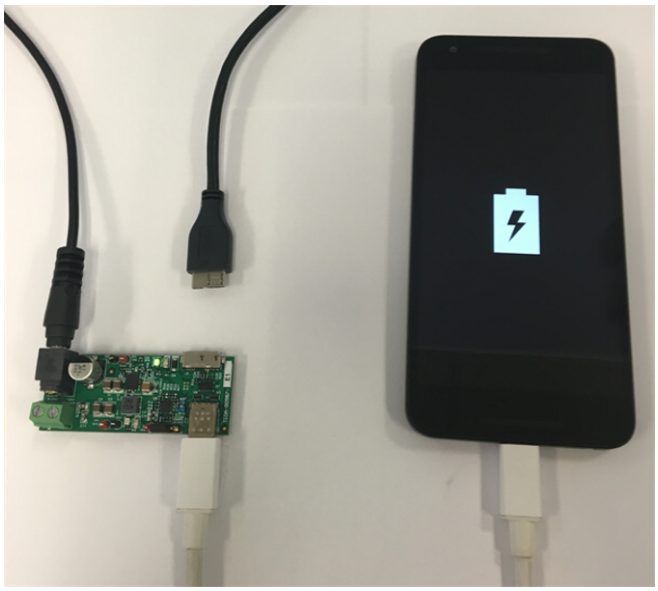

Figure 33. Type-C Does Not Need Host Connection

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4 Testing and Results

The following tests were conducted on the TIDA-00987 to show performance characteristics.

4.1 Power Supply

The following sections outline the tests run on the power supply to analyze performance of the LM53635-Q1.

4.1.1 Output Ripple

In Figure 34, Figure 35, and Figure 36, output ripple was measured across the output capacitor C_{OUT1} of the LM53635-Q1 using a short ground loop connected to the probe. The following measurements were taken with resistive loads resulting in I_{OUT} = 0 A, 500 mA, and 2 A, respectively, with a power supply set to 14.5 V_{IN}.

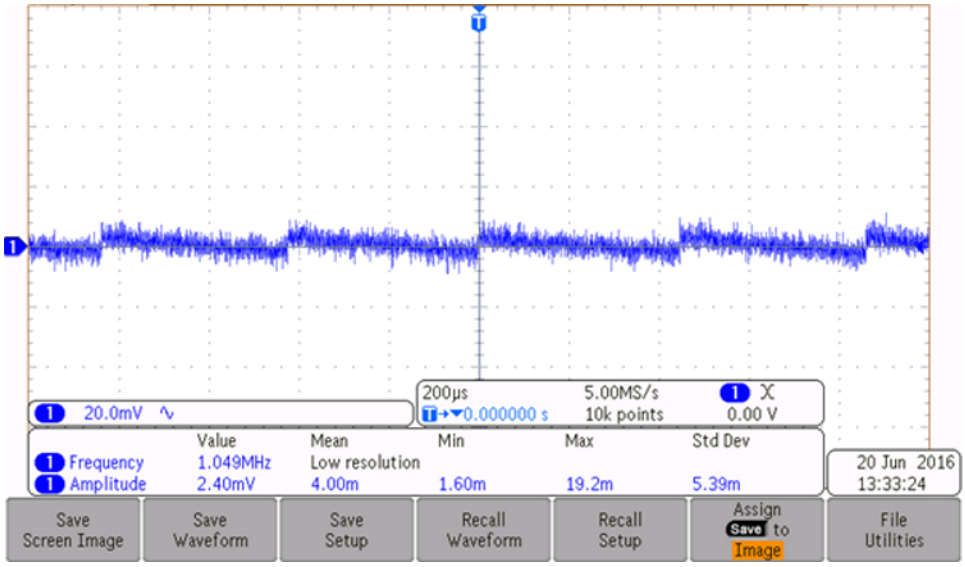

Figure 34. Output Ripple With No Load (2.4 mV)

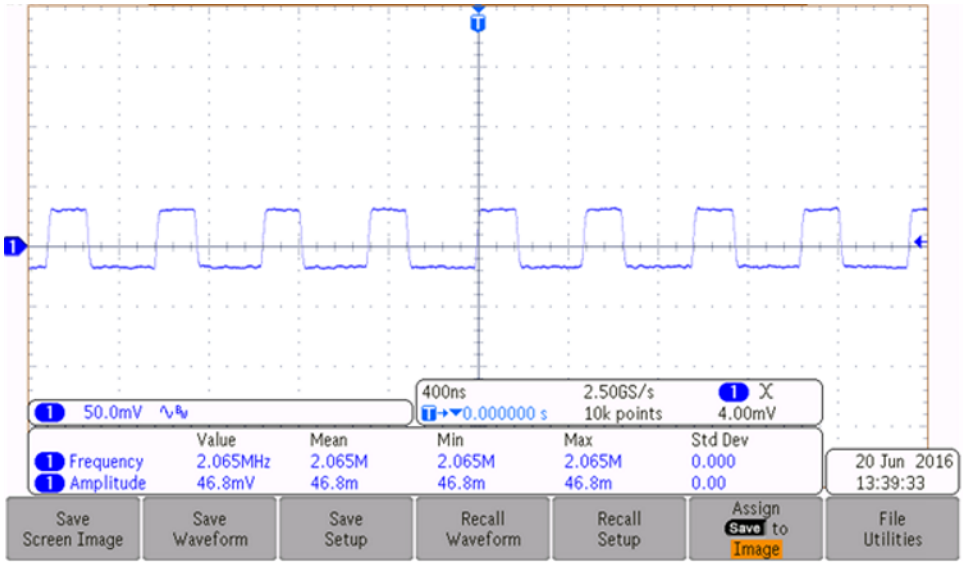

Figure 35. Output Ripple With 500-mA Load Current (46.7 mV)

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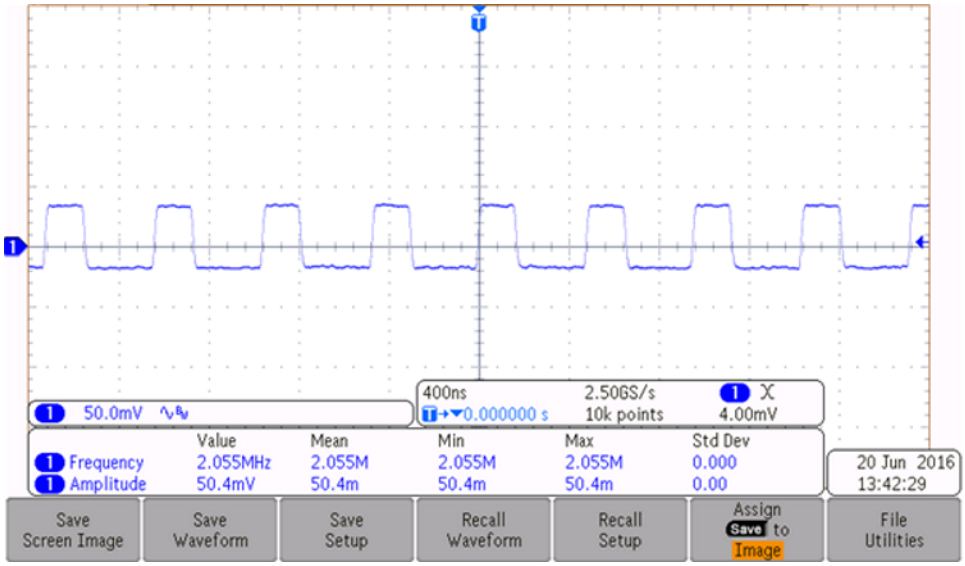

Figure 36. Output Ripple With 2-A Load Current (50.4 mV)

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4.1.2 Start-up and Shutdown

In Figure 37, Figure 38, Figure 39, and Figure 40, start-up and shutdown were measured as in Section 4.1.1 across the output capacitor C_{OUT1} of the LM53635-Q1 using a short ground loop connected to the probe. The following measurements were taken with resistive loads resulting in I_{OUT} = 0 A and 2 A, respectively, with a power supply set to 14.5 V_{IN}.

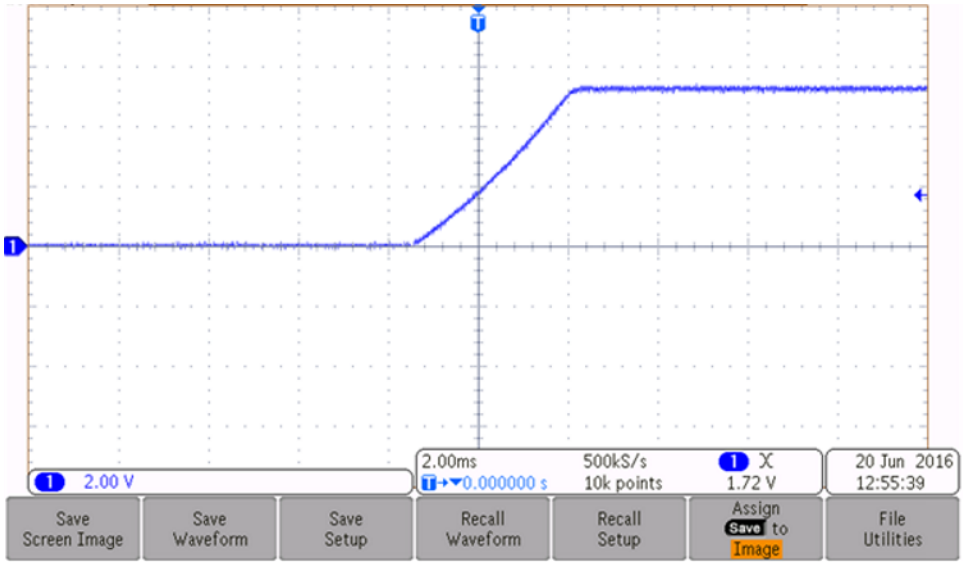

Figure 37. Start-up With No Load (2.4 ms)

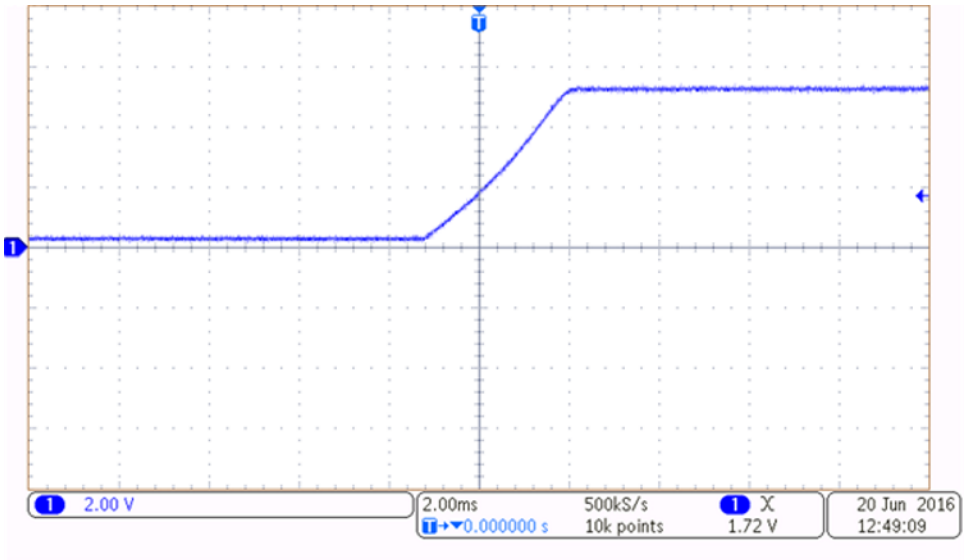

Figure 38. Start-up With 2-A Load Current (2.0 ms)

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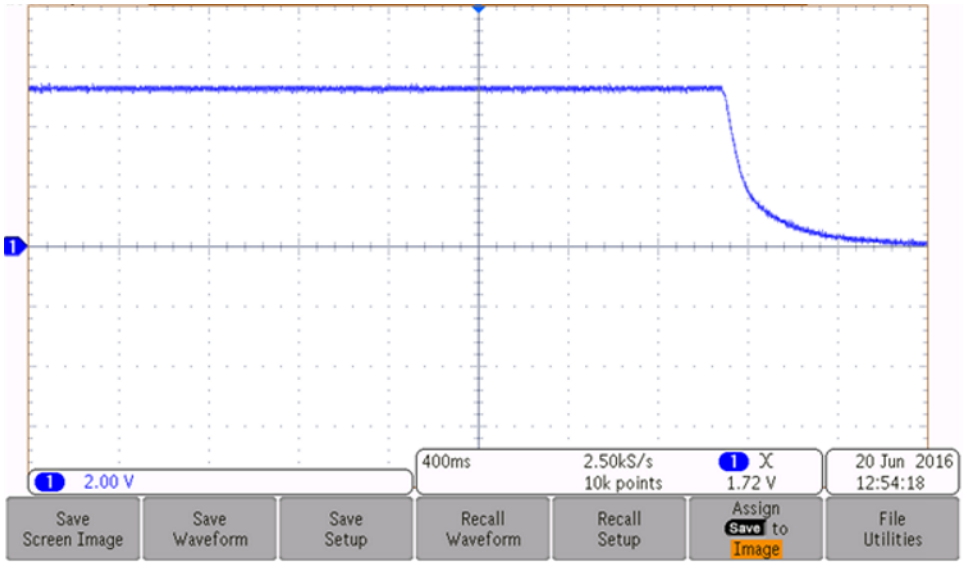

Figure 39. Shutdown With No Load (400 ms)

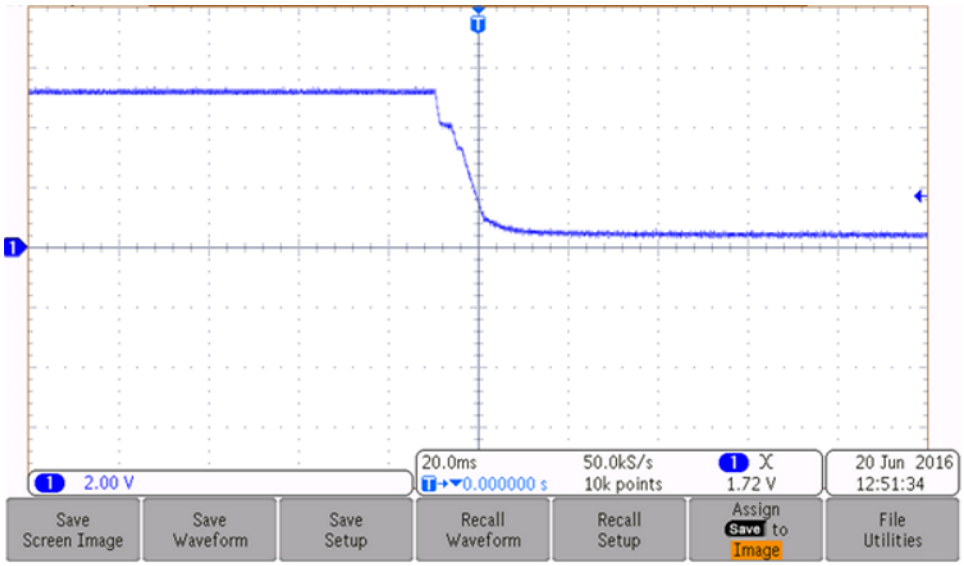

Figure 40. Shutdown With 2-A Load Current (12 ms)

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4.1.3 Switch Node

In Figure 41, Figure 42, and Figure 43, the switch node was measured using a short ground loop connected to the probe. The following measurements were taken with resistive loads resulting in I_{OUT} = 0 A, 500 mA, and 2 A, respectively, with a power supply set to 14.5 V_{IN}.

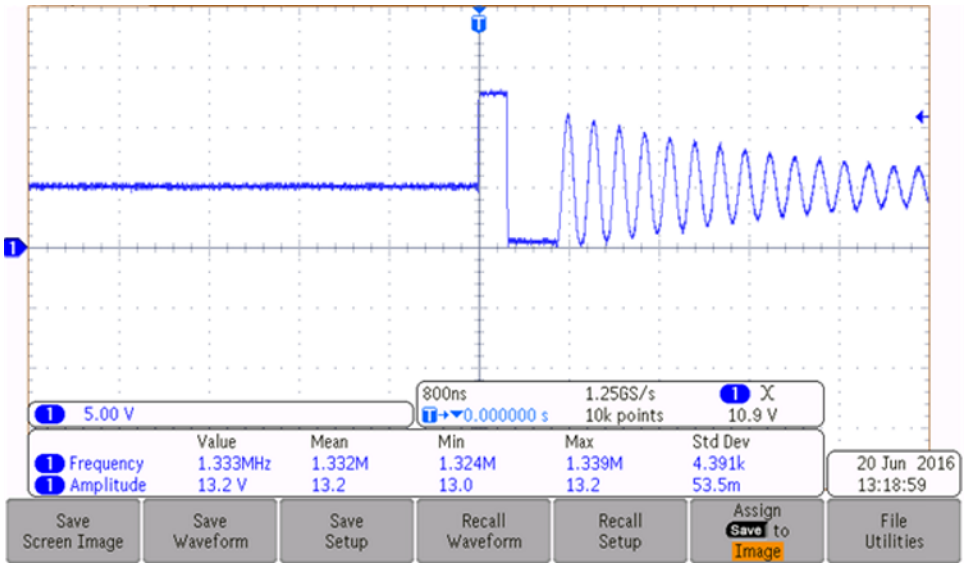

Figure 41. Switch Node With No Load

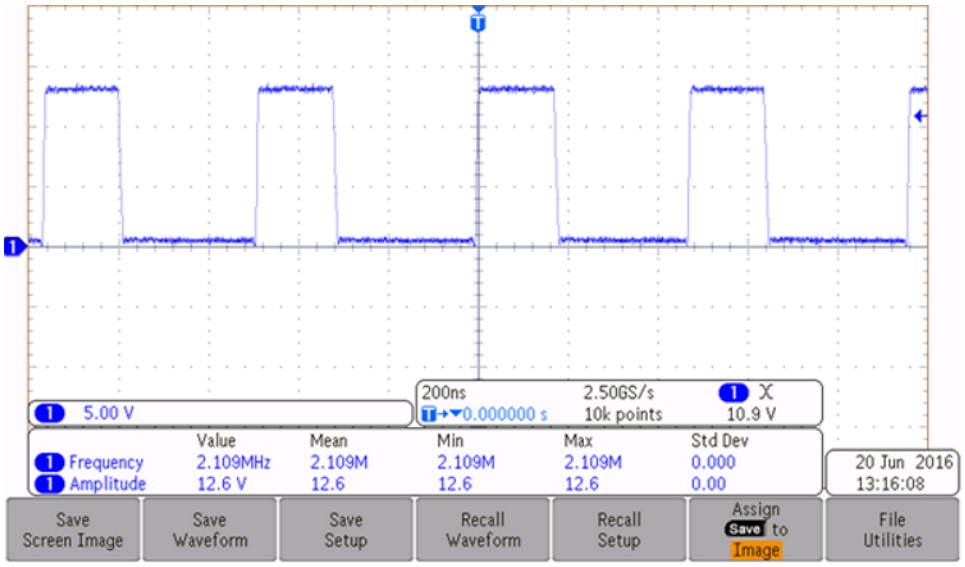

Figure 42. Switch Node With 500-mA Load Current

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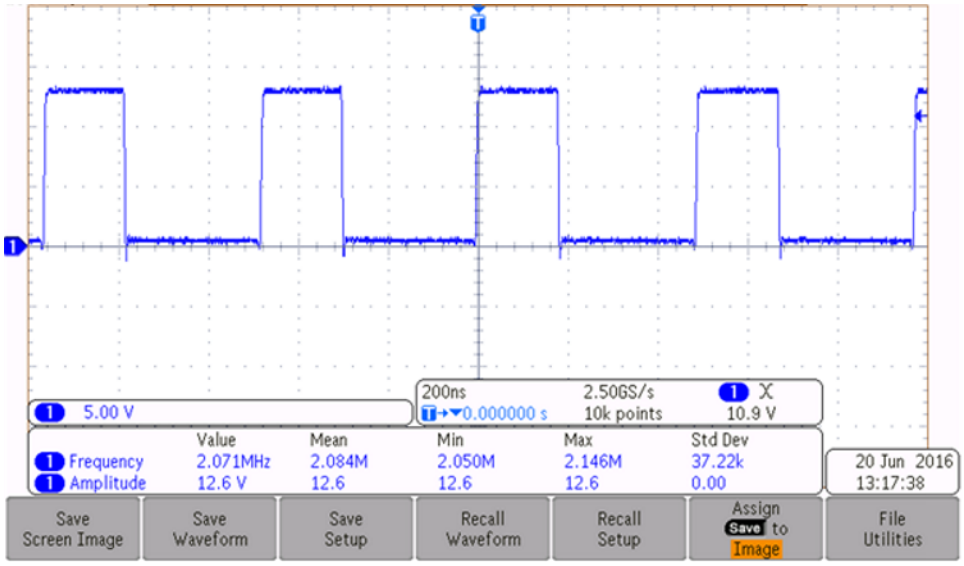

Figure 43. Switch Node With 2-A Load Current

4.1.4 Efficiency

In Figure 45 and Figure 46, the efficiency was measured with four multimeters testing input voltage, input current, output voltage, and load current. A decade box was used as a load. These tests were measured with 12 V_{IN}, 14.5 V_{IN}, and 20 V_{IN}. Due to the voltage drop across wires and additional circuits in the power path, the efficiency was measured directly at the output of the LM53635-Q1 as well as where the load was being applied on an external load board as seen in Figure 44.

Figure 44. Efficiency Measurement Setup

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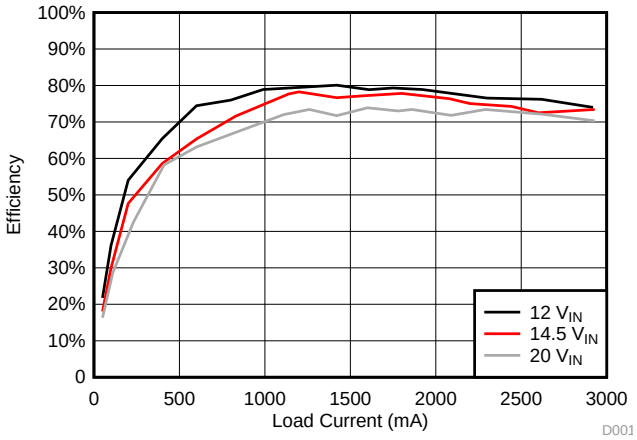

Figure 45. Efficiency After Type-C Switch

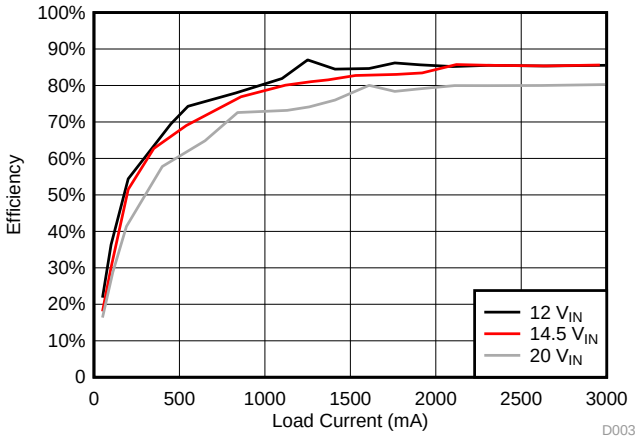

Figure 46. Efficiency at Regulator Output

4.1.5 Load Regulation

In Figure 47 and Figure 48, the load regulation was measured in the same manner as in Section 4.1.4.

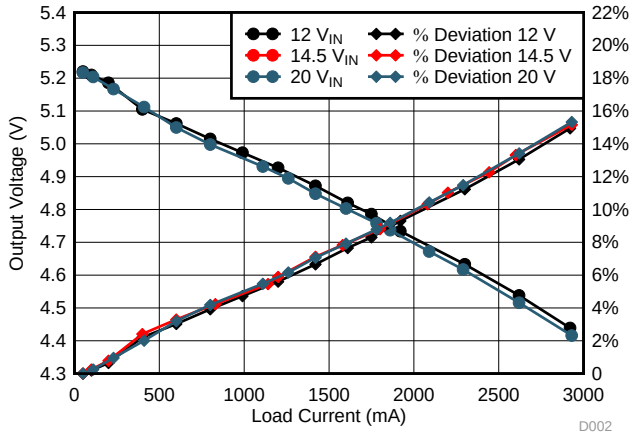

Figure 47. Load Regulation After Type-C Switch

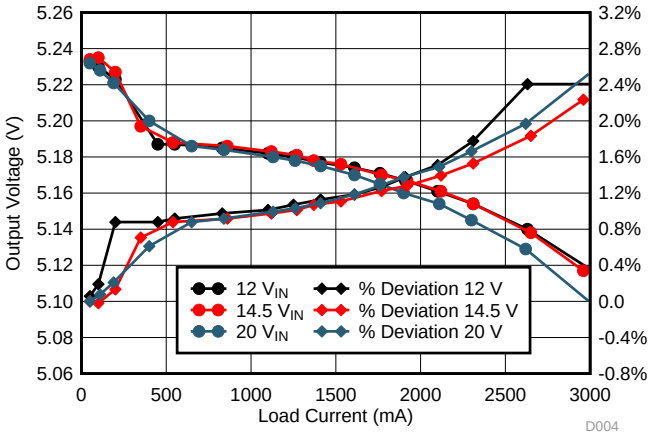

Figure 48. Load Regulation at Regulator Output

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4.2 USB Data Pass Through

To prove that the data pass-through capabilities were not being bottlenecked by the TIDA-00987, a free online USB Flash Speed Tester was used to track read and write capabilities. Using a USB3.0-capable port on a computer, a USB3.0-capable hard drive and USB2.0 flash drive were connected both through the board and then directly to the computer's USB ports as shown in Figure 49.

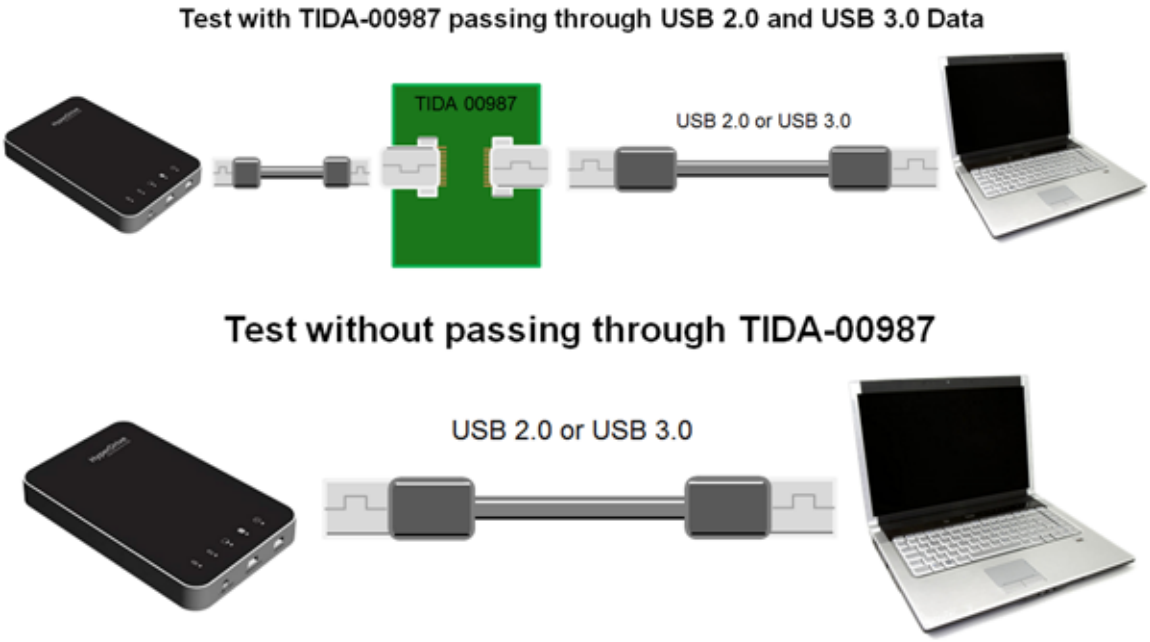

Figure 49. Tests Conducted for Both USB2.0 and USB3.0 With (Top) and Without (Bottom) TIDA-00987

Figure 50, Figure 51, Figure 52, and Figure 53 are results using the USB Flash Benchmark.

The data listed in the right hand corner are the data points from each sample starting with 16 MB and finishing with the last bullet point 1 kB. As it can be seen between the rates for tests done without the TIDA-00987 and with the TIDA-00987, the data is being passed through at a similar, if not identical, speed. Note that although the data rates shown are supposed to be for USB2.0 and USB3.0 (that is, 480 Mbps and 5 Gbps) the rate for both directly plugging into the port as well as passing through the TIDA-00987 is much less than anticipated. As noted in the USB-IF Universal Serial Bus 3.0 Specification, under Section 4.4.11, the "SuperSpeed efficiency is dependent on a number of factors including 8b/10b symbol encoding, packet structure an framing, link level flow control, and protocol overhead. At a 5-Gbps signaling rate with 8b/10b encoding, the raw throughput is 500 Mbps. When link flow control, packet framing, and protocol overhead are considered, it is realistic for 400 MBps or more to be delivered to an application." Furthermore, the device-side controller within the SSD and the host controller within the computer are also limiting factors when it comes to data rate performance. With higher performing host computer and higher performing SSD, the data rates could expect to be much faster than what was tested in this TI Design.

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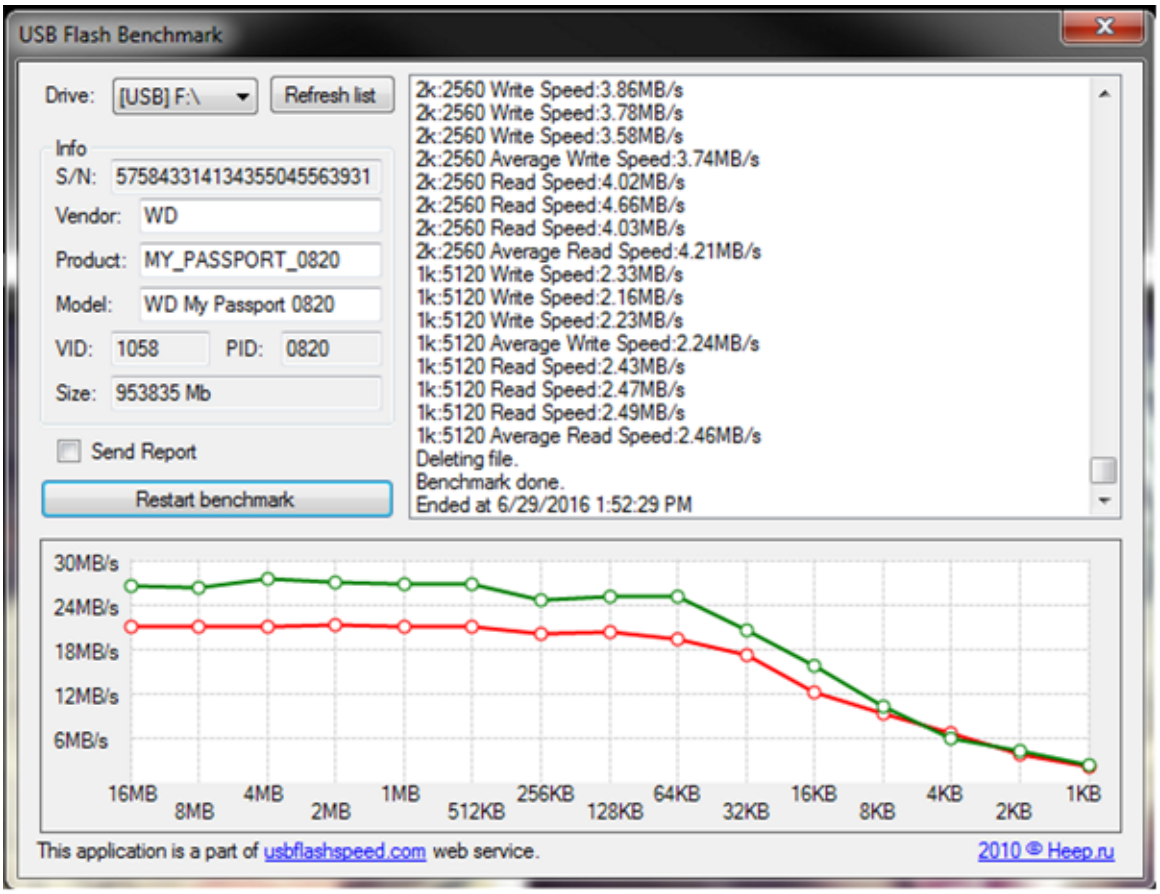

Figure 50. USB3.0 Data Without TIDA-00987

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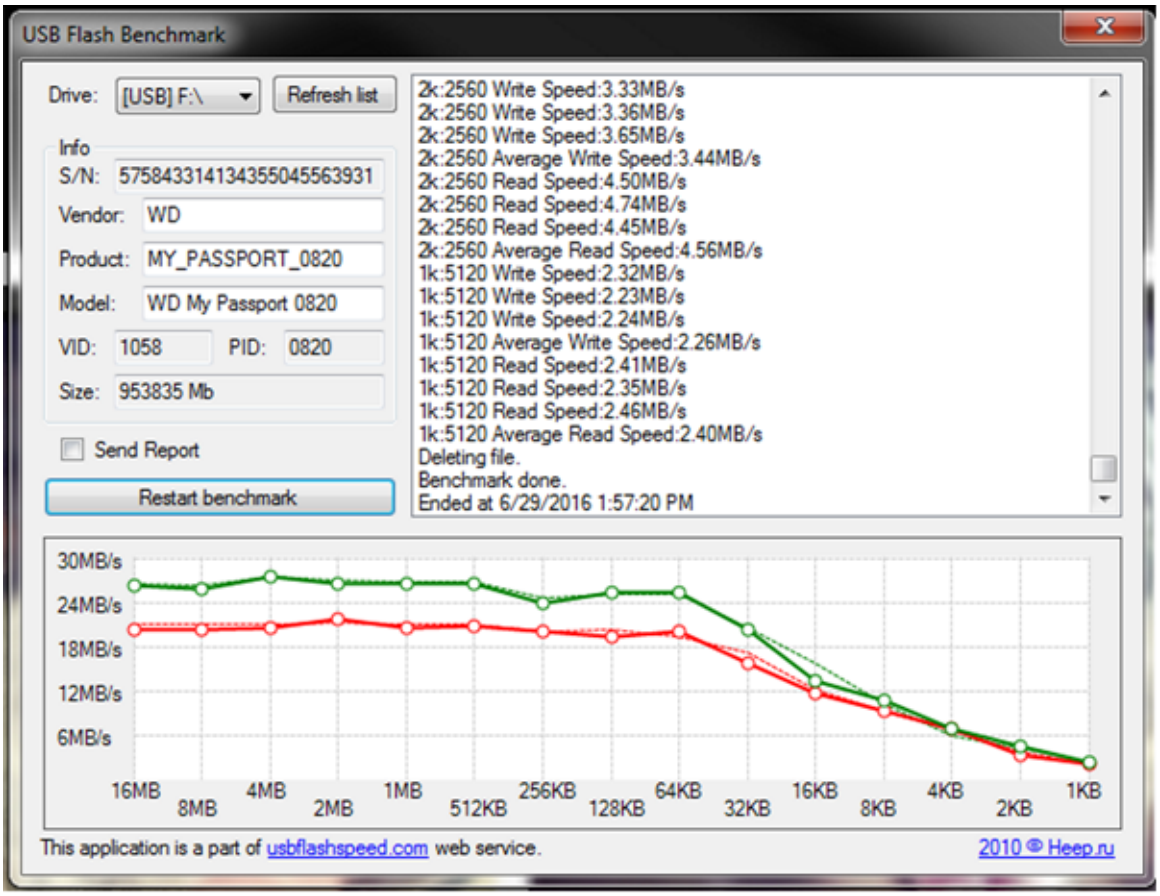

Figure 51. USB3.0 Data With TIDA-00987

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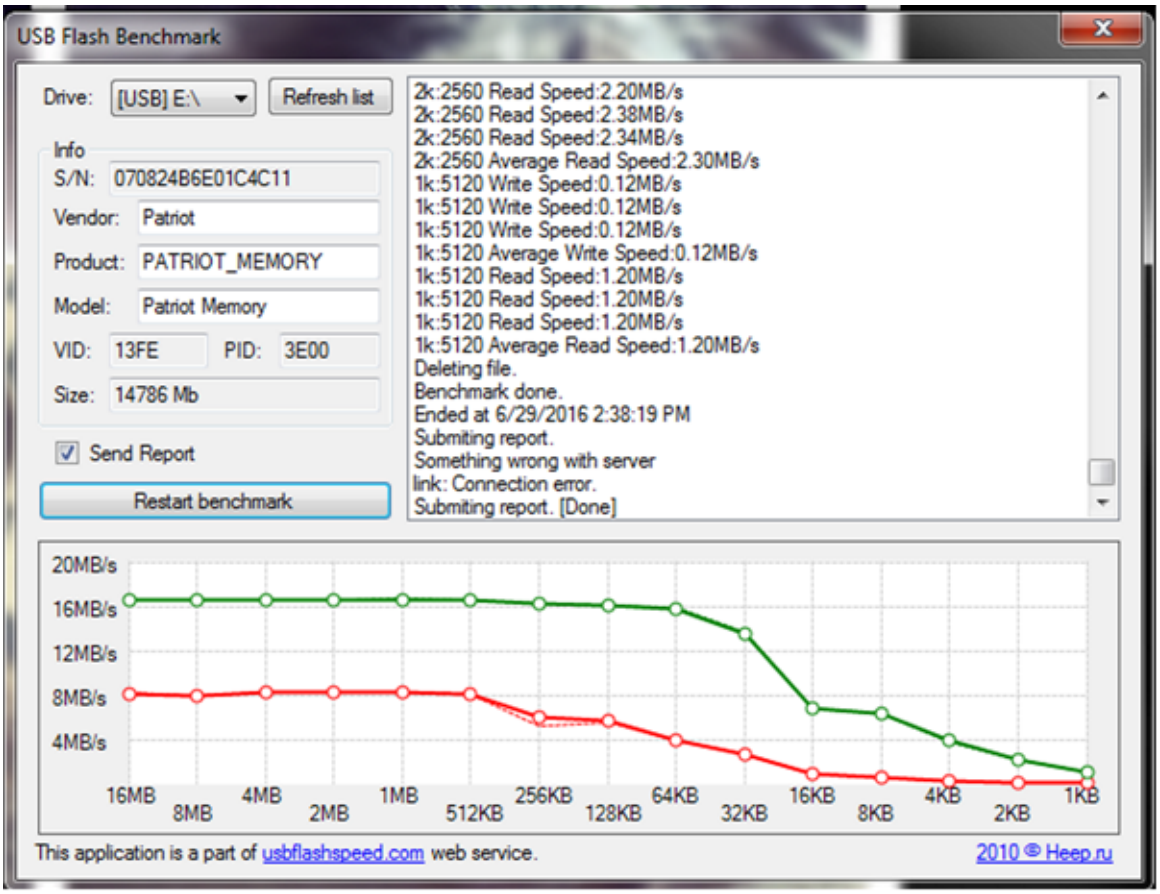

Figure 52. USB2.0 Data Without TIDA-00987

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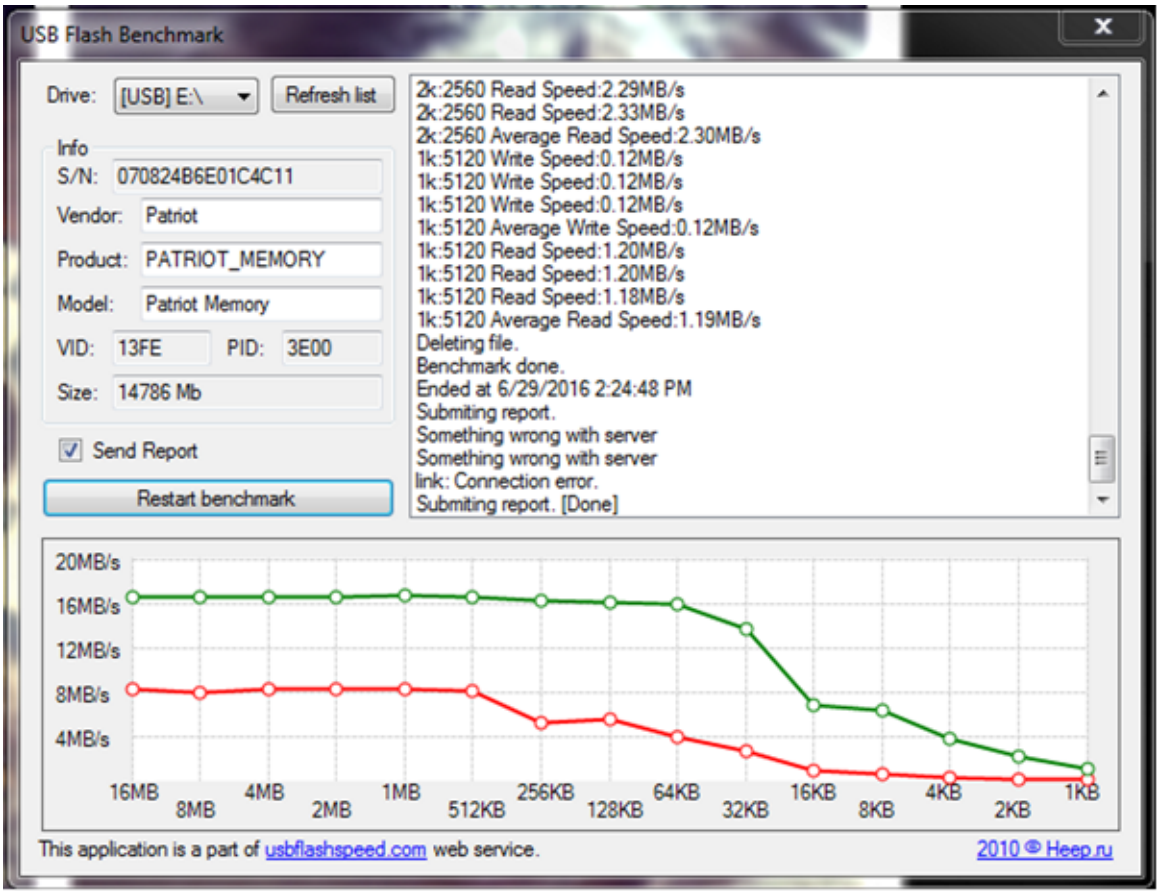

Figure 53. USB2.0 Data With TIDA-00987

4.3 CISPR 25 Class 5

This TI Design was built and tested with the goal to pass CISPR 25 Class 5 standards[18], the strictest of the CISPR classification standards. This CISPR EMI testing was done with a third party facility and follows this international standard "to protect on-board receivers from disturbances produced by conducted and radiate emissions arising in a vehicle" (CISPR 25 Ed. 3.0 b: 2008, pg. 7) meaning that this particular TI Design is tested to make sure that it does not interfere with other equipment in the vehicle. As outlined in the standard, that radiated disturbances do not disrupt the broadcast and mobile service or band. For this particular TI Design, Broadcast standards were tested at Peak, Quasi-Peak, and Average ratings. Individual tests for Radiated and Conducted are outlined in Section 4.3.1 and Section 4.3.2, respectively.

For both types of tests, a car battery or a 14.5-V power supply was used in conjunction with short cables in order to test at optimized performance. Additionally, resistive loads at 1 A and 2.3 A were used to emulate similar types of loads that USB devices might draw.

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4.3.1 Radiated Emissions

For radiated emissions testing, the absorber-lined shielded enclosure (ALSE) procedure was used for testing. This procedure involves a chamber that has RF absorber material lining the walls and ceiling of the enclosure. Table 12 and Table 13 are the broadcast lists of examples for quasi-peak, peak, and average limits for radiated disturbances for this particular ALSE method.

Table 12. CISPR 25 Class 5 Examples of Quasi-Peak and Peak Limits for Radiated Disturbances (ALSE Method)

SERVICE/ BAND	FREQUENCY (MHz)	LEVELS IN dB (µV/m)									
		CLASS 1		CLASS 2		CLASS 3		CLASS 4		CLASS 5	
		PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK
BROADCAST											
LW	0.15-0.30	86	73	76	63	66	53	56	43	46	33
MW	0.53-1.8	72	59	64	51	56	43	48	35	40	27
SW	5.9-6.2	64	51	58	45	52	39	46	33	40	27
FM	76-108	62	49	56	43	50	37	44	31	38	25
TV Band I	41-88	52	—	46	—	40	—	34	—	28	—
TV Band III	174-230	56	—	50	—	44	—	38	—	32	—
DAB III	171-245	50	—	44	—	38	—	32	—	26	—
TV Band IV/V	468-944	65	—	59	—	53	—	47	—	41	—
DTTV	470-770	69	—	63	—	57	—	51	—	45	—
DAB L Band	1447-1494	52	—	46	—	40	—	34	—	28	—
SDARS	2320-2345	58	—	52	—	46	—	40	—	34	—

Table 13. CISPR 25 Class 5 Examples of Average Limits for Radiated Disturbances (ALSE Method)

SERVICE/ BAND	FREQUENCY (MHz)	LEVELS IN dB (µV/m)				
		CLASS 1	CLASS 2	CLASS 3	CLASS 4	CLASS 5
		AVERAGE	AVERAGE	AVERAGE	AVERAGE	AVERAGE
BROADCAST						
LW	0.15 to 0.30	66	56	46	36	26
MW	0.53 to 1.8	52	44	36	28	20
SW	5.9 to 6.2	44	38	32	26	20
FM	76 to 108	42	36	30	24	18
TV Band I	41 to 88	42	36	30	24	18
TV Band III	174 to 230	46	40	34	28	22
DAB III	171 to 245	40	34	28	22	16
TV Band IV/V	468 to 944	55	49	43	37	31
DTTV	470 to 770	59	53	47	41	35
DAB L Band	1447 to 1494	42	36	30	24	18
SDARS	2320 to 2345	48	42	36	30	24

For the ALSE method of radiated emissions testing, four different antennas are used to measure the full range of testing and three antennas were tested in a vertical polarization as well as horizontal polarization. Additionally, ambient readings were taken before each test. A diagram of the first test is seen in Figure 54, using a rod antenna (only one polarization option). This test was done for the frequency range between 150 kHz to 30 MHz. This band is particularly important to test because it captures the range for the AM and FM radio frequencies.

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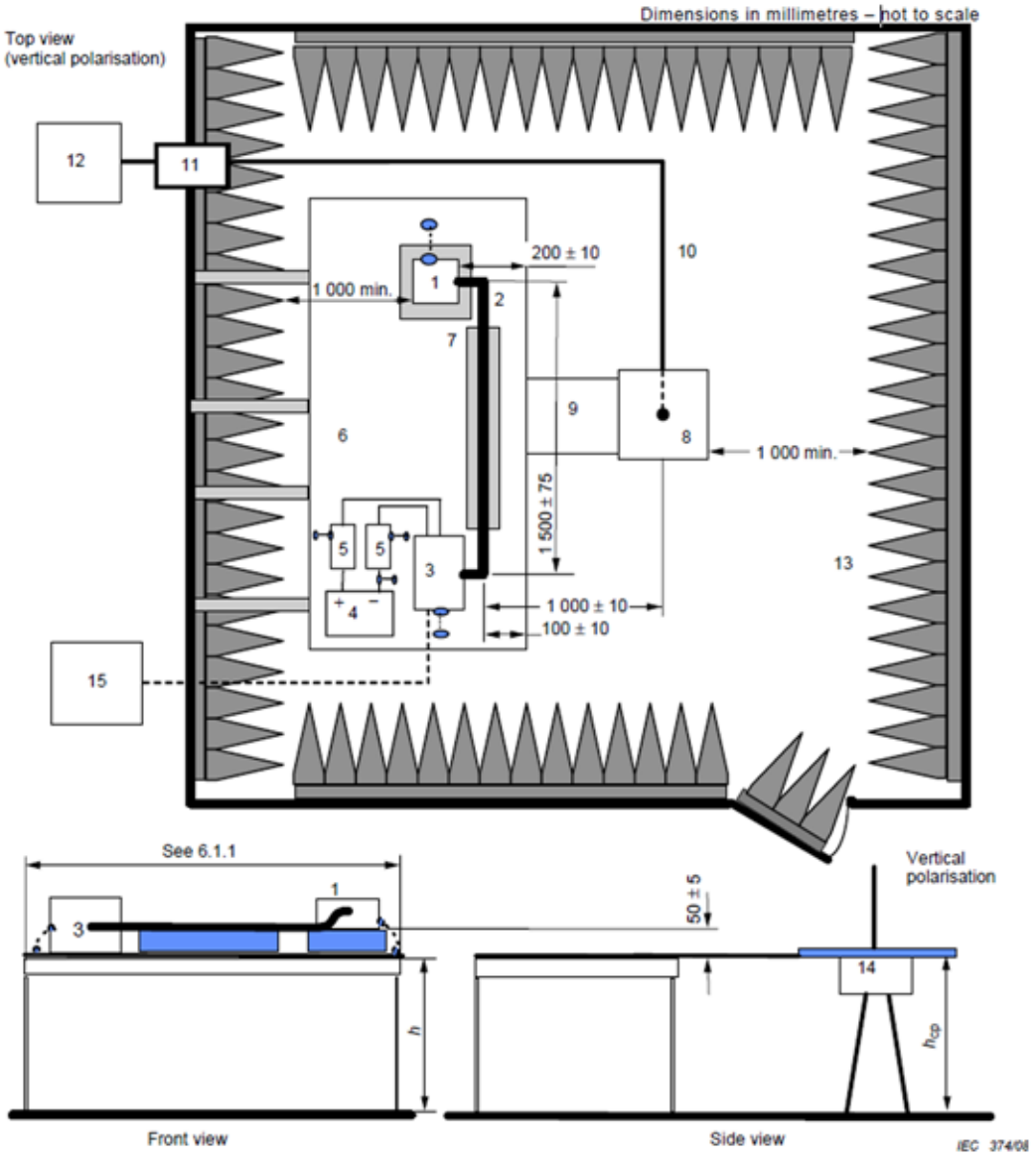

Figure 54. CISPR 25 Class 5 Radiated Emissions Test Setup (ALSE)

1 EUT (grounded locally if required in test plan)
2 Test harness
3 Load simulator
4 Power supply (location optional)
5 Artificial network (AN)
6 Ground plane (bonded to shielded enclosure)
7 Low relative permittivity support
8 Rod antenna with counterpoise (dimensions: 600 mm × 600 mm, typical)
h (900 ±100) mm
h_{cp} *h* + (+10/–20) mm
9 Grounding connection (full width bond between counterpoise and ground plane)
10 High-quality coaxial cable (for example, double-shielded 50 Ω)
11 Bulkhead connector
12 Measuring instrument
13 RF absorber material
14 Antenna matching unit (the preferred location is below the counterpoise; if above the counterpoise, then the base of the antenna rod shall be at the height of the ground plane)
15 Stimulation and monitoring system

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Figure 55 shows the ambient reading. In Figure 56, the first peak at 2.1 MHz can be identified and corresponds to the switching frequency of the LM53635-Q1. Subsequent peaks can be seen at the fundamentals for the switching frequency approximately at 4.2 MHz, 6.3 MHz, 8.4 MHz, and so on. This TI Design passed all peak and quasi-peak limits as indicated in CISPR 25 Class 5 documentation for ranges 150 kHz to 2 GHz. (Note: At 200 MHz, the average limit was exceeded due to coupling of the switching frequency into the board. Documentation on this can be found in the LM53635-Q1 product folder. At 750 MHz, a violation occurred at the average limit but was seen even in ambient readings due to local equipment in the testing facility.)

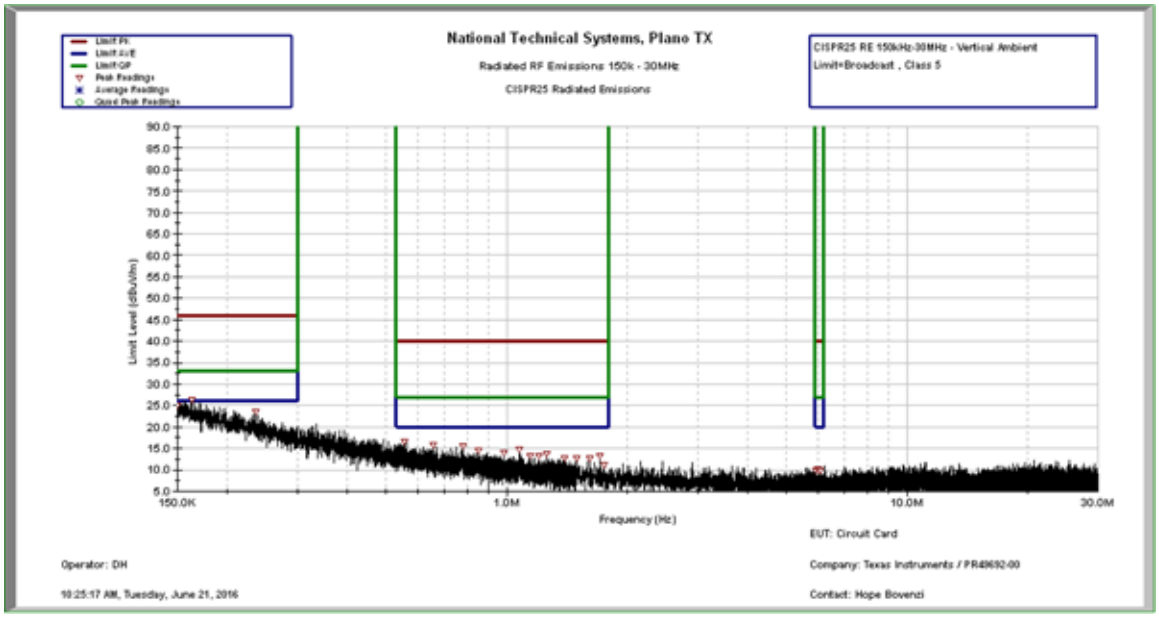

Figure 55. CISPR 25 Class 5 Radiated Emissions Ambient Reading

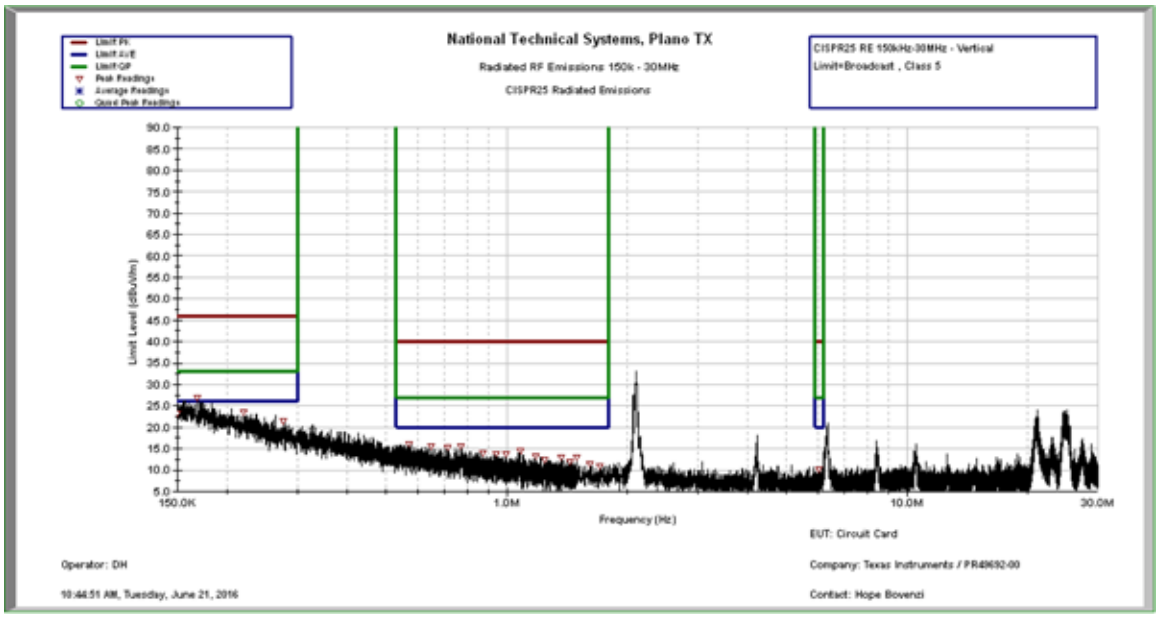

Figure 56. CISPR 25 Class 5 Radiated Emissions Range 150-kHz to 30-MHz Rod Antenna

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4.3.2 Conducted

A similar test setup is needed for conducted emissions testing; however, no antennas are used. There are several variations in testing that are dependent upon the system being tested. For this particular TI Design, the voltage method was used and Table 14 and Table 15 indicate the quasi-peak, peak, and average limits for these tests.

Table 14. CISPR 25 Class 5 Examples of Quasi-Peak and Peak Limits for Conducted Disturbances (Voltage Method)

SERVICE/ BAND	FREQUENCY (MHz)	LEVELS IN dB (µV/m)									
		CLASS 1		CLASS 2		CLASS 3		CLASS 4		CLASS 5	
		PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK
BROADCAST											
LW	0.15 to 0.30	110	97	100	87	90	77	80	67	70	57
MW	0.53 to 1.8	86	73	78	65	70	57	62	49	54	41
SW	5.9 to 6.2	77	64	71	58	65	52	59	46	53	40
FM	76 to 108	62	49	56	43	50	37	44	31	38	25
TV Band I	41 to 88	58	—	52	—	46	—	40	—	34	—
TV Band III	174 to 230	Conducted emission (voltage method) Not applicable									
DAB III	171 to 245										
TV Band IV/V	468 to 944										
DTTV	470 to 770										
DAB L Band	1447 to 1494										
SDARS	2320 to 2345										

Table 15. CISPR 25 Class 5 Examples of Average Limits for Conducted Disturbances (Voltage Method)

SERVICE/ BAND	FREQUENCY (MHz)	LEVELS IN dB (µV/m)				
		CLASS 1	CLASS 2	CLASS 3	CLASS 4	CLASS 5
		AVERAGE	AVERAGE	AVERAGE	AVERAGE	AVERAGE
BROADCAST						
LW	0.15 to 0.30	90	80	70	60	50
MW	0.53 to 1.8	66	58	50	42	34
SW	5.9 to 6.2	57	51	45	39	33
FM	76 to 108	42	36	30	24	18
TV Band I	41 to 88	48	42	36	30	24
TV Band III	174 to 230	Conducted emission (voltage method) Not applicable				
DAB III	171 to 245					
TV Band IV/V	468 to 944					
DTTV	470 to 770					
DAB L Band	1447 to 1494					
SDARS	2320 to 2345					

For the voltage method of conducted emissions testing, both the positive terminal and negative terminal of the LISNs were used to measure the full range of testing. Additionally, ambient readings were taken before each test. A diagram of the conducted test is seen in Figure 57. This test was done for the frequency range between 150 kHz to 108 MHz. This band is particularly important to test because it captures the range for the AM and FM radio frequencies.

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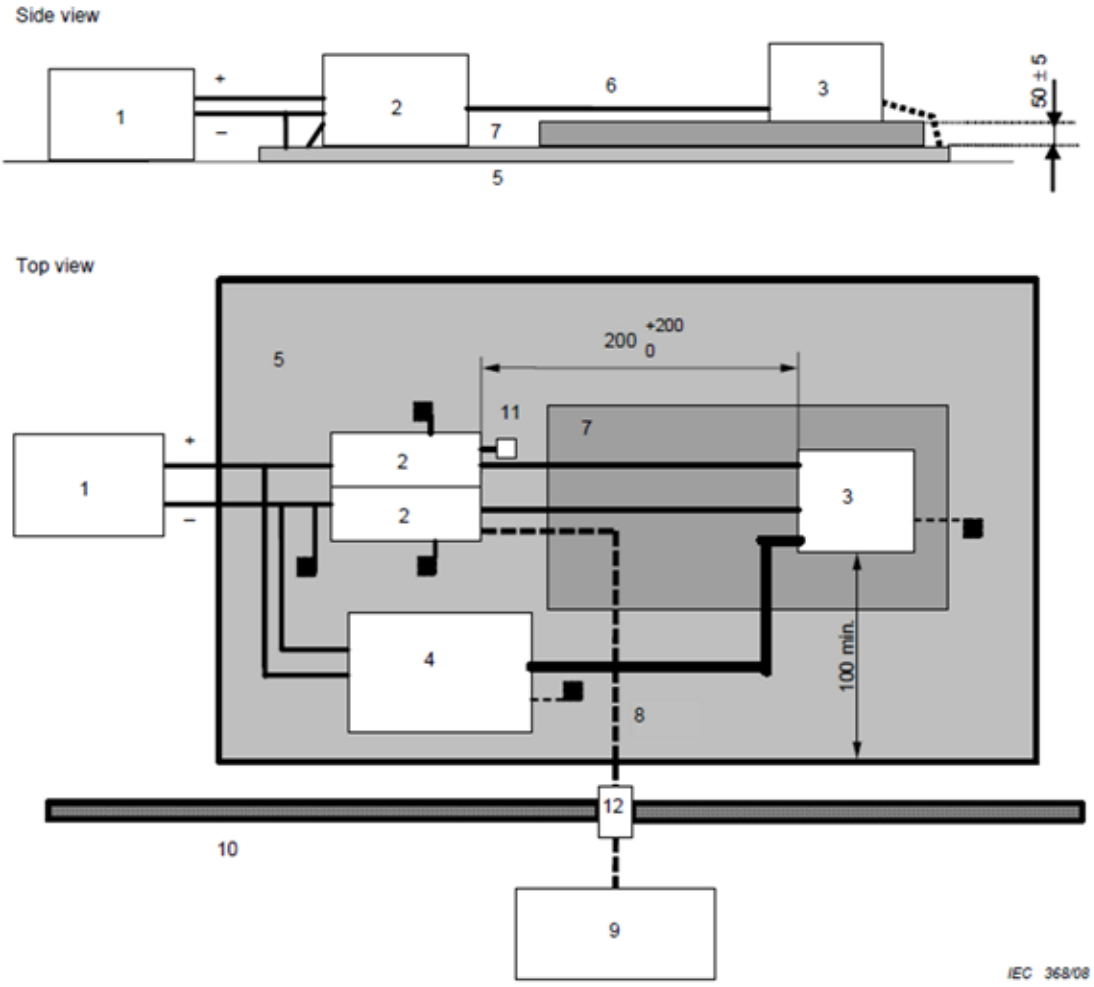

Figure 57. CISPR 25 Class 5 Conducted Emissions Test Setup (Voltage Method)

1 Power supply (may be placed on the ground plane)
2 Artificial network (AN)
3 EUT (grounded locally if required in test plan)
4 Load simulator (metallic casing grounded if required in test plan)
5 Ground plane
6 Power supply lines

Note: The EUT housing ground lead, when required in the test plan, should not be longer than 150 mm.

7 Low relative permittivity support
8 High-quality coaxial cable (for example, double-shielded 50 Ω)
9 Measuring instrument
10 Shielded enclosure
11 50-Ω load
12 Bulkhead connector

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Figure 58 and Figure 59 show the ambient reading and low-side reading, respectively. There was not any major deviation between low side and high side measurements, so only the low side is shown. There is a jump in the ambient reading due to the change in bandwidth to 125 kHz. As shown in Figure 59, the first peak at 2.1 MHz can be identified and corresponds to the switching frequency of the LM53635-Q1. Subsequent peaks can be seen at the fundamentals for the switching frequency approximately at 4.2 MHz, 6.3 MHz, 8.4 MHz, and so on. This TI Design passed all peak and quasi-peak limits as indicated in CISPR 25 Class 5 documentation for ranges 150 kHz to 108 MHz. (Note: At 108 MHz, the average limit was exceeded due to coupling of the switching frequency into the board. Documentation on this can be found in the LM53635-Q1 product folder.)

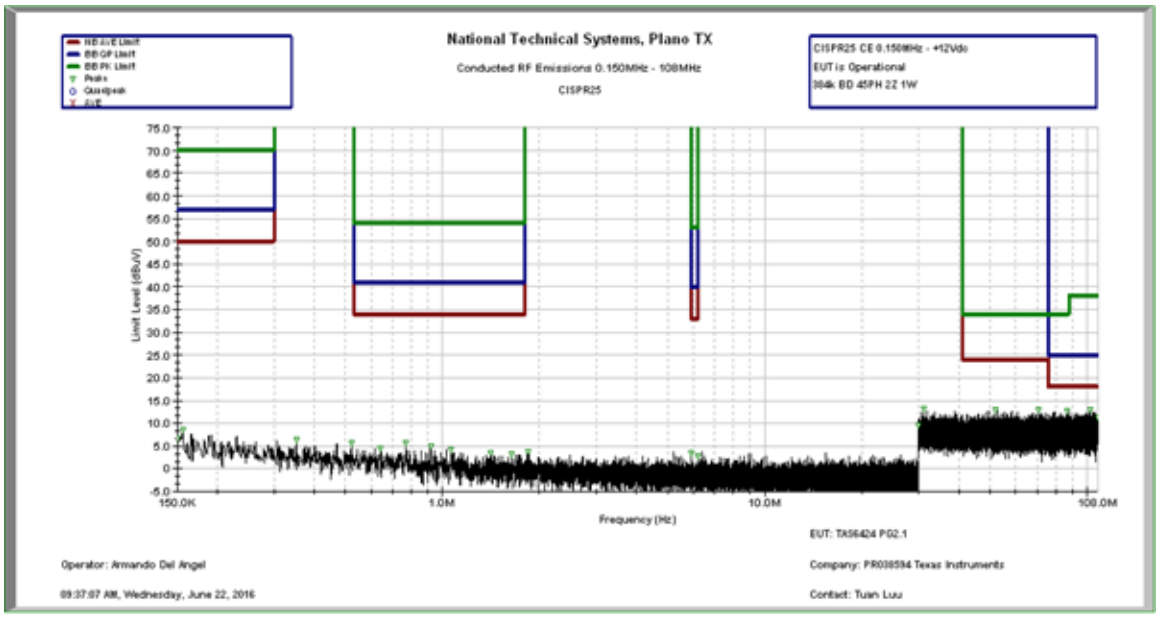

Figure 58. CISPR 25 Class 5 Conducted Emissions Ambient Reading (Voltage Method)

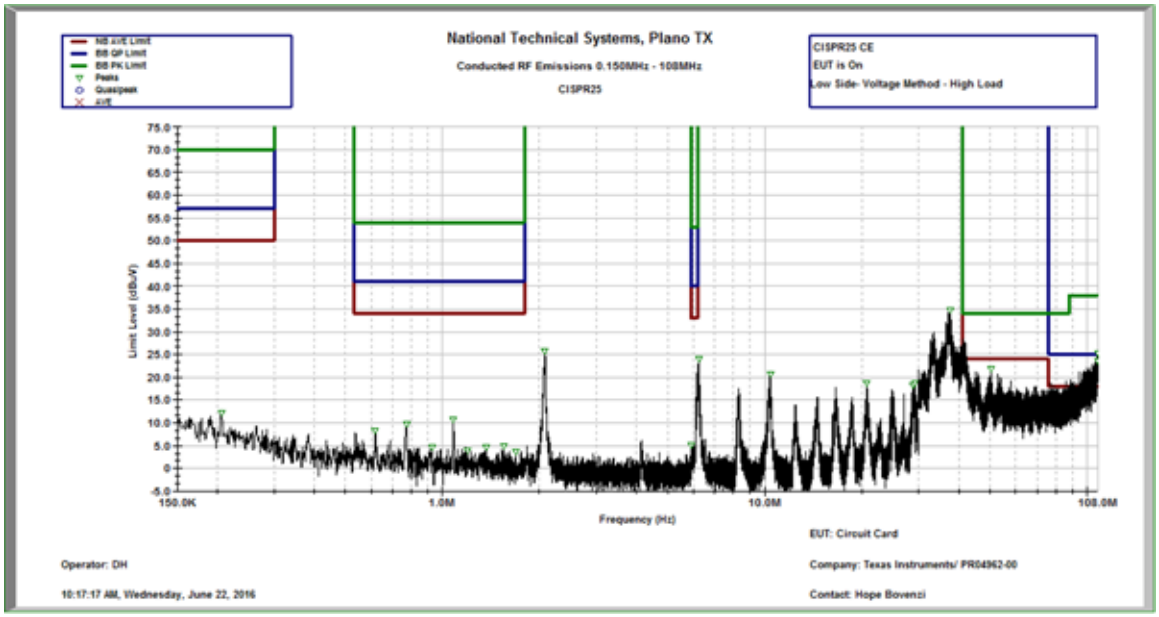

Figure 59. CISPR 25 Class 5 Conducted Emissions Low-Side High Load (Voltage Method)

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00987.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00987.

5.3 PCB Layout Recommendations

The TIDA-00987 PCB is a four-layer board:

- The top layer has the majority of components.
- The second layer is a GND plane.
- The third layer is the power layer PWR.
- The bottom layer is for signals.

For most of the components, the recommendation from the datasheet is followed diligently with some slight deviations in order to optimize for EMI and size constraints. The top and bottom layer should ideally be fully filled with copper for thermal performance. To keep high-speed and SuperSpeed traces from coupling, the second layer is a full ground layer. The third layer is used to route input, 5-V, and 3.3-V power rails. For a layout guide, follow the recommendations for individual components in the following subsections and their respective datasheets.

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00987.

5.3.2 Reverse Battery Protection

For the reverse battery protection (Figure 60), the input capacitors are placed on the front of the board with capacitors C8 and C11 rotated 90 degrees from one another, as mentioned in Section 2.2.2, due to possible flexing of the board. Take care to keep these components close to the input connectors of the board. The rest of the reverse battery protection is placed on the reverse side of the board, as seen in Figure 60, to optimize for space. The input to the LM74610 passes through the TVS diodes to pin 4 and the anode of Q1. To make routing easier, Q1 is placed below the LM74610 with C12 so that the gate drive and gate pull down of Q1 and VCAPH/VCAPL can be routed directly underneath the part. The output/cathode of Q1 goes directly to the pi filter. For additional EMI protection, a common-mode choke can be used with the pi filter to reduce high-frequency EMI.

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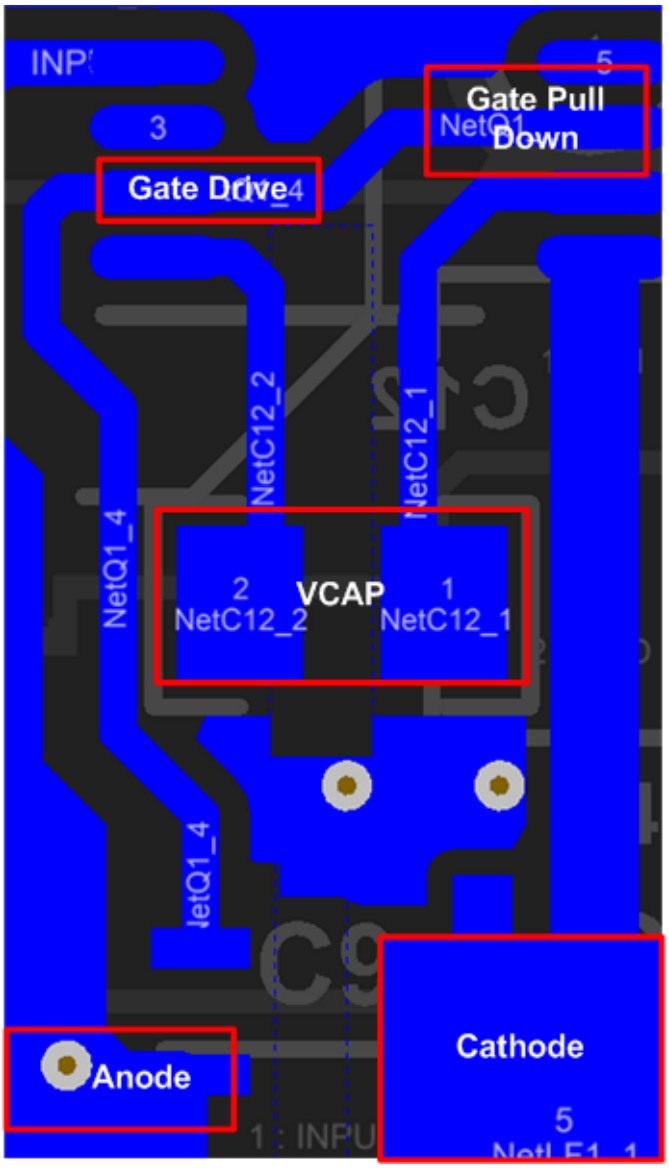

Figure 60. Reverse Battery Protection Layout

5.3.3 Power Supply

Although this component is optimal for EMI performance, carefully consider using the LM53635 to reduce EMI. To follow the direct recommendations for this particular part, see the LM53635-Q1 datasheet (SNVSAA7). The following instructions highlight some slight variances of the datasheet recommendation that pertain specifically to this TI Design.

5.3.3.1 General Recommendations

1. The solid copper plane below input capacitors will make sure a solid connection between the GNDs on both sides of the regulator. Ultimately this is to reduce parasitic loop inductance and thus minimize switch node ringing, EMI and help with power dissipation.
2. Flood GND surrounding the switch node to isolate switch node from coupling into surrounding pins.
3. Vias were placed on the inside of the input and output capacitors to help lower parasitics.

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5.3.3.2 Specific Discreet Power Component Layout Recommendations

1. Input capacitors: Because the IC has symmetric inputs, the parasitic input inductance is halved. Optimally two matching input capacitors can be place as close as possible to the input pins to maximize this performance. For the sake of minimal board size, the larger input capacitors were only used on the pin 4 side of the regulator.
2. Inductor: An important rule when designing any power supply is to keep the switch node as small as possible and away from any feedback resistors that might be susceptible to the switching. The inductor was placed as close to the switch node pin as possible with C_{BOOT} placed in between. A 3- to 10-Ω resistor can be placed in series with the C_{BOOT} to the switch node, in order to tune the rise time of the switching and reduce EMI.
3. Output capacitors: Capacitors were placed on both sides of the board to save space and were place as close to the inductor as possible.
4. A snubber network can be added from the switch node to ground to help minimize switch ringing.

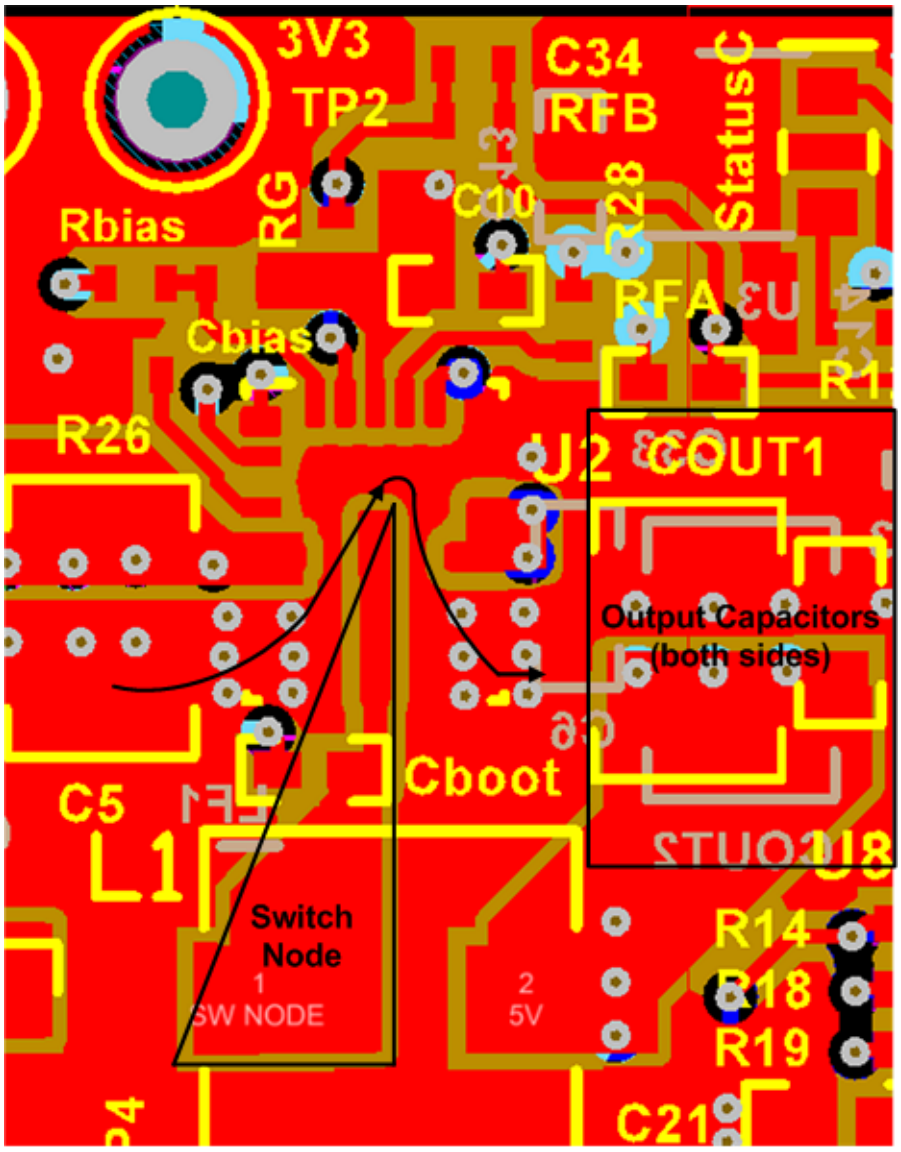

Figure 61. Power Supply Layout

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5.3.4 Legacy Charge Controller

To follow the direct recommendations for this particular part, see the datasheet. The following instructions highlight some slight variances of the datasheet recommendation that pertain specifically to this TI Design.

Many of the surrounding components are simply configuration passives and it is important to create a close, compact placement between these components and the TPS254900. For this particular TI Design, extra 0-Ω resistors and DNP pads were added for flexibility in configuration. These additional components may not be necessary for a final design.

One of the most important considerations for the layout of this component are the DP_IN, DN_IN, DP_OUT, and DN_OUT signals. USB-IF Standards for USB2.0, Universal Serial Bus 2.0 Specification, data require that these lines must be 90-Ω differential pairs. Additionally, trace length matching is a concern so adding trace length is beneficial to maintaining signal integrity. A free online Impedance Calculator from Mantaro Product Development Services can be used to calculate the differential micro strip impedance, trace width, separation, and so on.

For the DP_IN/DN_IN signal pair coming from the Type-C connector, the signals are differentially routed on the bottom layer. As seen in Figure 62, MidLayer2 has a GND plane directly below the DP_IN/DN_IN layer to keep the signals from coupling with other traces. The same GND layer consideration should be taken for DP_OUT/DN_OUT that is routed to the Micro-3.0 connector.

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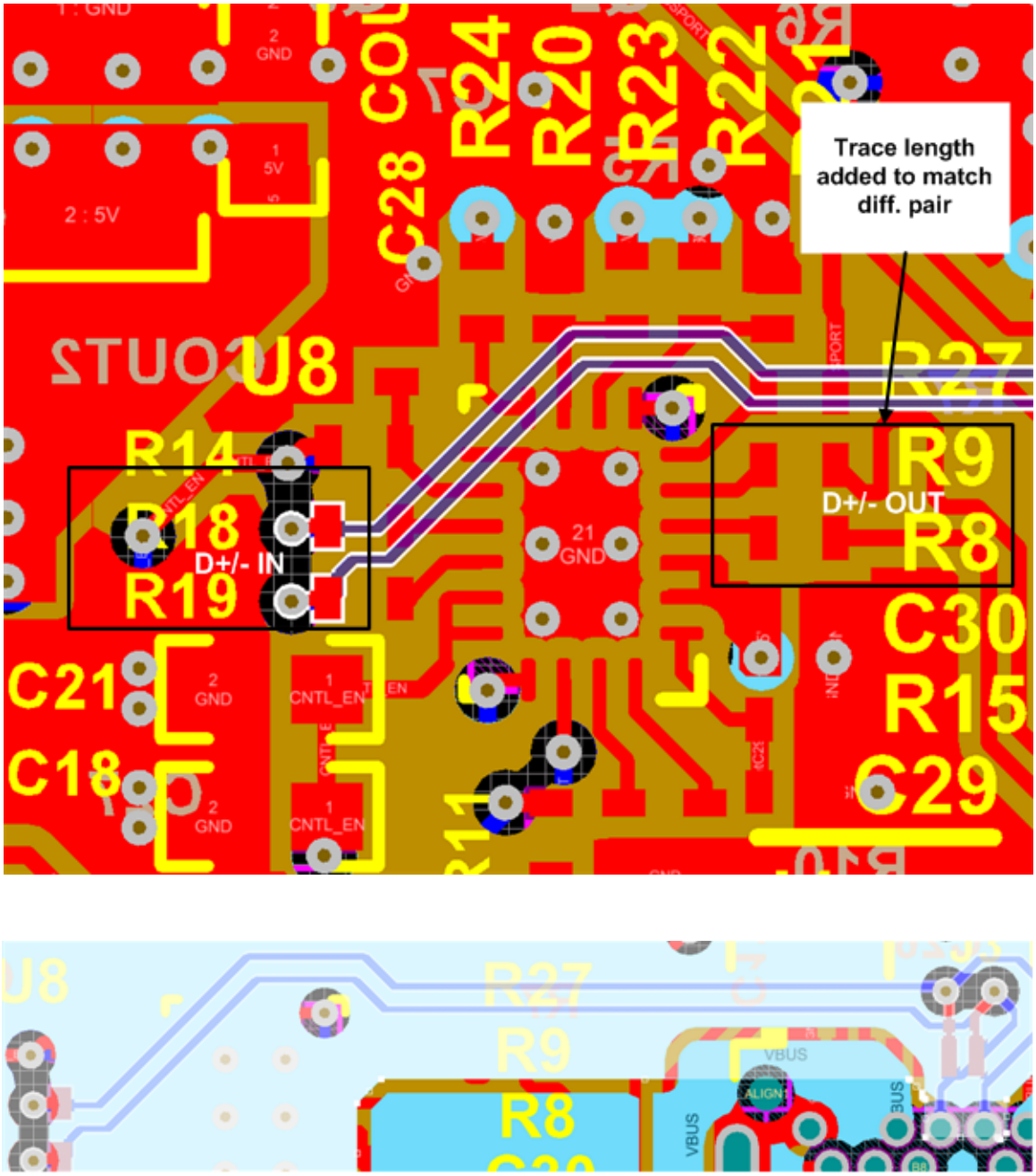

Figure 62. Legacy Charger Layout Recommendation: Top Layer (Top) and MidLayer2 (Bottom)

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5.3.5 Type-C Charge Controller

To follow the direct recommendations for this particular part, see the TPS25810 datasheet (SLVSCR1). The following instructions highlight some slight variances of the datasheet recommendation that pertain specifically to this TI Design.

If blocking FET protection is being used for non-compliant DFPs, keep the blocking FET close to the output of the TPS25810. For power paths carrying high current, keep the connections as short as possible. As seen in Figure 63, the blocking FET is placed close to the output of the TPS25810 and it is routed with substantive trace widths to accommodate the higher current.

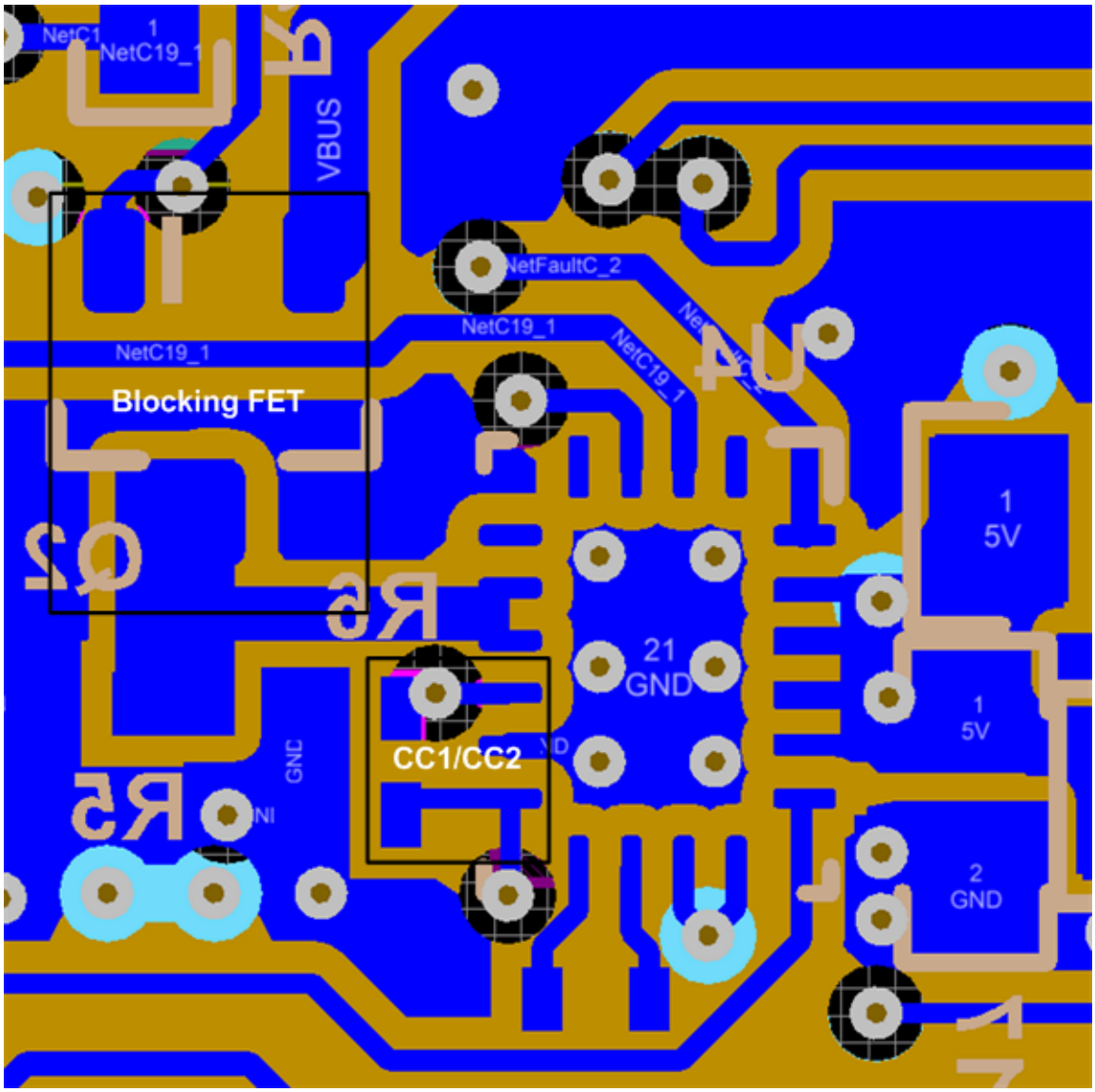

Figure 63. Type-C Controller Layout Recommendations

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5.3.6 SuperSpeed Routing

There are four main components that must be considered for routing the SuperSpeed lines:

- Type-C connector
- TPD4E05U06 ESD device
- HD3SS3212 MUX
- Micro-3.0 connector

For the TPD4E05U06 and the HD3SS3212, see the respective datasheets (SLVSCO7 and SLASE74) for IC specific recommendations.

5.3.6.1 Type-C Connector and TPD4E05U06

In this TI Design, an Amphenol 124015458E4#2A connector was used with careful consideration given to the SuperSpeed lines. As noted in USB-IF Standards for USB3.0, Universal Serial Bus 3.0 Specification, the T_x+/T_x– and R_x+/R_x– signals should be routed as 90-Ω differential pairs. Due to the flip-ability of the Type-C Connector, there are eight pins that correlate to the T_{x1}+/T_{x1}–, R_{x1}+/R_{x1}–, T_{x2}+/T_{x2}–, and R_{x2}+/R_{x2}– (see Figure 19). The top pins are A2, A3, A10, and A11, and the bottom pins are B2, B3, B10, and B11, as seen in Figure 64. A10, A11 and B3, B2 (associated as R_{x2}–/R_{x2}+ and T_{x2}–/T_{x2}+) are routed through TPD4E05U06 (U5). A2, A3 and B10, B11 (associated as T_{x1}+/T_{x1}– and R_{x1}–/R_{x1}+) are routed through TPD4E05U06 (U6).

As was the case in Section 5.3.4 with the D+/D– lines, the differential micro strip impedance was calculated using the free online calculator tool [19] and trace lengths were matched as best as possible. Although the TPD4E05U06 has six pins that need to be connected, the TPD4E05U06 was designed to be routed through the IC for better ease of use.

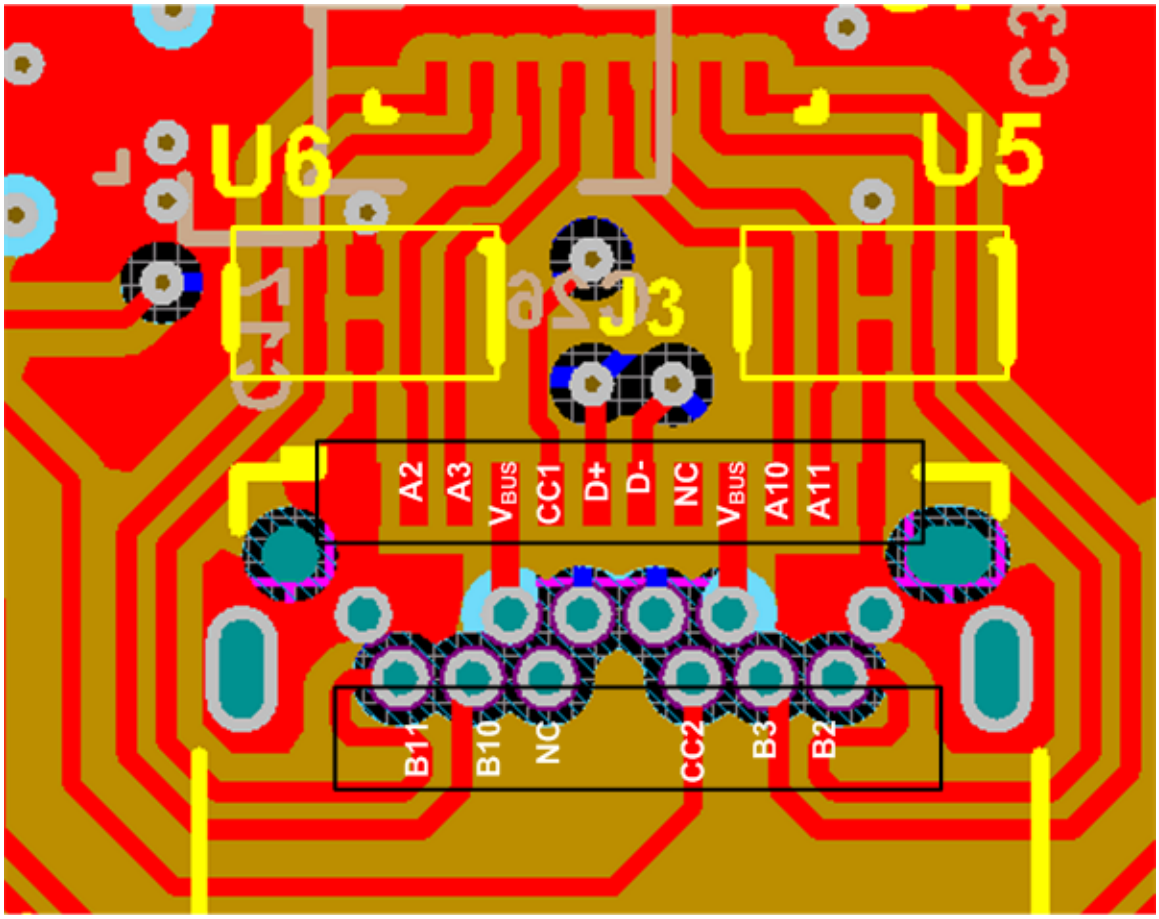

Figure 64. Type-C Connector and ESD Layout Recommendation

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5.3.6.2 SuperSpeed MUX

As mentioned in Section 2.6, if the polarity on the T_x lines were not switched then the ± signals would need to cross coming from the Type-C connector or from the ESD device. By connecting the T_x lines to the opposite polarity of the MUX, a straight connection is ensured all the way from the Type-C connector, through the ESD, to the MUX that ultimately maintains signal integrity. Fortunately, the MUX pins are capable of all the polarity being switched as long as the polarity of the output pins on the MUX for the T_x lines is switched as well.

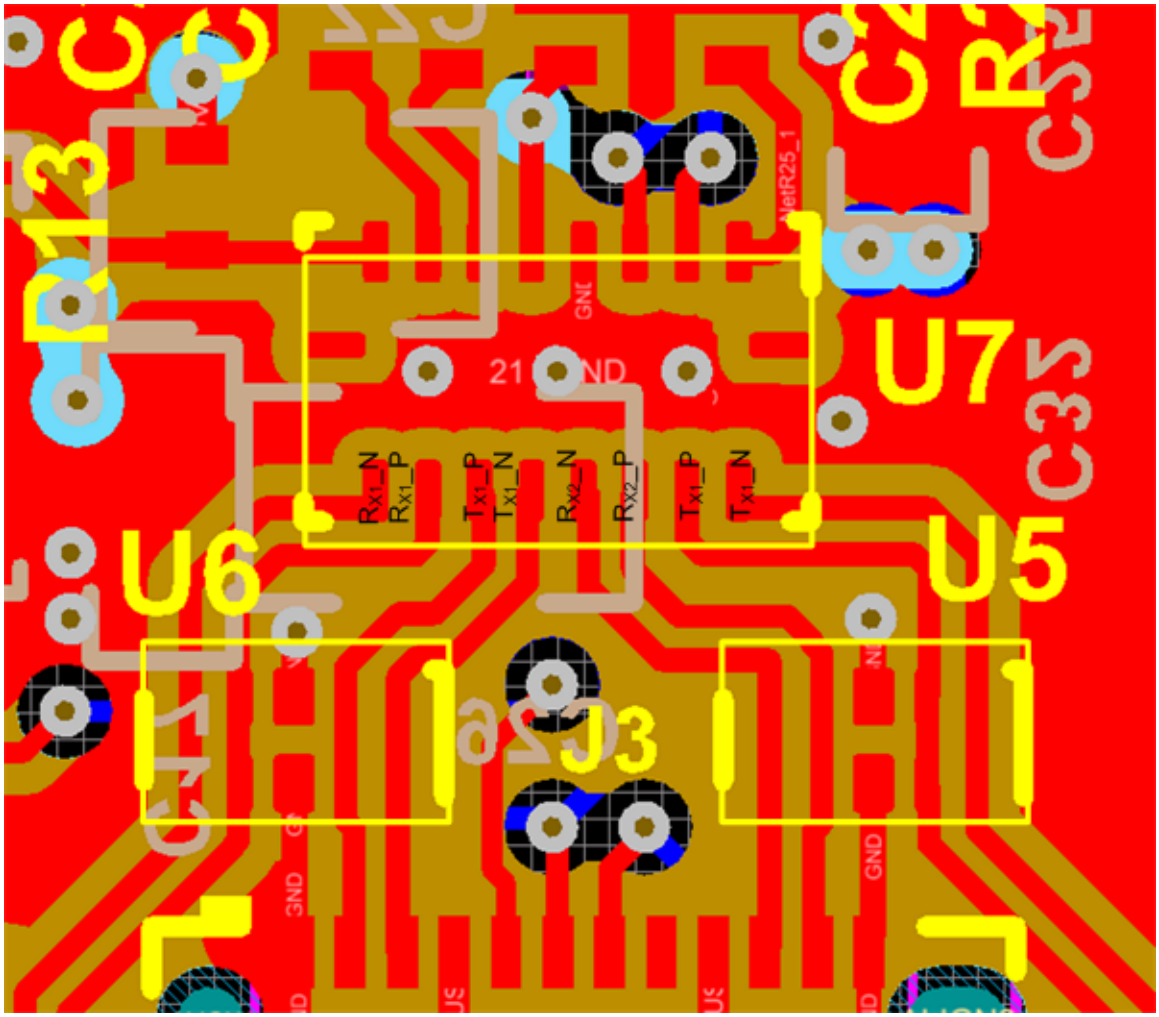

Figure 65. SuperSpeed MUX Layout Recommendations

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00987.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00987.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00987.

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6 References

Texas Instruments References:

1. Texas Instruments, *Zero IQ Reverse Polarity Protection Smart Diode Controller*, LM74610-Q1 Datasheet (SNOSCZ1)
2. Texas Instruments, *3.5 A, 36 V Synchronous, 2.1 MHZ, Step-Down DC-DC Converter*, LM53635-Q1 Datasheet (SNVSAA7)
3. Texas Instruments, *200 mA, Low-IQ Low-Dropout Regulator*, TLV70033-Q1 Datasheet (SLVSA61)
4. Texas Instruments, *USB Type-C DFP Controller and Power Switch with Load Detection*, TPS25810-Q1 Datasheet (SLVSCR1)
5. Texas Instruments, *Automotive USB Host Charger With Short-to-V_{BATT} Protection*, TPS254900-Q1 Datasheet (SLUSCO9)
6. Texas Instruments, *4 Channel Protection Solution for SuperSpeed (Up to 5 Gbps) Interface*, TPD4E05U06-Q1 Datasheet (SLVSCO7)
7. Texas Instruments, *Two-Channel Differential 2:1/1:2 USB3.1 Mux/Demux*, HD3SS3212 Datasheet (SLASE74)
8. Texas Instruments, *TPS25810 Charging Port Over USB Type-C*, Application Report (SLVA768)
9. Texas Instruments, *Protection the TPS25810 from High Voltage DFPs*, Application Report (SLVA751)
10. Texas Instruments, *AN-2162 Simple Success with Conducted EMI from DC-DC Converters*, Application Report (SNVA489)

Standards References:

11. Universal Serial Bus Type-C Cable and Connection Specification (USB Type-C)
12. Universal Serial Bus 3.1 Specification (USB 3.1, Gen 1 and Gen 2)
13. USB Battery Charging 1.2 Compliance Plan
14. Universal Serial Bus 2.0 Specification
15. *Electromagnetic compatibility (EMC)- Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test*, IED61000-4-2
16. *International Standard, Road Vehicles – Environmental conditions and testing for electrical and electronic equipment*, ISO 16750-2
17. *Road Vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*, ISO 7637-2
18. CISPR 25 Class 5 *International Standard, Edition 3.0, March 2008*

Other Tools:

19. Mantaro Product Development Services Impedance Calculator
20. USB Flash Speed Tester
21. National Technical Systems, CISPR 25 Class 5 Broadcast Radiated and Conducted Emissions Testing

7 About the Author

HOPE BOVENZI is a systems engineer at Texas Instruments. Hope earned her bachelor of science in electrical engineering from the University of California at Davis in 2012. As a member of the Automotive Systems Engineering team at Texas Instruments, she is responsible for developing reference design solutions for the Automotive Infotainment and Cluster segment and has a background in power design.

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to A Revision	Page
• Changed from preview draft	1

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