TI Designs

IGBT Gate Driver Reference Design for Parallel IGBTs With Short-Circuit Protection and External BJT Buffer

Overview

Paralleling IGBTs become necessary for power conversion equipment with higher output power ratings, where a single IGBT cannot provide the required load current. This TI Design implements a reinforced isolated IGBT gate control module to drive parallel IGBTs in half-bridge configuration. Paralleling IGBTs introduces challenges at both the gate driver (insufficient drive strength) as well as at system level in maintaining equal current distribution in both the IGBTs while ensuring faster turnon and turnoff. This reference design uses reinforced isolated IGBT gate driver with integrated features like desaturation detection and soft turnoff to protect the IGBT during fault conditions. An increased gate drive current (15 A) is obtained through external BJT current booster stage without sacrificing the soft turnoff feature. Further, this design demonstrates the mechanism of avoiding gate current loops while operating IGBTs in parallel.

Resources

TIDA-00917	Design Folder
ISO5852S	Product Folder

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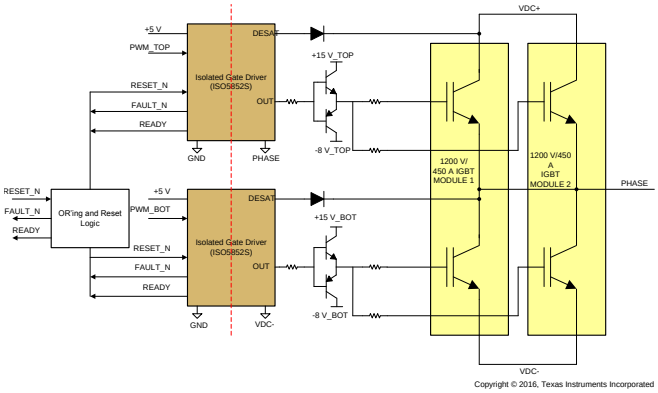
Features

- Suited for Low-Voltage Drives up to 480-V_{AC}
- Designed to Drive Parallel IGBT Modules of a 1200-V Rating With Total Gate Charges up to 10 µC Translating to Collector Currents of 500 A
- Sourceand Sink Current Ratings of up to 15 A_{pk} With External BJT Buffer Stage
- Bipolar Gate Drive Voltages
- Split Output for Independent Turnon and Turnoff Control
- IGBT Short-Circuit Protection Using Built-in DESAT and Adjustable Soft Turnoff Time
- Built-in Common-Mode Choke and Emitter Resistance for Limiting Emitter Loop Current
- Generates Fault Output During IGBT Short-Circuit Condition and Gate Driver Undervoltage Scenario
- 8000-V_{pk} V_{IOTM} and 2121-V_{pk} V_{IORM} Reinforced Isolation
- Very High CMTI of 100 kV/µs

Applications

- Variable Speed Drives
- UPS
- Traction Inverter
- Wind and Solar Inverter



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1 System Overview

1.1 System Description

Insulated gate bipolar transistors (IGBTs) are considerably used in three-phase inverters that have numerous applications like variable-frequency drives that control the speed of AC motors, uninterruptible power supplies (UPS), solar inverters, and other similar inverter applications.

IGBTs have the advantages of high-input impedance as the gate is insulated, has a rapid response ability, good thermal stability, simple driving circuit, good ability to withstand high voltage, snubber-less operation, and controllability of switching behavior providing reliable short-circuit protection. The IGBT is a voltage controlled device, which gives it the ability to turn on and off very quickly.

Paralleling IGBT modules becomes necessary when the output current requirement cannot be provided by a single IGBT module. A single module of an IGBT is capable of handling currents up to 600 A in the dual configuration. Higher currents in the range of kilo amperes are required in case of high power rated equipments. Higher currents can be obtained either by paralleling inverters or by paralleling the IGBT modules inside the inverter as shown in Figure 1. An advantage of paralleling includes distributing heat sources so that higher levels of power loss can be dissipated.

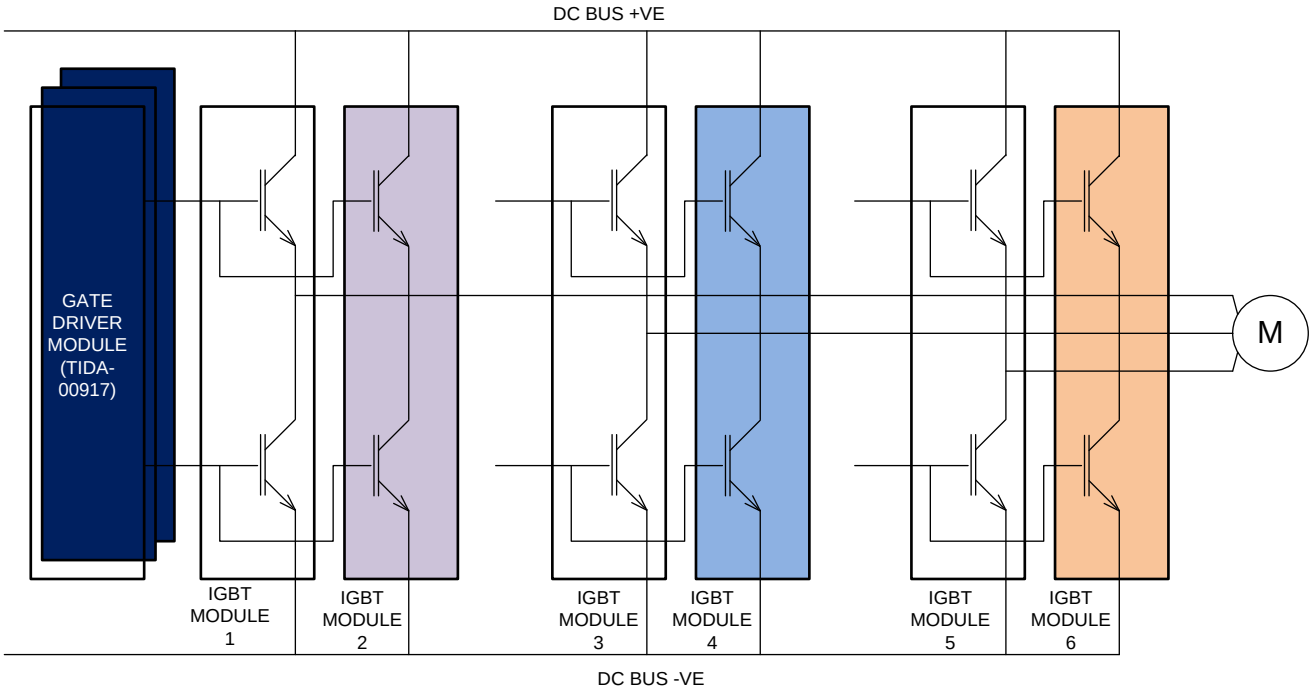

Figure 1. Inverter Stage With Half-Bridge IGBT Module Paralleling

This isolated gate driver circuit is designed for low voltages and medium power drives, operating from a three-phase AC supply up to 480 V_{AC}. Medium power drives rated for greater than 100 kW can have IGBT modules with gate charges up to 10 μC, necessitating high peak currents to turn on and off the IGBT. Gate driver ICs have a limited peak current capability; typical values are 2.5 A for source and 5 A for sink.

This reference design shows how to generate higher gate drive currents from a lower source-sink capable driver without sacrificing the inbuilt features of desaturation (DESAT) detection and soft turnoff. The design uses the ISO5852S gate driver along with an external BJT current buffer stage.

The reference design provides the following key benefits:

- High gate source sink current capability due to use of external BJT current buffer stage
- IGBT DESAT detection and soft turnoff
- Adjustable soft turnoff feature
- Optional auto-reset functionality
- Reinforced isolation

1.2 Key System Specifications

Table 1. Key System Specifications

FEATURE	PARAMETER	SPECIFICATION
System	IGBT module	1200 V, 450 A
	Number of IGBT modules	2
	IGBT module configuration	Half bridge
Gate drive	Primary side voltage	5 V ± 5 %
	Secondary side voltage	24 V ± 5 %
	Source current / IGBT	7.5 A (max)
	Sink current / IGBT	7.5 A (max)
Isolation	Creepage	8 mm
	CMTI	100 KV/µs at V_{CM}= 1500 V
	Isolation	5700 V_{RMS} per minute
	Working voltage	800 V_{DC} (max)
Protection	IGBT overcurrent, undervoltage lockout on both primary and secondary side of gate driver	

1.3 Block Diagram

The block diagram for the TIDA-00917 is shown in Figure 2.

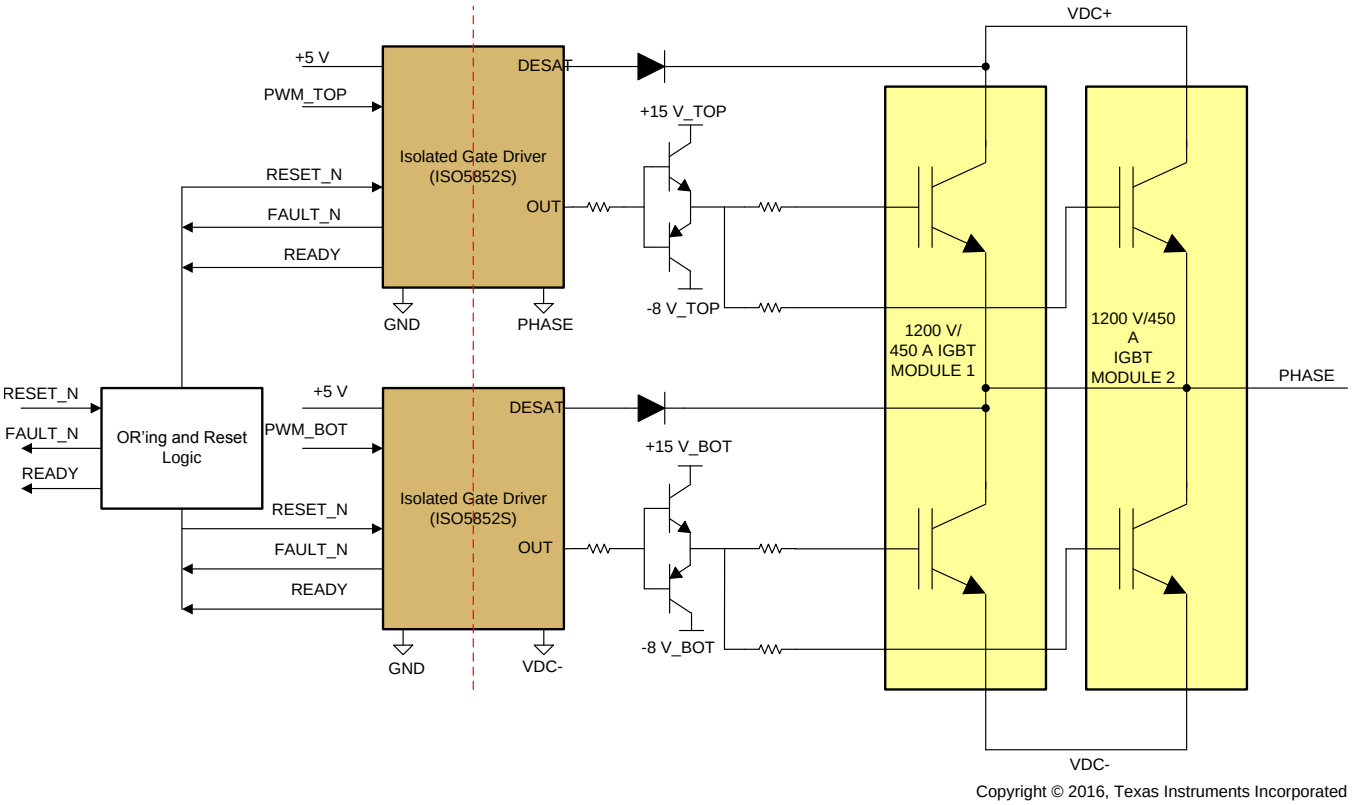

Figure 2. Block Diagram of TIDA-00917

This TI Design uses two reinforced isolated IGBT gate drivers (ISO5852S) with an external BJT buffer for driving two paralleled IGBT modules in half-bridge configuration. The primary side of the driver is powered from 5 V. The 23-V high-side supply voltage is split into 15 V and –8 V through a Zener network. The IGBT is turned off with a negative voltage of –8 V on its gate with respect to its emitter. This prevents the IGBT from unintentionally turning on because of voltage induced at the gate due to the Miller effect.

The split outputs of the gate driver can provide 2.5-A source and 5-A sink currents. An external current buffer stage, consisting of NPN and PNP transistors, is used to increase the source/sink current up to 15 A for driving IGBT modules with a gate charge of approximately 5000 nC. The board also provides option to reset the gate drivers through a microcontroller (MCU) or automatically after a preset time in case of fault or DESAT detection. Fault and READY signals from the gate drivers are OR'ed together.

1.4 Highlighted Products

The TIDA-00917 reference design features the following device from Texas Instruments.

1.4.1 ISO5852S

The ISO5852S is a 5.7-kV_{RMS}, reinforced isolated, IGBT gate driver with split outputs, OUTH and OUTL, providing 2.5-A source and 5-A sink currents. The primary side operates from a single 3-V or 5-V supply.

The output side allows for a supply range from minimum 15 V to maximum 30 V. An internal DESAT detection recognizes when the IGBT is in an overload condition. Upon a DESAT detect, a Mute logic immediately blocks the output of the isolator and initiates a soft-turnoff procedure, which disables OUTH and reduces the voltage at OUTL over a minimum time span of 2 μs. When OUTL reaches 2 V with respect to the most negative supply potential, VEE2, the output is hard-clamped to VEE2. During normal operation with a bipolar output supply, the output is hard clamped to VEE2 when the IGBT is turned off.

Also when DESAT is active, a fault signal is sent across the isolation barrier, pulling FLT output at the input side low and blocking the isolator input. The FLT output condition is latched and can be reset only after RDY goes high, through a low active pulse at the RST input. This is taken care of by implementing an auto-reset circuit between the Reset and Ready pins.

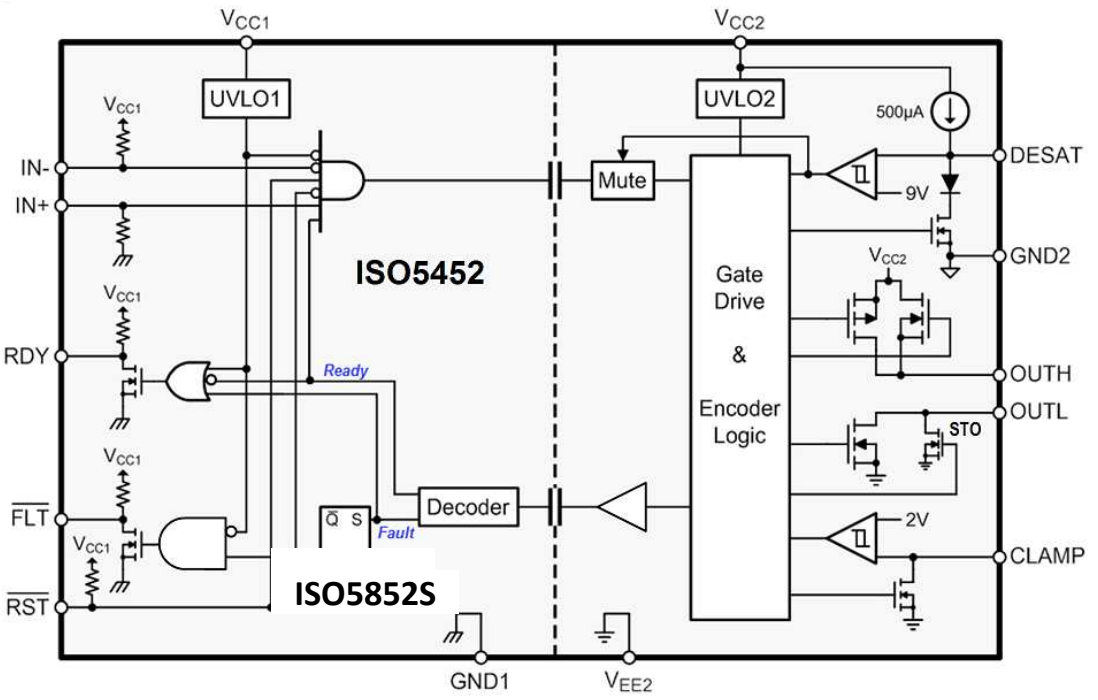

Figure 3. ISO5852S Functional Block Diagram

For more information on this device, see the ISO5852S product folder at www.TI.com or click on the link for the product folder on the first page of this reference design under Resources.

2 System Design Theory

2.1 Isolated IGBT Gate Driver

The isolated gate driver is required for driving the top switch of the half-bridge module as the gate voltage has to be applied with respect to the switch node terminal. Isolation is also required to electrically separate the low-voltage operator side from the high-voltage drive side to meet safety requirements. This section describes the design of an isolated gate driver with an external push-pull current buffer stage to increase the drive capability of the gate driver.

2.1.1 Secondary Side Gate Driver Voltage

High-side gate driver voltages are obtained by using a 23-V isolated power supply and splitting it using a 15-V Zener and a 511-Ω resistor as shown in Figure 4 to generate 15 V and –8 V. The voltage split circuit is a compromise between the solution size and regulation. For the centralized-driver bias supply design, it is impractical to have eight windings to power all IGBTs in a three-phase inverter configuration given the requirements of high-voltage insulation spacing. With the Zener diode, the 15-V rail can have a stable output with a tight regulation tolerance, which is important for the turnon speed of high power IGBTs. For –8 V, using the resistor provides a larger variation margin, but the negative bias is less critical in terms of the level of accuracy. The purpose of the negative bias is to prevent a high dv/dt induced false turnon of the IGBT in motor drive and high-voltage inverter applications. As long as the negative bias has low enough potential, it can maintain the secure turnoff of an IGBT. Another benefit of the voltage split scheme is the flexibility of setting the positive and negative voltage levels.

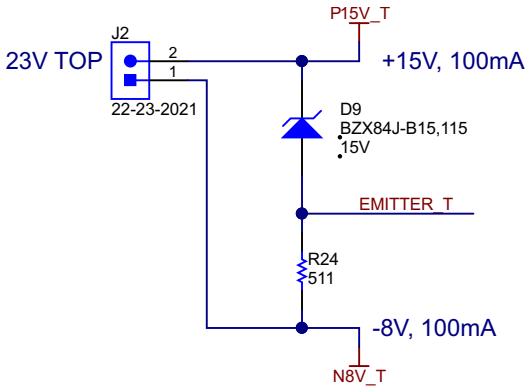

Figure 4. Zener Voltage Divider

The current flowing in the Resistor R24 can be calculated as follows:

$$I_{R24} = \frac{23\ V - 15\ V}{511\,\Omega} = 15.66\ mA \quad (1)$$

The power dissipation across R24 = 15.66 mA × 15.66 mA × 511 Ω = 125.31 mW.

As a result, a resistor with 1206 package is used so that the power can be dissipated without overheating the resistor. The amount of current flowing through the Zener is also approximately equal to the current flowing in the resistor R24. The peak currents required for driving IGBT gate will be supplied from the decoupling capacitors.

The power dissipation of the Zener = 15V × 15.66 mA = 234.9 mW.

Any diode with the power dissipation value higher than 235 mW can be used. The power dissipation capacity of the diode used is 550 mW.

2.1.2 Supply Voltage Capacitors

VCC1 and GND1 are the supply pins for the input side of the ISO5852S. The supply voltage at VCC1 can range from 3 to 5.5 V with respect to GND1, thus supporting the direct interface to 3.3-V low-power controllers as well as legacy 5-V controllers. A 4.7-µF bulk capacitor C1 is placed close to the IC power supply followed by an RC filter used to provide stable and clean power supply to the primary side of the gate driver.

VCC2 and GND2 are the supply pins for the output side of the ISO5852S. VEE2 is the supply return for the output driver and GND2 is the reference for the logic circuitry. The supply voltage at VCC2 can range from 15 V up to 30 V with respect to VEE2. A positive VGE of typically 15 V is required to switch the IGBT well into saturation. In this TI Design, VCC2 is fed with 15 V to ensure that IGBT is in full saturation.

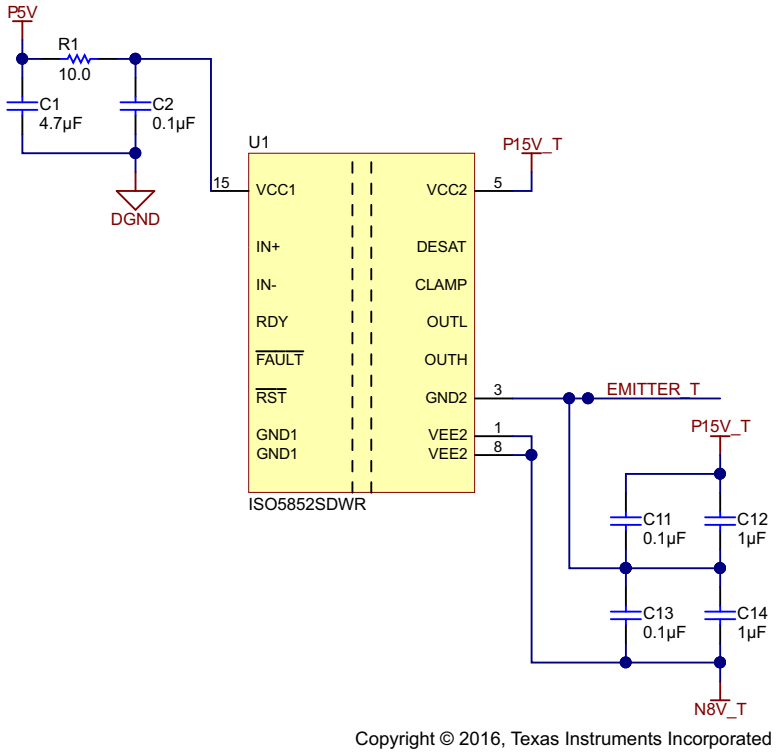

Figure 5. Power Supply Decoupling Capacitors

For larger IGBTs, negative values of V_{GE}, ranging from a required minimum of –5 V up to the recommended –15 V, are necessary to keep the IGBT turned off and to prevent it from unintentional conducting due to noise transients, particularly during short-circuit faults. In this design, VEE2 is fed with –8 V.

2.1.3 Gate Resistor Selection

When designing gate drivers, selecting the right gate resistor is an important part of the process. The value of the gate resistor affects the following parameters:

- IGBT turnon and turnoff times
- Switching losses
- dv/dt across the IGBT collector to emitter
- di/dt of the IGBT current
- EMI due to IGBT switching

Increasing the value of the gate resistor increases the turnon and turnoff times of the IGBT, which in turn reduces the dv/dt and di/dt, causing reduced EMI. Higher gate resistance also increases switching losses. Decreasing the gate resistance reduces switching losses but increases EMI. In this TI Design, turnon gate resistance is set to 0.9 Ω and turnoff is 0.6 Ω.

2.1.4 Source and Sink Currents

The source and sink currents play a major role in determining turnon and turnoff delays of the IGBT. Ideally, the maximum current that can be sourced and sinked into the IGBT can be found as follows:

- DC resistance of the common-mode choke = 0.25 Ω
- Internal gate resistance of IGBT (FF450R12ME4) = 1.7 Ω
- Collector resistance in the ON path (R36) = 0.3 Ω
- $R_{total(ON)}$ = Collector resistance in the ON path + R7 + R9 + DC resistance of the common-mode choke + Internal gate resistance of IGBT = 0.3 Ω + 0.3 Ω + 0.3 Ω + 0.25 Ω + 1.7 Ω = 2.85 Ω

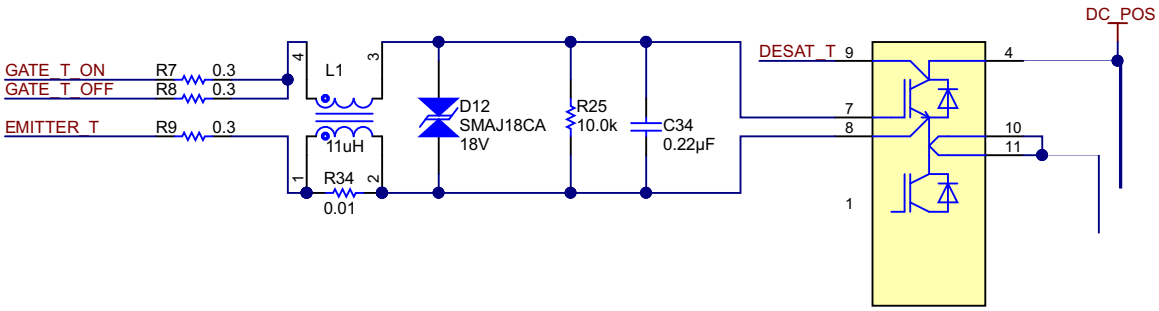

Figure 6. IGBT Gate Current Control Components

$$I_{total\_source} = \frac{\text{Voltage across the IGBT gate}}{\text{Rtotal}} = \frac{23\ \text{V}}{2.85} = 8.07\ \text{A} \quad (2)$$

Similarly, the sink current can be found as follows:

- Internal gate resistance of IGBT = 1.7 Ω
- $R_{total(OFF)}$ = R8 + R9 + DC resistance of the common-mode choke + Internal gate resistance of IGBT = 0.3 Ω + 0.3 Ω + 0.25 Ω + 1.7 Ω = 2.55 Ω

$$I_{total\_sink} = \frac{\text{Voltage across the IGBT gate}}{\text{Rtotal}} = \frac{23\ \text{V}}{2.55} = 9.01\ \text{A} \quad (3)$$

Figure 7 shows the simulation circuit for finding the source and sink currents. From these simulation results, the simulated values complies with the calculated values.

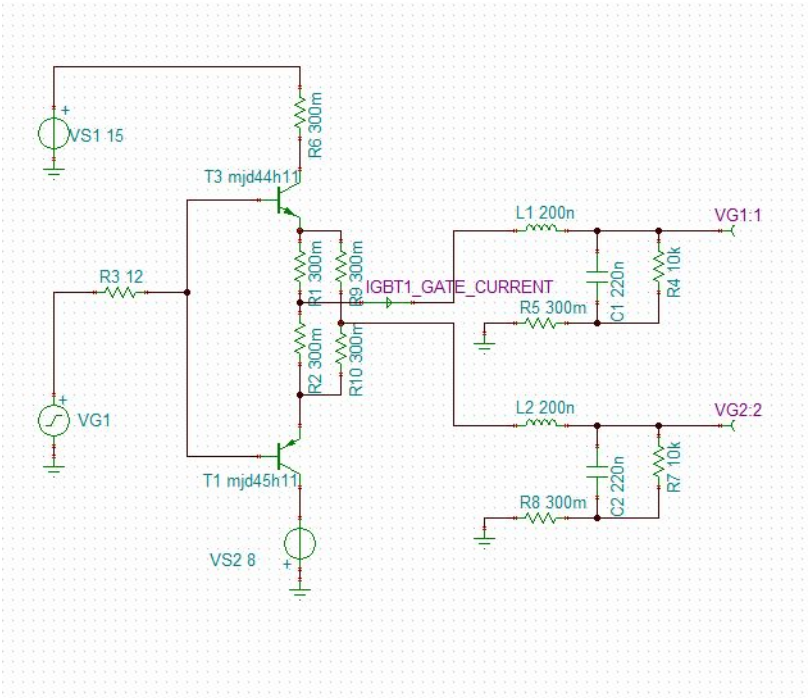

Figure 7. Schematic for Calculating Gate Current of IGBT

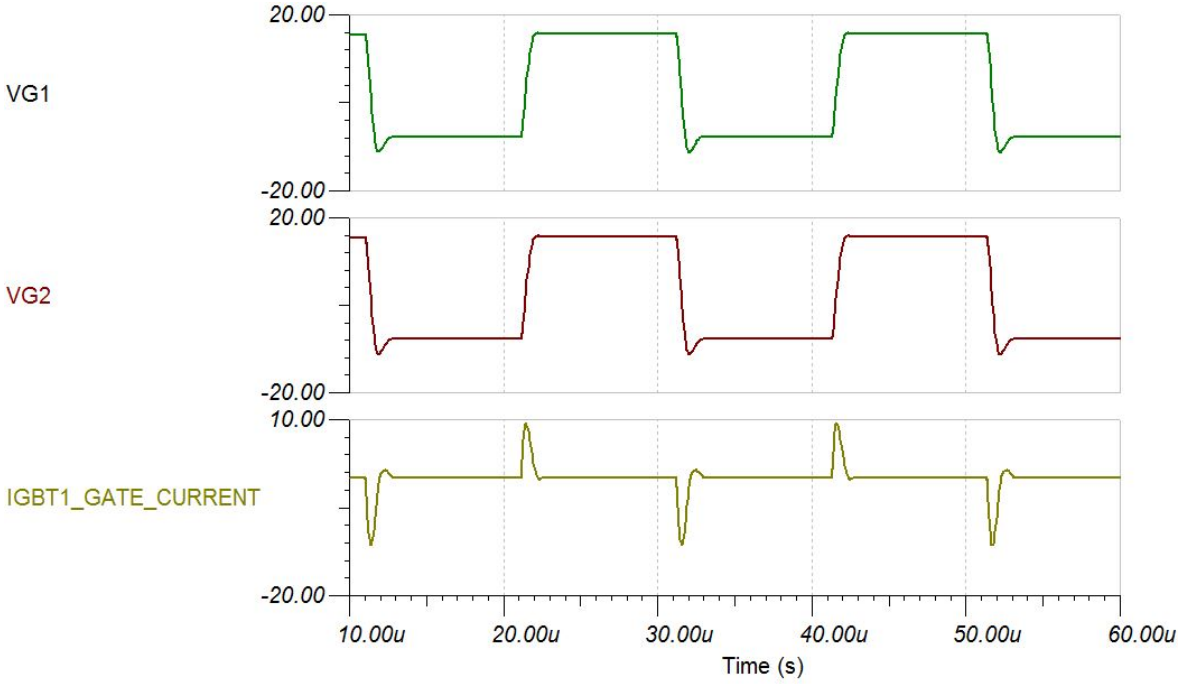

Figure 8. Simulation Results for Gate Current of IGBT

The actual source and sink current will be slightly less than the calculated values because of the turnon delays and rise and fall times of the buffer stage BJTs.

2.1.5 DESAT Pin

The DESAT fault detection prevents IGBT destruction due to excessive collector currents during a short-circuit fault. Short circuits caused by bad wiring or overload conditions induced by the load can cause a rapid increase in an IGBT current, leading to excessive power dissipation and heating. IGBTs become damaged when the current approaches the saturation current of the device and the collector-emitter voltage, V_{CE}, rises above the saturation voltage level, V_{CE-sat}. The drastically increased power dissipation overheats and destroys the IGBT.

To prevent damage to the IGBT, the ISO5852S slowly turns off the IGBT in the event of a fault detection. A slow turnoff ensures the overcurrent is reduced in a controlled manner during the fault condition. The DESAT fault detection involves a comparator that monitors the V_{CE} of the IGBT and compares it to an internal 9-V reference. If voltage across the IGBT reaches the threshold, DESAT detects it immediately, blocks the gate driver output, and initiates a soft-turnoff procedure that disables the OUTH and reduces the voltage at OUTL over a minimum time span of 2 µs. The output is hard clamped to VEE2 when OUTL reaches 2 V with respect to VEE2.

The DESAT diode D1 (D2 is shorted) conducts the bias current from gate driver, which allows sensing of the IGBT's saturated collector to emitter voltage when the IGBT is in the ON condition. D1 blocks high voltage when the IGBT is in the OFF condition. In this TI Design, D1 blocks a maximum of 1200 V during the IGBT OFF condition. D2 allows changing the threshold at which DESAT comparator triggers by replacing it with Zener of suitable breakdown voltage.

Switching inductive loads cause large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients results in large negative spike in the DESAT pin, which draw substantial current out of the device. To limit this current below damaging levels, a 1-kΩ resistor is connected in series with the DESAT diode.

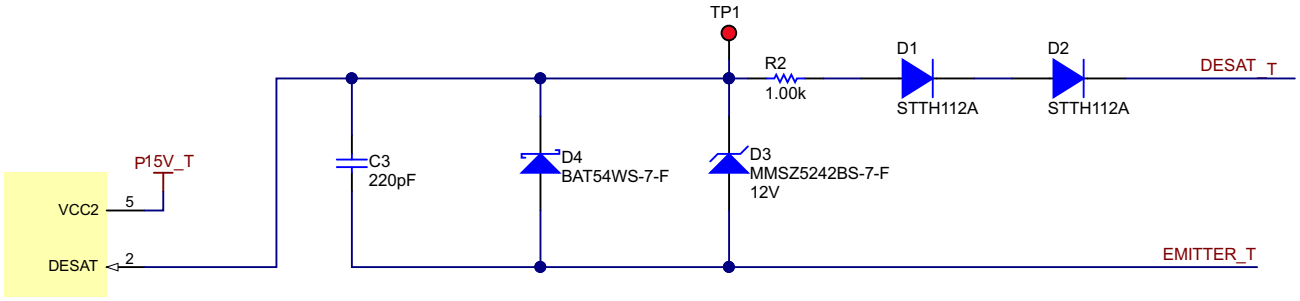

Figure 9. IGBT Desaturation Sensing Circuit

A 220-pF blanking capacitor C3 is required, which disables the DESAT detection during the off-to-on transition of the power device. Equation 4 calculates the blanking time.

$$t_{blank} = \frac{C_{blank} \times V_{DSTH}}{I_{charge}} = \frac{220\ pF \times 9\ V}{0.5\ mA} = 3.96\ \mu s \quad (4)$$

During the transition time, when the IGBT is changing state, a high dVCE/dt voltage ramp rate occurs across the IGBT. Equation 5 calculates the resultant charging current.

$$I_{charge} = C_{D\_DESAT} \times \frac{dV_{CE}}{dt} \quad (5)$$

$C_{D-DESAT}$ is the diode capacitance at DESAT. This current charges the blanking capacitor C3. The diode capacitance $C_{D-DESAT}$, along with C3, forms the voltage divider network. This voltage divider network results in IGBT collector voltage transients appearing at the DESAT pin attenuated by the ratio determined by Equation 6.

$$V_{DSAT\_transient} = \frac{V_{CE}}{\left(1 + \frac{C16}{C_{D\_DESAT}}\right)} \quad (6)$$

To avoid false DESAT triggering, fast recovery diodes with low capacitance are used. This design uses the STTH112A. The STTH112A is a 1-A, 1200-V_{RRM} diode with a reverse recovery time of 75 ns. The blanking capacitor chosen must have a large value, as a small value will lead to high transient voltage on the DESAT pin.

The voltage at the DESAT pin equals the sum of the forward voltage drop of D1 and the IGBT collector to emitter voltage. Equation 7 calculates the V_{CE} level that triggers a fault condition.

$$V_{CE\_Fault(TH)} = 9 - V_f - (0.5\ mA \times 1\ k\Omega) = 9 - 1.5 - 0.5 = 7\ V \quad (7)$$

2.1.6 Fault Detection

During IGBT overcurrent condition, a Mute logic initiates a soft-turnoff procedure that disables OUTH and pulls OUTL to low over a time span through internal constant current sink. When desaturation is active, a fault signal is sent across the isolation barrier pulling the FLT output at the input side low and blocking the isolator input. The FLT output condition is latched and can be reset only after RDY goes high, through an active low pulse at the RST input. The IGBT gate driver is disabled when a fault is detected and will not resume switching until the MCU applies a reset signal of 800 ns.

In this TI Design, an auto-reset circuit shown in Figure 10 has been provided externally. RST is pulled high at 5 V using a 20-kΩ resistor and a capacitor value of 0.01 µF. The RDY pin is logic high under normal conditions and the external Schottky diode is reverse biased so the RST pin also remains high; however, when a fault is encountered, the Ready pin goes low and the Schottky conducts thus pulling down the RST. By asserting RST low for at least the specified minimum duration (800 ns), the device input logic can be enabled or disabled.

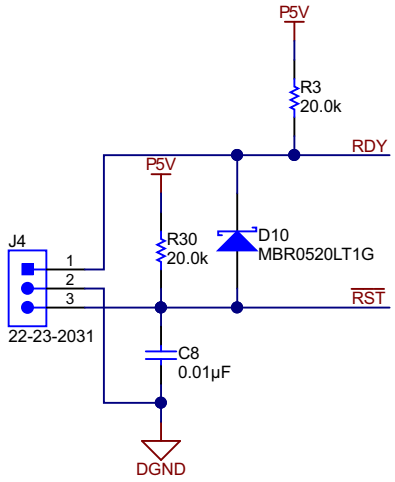

Figure 10. Auto-Reset Circuit

The time it takes for the RST to go high is dependent upon the time constant, which is given by T = RC = 20 kΩ × 0.01 µF = 0.2 ms. When RST is pulled down, the circuit resets itself automatically.

2.1.7 Adjustable Soft Turnoff

If a short circuit is applied to an IGBT that is already conducting, the dv/dt resulting from the rapid desaturation of the IGBT would boost the gate voltage of the IGBT and results in higher peak short-circuit current. The increased peak current increases the power dissipation and could cause IGBT failures. The effective way of protecting the IGBTs under overcurrent conditions is to use soft turnoff methods. Selectively slowing the IGBT turnoff under overcurrent conditions could reduce the transient voltage spike applied on the IGBT and improve the reliability of the system.

After overcurrent detection, the ISO5852S initiates a soft-turnoff procedure that disables OUTH and pulls OUTL to low over a time span of 2 μs. If the IGBT module is directly connected to the gate driver IC, the gate charge of the IGBT is slowly discharged through the internal current sink of the Isolator during turnoff. But in this TI Design, a current booster stage is present in between the driver and the IGBT. Therefore, in order to provide a soft turnoff of the device, an additional circuit consisting of a resistor, R10, and a capacitor, C39, is connected at the OUTL arm. The capacitor C39 aids in the slow discharging of current through the internal current sink. The soft-turnoff time can easily be adjusted by varying the values of R10 and C39, as shown inFigure 11.

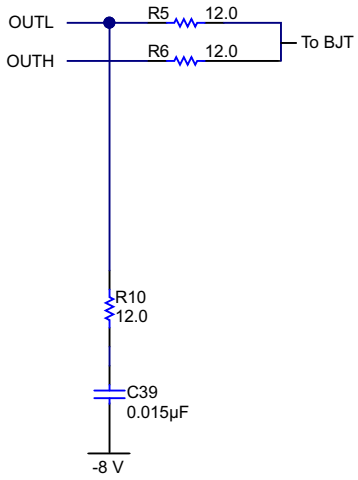

Figure 11. Adjustable Soft Turnoff Circuit

2.2 Current Sharing Between Parallel IGBT Modules

In many high-power applications, the required current levels can only be achieved by connecting two or more IGBT modules in parallel. When connected in parallel, it is important that the circuit design allows for an equal flow of current to each of the modules. If the current is not balanced among the IGBTs, a higher current may build up in just one device and destroy it. Differences on static and dynamic behavior of paralleled IGBTs affect the current sharing each branch and also de-rate the effective output current.

2.2.1 Static Variations

These variations are primarily due to the following sources:

- V_{CE-SAT}
- Transconductance

Because the two devices are connected in parallel, the conducting stage voltage across the devices is the same. The static current (I_{load} = IC2 + IC1) splits as determined by the set of output characteristics, which in turn are dependent on those two factors.

Selecting a proper IGBT with a positive temperature co-efficient as well as less parametric variation is the key in overcoming the imbalance in current.

2.2.2 Dynamic Variations

The dynamic current imbalance is mainly due to the following parameters:

- The distribution of device parameters, for example, the threshold voltage $V_{GE(th)}$ and the switching characteristics of IGBT, especially the gate-emitter capacitance and miller capacitance.
- The propagation delay through the gate drive circuit.
- The parasitic inductance in the paralleled branches.

The turnon delay of the IGBT is dependent on the threshold Voltage $V_{GE(th)}$, the gate resistance and the equivalent input capacitance of the IGBT. So if the two devices are not turning on at the same time, then the one that is turning faster has to carry more current at that moment.

If one of the IGBT has lower value of $V_{GE(th)}$ or gate capacitance then it will turn on faster than the other one. If the driver had one common gate resistance, then during the Miller region of the faster IGBT, the gate voltage of the slower device will not be able to rise and it will remain off. As a result, the collector current will not be shared between the two devices with majority passing only through the faster IGBT during transition. To avoid this, two separate gate resistors have been provided in the gate drive path, which helps the gate voltage of the paralleled IGBTs increases independently. Providing a gate resistor for each IGBT also reduces the possibility of oscillations between the paralleled devices.

The rate of rise of collector currents will dependent on the parasitic inductances on the emitter side of the IGBTs, which is another contributing factor for the mismatch in the dynamic current shared between the two devices. See Section 2.2.3 for more info.

In order to match the switching speeds of the paralleled devices as much as possible, proper layout techniques are essential. To achieve this, the layout must be as symmetrical as possible to match the parasitic inductances as closely as possible. Minimizing the impedance and impedance mismatch is very important. See Section 5.3 for more details.

2.2.3 Common Emitter Inductance

Some stray inductance is present at the emitter of the IGBT modules. The value of stray inductance for the two IGBTs could differ. Because the IGBTs are connected in parallel, the common ground voltage will remain the same for both the IGBTs but the auxiliary emitter voltages will differ. This voltage difference between the auxiliary emitter terminals of the two IGBTs results in current flow from one terminal to the other as shown in Figure 12. Depending on the direction of the circulating current the actual voltage at the IGBT gates will either increase or decrease resulting in unequal current sharing.

The voltage at the gate of the IGBTs is given by Equation 8 and Equation 9.

$$V_{ge1} = V_{ge} - V_{Rg1} - V_{Zpar1} \quad (8)$$

$$V_{ge2} = V_{ge} - V_{Rg2} - V_{Zpar2} \quad (9)$$

where:

- Rg1 and Rg2 are the gate resistors
- Zpar1 and Zpar2 are the parasitic track impedances

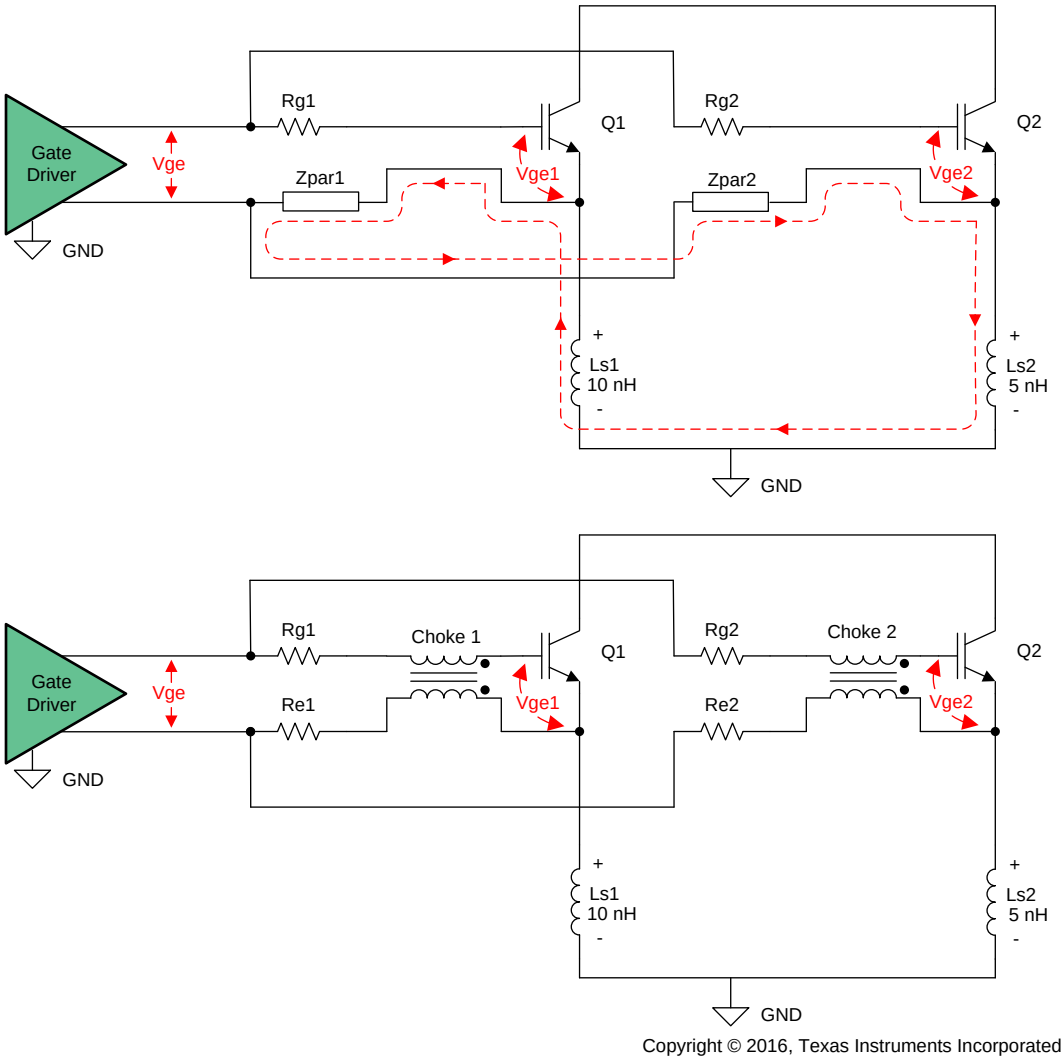

Figure 12. Effect of Parasitic Emitter Inductance

Assuming equal current sharing and equal di/dt during turnon in both the parallel connected IGBTs, the induced voltage across the stray inductances can be calculated in Equation 10 and Equation 11.

$$V_{Ls1} = \frac{di_{e1}}{dt} \times L_{s1} = \frac{150\ A}{\mu s} \times 10\ nH = 1.5\ V \quad (10)$$

$$V_{Ls2} = \frac{di_{e2}}{dt} \times L_{s2} = \frac{150\ A}{\mu s} \times 5\ nH = 0.75\ V \quad (11)$$

where:

- Ls1 is the stray inductance of the connection between the emitter of Q1 and the common ground
- Ls2 is the stray inductance of the connection between the emitter of Q2 and the common ground
- die1/dt is the rate of change of current through Q1 during turnon
- die2/dt is the rate of change of current through Q2 during turnon

The drop of 0.75 V between the two auxiliary emitter terminals causes a circulating current I_{cir} through Zpar1 and Zpar2. The gate voltage Vge1 decreases by I_{cir} × Zpar1 and the gate voltage Vge2 increases by I_{cir} × Zpar2 causing both IGBT modules to turn on at slightly different instants resulting in unequal current sharing.

There are two ways in which the circulating current can be overcome:

1. Addition of emitter gate resistor Re1. This helps in attenuating the circulating current.
2. Use of common-mode choke in the gate path. The effect of common mode choke is explained in detail in Section 2.2.4

2.2.4 Common-Mode Choke

A common-mode choke works as a simple wire against a differential mode current. The differential mode current flows in opposite directions through the choke windings and creates equal and opposite magnetic fields, which cancel each other out. This results in the choke presenting zero impedance to the differential mode signal. Thus, the differential signal passes through the choke unattenuated.

The common-mode choke works as inductor against a common-mode current. The common-mode current, flowing in the same direction through each of the choke windings, creates equal and in-phase magnetic fields, which add together. The magnetic flux caused by the common-mode current is accumulated and hence produces impedance. The choke presents a high impedance to the common-mode signal, which passes through the choke heavily attenuated.

To prevent noise, select the common-mode choke coil whose common-mode insertion loss is large in noise frequency. The insertion loss (α) for the common-mode signal and the differential-mode signal provided by the common-mode choke used in this TI Design is expressed graphically in Figure 13.

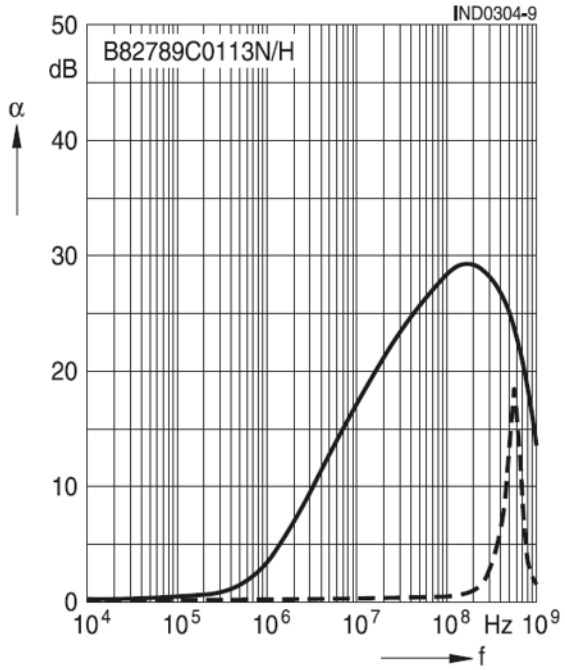

Figure 13. Common-Mode Choke Insertion Loss

See Figure 12 for how the common-mode choke is used at the gate terminals of the IGBT to avoid circulating currents due to emitter inductance mismatch.

3 Getting Started Hardware

3.1 Board Description

Figure 14 shows the TIDA-00917 board mounted on IGBT modules. The board has to be powered up by supplying the primary side voltage of 5 V and secondary side voltage of 23 V. The 5-V supply is provided using the connector J1 and 23-V supply is provided by using the connector J2 and J3 for the top and bottom IGBT driver, respectively. After powering up the board, the status of the Ready pin can be checked to ensure that there is no problem with the supply voltages. Connector J4 provides a pin to indicate the Ready signal. Now the PWM signal can be applied to the connector J1 for the top and bottom IGBTs, and the output can be observed in the form of a gate voltage of the IGBTs.

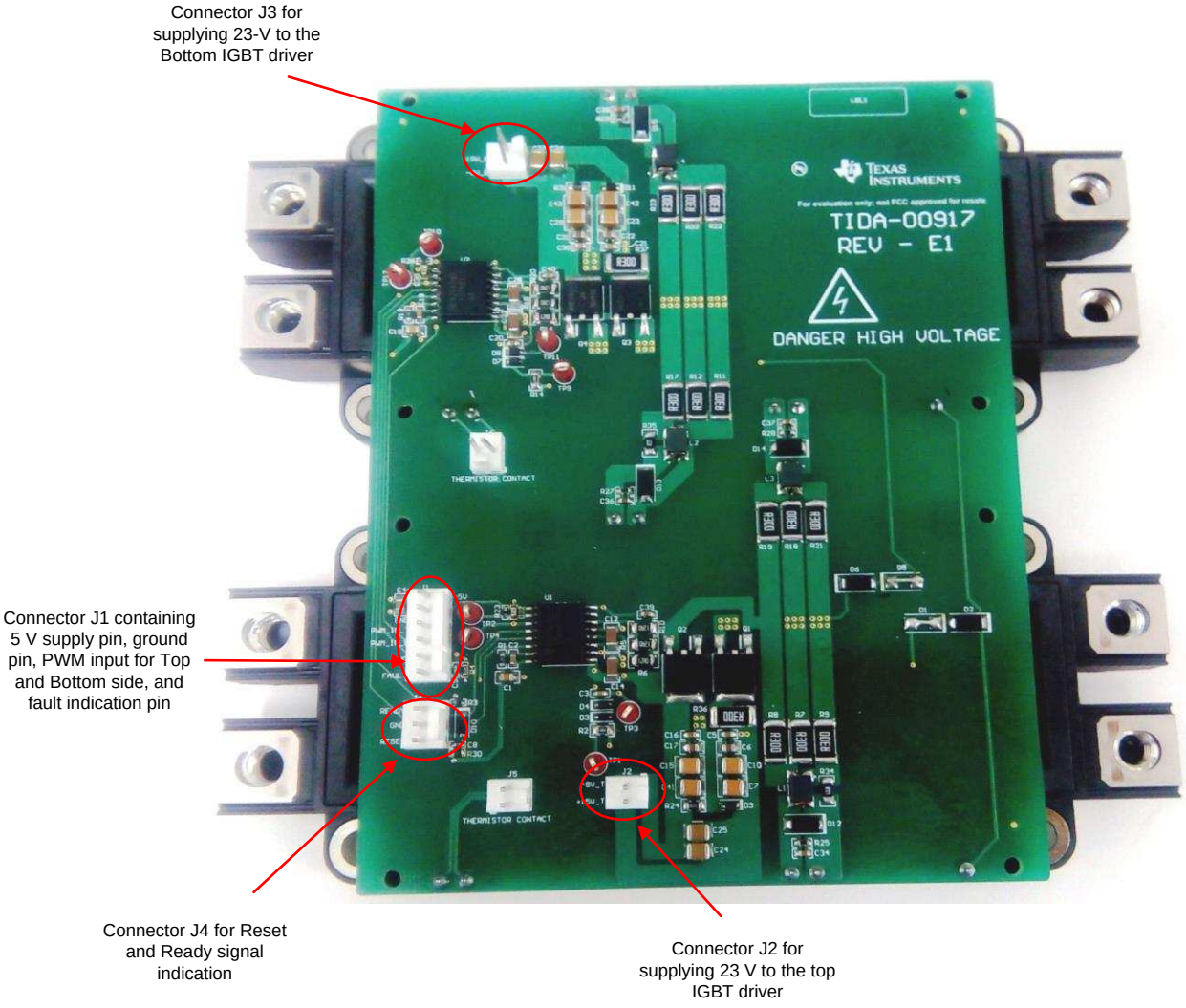

Figure 14. Board Description

3.2 Connector Description

Table 2. Connector Pin Description

CONNECTOR	PIN NUMBER	PIN NAME	I/O	DESCRIPTION
J1	1	P5V	PWR	Primary side supply voltage
	2	DGND	PWR	Ground pin
	3	PWM_IN_TOP	I	PWM signal for top IGBT gate driver
	4	PWM_IN_BOTTOM	I	PWM signal for bottom IGBT gate driver
	5	FLT	O	Active low if any of the IGBT driver detect desaturation of associated IGBT
	6	DGND	PWR	Ground pin
J2	1	P15V_T	PWR	VCC2 for top IGBT gate driver
	2	P8V_T	PWR	VEE2 for top IGBT gate driver
J3	1	P15V_B	PWR	VCC2 for bottom IGBT gate driver
	2	P8V_B	PWR	VEE2 for bottom IGBT gate driver
J4	1	RDY	O	Power-good output, active high when both supplies are healthy
	2	RST	I	Reset input, apply a low pulse to reset fault latch
	3	DGND	PWR	Ground pin

4 Testing and Results

4.1 UVLO Protection

The following waveforms show the UVLO protection feature of the gate driver. The IGBT is turned off if the supply VCC1 drops below 1.7 V irrespective of IN+, IN–, and RST until VCC1 goes above 2.25 V. In a similar manner, the IGBT is turned off if the supply VCC2 drops below 11 V irrespective of IN+, IN–, and RST until VCC2 goes above 12 V. As shown in Figure 15, as soon as the secondary side positive voltage falls below 11.7 V, the gate driver output turns off immediately.

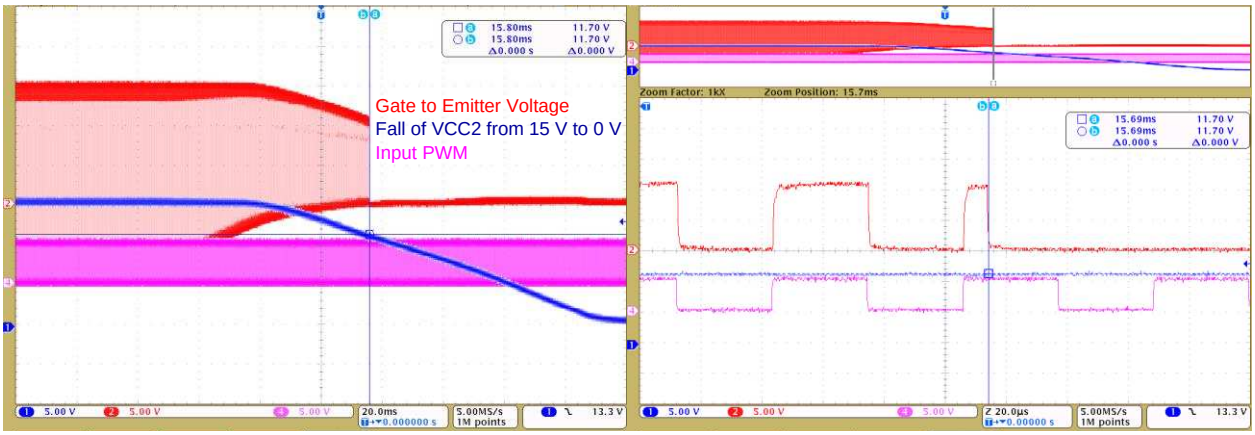

Figure 15. UVLO Detection for V_{CC2}

4.2 Auto-Reset Functionality

To capture the effect of the auto-reset circuit, the DESAT pin of the gate driver is disconnected from the collector pin of the IGBT module. A continuous PWM signal of 16.67 kHz is applied at the input. The gate voltage and RESET and FAULT pins are observed in the oscilloscope. As seen in Figure 16, when the Ready pin goes low, the signal at the Reset pin is also pulled low.

The time constant associated with the RC circuit is 200 µs. Positive-going input threshold voltage for the RESET pin is 3.5 V. The negative side voltage is limited by the diode that is put in parallel to the resistor, hence its value is 0.7 V. In order to drive the voltage from 0.7 V to 3.5 V, the time required is approximately 0.6 times the time constant associated with the circuit, which comes out to be 120 µs. This value is in perfect relation with the experimental value as shown in Figure 16. This time period can be varied by changing the time constant associated with the circuit.

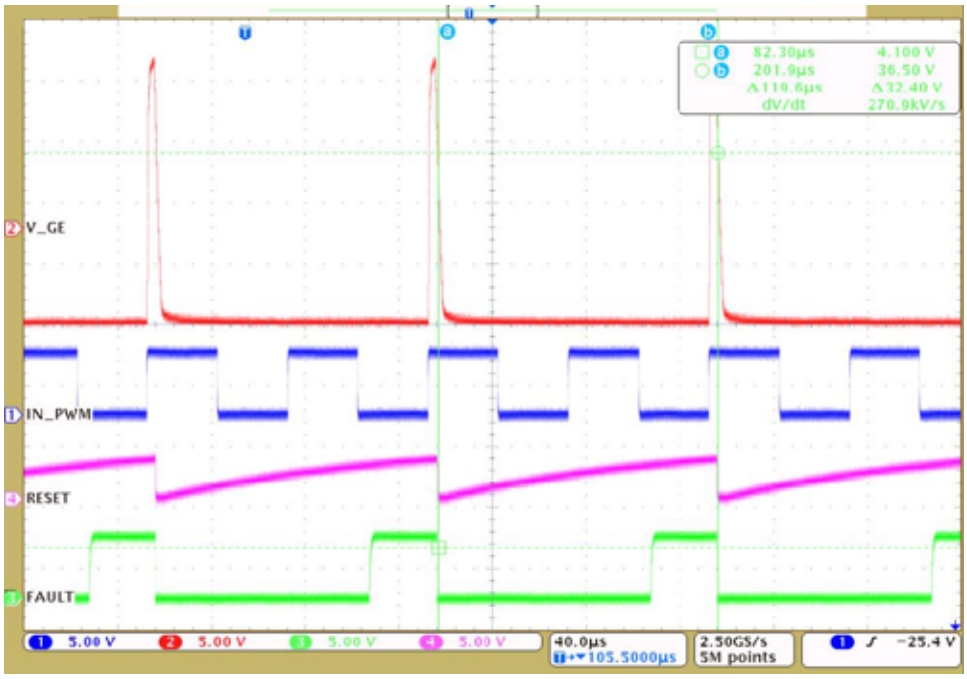

Figure 16. Auto-Reset Waveforms

4.3 Soft Turnoff Time

The soft-turnoff is 2 µs for a 10-nF load. Because this TI Design uses a load of 15 nF, the expected soft-turnoff time is 3 µs. This complies approximately with the experimental value of 4 µs as shown in Figure 17.

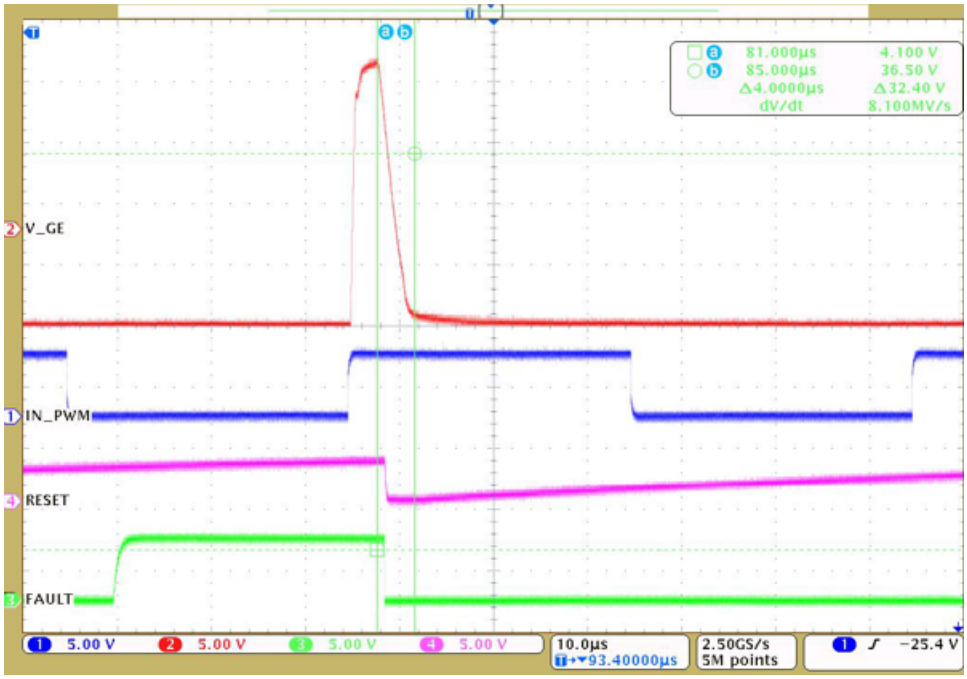

Figure 17. Soft Turnoff Time

4.4 Source and Sink Currents

The source and sink current waveforms have been captured for the top IGBTs by measuring the voltage drop across the emitter resistors R9 and R21. Figure 18 shows the left and right IGBT modules.

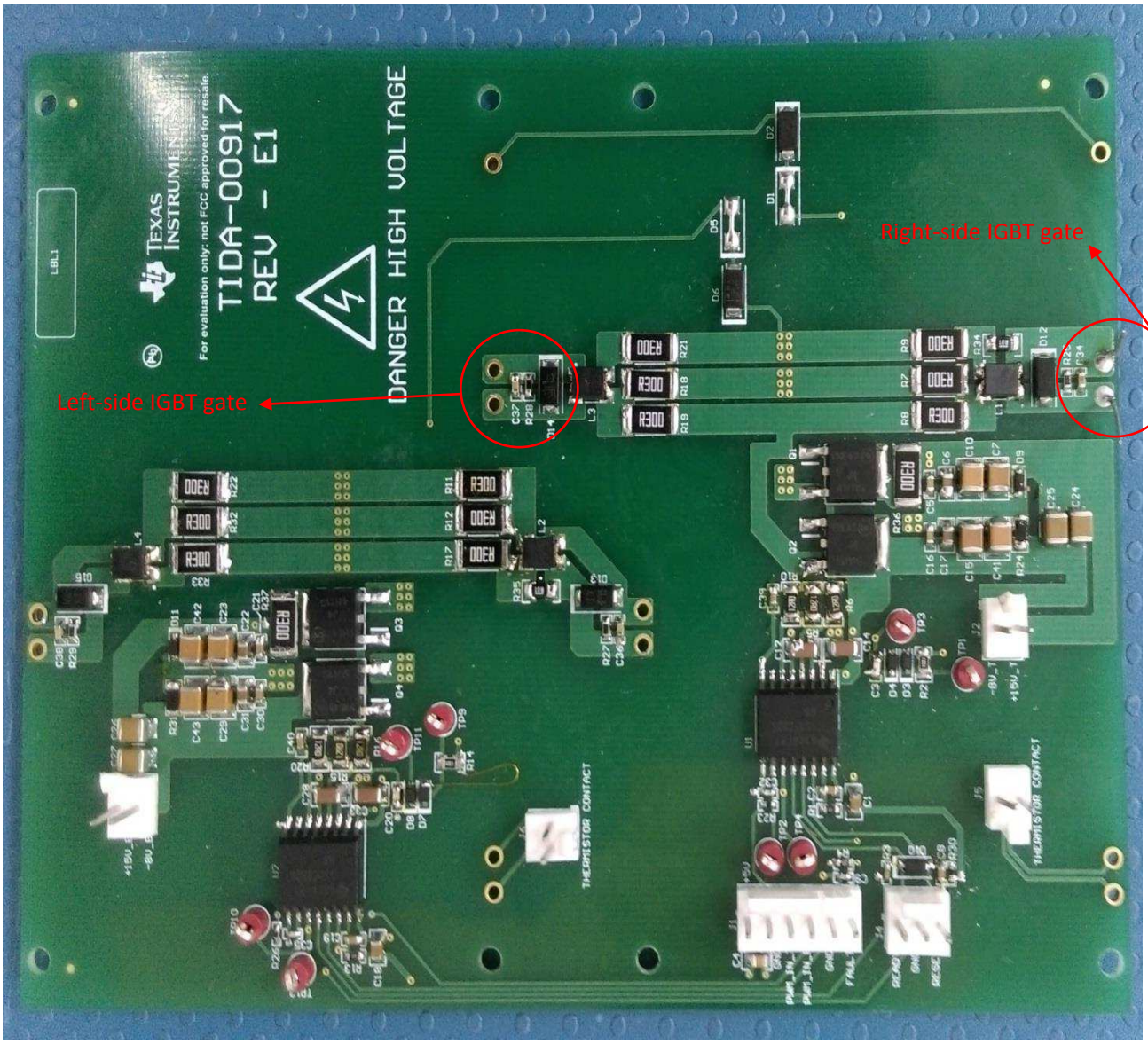

Figure 18. Left and Right IGBT Modules

4.4.1 Source Current

As shown in Figure 19, the voltage drop across the R9 is same as that for R21. As a result, the source currents going into the gates of both the IGBTs are equal and can be calculated with Equation 12:

$$\text{Source current} = \frac{\text{Voltage drop across R9 / R21 with trigger point set origin}}{\text{Value of R9 / R21}} = \frac{2\ \text{V}}{0.3\ \Omega} = 6.67\ \text{A} \quad (12)$$

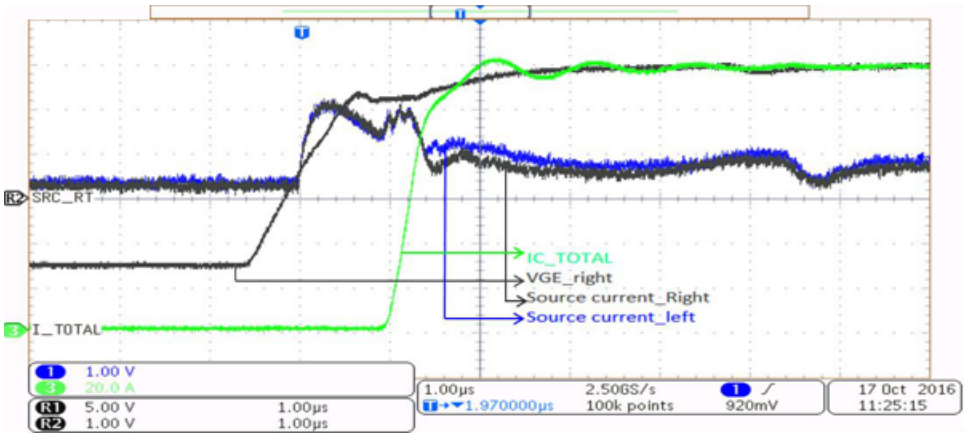

Figure 19. IGBT Gate Source Current Waveforms

In Figure 19:

- IC_TOTAL is the total phase current into the parallel IGBT module
- VGE_right is the gate to emitter voltage of one of the parallel IGBTs (right side IGBT)
- Source current_Right is the gate current of one of the parallel IGBTs (right side IGBT)
- Source current_Left is the gate current of the other parallel IGBT (left side IGBT)

4.4.2 Sink Current

As shown in Figure 20, the voltage drop across the R9 is same as that for R21. The sink currents coming out of the gates of both IGBTs are equal and can be calculated with Equation 13:

$$\text{Sink current} = \frac{\text{Voltage drop across R9 / R21 with trigger point set origin}}{\text{Value of R9 / R21}} = \frac{2.4\ \text{V}}{0.3\ \Omega} = 8\ \text{A} \quad (13)$$

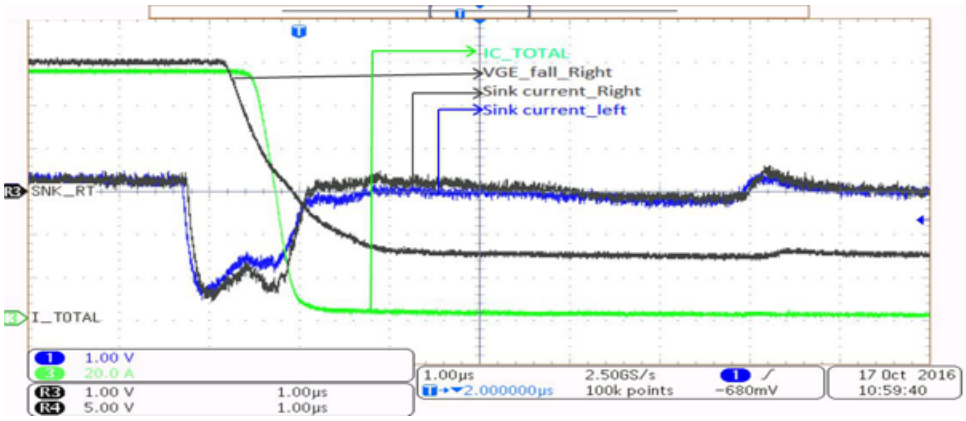

Figure 20. IGBT Gate Sink Current Waveform

In Figure 20:

- IC_TOTAL is the total phase current into the parallel IGBT module
- VGE_fall_right is the gate to emitter voltage of one of the parallel IGBTs (right side IGBT)
- Sink current_Right is the gate current of one of the parallel IGBTs (right side IGBT)
- Sink current_Left is the gate current of the other parallel IGBT (left side IGBT)

4.5 Rise and Fall Time of V_{CE}

The test setup for measuring the V_{CE} rise and fall times has been shown in Figure 21. For validating the board, Infineon IGBT with part number FF450R12ME4 has been used. The bus voltage is set to 600 V through an external power supply, with the positive terminal connected to the collector of the top IGBTs and negative terminal connected to the emitter of the bottom IGBTs. A 4.7-Ω resistor is used as a load for the setup. The probing points for measuring currents have been highlighted in Figure 21.

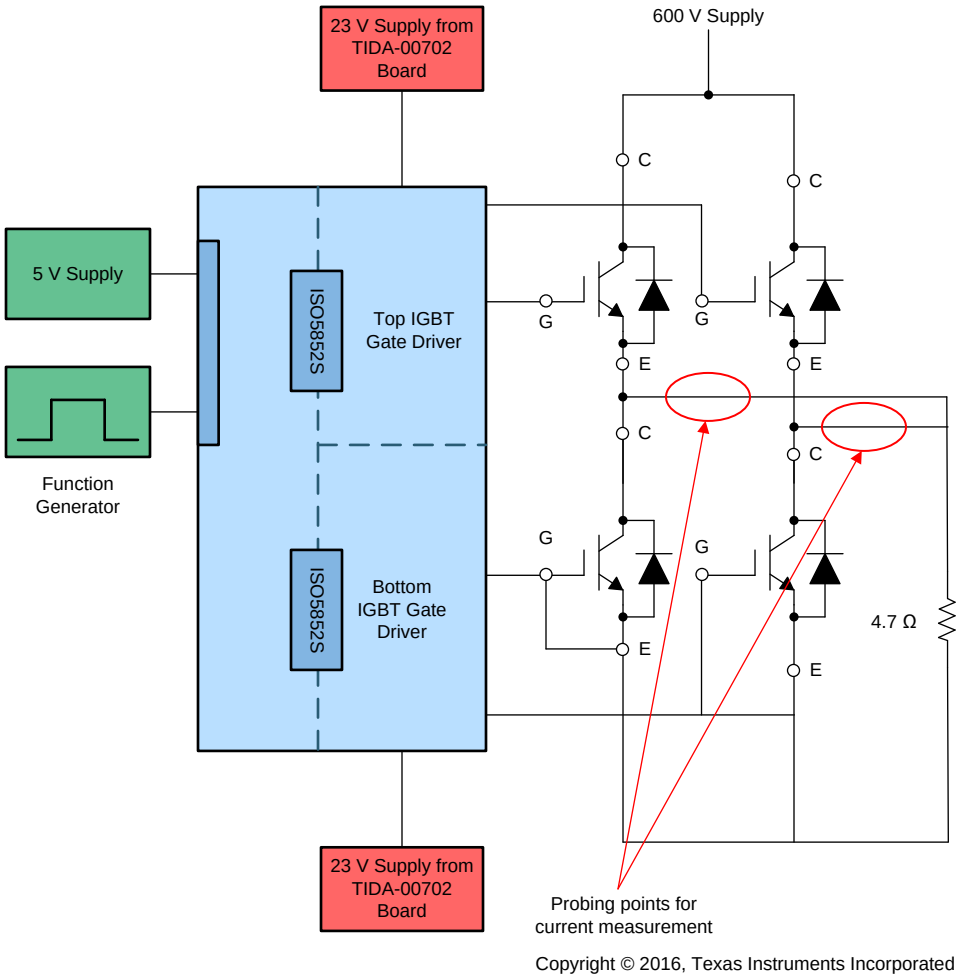

Figure 21. Test Setup for Measuring Collector Currents and V_{CE} Rise and Fall Times

Figure 22 and Figure 23 show the rising and falling edges of the V_{CE}, respectively. With the setup shown in Figure 21, switching times of 400 ns have been achieved. For applications that require smaller switching times, gate resistors can be reduced to obtain higher source and sink currents.

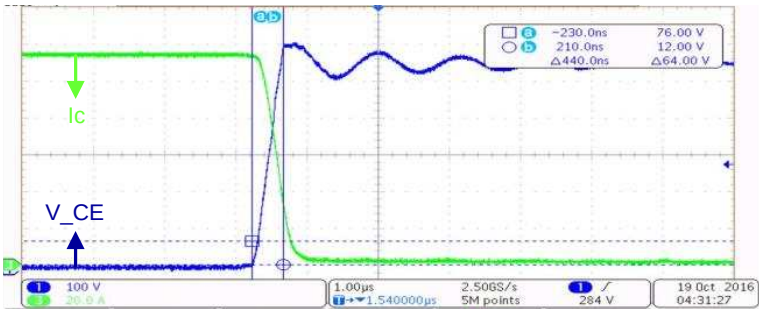

Figure 22. V_{CE} Rise Time

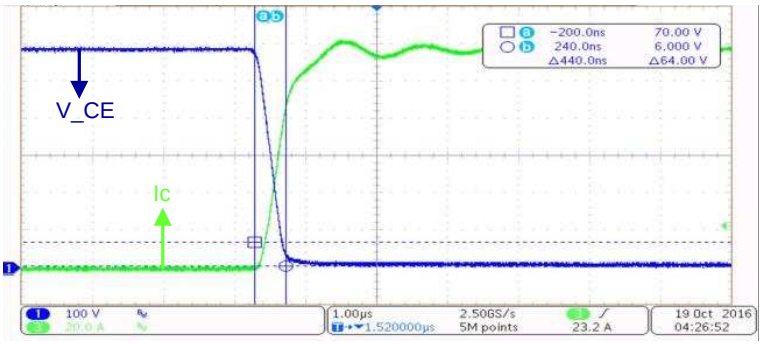

Figure 23. V_{CE} Fall Time

4.6 Current Sharing Between Right and Left IGBTs

Figure 26 shows the current sharing between the top IGBTs when an input pulse of 100 µs is applied to the primary side of the gate driver. As shown in Figure 24, there is a difference of 20 A between the dynamic current shared by the two devices. This difference is because of the turnon delay time of the two IGBTs, V_{CE-SAT}, and the parasitic inductances of the paralleled branches. As shown in Figure 25, the static current shared between the two devices becomes almost equal after a time period of 60 µs as shown in Figure 26.

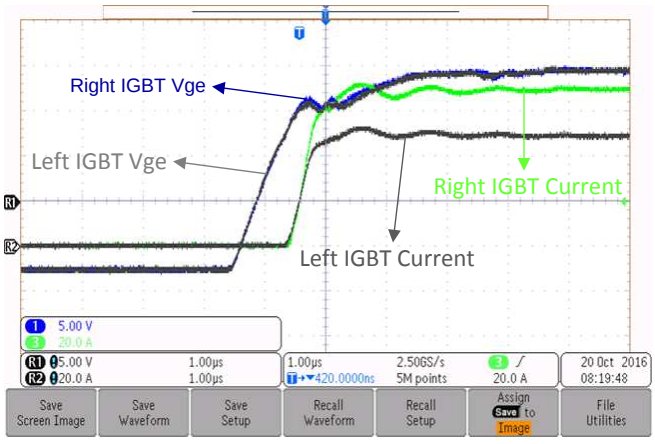

Figure 24. Current Sharing During IGBT Turnon

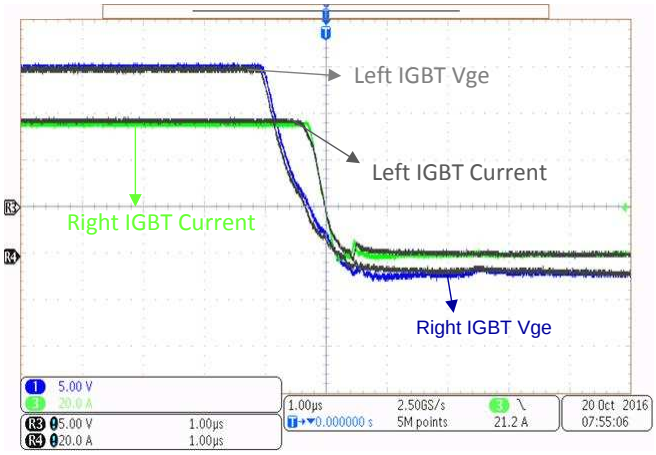

Figure 25. Current Sharing During IGBT Turnoff

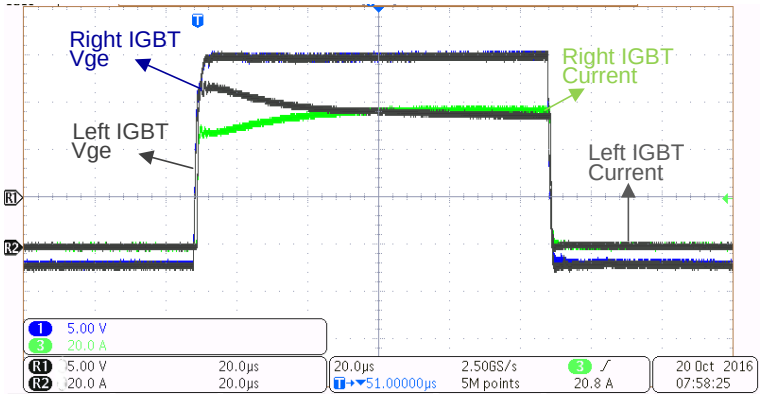

Figure 26. Current Sharing During One PWM Pulse

4.7 Short-Circuit Test

Figure 27 shows the setup for the short-circuit test. The short-circuit test is conducted to make sure that the input PWM is blocked as soon as the condition for overcurrent is detected by the DESAT pin of the gate driver I_C.

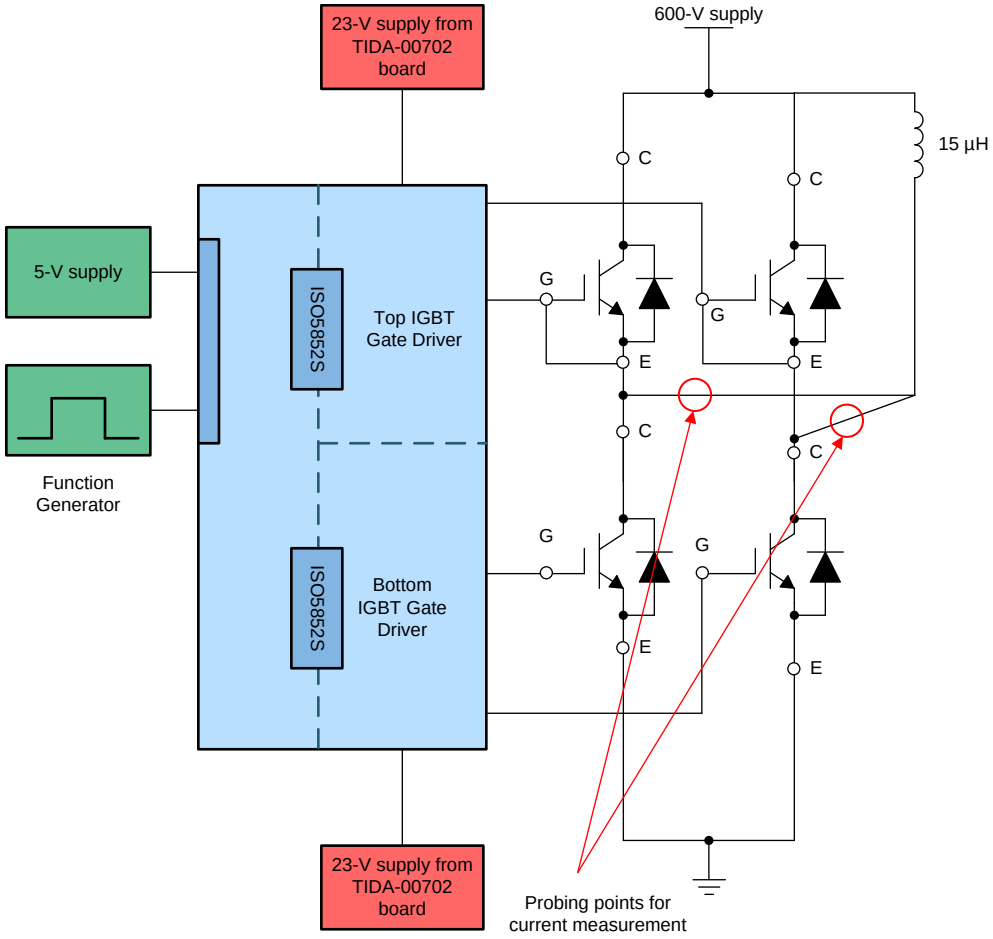

Figure 27. Short-Circuit Test Setup

In order to drive the IGBT into saturation at 15 V, a current of approximately 2000 A needs to be passed through each IGBT. Due to test setup limitations, 360 A of current is passed through each IGBT and the DESAT voltage sense threshold is decreased by adding a 5.1-V Zener diode at D6 and increasing R14 resistor to 2.5K.

The DESAT pin voltage gets charged up to a value of about 8.8 V due to the charging of the 220-pF capacitor. The time taken by the blanking capacitor to charge to 8.8 V can be calculated using Equation 14:

$$t_{charge} = \frac{C_{blank} \times V}{I_{charge}} = \frac{220\ pF \times 8.8\ V}{0.5\ mA} = 3.87\ \mu s \quad (14)$$

This charging time can be approximated to 5 µs, which can be seen in the test results shown in Figure 28 and Figure 29.

After 5 µs as the current flowing through the IGBT increases, the saturation voltage of the IGBT also increases. Finally, as the current flowing through the IGBT reaches 360 A, the DESAT pin voltage reaches to 9 V.

Figure 29 shows that when the DESAT pin voltage reaches 9 V, the fault signal is triggered. Triggering the fault signal blocks the isolator input and initiates a soft turnoff process, pulling the output of the isolator low.

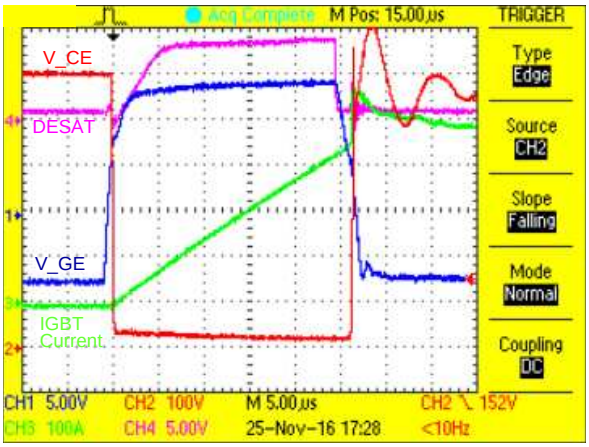

Figure 28. IGBT DESAT Waveform Showing V_{CE}

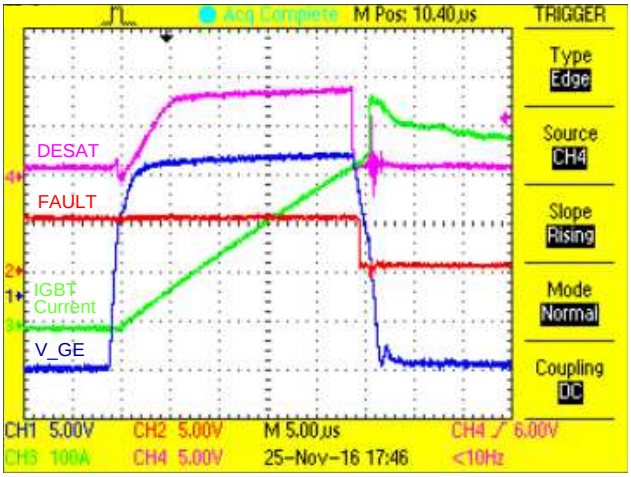

Figure 29. IGBT DESAT Waveform Showing Fault Signal

4.8 Improving Turnon and Turnoff of IGBT

The rise and fall times of V_{CE} can be improved by increasing the source and sink currents, respectively. The BJTs used in this TI Design are rated to handle 16 A of the pulse current, so a BJT with a higher current rating needs to be used to accommodate the increase in the source and sink currents. A capacitor can also be used in parallel to the base resistor of the BJT in order to supply the excess current in the base. For obtaining the improved fall time, the value of base resistor recommended is 12 Ω. In parallel to this resistor, a capacitor of 10 nF is also recommended.

Moreover, the use of resistive load would limit the rise and fall time of the V_{CE} due to stray components. In order to avoid this and further improve the switching times, an inductive load can be used instead of the 4.7-Ω resistor.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00917.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00917.

5.3 PCB Layout Recommendations

Layout is very important in ensuring equal current sharing between the two IGBTs. The switching loops must be kept to a minimum to reduce EMI and ringing.

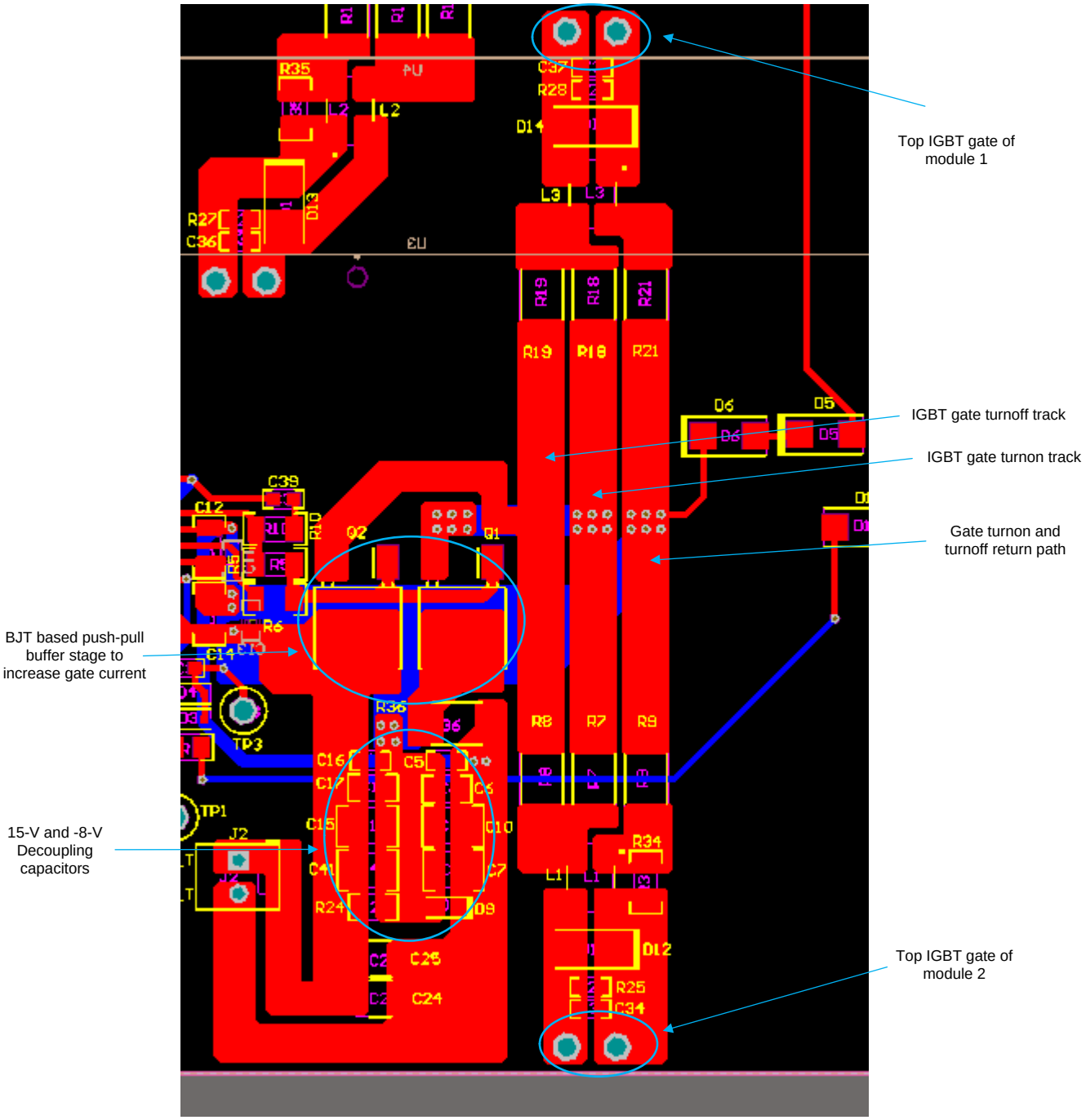

Figure 30. Current Buffer Stage Interface to IGBT Gate

Figure 30 shows the location of the gates of the two IGBT modules connected in parallel. Also shown are the IGBT turnon and turnoff gate current paths and the gate current return path. Both are driven from a single push-pull buffer stage. The following guidelines ensure reliable operation:

- Place the 15-V and –8-V decoupling capacitors close to the BJT buffer stage. This ensures the smallest possible gate current drive loop area.
- Connect the output of the push-pull buffer stage to the gate drive tracks in such a way that the distance to each of the IGBT gates is equal as shown in Figure 31.

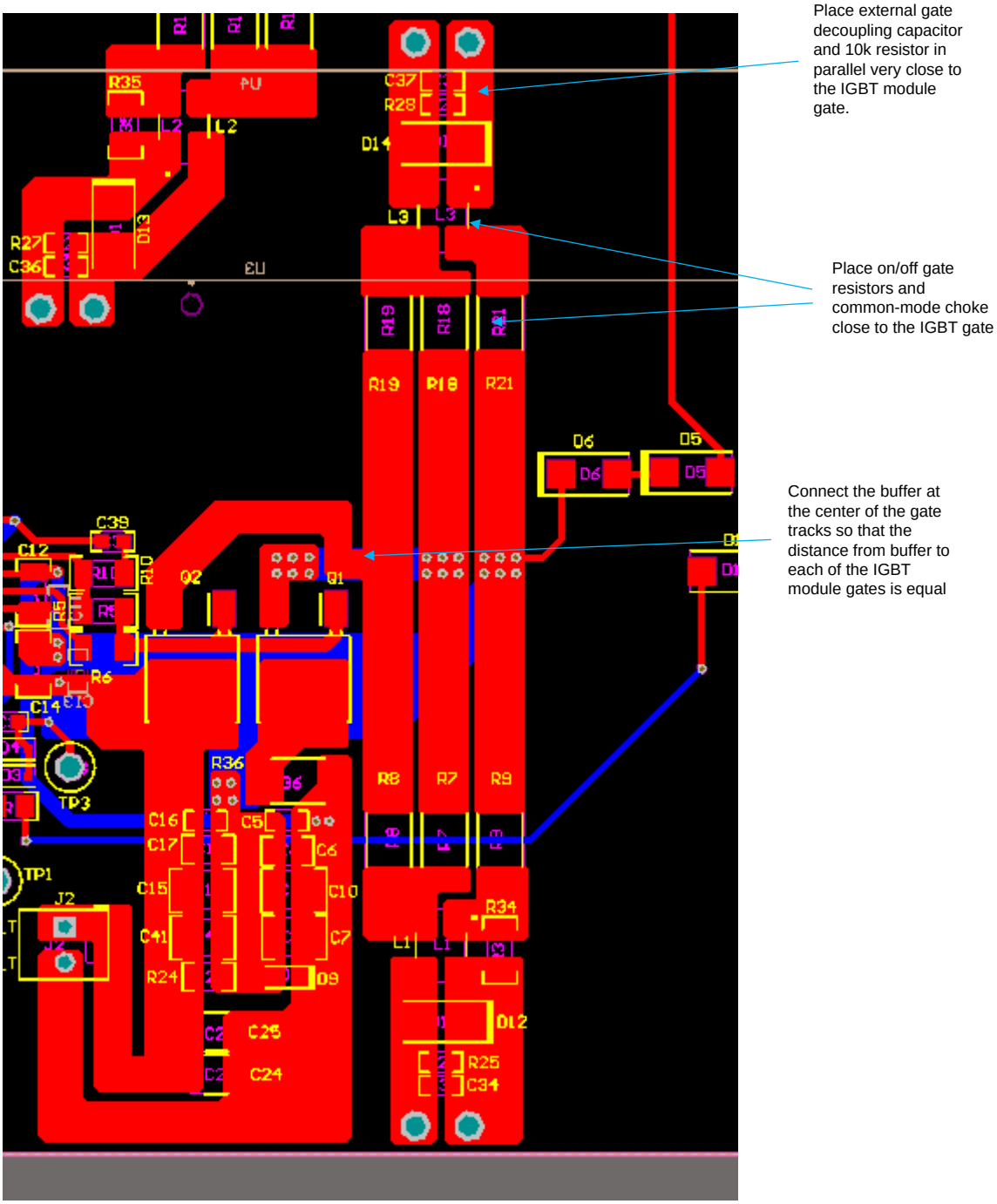

Figure 31. Connection of Buffer to Gate Track

- Make the gate on and off current tracks as wide as possible to minimize track impedance.
- Place the external gate decoupling capacitor right next to the module gate.
- Place the 10-kΩ resistor next to the decoupling cap. This resistor ensures that the IGBT is turned off in case the gate drive is floating due to faulty conditions.
- Place the common-mode choke and the gate current control resistors close to the module gate.
- Maintain a minimum spacing of 8 mm between the primary and secondary sides to ensure reinforced isolation as shown in Figure 32.

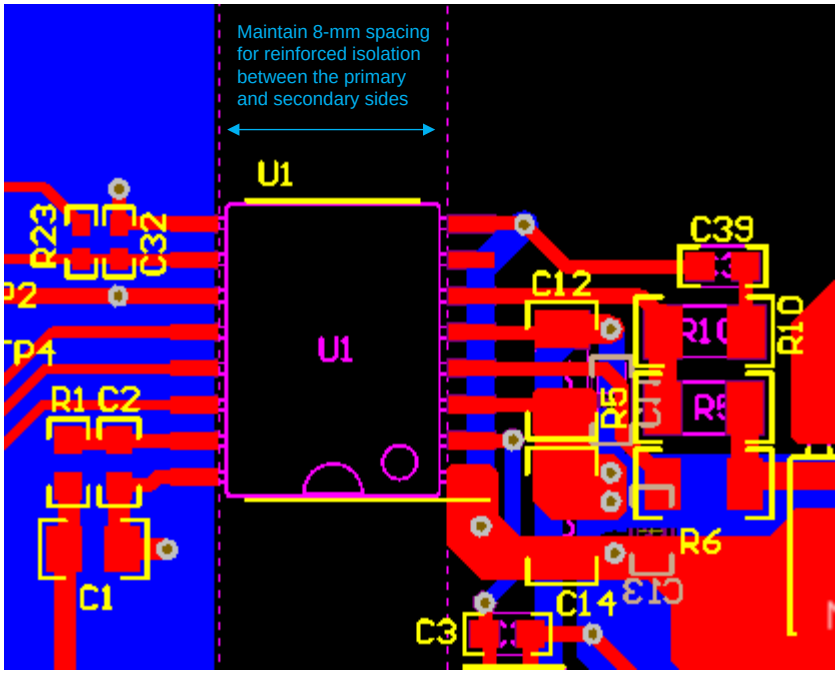

Figure 32. Spacing for Reinforced Isolation

- Keep the gate turnon and turnoff paths equidistant to both the IGBT module gates as shown in Figure 33 and Figure 34. The paths should have as minimum a loop area as possible to reduce parasitic inductance and capacitance due to the track length.

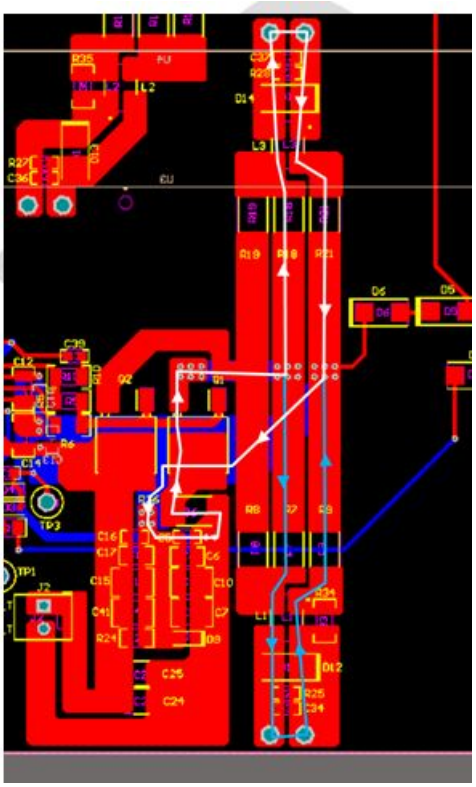

Figure 33. IGBT Gate Turnon Current Path

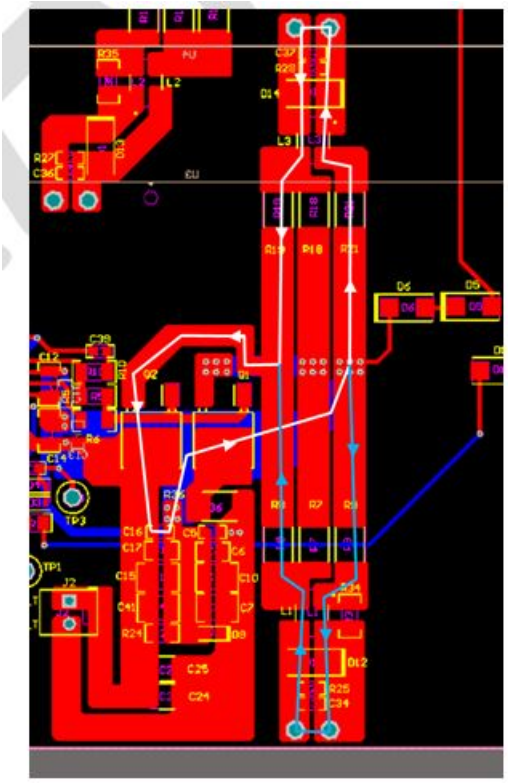

Figure 34. IGBT Gate Turnoff Current Path

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00917.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00917.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00917.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00917.

6 References

1. Texas Instruments, *High-voltage reinforced isolation: Definitions and test methodologies*, Marketing White Paper (SLYY063)
2. Texas Instruments, *60-W, 24-V, High-Efficiency Industrial Power Supply With Precision Voltage, Current, and Power Limit*, TIDA-00702 Design Guide (TIDUB51)

6.1 Trademarks

7 Terminology

IGBT— Insulated gate bipolar transistor

PWM— Pulse width modulation

NTC— Negative temperature coefficient thermistor

8 About the Authors

AISHWARYA BHATNAGAR is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems. Aishwarya earned her bachelor of technology in electronics and communication engineering from MNNIT, Allahabad.

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision	Page
• Changed language and images to fit current style guide	1

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