Design Guide: TIDA-050058

Zero-Cross Switching for Solid-State Relays Reference Design

Description

This reference design shows how to achieve zero cross switching (ZCS) with a solid-state relay. The reference design features the TPSI3050-Q1 isolated switch driver. TPSI3050-Q1 device integrates a laminate transformer to achieve isolation while transferring signal and power to the secondary side. This removes the need for any isolated bias supply. In addition, the TPSI3050-Q1 device can supply auxiliary current (I_{AUX}) to external circuitry located on the high voltage (HV) side. Zero-cross switching is done while maintaining signal isolation between the low voltage (LV) and HV side. This reference designed achieved a 12-V, 200-us delay ZCS with a 110 V_{RMS}, 60 Hz AC source.

Features

- No isolated secondary supply required
- 5-kV_{RMS} reinforced isolation
- 500-V_{DC}/350-V_{RMS} load with 4-A max
- Zero-voltage switching (ZVS)
- Solid-state relay (SSR) solution
- < 4-us immediate load disconnect

Applications

- Solid State Relay (SSR)
- Grid infrastructure
- Building automation
- Factory automation and control
- Appliances

Resources

TIDA-050058	Design Folder
TPSI3050-Q1	Product Folder
AMC23C10	Product Folder
SN74HCS72-Q1	Product Folder
TMUX1219	Product Folder

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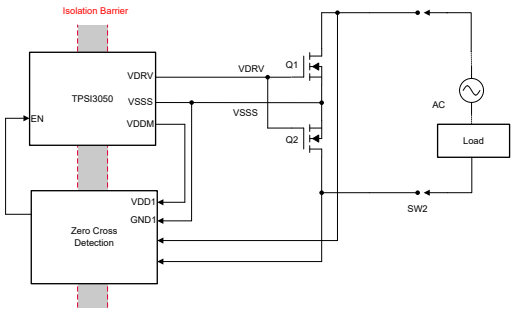

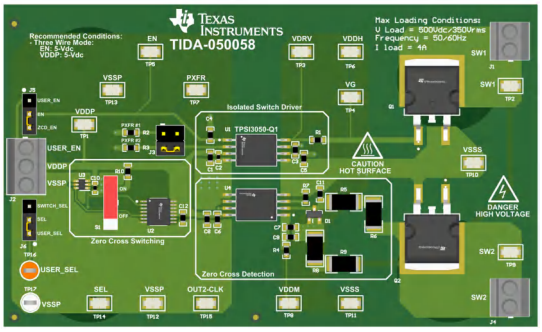

1 System Description

Zero cross detection allows a circuit to detect when the load AC waveforms has reached the zero-voltage point. Switching ON when the AC source is at zero volts increases the system efficiency and reliability. If an AC source is switched ON while the source is on its peak voltage, it could result in high frequency switching noises, high inrush current spikes, and dangerous stress to the system. This reference design features a SSR implemented with the TPSI3050-Q1 isolated switch driver and back to back N-Channel MOSFETs. TPSI3050-Q1 generates a 10 V rail to drive the gate of the power FETs and a mid-rail supply of 5 V to power HV side circuitry needed for the zero-cross switching logic. The TPSI3050-Q1 offers 5 kV_{RMS} reinforced isolation and AEC-Q100 qualification for automotive applications while the TPSI3050 offers 3 kV_{RMS} basic isolation for industrial applications.

Figure 1-1 shows the operation of designs with and without zero-cross detection. When zero cross detection is not implemented, the load is immediately connected to the source when an enable signal is received. The load could be turned ON at any voltage level. The worst case scenario is when the source is at the maximum voltage condition and the load is connected. Inrush currents generated can damage sensitive circuits and EMI switching noises can propagate throughout the system. If a mechanical relay is used, switching at peak voltage can cause arcing or welding which could damage the relay as well as the system down stream. These challenges are eliminated using zero-cross switching SSR. This reference design uses the AMC23C10 isolated comparator to detect zero voltage crossing and sends a signal to the low voltage side. The signal changes from high to low at OUT2 output of the comparator. Then the falling edge is detected by SN74HCS72 flip-flop and the signal is latched so that TPSI3050-Q1 remains ON. In addition, the zero-cross switching logic uses a switch and a multiplexer to provide the user the ability to disconnect the load at any time.

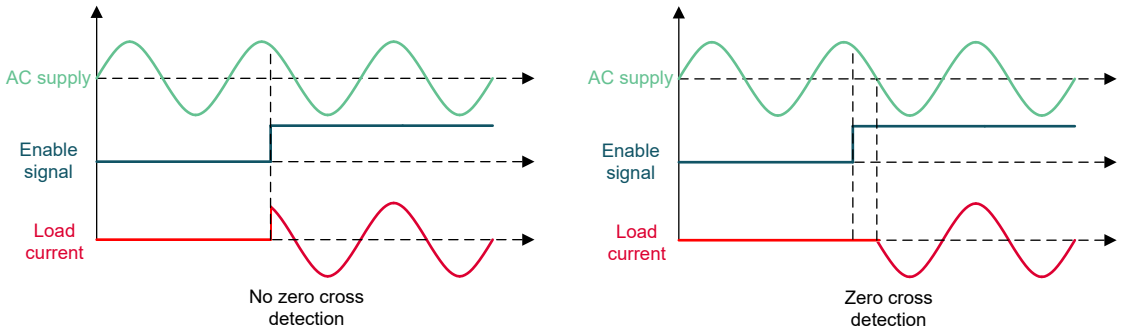

Figure 1-1. Zero-Cross Switching

1.1 System Design Theory

The following section provides a complete summary of the reference design and the results. This reference design uses four main components (TPSI3050-Q1, AMC23C10, SN74HCS72, TMUX1219) in order to achieve zero-cross switching. Figure 1-2 shows the overall system behavior for the reference design.

- AC supply is the ac source for the load.
- OUT2 is the output of the isolated comparator (AMC23C10).
- SEL is the output select signal for the multiplexer (TMUX1219).
- EN is the enable signal for the isolated switch driver (TPSI3050-Q1).
- ILOAD is the load current through the load.

When the AC supply is connected to the back to back MOSFETs, the antiparallel diodes D1 create a forward bias voltage drop that is used by the AMC23C10 to toggle OUT2. OUT2 toggles at every zero-cross of the AC supply. OUT2 signal is provided as a clock signal to the flip-flop SN74HCS72. SN74HCS72 is a D-type negative-edge-triggered flip-flop and will only change the output Q during the falling edge of the clock signal, in this case OUT2. SEL signals control the output of the multiplexer. While SEL is low, EN remains low maintaining the load disconnected. When SEL changes to high, the flip-flop awaits for the next falling edge and changes the output Q to high. The output of the multiplexer (EN) is toggled high and the load connected. When SEL signal is toggled low, the load is disconnected immediately.

This reference design was tested with a 110 V_{RMS}, 60 Hz AC supply and a resistive load of 2 kΩ. The design switches ON at 12 V with a propagation delay (t2) of approximately 200 us from the zero voltage cross to when

the load is connected. When SEL is toggled high, the load is not connected immediately and the system awaits for a zero-cross that produces a falling edge of OUT2. The await time from SEL to a load connection can be described by (t1+t2). The maximum await time is the case of a full cycle of the 60-Hz supply or t1 = 16.67 ms plus the propagation delay t2 = 200 us. This reference design features an immediate load disconnect. When SEL is toggled low, the load is immediately disconnected. Visit Section 3.3 for more information.

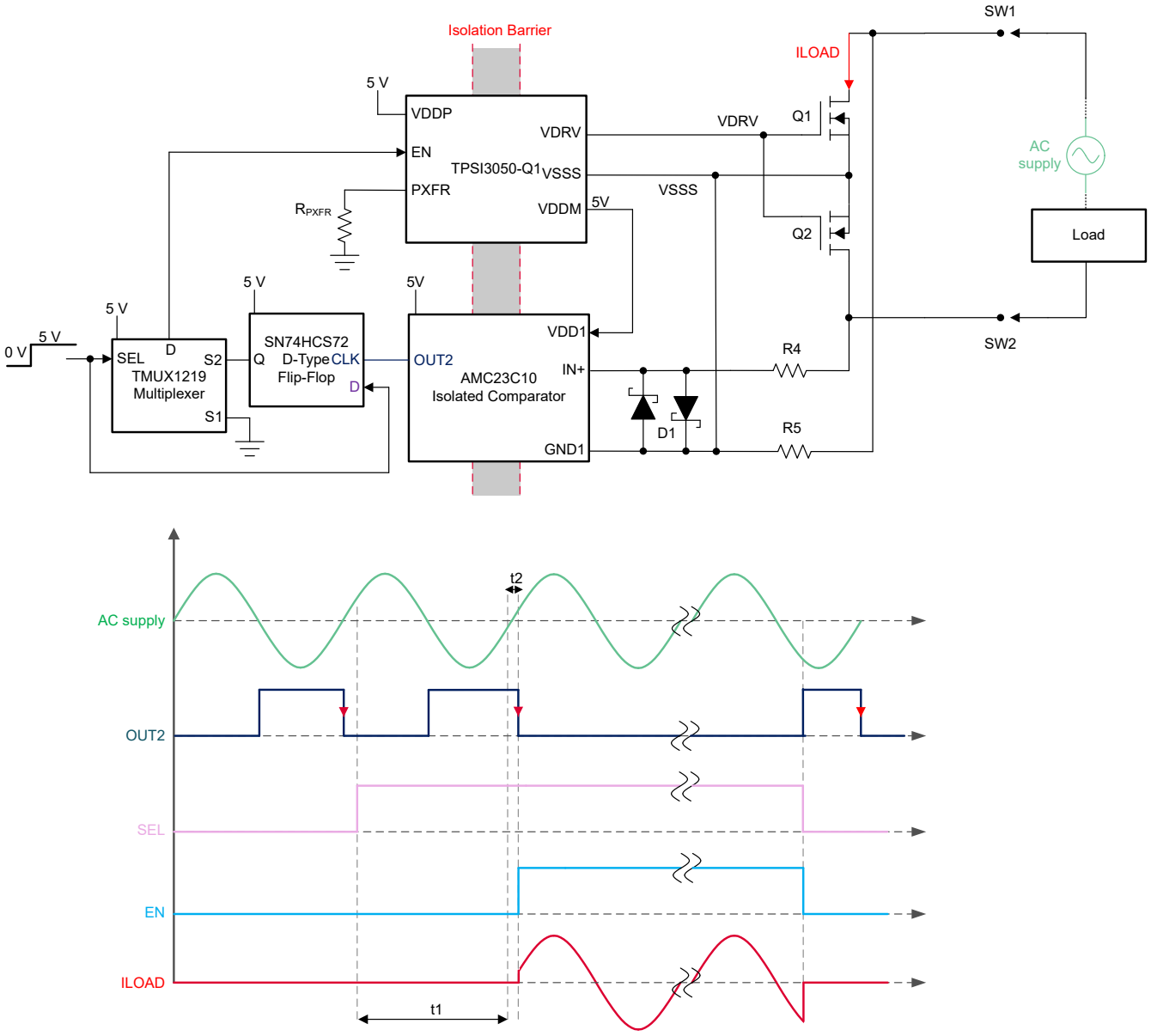

Figure 1-2. Zero-Cross Switching Operation

2 System Overview

2.1 Block Diagram

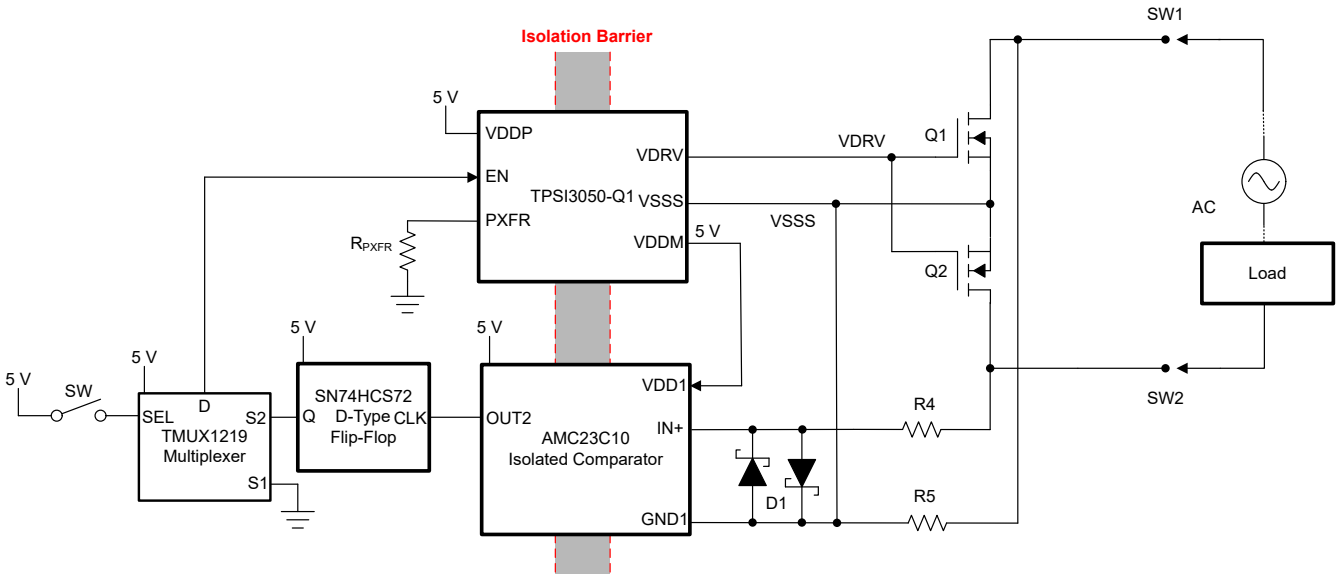

Figure 2-1. Block Diagram

2.2 Highlighted Products

The reference design features the TPSI3050-Q1, AMC23C10, SN74HCS72-Q1, and TMUX1219.

2.3 Design Considerations

2.3.1 TPSI3050-Q1

The TPSI3050-Q1 is a fully integrated, isolated switch driver, which when combined with an external power switch, forms a complete isolated solid-state relay (SSR) solution. With a nominal gate drive voltage of 10 V and 1.5/3.0 A peak source and sink current, a large variety of external power switches can be chosen to meet a wide range of applications. The TPSI3050-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required. Additionally, the TPSI3050-Q1 can supply power to external supporting circuitry for various application needs. In three-wire mode, the primary supply of 3 V to 5.5 V is supplied externally, and the switch is controlled through a separate enable.

TPSI3050-Q1 features:

- Adjustable power transfer
- Integrated 10-V gate supply
- Up to 50-mW supply to power auxiliary circuitry (I_{AUX})

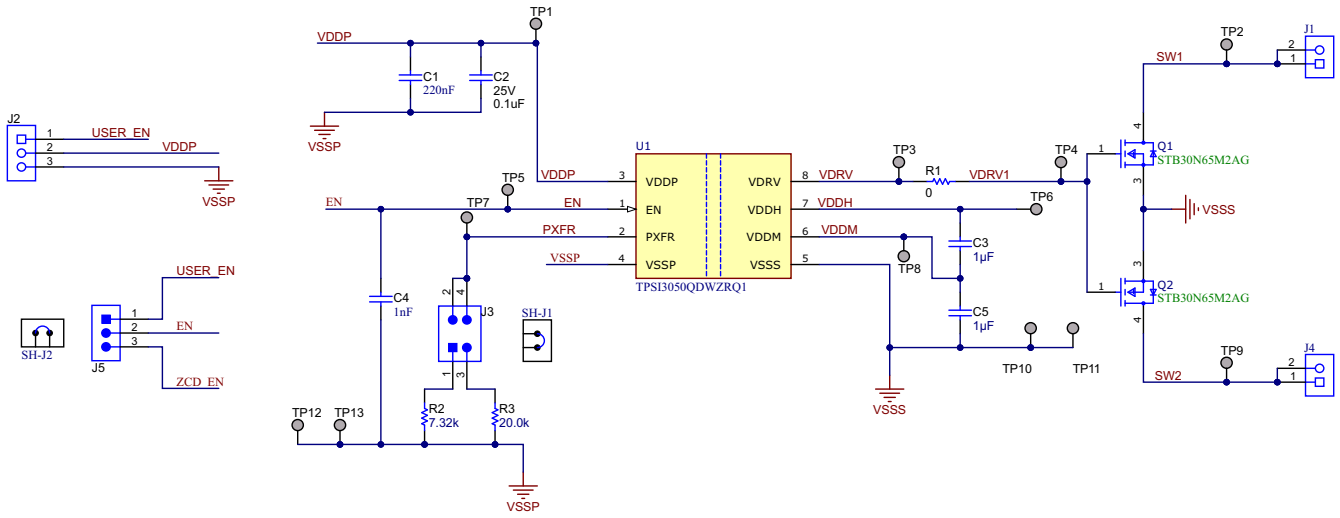

Figure 2-2. Solid-State Relay Circuit

For the primary side, TPSI3050-Q1 is set to three-wire mode configuration in order to achieve the highest power transfer available. Using a 20 kΩ resistor with a 1 % tolerance in PXFR pin provides the highest power transfer available and supports up to 50 mW of I_{AUX}. It is recommended to add a 1 uF in parallel with a 0.1 uF ceramic capacitor with low ESR to VDDP.

For the secondary side, C_{DIV1} (C3) and C_{DIV2} (C4) capacitors need to be properly selected to drive the back to back MOSFETs. If C_{DIV1} and C_{DIV2} are too small, then the voltage drop in VDDH will trigger an undervoltage lockout (UVLO) and disable the driver. The following two equations can be used for calculating the proper capacitance values.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V} \quad , \quad n \geq 1.0 \tag{1}$$

$$C_{DIV2} = n \times C_{DIV1} \quad , \quad n \geq 1.0 \tag{2}$$

- n is a real number greater than or equal to 1.0.
- C_{DIV1} is the external capacitance from VDDH to VDDM.
- C_{DIV2} is the external capacitance from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

The MOSFETs selected for this design each have a gate charge (Q_G) of 31 nC. Since the design uses back to back MOSFETs, then the total Q_G is 62 nC. If C_{DIV1} = C_{DIV2}= C_{DIV}, then C_{DIV} must be selected with capacitance higher than 124 nF to ensure that VDDH voltage drop is less than 1 V. Use this excel calculator to calculate for capacitors and power transfer selection. For this design a 1 uF capacitor was selected to have a VDDH voltage drop of 0.124 V.

2.3.2 AMC23C10

The AMC23C10 is a precision, isolated comparator with short response time that is specifically designed for zero-crossing detection of high-voltage signals that must be galvanically isolated from low-voltage circuitry. The open-drain and push-pull outputs are separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 5 kV_{RMS} according to UL1577, and supports a working voltage of up to 1 kV_{PK}. The device offers an open-drain and a push-pull output with a propagation delay of less than 300 ns. The integrated LDO supports an operating voltage range of 3 V to 27 V on the high-voltage side, allowing the comparator to be powered from a gate-driver supply. The operating voltage range on the low-side is 2.7 V to 5.5 V.

AMC23C10 features:

- Wide high-side supply range: 3 V to 27 V
- Low-side supply range: 2.7 V to 5.5 V

- Trip threshold error: ±6 mV (max)
- Propagation delay: 290 ns (typ)
- High CMTI: 100 kV/µs (min)
- Open-drain and push-pull output

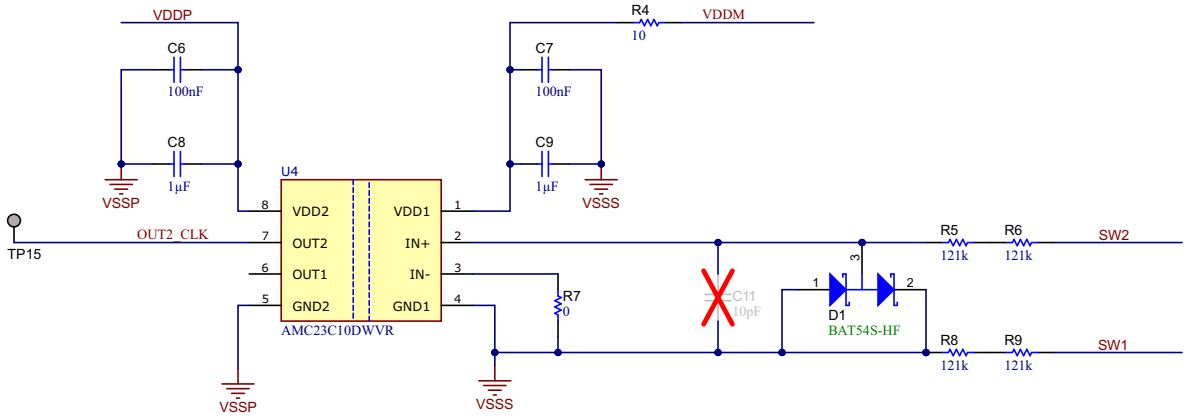

Figure 2-3. Zero-Cross Detection Circuit

For VDD1 and VDD2, it is recommended to add a 1 uF in parallel with a 0.1 uF ceramic capacitors with low ESR. AMC23C10 is powered on the HV side by TPSI3050-Q1 from the VDDM pin with a 5 V rail. This feature of TPSI3050-Q1 reduces system complexity, cost, and board space.

Figure 2-3 shows IN- input is grounded to effectively compare the voltage swing across the antiparallel diodes D1. Input IN+ is connected to the AC source through R4, R5, R7, and R8. When selecting these resistors it is important to pay attention to the voltage rating, power dissipation and switching delay. The resistors must be able to sustain the high voltage AC source. It is recommended to use resistors in series to meet the voltage specifications. This reference design uses two resistors sized (2010) with a rating of 400V DC. It is important to note the trade-off between the power dissipation across the resistors and the zero voltage detection accuracy. The parasitic capacitance of the power switches and the resistors creates a RC delay for the zero voltage detection. This delay affects the voltage at which zero cross switching happens. Decreasing the resistor value reduces the delay and the load is connected to the source closer to zero volts.

For this design, a resistance of 242 kΩ is used to bias the diodes and achieve zero-cross detection. The AC source is a 110 VAC signal with a 60 Hz frequency. The design connects the load with 180.8 µs delay at 10.4 V. This delay is dominated by the RC constant of (R4+R5) and the output capacitance of the power FETs and not the isolated comparator, the logic circuit on the low side, or the enable delay of the TPSI3050-Q1. Figure 3-3 shows the details of the switching operation. The following equations show the calculation for peak and average power dissipation for the selected resistors. The value R is the addition of the series resistances R = (R4+R5) = (R7+R8).

$$I_{PK} = \frac{V_{PK}}{R} = \frac{110\ V_{RMS} \times \sqrt{2}}{242\ k\Omega} = 0.64\ mA \quad (3)$$

$$P_{PK} = \frac{(V_{RMS} \times \sqrt{2})^2}{R} = \frac{(110\ V_{RMS} \times \sqrt{2})^2}{242\ k\Omega} = 100\ mW \quad (4)$$

$$P_{AVG} = \frac{V_{RMS}^2}{R} = 50\ mW \quad (5)$$

When selecting the series diodes, the voltage drop must higher than the nominal switching threshold voltage for the AMC23C10. AMC23C10 requires a voltage greater than its nominal switching threshold of +/-12.5 mV to detect a valid input. The diode selected for this reference design is a BAT54S-HF. This diode is able to provide the necessary voltage drop at very low current levels. Figure 2-4 shows the forward voltage drop characteristic of BAT54S-HF. Capacitor C11 helps to filter high frequency noises from the AC source, however, C11 can also increase the propagation delay to detect the zero voltage cross. For this design, C11 was not populated in order to maintain lower propagation delay.

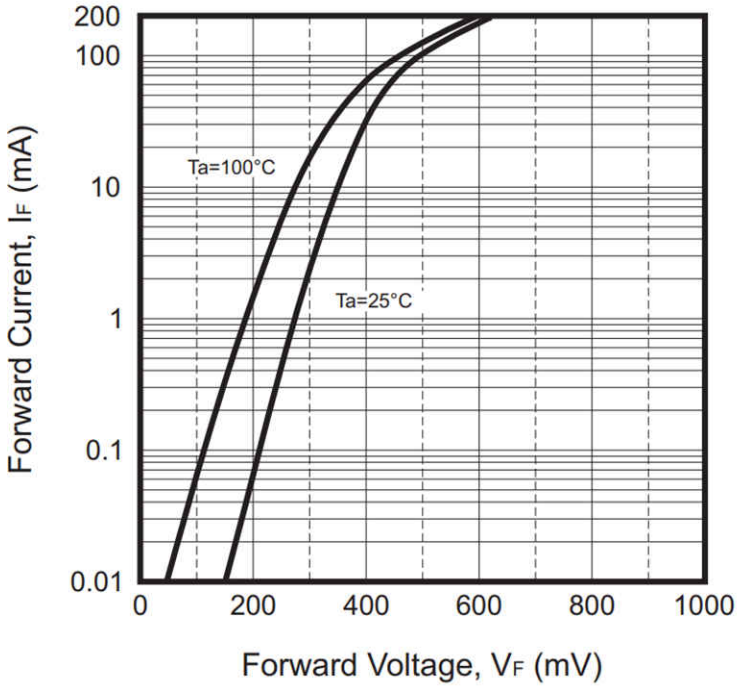

Figure 2-4. Diode Voltage Drop

2.3.3 SN74HCS72 and TMUX1219

The SN74HCS72 is a dual D-type flip-flop (DFF) with negative-edge-triggered clock inputs. This device is part of the HCS logic family, which includes Schmitt-trigger architecture on all input pins improving noise margins and dynamic power consumption. Additionally, the HCS family provides some of the lowest static power consumption and input leakage current on the market.

SN74HCS72 features:

- Wide operating voltage range: 2 V to 6 V
- Extended ambient temperature range: –40°C to +125°C, TA
- Schmitt-trigger input architecture supports slow input transitions and improves noise margins
- Low power consumption with typical static ICC of 100 nA
- 8 ns typical delay with 5-V supply

The SN74HCS72 DFF provides the negative edge detection with a very short delay to control the switch immediately when the zero crossing is detected by the AMC23C10 comparator. The push-pull output provides excellent drive strength to control the TPSI3050-Q1 enable signal.

The flip-flop detects the falling edge of OUT2 from AMC23C10 effectively detecting the zero voltage cross. Since the design detects only the falling edge of OUT2, then the circuit has a max delay of a full cycle of the 60 Hz source or 17 ms max. Switch S1 is used in combination with TMUX1219 to enable or disable the zero cross switching circuit. Table 2-1 shows the logic of the circuit based on the states of S1, EN, OUT2, and 1Q.

This circuit detects zero cross voltage while the back to back FETs are disabled. Once the FETs are enabled, the anti-parallel diodes would not be biased to detect a zero cross voltage. If S1 is asserted low, the zero cross detection circuit is disabled. The Flip-Flop will only change state when OUT2 is changing from high to low.

If TPSI3050-Q1 is disabled, S1 is high, and OUT2 changes from low to high, only then TPSI3050-Q1 asserts VDRV high. Once VDRV is asserted high, then the FETs are turned ON.

Table 2-1. Output Logic Table

SEL	OUT2_CLK	1Q	ZCD_EN	TPSI3050-Q1 State
L	L	L	L	**Disabled**
H	H->L	H	1Q	**Enabled**
H	L	H	1Q	**Enabled**
L	L->H	L	L	**Disabled**

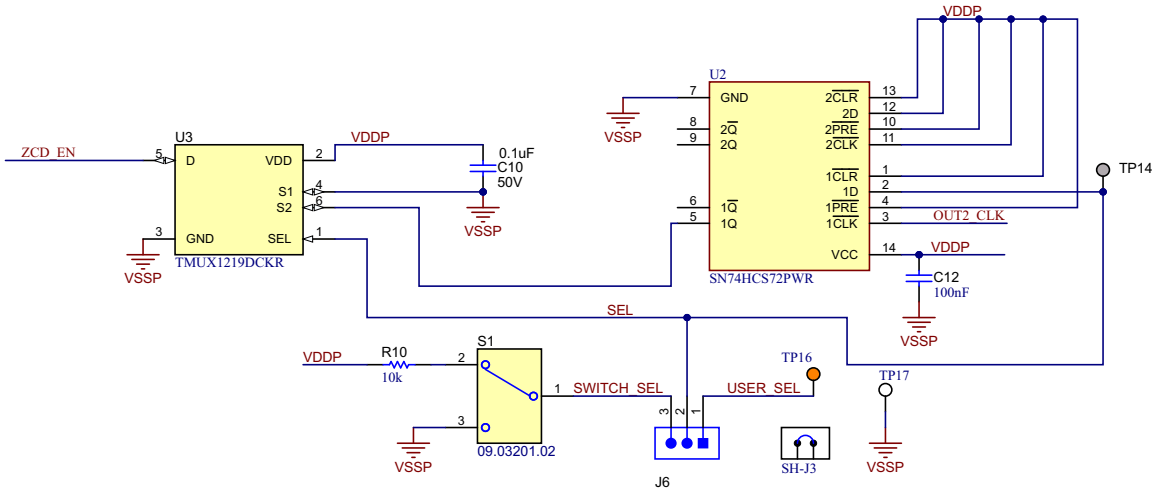

Figure 2-5. Flip-Flop and Multiplexer Circuit

3 Hardware, Software, Testing Requirements, and Test Results

This reference design was tested using the following equipment:

1. 5-V DC power source
2. Oscilloscope
3. Isolated probes
4. AC power source
5. Load resistor

3.1 Hardware Requirements

3.2 Test Setup

To test the zero-cross detection reference design it is recommended to connect an oscilloscope to EN, SEL, a differential probe to the AC source, and a current probe to the load. Connect a 5-V power source and ensure that the TPSI3050-Q1 has powered up by measuring VDDH (10-V) and VDDM (5-V). Finally, connect the AC source and load to test the design. The circuit should look as Figure 3-1.

Table 3-1. Test Points and Connectors

Name		Description
J1, TP2	SW1	AC source connection
J2	USER_EN	External signal to control TPSI3050-Q1 EN signal
	VDDP	Power supply for primary side
	VSSP	Ground supply for primary side
J3		Power transfer selection
J4, TP9	SW2	Load connection
J5	USER_EN	External signal to control TPSI3050-Q1 EN signal without zero-cross detection
	EN	TPSI3050-Q1 Active high driver enable
	ZCD_EN	Zero-cross switching enable signal to control TPSI3050-Q1
J6	SWITCH_SEL	Signal to control the output of the multiplexer using switch (S1)
	SEL	Signal to control the output of the multiplexer
	USER_SEL	External signal to control the output of the multiplexer
TP1	VDDP	TPSI3050-Q1 Power supply for primary side
TP3	VDRV	TPSI3050-Q1 Active high driver output
TP4	VG	Gate voltage of the power switches
TP5	EN	TPSI3050-Q1 Active high driver enable
TP6	VDDH	TPSI3050-Q1 Generated high supply
TP7	PXFR	TPSI3050-Q1 Increase or decrease power transfer
TP8	VDDM	TPSI3050-Q1 Generated mid supply
TP10, TP11	VSSS	Ground supply for secondary side
TP12, TP13, TP17	VSSP	Ground supply for primary side
TP14	SEL	Multiplexer output select signal
TP15	OUT2_CLK	Output of the isolated comparator
TP16	USER_SEL	External signal to connect to SEL

Steps to Test the Reference Design

1. J3 connector should be connecting R3 (20 kΩ). This allows for the highest power transfer.
2. J5 connector should be connecting ZCD_EN to EN. This allows the TPSI3050-Q1 to be controlled by the zero-cross detection logic.
3. J6 connects SWITCH_SEL or USER_SEL to the SEL signal of the multiplexer. For this test, an external signal (USER_SEL) is provided to control the multiplexer output.
4. Connect 5-V supply to VDDP.
5. Check that VDDM and VDDH rails are 5-V and 10-V respectively.
6. Connect AC source with a load.

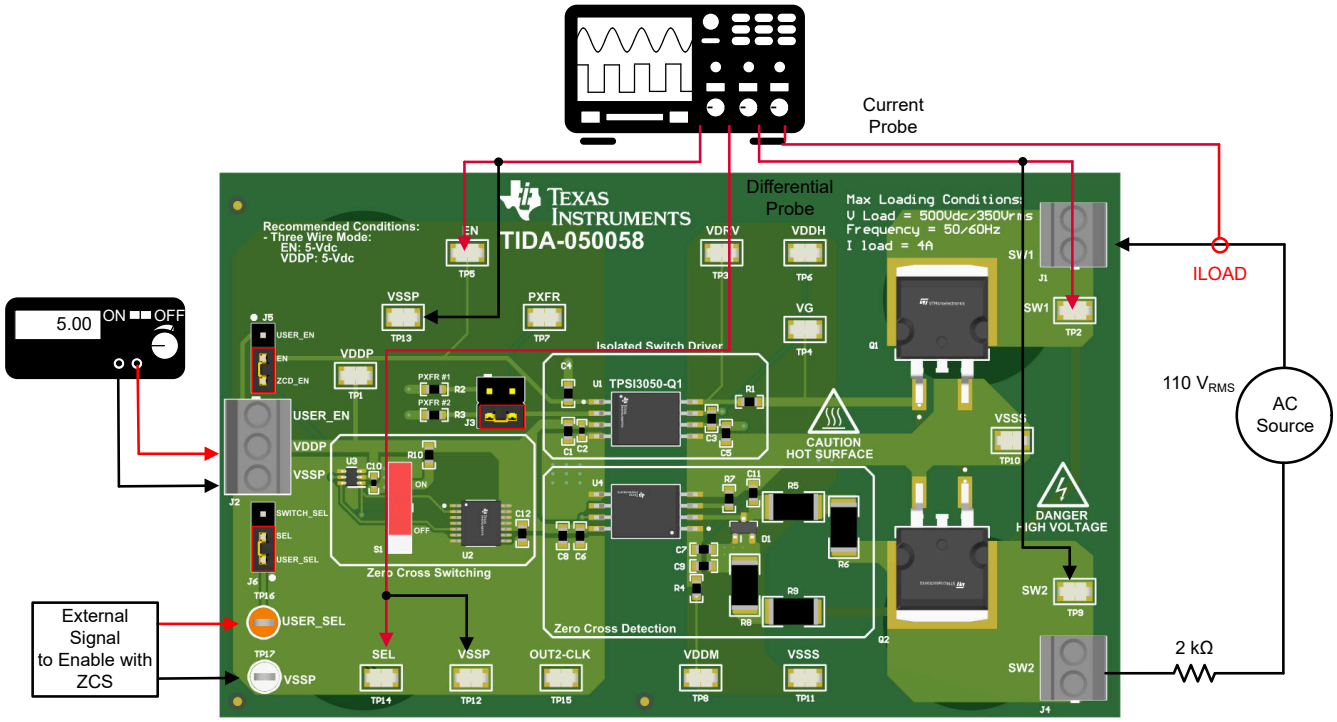

Figure 3-1. Test Setup

3.3 Test Results

Figure 3-2 shows how the EN signal changes state when the voltage of the AC load reaches the zero voltage point. The SEL signal represents an input signal which signifies that the user is trying to connect the load. The signal does not connect the load immediately because the circuit awaits for the moment when the AC voltage reaches zero. SW1-SW2 is the voltage drop across the back to back MOSFETs and ILOAD is the current on the load. For this design, EN signal is detected at the falling edge of OUT2_CLK using the flip-flop. Once EN is high, TPSI3050-Q1 connects the load. The load remains connected until the user sends a low signal for SEL. This reference design features a immediate load disconnect that allows the user to disconnect the load at any point.

- SW2-SW1 is the voltage drop across the back to back MOSFETs.
- EN is the enable input to TPSI3050-Q1.
- SEL is the input provided by the user when desired to connect the load.
- ILOAD is the current through the load.

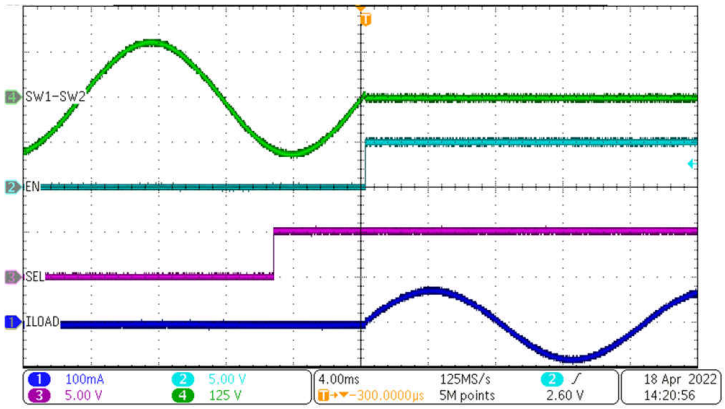

Figure 3-2. Zero-Cross Voltage Switching

Figure 3-3 shows a zoomed in capture of Figure 3-2 to measure the propagation delay and the voltage at which the circuit switches ON. Note that switching ON does not happen right at the zero voltage level and instead it happens at 12 V. This voltage offset is because the input voltage to the isolated comparator has a RC delay constant. This delay is formed by (R4+R5) resistors and the parasitic source-drain capacitance of the power FETs. The voltage level at which the load is connected depends on the value of the bias resistors R4, R5, R7, R8 and the parasitic capacitance of the FETs. The lower the bias resistors values the lower the voltage at which the load is connected. However, there is a important trade off between switching voltage accuracy and the power dissipation across the biasing resistors as previously discussed in section 2.3.

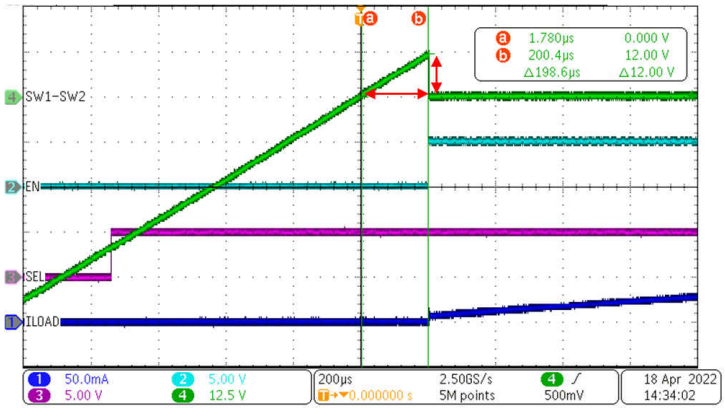

Figure 3-3. Zero-Cross Voltage Switching Zoomed

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050058.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050058.

4.1.3 Altium Project

To download the Altium Designer™ project files, see the design files at TIDA-050058.

4.1.4 Assembly Drawings

To download the assembly drawings files, see the design files at TIDA-050058.

4.1.4.1 Gerber Files

To download the Gerber files, see the design files at TIDA-050058.

4.2 Documentation Support

1. Texas Instruments, TPSI3050-Q1 EVM Automotive Reinforced Isolated Switch Driver with Integrated 10-V Gate Supply EVM User's Guide user's guide.
2. Texas Instruments, Cascoding Two TPSI3050 Isolated Switch Drivers to Increase Gate Drive Voltage application note.
3. Texas Instruments, AMC23CxxEVM Isolated Comparator Evaluation Module User's Guide user's guide.
4. Texas Instruments, 14-24-Logic-EVM User's Guide user's guide.
5. Texas Instruments, TMUX1219 Evaluation Module User's Guide user's guide.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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