TI Designs

Automotive 10-V to 80-V Ultra-Wide-V_{IN}, 12-V V_{OUT} Flyback Reference Design For 48-V Car Battery

Design Overview

This TIDA-01344 design is a 24-W, automotive 48-V battery, front-end power supply which generates a 12-V output voltage and 2-A output current from a wide input range of 10- to 80-V DC, up to 100-V transient. The system consists of electromagnetic interference (EMI) filters for CISPR-25 compliance and a protection circuit for clamping high-voltage conducted transients. The flyback controller implements primary-side regulation without an optocoupler. The flyback transformer is designed and qualified as Automotive AEC-Q200 Grade 1.

Design Resources

TIDA-01344	Design Folder
LM5022-Q1	Product Folder

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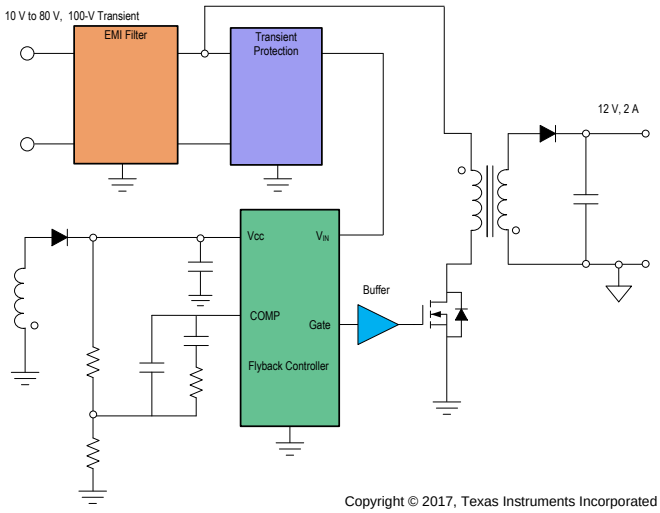
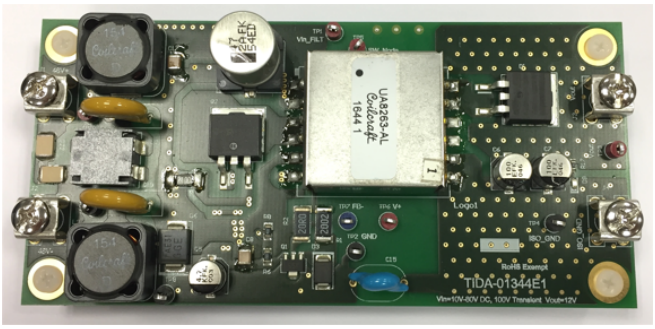
Design Features

- Wide-V_{IN} Flyback Converter Over Input Voltage of 10- to 80-V DC, 100-V Transient; 12-V Output Voltage and Current up to 2 A
- Protection for Clamping High-Voltage Conducted Transients to Safe Levels for Downstream Circuitry
- Automotive AEC-Q200 Grade-1 Qualified Transformer Design
- Primary-Side Regulation Without Optocoupler for Extended Lifetime and Compact Board Design
- Tested for CISPR25 Conducted EMI (Class 5)

Applications

- HEV/EV Traction Inverter
- Dry Double Clutch Transmission
- Electronic Control Units
- Car Battery Front-End Power





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1 System Overview

1.1 System Description

This TIDA-01344 TI Design is an ultra-wide input, 20-W front-end power supply for a 48-V car battery in the hybrid electric vehicle (HEV) or electric vehicle (EV) traction inverter system. The design implements flyback which is able to handle a wide input voltage range of 10- to 80-V DC and 100-V transient to comply with the LV148 standard. The flyback transformer is designed as Automotive AEC-Q200 Grade-1 Qualified and provides reinforced isolation up to 3.5 kV from the 48-V battery side to the 12-V battery side. The flyback converter regulates the output voltage through the transformer primary side, which eliminates the use of an optocoupler and leads to higher reliability and a smaller form-factor board design. The controller has the internal compensator to provide better load regulation and transient response.

Figure 1 shows a block diagram example of the 48-V battery inverter driven motor system. The TIDA-01344 serves as a redundant supply to the 12-V battery voltage rail. As the diagram shows, the isolated DC-DC (connected to the 48-V battery side of TIDA-01134) and the non-isolated DC-DC (connected to the 12-V battery side of TIDA-01179 [1]) are in an O-ring configuration and provide the power to the downstream loads. The TIDA-01179 includes a buck-boost converter and a buck converter, which create the front-end power for the 12-V car battery.

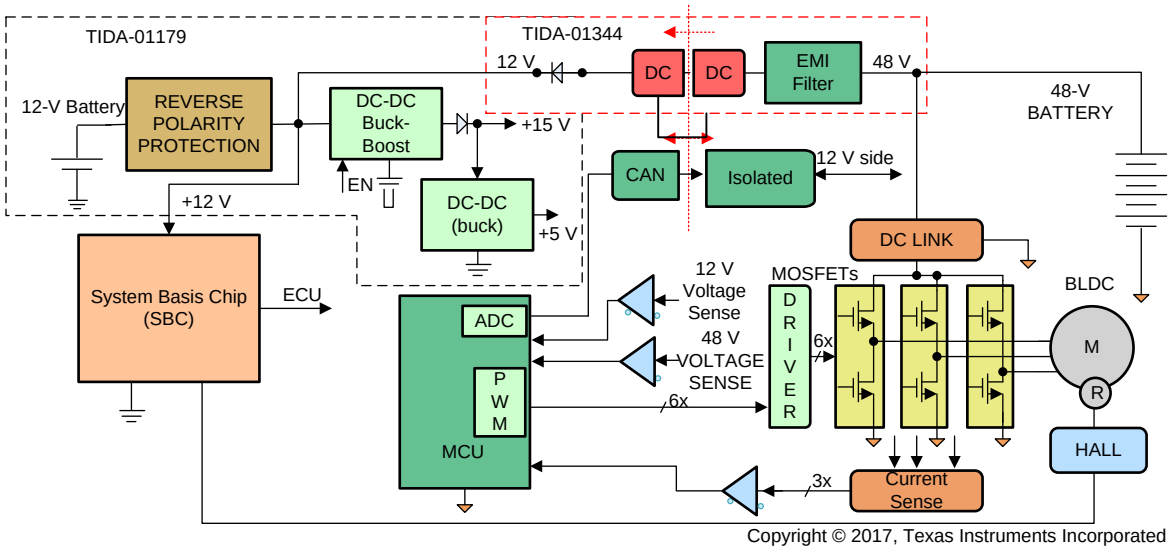


Figure 1. System Block Diagram for 48-V Battery-Driven Inverter and Implementation of TIDA-01344

1.2 Key System Specifications

Table 1 shows the key system specifications of TIDA-01344.

Table 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
System Input						
V_{IN}	Input voltage	Battery voltage range (DC)	10	48	80	V
V_{IN}	Input voltage	Transient	8	—	100	V
V_{CLAMP+}	Positive clamping voltage	Positive input protection TVS clamping range	60	—	100	V
P_{PK}	Peak pulse power dissipation	Maximum TVS power dissipation	—	600	—	W
F_{SW}	Switching frequency	—	—	350	—	kHz
V_{OUT}	Output voltage	System output voltage, across load	10.6	12	13.4	V
I_{OUT}	Output current	Max output current. Drawing more than 2 A is not recommended for thermal reasons. See the thermal images testing in Section 4.7 to view the temperature rise at different load levels.	—	1.7	2	A

1.3 Block Diagram

Figure 2 shows the system block diagram. The design consists of three main functional blocks:

1. Electromagnetic interference (EMI) filter – Contains differential mode (DM) filter and common-mode (CM) filter, respectively.
2. Electrical transient protection circuit – Clamps high-voltage electrical transients (up to 100 V) to safe levels for downstream circuitry. Automotive electronics operate from the car battery, which experiences transient loads such as cold cranks and load dumps that can range from 10 V to 100 V.
3. Flyback converter – Provides the isolation and can withstand a wide input voltage range. Other benefits include a low parts count and single magnetic for buck-boost conversion.

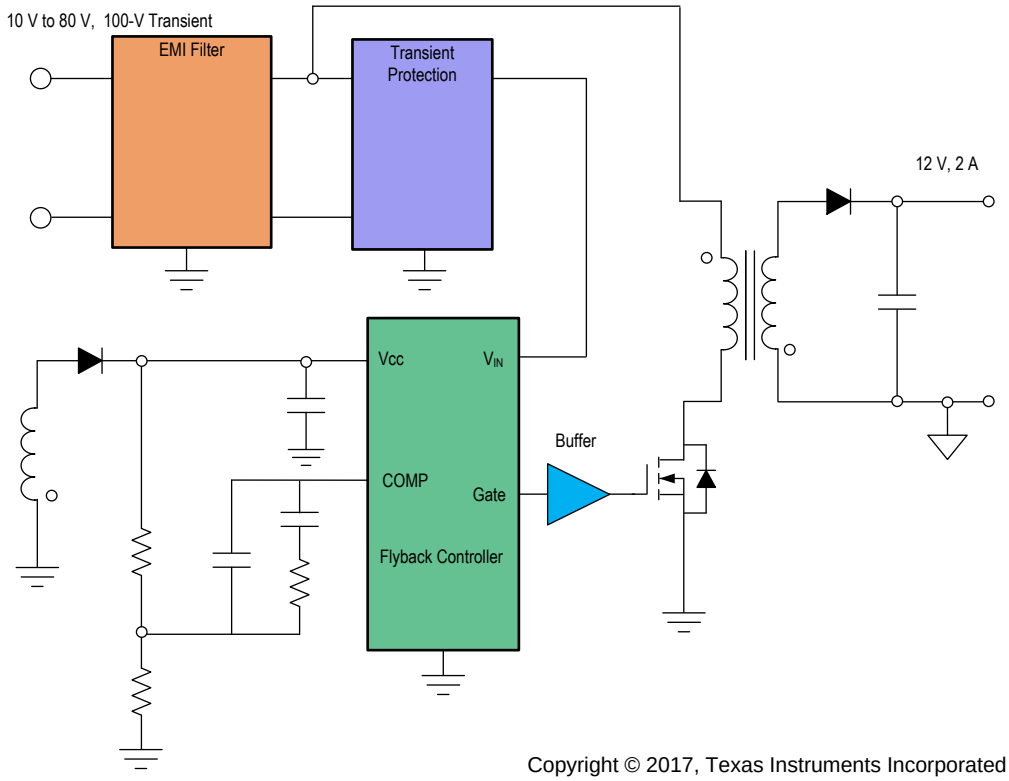


Figure 2. TIDA-01344 Block diagram

1.4 Highlighted Products

The TIDA-01344 reference design features the following devices from Texas Instruments.

1.4.1 LM5022-Q1

The LM5022-Q1 is a high-voltage, low-side, N-channel MOSFET controller with a wide input voltage range from 6 V to 60 V. The controller contains all of the features required to implement single-ended, primary-side-regulation power supply topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent input voltage feed-forward.

2 System Design Theory

2.1 Electrical Transient Protection

The electrical transient protection circuit is implemented on the supply input of the system to protect against positive electrical transients as per the LV148 standard and attempts to shut the transients while maintaining the downstream circuit operation.

Figure 3 shows a schematic of the input transient protection circuit. The circuit consists of the Zener diode D3, the high-voltage blocking transistor bipolar junction transistor (BJT) Q1, and transient voltage suppressor (TVS) diode D6. R1 and R2 limit the current flowing into the base and collector of Q1, respectively.

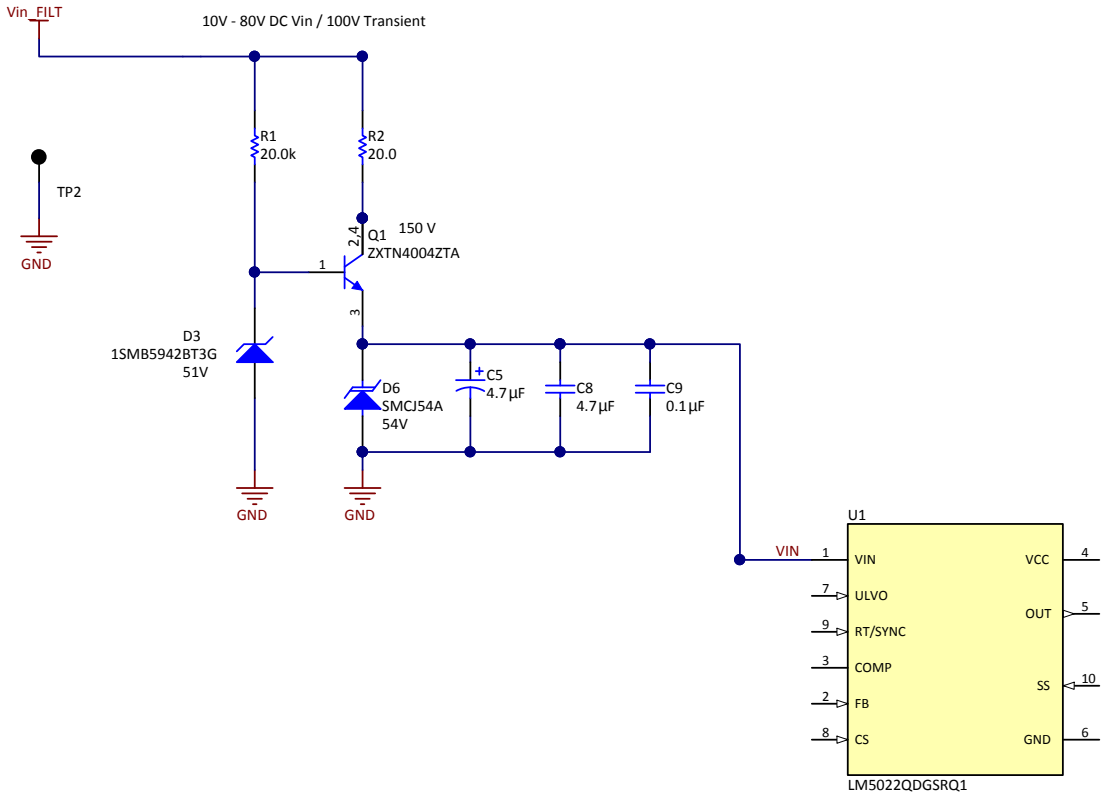


Figure 3. Schematic of Input Transient Protection and Reverse Polarity Protection

The Zener diode D3 clamps the base voltage of Q1 to the integrated circuit (IC) chip-safe level. The emitter of Q1 is connected to protection pins. The TVS diode D6 is applied in parallel to shunt the fast overvoltage transient spikes that appear on the input line. Equation 1 calculates the power rating of D6. The worst-case assumption is that the load is drawing zero current and all the current flows through the TVS diode.

$$P_{TVS} = \frac{(V_{Pulse} - V_{Clamp})}{R2} \times V_{Clamp} = \frac{(100 - 60)}{20} \times 60 = 120\ W \quad (1)$$

A TVS diode with a 600-W peak-pulse power dissipation on the system management bus (SMB) side has been selected for this design.

2.2 Flyback Converter

This section provides the procedure for calculating the surrounding components of the flyback converter. Table 2 shows the design specifications and Figure 4 shows a schematic of the converter.

Table 2. Flyback Converter Specifications

PARAMETER	SPECIFICATION
Input voltage (V_{IN})	10-V DC to 80-V DC (100-V transient)
Output voltage (V_{OUT})	12 V
Output ripple	± 3%
Maximum output current (I_{OUT_MAX})	2 A
Switching frequency	350 kHz
Maximum output power (P_{OUT_MAX})	24W

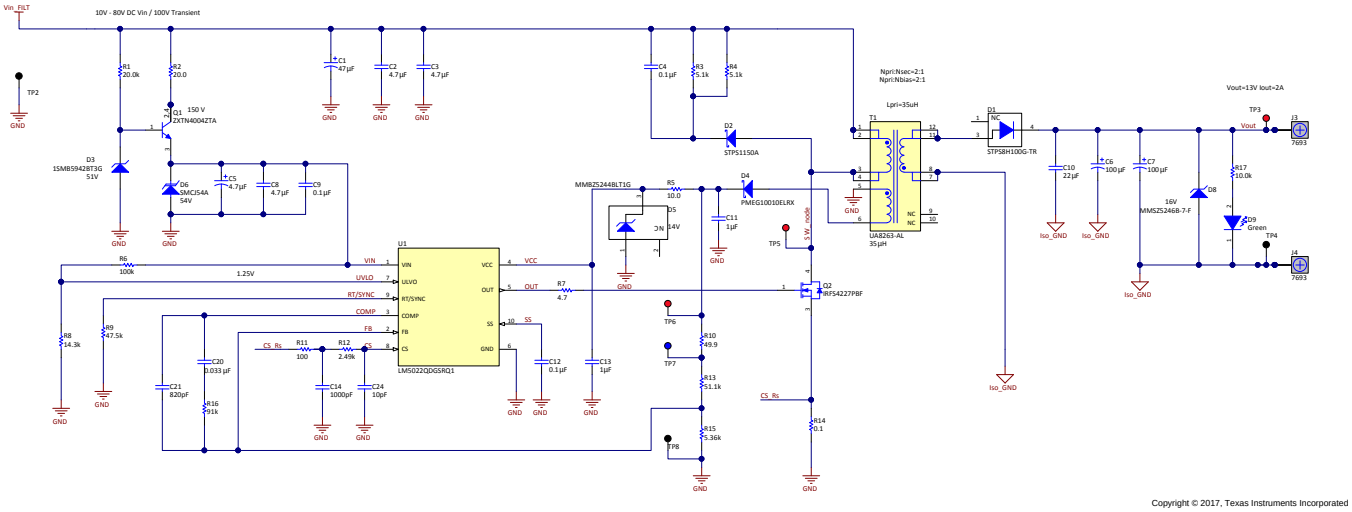


Figure 4. Flyback DC-DC Converter Schematic

2.2.1 Switching Frequency

The switching frequency of the LM5022-Q1 device is set by the oscillation resistor, which is connected to the RT/SYNC pin (R9 in Figure 4). A switching frequency of 350 kHz is selected as a compromise between component size, EMI, and efficiency. 350 kHz is located in between the MW (medium wave) and SW (short wave) frequency bands, where no limit is given per the CISPR25 standard. The value of RT is calculated in Equation 2 as:

$$R_T = \frac{1 - 8 \times 10^{-8} \times F_{sw}}{F_{sw} \times 5.77 \times 10^{-11}} = 48.1\ k\Omega \quad (2)$$

where:

- F_{SW} is the switching frequency.

2.2.2 Transformer Design

The transformer is one of the most important elements to ensure that the flyback converter operates reliably and efficiently. A flyback transformer is used as an energy storage device. The energy is stored in the air-gap of the core. The flyback converter is designed for continuous-conduction mode (CCM). In comparison with the discontinuous mode, the advantages are lower peak currents, lower output voltage spikes, and lower core losses.

If ignoring the drop voltage across the switching MOSFET and output rectification diode, the winding turns ratio is calculated in Equation 3 as:

$$V_{IN\_Min} \times T_{on} = V_{OUT} \times T_{off} \times N_{PS} \quad (3)$$

where:

- V_{IN_Min} is the minimum input voltage
- T_{on} is the switch-on time of the switching MOSFET
- T_{off} is the off time of the switching MOSFET
- N_{PS} is the turn ratio between the primary turns and secondary turns of the transformer.

Considering $D = T_{on} / (T_{on} + T_{off})$ is the duty cycle and the maximum duty cycle is chosen as 70%, the turn ratio of the transformer primary winding to the secondary winding is calculated in Equation 4 as:

$$N_{PS} = \frac{V_{IN\_Min}}{V_{OUT}} \times \frac{D}{1 - D} = \frac{11 \times 0.7}{13 \times 0.3} = 1.97 \quad (4)$$

N_{PS} is selected as 2. Therefore the actual duty cycle (D_{ON_act}) is calculated in Equation 5 as:

$$D_{ON\_act} = \frac{(V_{OUT} + V_f) \times N_{PS}}{V_{IN\_Min} + (V_{OUT} + V_f) \times N_{PS}} = \frac{(13 + 0.6) \times 2}{11 + (13 + 0.6) \times 2} = 0.71 \quad (5)$$

where:

- V_f is the forward drop voltage of the output rectification diode.

The turnoff time duty cycle of the MOSFET is calculated in Equation 6 as:

$$D_{OFF\_act} = 1 - D_{ON\_act} = 0.29 \quad (6)$$

The average peak current (I_{sec_avgpk}) at the transformer secondary side is calculated in Equation 7 as:

$$I_{sec\_avgpk} = \frac{I_{sec\_avg}}{D_{OFF\_act}} = \frac{1.7}{0.29} = 5.86\ A \quad (7)$$

The peak current at the transformer secondary side (I_{sec_pk}) is calculated in Equation 8 as:

$$I_{sec\_pk} = \frac{2 \times I_{sec\_avgpk}}{2 - D_{OFF\_act}} = \frac{2 \times 5.86}{2 - 0.29} = 6.85\ A \quad (8)$$

The average current flowing into the transformer secondary side is 1.7 A; therefore, the RMS current at the transformer secondary side (I_{sec_rms}) is calculated in Equation 9 as:

$$I_{sec\_rms} = I_{sec\_avgpk} \times \sqrt{D_{OFF\_act}} = 5.86\ A \times \sqrt{0.29} = 3.16\ A \quad (9)$$

The average peak current (I_{pri_avgpk}) at the transformer primary side is calculated in Equation 10 as:

$$I_{pri\_avgpk} = \frac{I_{sec\_avgpk}}{N_{PS}} = \frac{5.86\ A}{2} = 2.93\ A \quad (10)$$

The peak current at the transformer primary side (I_{pri_pk}) is calculated in Equation 11 as:

$$I_{pri\_pk} = \frac{2 \times I_{pri\_avgpk}}{2 - D_{on\_act}} = \frac{2 \times 2.93\ A}{2 - 0.71} = 4.54\ A \quad (11)$$

The RMS current at the transformer Primary side (I_{pri_rms}) is calculated in Equation 12 as:

$$I_{pri\_rms} = I_{pri\_avgpk} \times \sqrt{D_{On\_act}} = 2.93 \times \sqrt{0.71} = 2.46\ A \quad (12)$$

The RMS current of the bias winding is selected as 50 mA according to the current limit of the internal regulator. The turn ratio of the transformer bias winding to the secondary winding is selected as 1:1 for better regulation. As a result, the output voltage of the bias winding is $V_{bias} = V_{OUT} = 12$ V.

Table 3 summarizes the specifications of the designed flyback transformer.

Table 3. Flyback Transformer Specifications

PARAMETER		SPECIFICATION
Qualification		AEC-Q200 Grade-1 qualified
Safety insulation		Reinforced
Power rating		20 W
Input voltage		10 V to 100 V
Frequency		350 kHz
Maximum duty cycle		75%
Primary side inductance		35 µH ±10% at 350 KHz
Leakage inductance		<1% of primary inductance
Output voltage		13.6 V at 1.7-A average current
Auxiliary winding output		13 V at 50 mA
Turns ratio	Primary to secondary	2:01
	Primary to auxiliary	2:01
Peak current	Primary	4.5 A
	Secondary	6.9 A
RMS current	Primary	2.5 A
	Secondary	3.2 A

TI recommends the automotive grade AEC-Q200 qualified flyback transformer UA8263-AL from CoilCraft for this reference design.

2.2.3 Input Capacitors

The input capacitor must supply the input current during the input voltage dip in the 48-V battery cold-crank conditions. At severe conditions, the input voltage can drop to 10 V. Input capacitors are essential in limiting the ripple voltage at the input pin of LM5022-Q1 while supplying most of the switch current during the MOSFET switch ON time.

The input capacitance is calculated in Equation 13 as:

$$C_{in} = \frac{I_{pri\_pk} \times D_{on}}{F_{SW} \times \Delta V_{ripple}} = \frac{4.54\ A \times 0.71}{350\ k \times 10\ V \times 3\%} = 30.6\ \mu F \quad (13)$$

One 47-µF aluminum capacitor and two 4.7-µF ceramic capacitors are chosen as the input capacitors.

Checking the current sharing between the aluminum capacitor and the ceramic capacitor to avoid any overheating issues is important. The equivalent series resistance (ESR) of an aluminum capacitor dominates its impedance and the reluctance of a ceramic capacitor dominates its impedance; therefore consult Equation 14:

$$Z_{AL} = ESR_{AL} = 320\ m\Omega$$

$$Z_{mlcc} = \frac{1}{2 \times \pi \times F_{SW} \times C_{mlcc}} = \frac{1}{2 \times 3.14 \times 350\ kHz \times 4.7\ \mu F \times 2} = 48\ m\Omega \quad (14)$$

where:

- ESR_{AL} is the equivalent series resistance of the input aluminum capacitor
- C_{mlcc} is the capacitance of the total input ceramic capacitor.

The RMS input current is 2.5 A; therefore, the currents flowing into the aluminum capacitor and the ceramic capacitor are calculated in Equation 15 as:

$$I_{rms\_AL} = I_{pri\_rms} \times \frac{Z_{mlcc}}{Z_{AL} + Z_{mlcc}} = 2.5 \times \frac{48}{320 + 48} = 326\ mA$$

$$I_{rms\_mlcc} = I_{pri\_rms} \times \frac{Z_{AL}}{Z_{AL} + Z_{mlcc}} \times \frac{1}{2} = 2.5 \times \frac{320}{320 + 48} \times \frac{1}{2} = 1.086\ A \quad (15)$$

The input capacitors must be selected such that the withstand RMS current is higher than the calculated values. EEV-FK2A470Q is selected as the aluminum capacitor. This capacitor has a 500-mA withstand current at 100 kHz according to the datasheet.

2.2.4 Output Capacitors

The output capacitance ensures that the converters have a small transient deviation to a step change of the load transient. The minimum required capacitance is calculated in Equation 16 in such a way as to maintain the output voltage drop less than 3% of the nominal voltage when the output current changes abruptly from the maximum to half (I_{step}):

$$I_{step} = \frac{I_{OUT}}{2} = \frac{1.7\ A}{2} = 0.85\ A$$

$$V_{DROP} = V_{OUT} \times 3\% = 13\ V \times 3\% = 0.39\ V \quad (16)$$

As with any forward converters, the right-half-plan zero (RHPZ) limits the bandwidth of the flyback. The frequency of the RHPZ is calculated in Equation 17 as:

$$f_{RHPZ} = \frac{R_o \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2}{L_{pri} \times 2\pi} = \frac{7.64 \times \left(\frac{10\ V}{13.6\ V}\right)^2}{35\ \mu H \times 2\pi} = 18.8\ kHz \quad (17)$$

The bandwidth of the system is estimated as 1/5 of the RHPZ in Equation 18:

$$f_{bandwidth} = \frac{1}{5} \times f_{RHPZ} = \frac{1}{5} \times 18.8\ kHz = 3.76\ kHz \quad (18)$$

As the result, the output capacitance at the bandwidth frequency is calculated in Equation 19 as:

$$C_{out\_min} = \frac{1}{2 \times \pi \times f_{bandwidth}} \times \frac{1}{\frac{\Delta V_{OUT}}{\Delta I_{loadstep}} - ESR_{OUT}}$$

$$= \frac{1}{2 \times 3.14 \times 3.76\ kHz} \times \frac{1}{\frac{390\ mV}{0.85\ A} - 0.34\ ||\ 0.34} = 147\ \mu F \quad (19)$$

The impedance of the aluminum and ceramic output capacitors are calculated in Equation 21 as:

$$Z_{AL1} = Z_{AL2} = ESR_{AL} = 340\ m\Omega \quad (20)$$

$$Z_{mlcc} = \frac{1}{2 \times \pi \times F_{SW} \times C_{mlcc}} = \frac{1}{2 \times 3.14 \times 350\ kHz \times 22\ \mu F} = 20\ m\Omega \quad (21)$$

where:

- ESR_{AL} is the equivalent series resistance of the output aluminum capacitor
- C_{mlcc} is the capacitance of the output ceramic capacitor.

The RMS current of the output is 3.16 A; therefore, the currents flowing into the aluminum capacitor and the ceramic capacitor are calculated in Equation 23 as:

$$I_{RMS\_AL} = I_{sec\_rms} \times \frac{Z_{mlcc}}{Z_{AL} + Z_{mlcc}} = 3.16 \times \frac{20\ m\Omega}{\frac{340\ \Omega}{2} + 20\ m\Omega} \times \frac{1}{2} = 166\ mA \quad (22)$$

$$I_{RMS\_mlcc} = I_{sec\_rms} \times \frac{Z_{AL}}{Z_{AL} + Z_{mlcc}} = 3.16 \times \frac{170}{170 + 20} = 2.83\ A \quad (23)$$

Therefore the output capacitors must be selected such that the withstand RMS current is higher than the calculated values. EEE-FK1E101XP is selected as the aluminum capacitor. This capacitor has 280-mA RMS withstand current at 100 kHz according to the datasheet. The selected ceramic capacitor can withstand 5-A RMS current with a temperature rise of 30°C.

2.2.5 RC Snubber Design

When the MOSFET turns off, a high-voltage spike occurs at the drain (switch node) because of the leakage inductor of the main transformer and the parasitic capacitance in the circuit. The parasitic capacitance comprises three components: the output capacitance of the MOSFET, the junction capacitance of the output diode which reflects to the primary side, and the parasitic capacitance of the transformer winding.

As a result, the implementation of an RC snubber circuit is very important to avoid a MOSFET from avalanche breakdown and damage. Figure 5 shows a schematic of the RC snubber circuit.

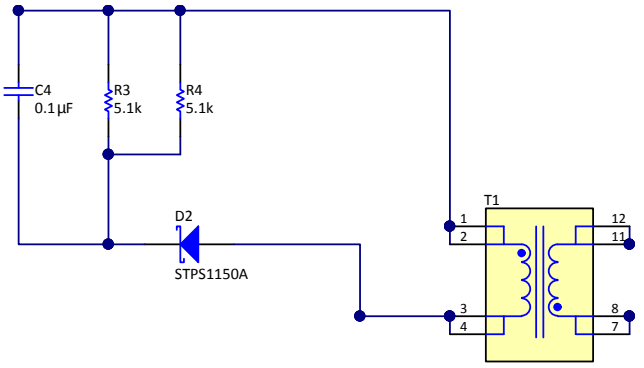


Figure 5. RC Snubber of Flyback DC-DC Converter

The damping resistance (R_{SN}) is calculated in Equation 24 as:

$$R_{SN} = \frac{V_{SN}^2}{\frac{1}{2} \times L_{lk1} \times i_{pri\_pk}^2 \times \frac{V_{SN}}{V_{SN} - n \times V_{OUT}} \times F_{SW}}$$

$$= \frac{83\ V \times 83\ V}{\frac{1}{2} \times 0.35\ \mu H \times 4.5\ A \times 4.5\ A \times \frac{83\ V}{83\ V - 2 \times 13.6\ V} \times 350\ kHz} = 3.8\ k\Omega \quad (24)$$

where:

- L_{lk1} is the leakage inductance of the primary side
- I_{pri_pk} is the peak current flowing into the transformer primary side
- V_{SN} is the voltage across the snubber capacitor, which is determined at the minimum input load and full-load condition
- F_{SW} is the switching frequency of the converter
- n is the turn ratio of the transformer primary to the secondary

- $V_{out}$is the output voltage.

Two 5.1-kΩ resistors are added in parallel for higher power dissipation. The power rating of the damping resistor is calculated in Equation 25 as:

$$P_{RSN} = \frac{V_{SN}^2}{R_{SN}} \times D = \frac{83\ V^2}{5.1\ k} \times 0.2 = 0.27\ W$$

. (25)

where:

- V_{SN} is the voltage across the snubber capacitor, which is determined at the minimum input load and full-load condition
- D is the maximum duty cycle of the voltage spike.

The damping capacitance is calculated in Equation 26 as:

$$C_{SN} = \frac{V_{SN}}{\Delta V_{SN} \times R_{SN} \times F_{SW}} = \frac{83V}{83\ V \times 10\% \times 2.55\ k \times 350\ kHz} = 11.2\ nF \quad (26)$$

The voltage rating of the damping capacitance is in Equation 27 calculated as:

$$V_{SN} = 3 \times n \times V_{OUT} = 3 \times 2 \times 13.6\ V = 81.6\ V \quad (27)$$

Therefore, a 100 nF with a 100-V rating damping capacitor has been chosen. The higher the damping capacitance is, the lower the voltage spike is, and the shorter the voltage spike duration.

The current flow through the freewheeling diode (D2) is calculated in Equation 28 as:

$$i_D = C \times \frac{dV}{dt} = 100\ nF \times \frac{0.1 \times 150\ V}{100\ ns} = 15\ A \quad (28)$$

A Schottky diode with 150-V reverse blocking voltage, 1-A average current, and 30-A repetitive current flow has been chosen in this design.

2.2.6 Selection of MOSFETs

The MOSFET selection is very important for a highly-efficient, size-optimized, and thermally-enhanced power supply design. The MOSFET drain-to-source breakdown voltage must be higher than the voltage imposed on the switch node. Losses in the MOSFET must be minimized. Calculations are done at the 48-V nominal input because this is the condition under which the MOSFET mostly works. Four components must be accounted for when selecting the MOSFET:

- ON-state conduction losses
- Gate driver losses
- Switching losses
- Output capacitance losses

The IRFS4227PBF 200-V, 62-A MOSFET has been selected for this TI Design. The conduction losses of the MOSFET (P_{on}) are calculated in Equation 29 as:

$$P_{on} = I_D^2 \times R_{DS(on)} \times D_{on} = (0.84\ A)^2 \times 125\ m\Omega \times 36.27\% = 0.032\ W \quad (29)$$

where:

- I_D is the conducting current during the turnon of the switch
- R_{dson} is the channel resistance when the switch is turned ON
- D_{on} is the duty cycle.

The gate driver losses (P_{drive}) are calculated in Equation 30 as:

$$P_{drive} = Q_g \times V_{driver} \times F_{SW} = 8.7\ nC \times 12\ V \times 350\ kHz = 0.0365\ W \quad (30)$$

where:

- Q_g is the gate charge
- V_{driver} is the gate driver voltage
- F_{SW} is the switching frequency.

The switching losses of the MOSFET (P_{SW}) are calculated in Equation 31 as:

$$P_{SW} = \frac{1}{2} \times V_{DS} \times F_{SW} \times (t_r \times I_{on} + t_{off} \times I_{off})$$

$$= \frac{1}{2} \times (48\ V + 2 \times 13.6V) \times 350\ kHz \times (15\ ns \times 0.63\ A + 20\ ns \times 2.04\ A) = 0.67\ W \quad (31)$$

where:

- V_{DS} is the drain-to-source voltage when the MOSFET is switching
- F_{SW} is the switching frequency
- t_r is the switching rise time
- I_{on} is the current buildup level during turnon
- t_{off} is the switching fall time
- I_{off} is the current level at the moment of turnoff.

The output capacitance losses (P_{coss}) are calculated in Equation 32 as:

$$P_{COSS} = \frac{1}{2} \times C_{OSS} \times {V_{DS}}^2 \times F_{SW}$$

$$= \frac{1}{2} \times 52\ pF \times (75.2\ V)^2 \times 350\ kHz = 0.051\ W \quad (32)$$

where:

- C_{oss} is the output capacitance of the MOSFET
- V_{DS} is the drain-to-source voltage when the MOSFET is switching
- F_{SW} is the switching frequency.

Therefore, the total losses in the MOSFET are calculated in Equation 33 and Equation 34 as:

$$P_{total} = P_{on} + P_{sw} + P_{coss} = 0.032\ W + 0.67\ W + 0.051\ W = 0.753\ W \quad (33)$$

$$V_{ds\_max} = n \times \frac{N_p}{N_s} \times (V_{OUT} + V_f) + V_{IN\_max}$$

$$= 1.5 \times \frac{2}{1} \times (13 + 0.6) + 100 = 140.8\ V \quad (34)$$

where:

- n is the safe margin, which is normally 1½ or 2 times the nominal value
- N_p / N_s is the turn ratio of the transformer primary winding to the secondary winding
- V_{OUT} is the output voltage
- V_f is the forward voltage of the output diode
- V_{IN_max} is the maximum input voltage.

Therefore, the selected MOSFET breaking voltage larger must be larger than 140.8 V.

2.2.7 Compensation Network

The LM5022-Q1 device implements current mode control. The output LC stage is a single-pole response. So the converter stability can be achieved using a type-II compensation design through its internal compensator. Primary side regulation is implemented as Figure 6 shows. The total loop consists of the power stage loop and the compensation loop.

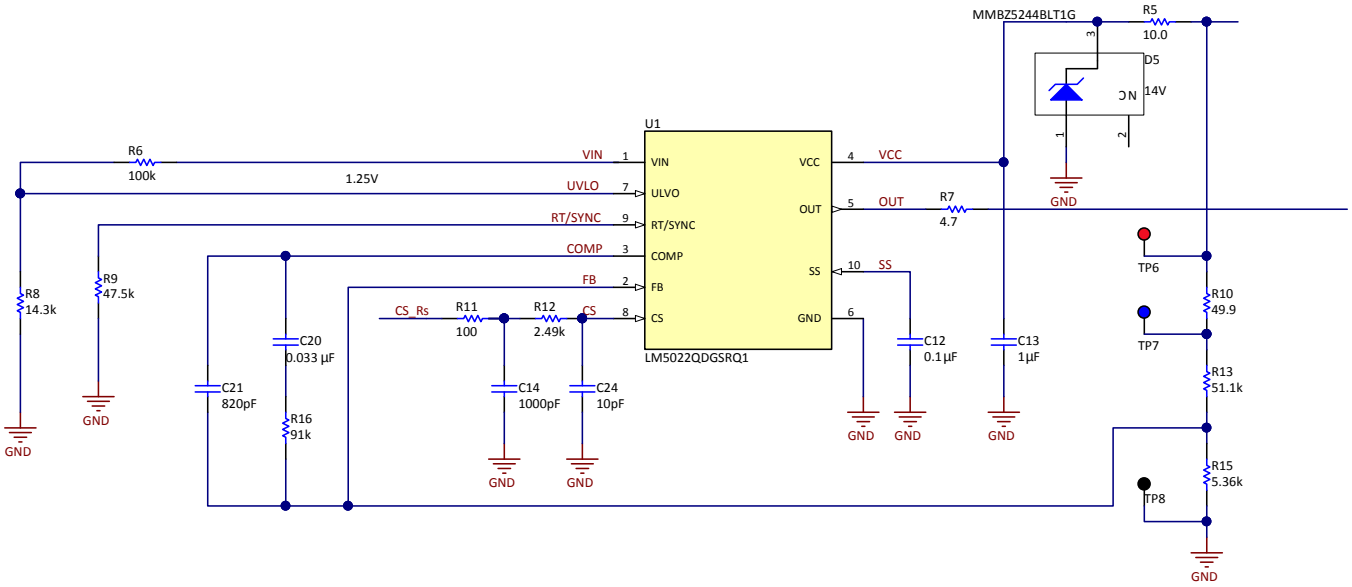


Figure 6. Compensation Network of Flyback DC-DC Converter

The calculation of the compensation components is based on the following rules:

1. Set the compensator Zero to the Pole frequency of the power stage.
2. Set the compensator Pole to the ESR frequency of the output capacitor.
3. Set the gain at around 1.8.

The equations correspond to the following:

$$\frac{1}{2\times\pi\times R_{Zero}\times C_{Zero}}=\frac{1}{2\times\pi\times R_{16}\times C_{20}}=\frac{1}{2\times C_{out}\times R_{Load}} \quad (35)$$

$$\frac{1}{2\times\pi\times R_{Zero}\times C_{Pole}}=\frac{1}{2\times\pi\times R_{16}\times C_{21}}=\frac{1}{2\times\pi\times C_{out}\times ESR_{out}} \quad (36)$$

$$G_{gain}=\frac{R_{16}}{R_{13}}=1.8 \quad (37)$$

R_{13} is selected as 51.1k and R_{Zero}, C_{Zero}, and C_{pole} are calculated and selected as 91k, 33 nF, and 820 pF, respectively.

2.3 EMI Filter

EMI compliance is very stringent in the automotive environment today to avoid interference with other subsystems. The filter design addressed in this section suppresses conducted emissions for CISPR-25 compliance. Radiated emissions mainly depend on the board layout, parasitics, and switching speed of the MOSFETs and are not the scope of this design.

The differential-mode (DM) filter suppresses the noise in the low-frequency range [2][3]. A CLC PI filter is added at the input of the flyback converter, close to the battery input. A common-mode (CM) filter is essential in filtering the noise in the high-frequency range. CM chokes in combination with Y capacitors are commonly used and placed at the input of the system for CM noise suppression. The CM choke must present high impedance over a broad, high-frequency range. Figure 7 shows a schematic of the EMI filter.

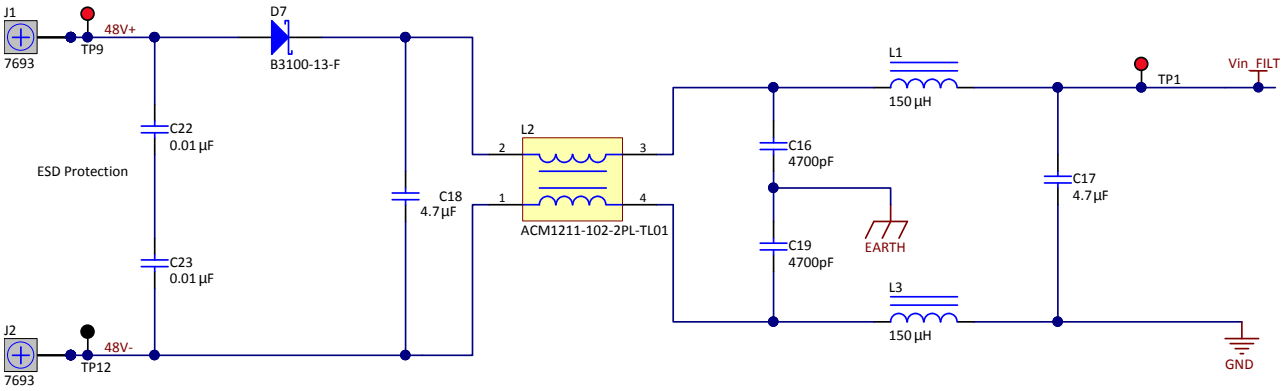


Figure 7. Schematic of EMI Filter

The CISPR25 specification does not define a limit at 350 kHz for components or modules. When between the middle frequency range from 530 kHz to 1.8 MHz, the limit is defined as a 54-dB(µV) peak for class 5 [4] (as Table 4 shows).

Table 4. Example of Quasi-Peak or Peak Limits for Conducted Disturbances

SERVICE OR BAND	FREQUENCY (MHz)	LEVELS IN dB(µV)									
		CLASS 1		CLASS 2		CLASS 3		CLASS 4		CLASS 5	
		PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK	PEAK	QUASI-PEAK
BROADCAST											
LW	0, 15 - 0, 30	110	97	100	87	90	77	88	67	70	57
MW	0, 53 - 1, 8	86	73	78	65	70	57	62	49	54	41
SW	5, 9 - 6, 2	77	64	71	58	65	52	59	46	53	40
FM	76 - 108	62	49	56	43	50	37	44	31	38	25
TV band I	41 - 88	58	—	52	—	46	—	40	—	34	—
TV band III	174 - 230	Conducted emission – voltage method Not applicable									
DAB III	174 -245										
TV band IV and V	468 - 944										
DTTV	470 - 770										
DAB L band	1447 - 1494										
SDARS	2320 - 2345										
MOBILE SERVICES											
CB	26- 28	68	55	62	49	56	43	50	37	44	31
VHF	30 - 45	68	55	62	49	56	43	50	37	44	31
VHF	68 - 87	62	49	56	43	50	37	44	31	38	25

The EMI filter is designed as follows. The first step is to simulate the magnitude of the primary DM noise source at the worst frequency in the system. Figure 8 shows the simulated triangular current waveform appearing at the primary side of the flyback converter, which is taken as the EMI noise source. The peak current is 3.46 A and the minimum current is 2.86 A. The switching frequency is 350 kHz and the duty cycle is 73.2%.

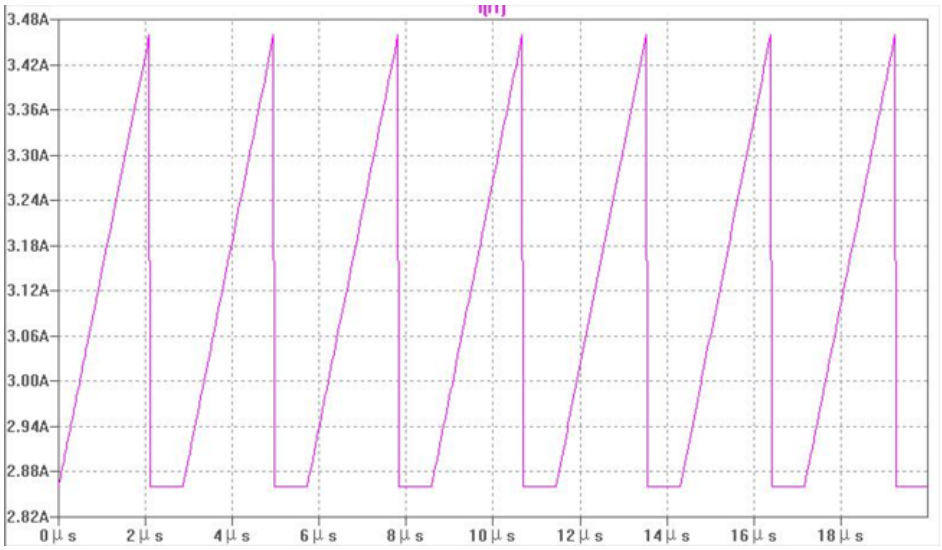


Figure 8. Triangular Current at Primary Side of Flyback

Next, a Fourier transform is performed on the current source of Figure 8. Figure 9 shows the result. Harmonic magnitudes at different frequencies are obtained. The peak amplitude is 166 mA at 350 kHz.

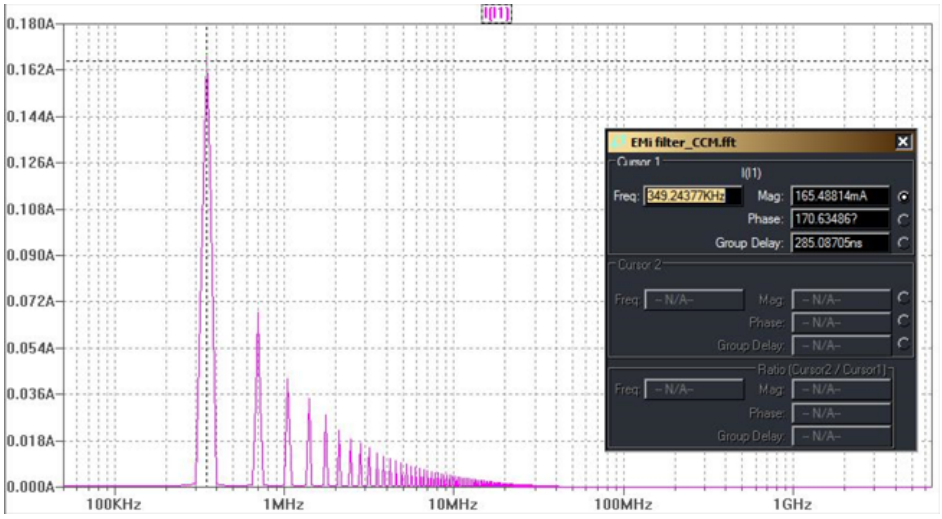


Figure 9. Fourier Component of Primary-Side Current

The noise magnitude, which is picked up by the line impedance stabilization network (LISN) VLISN (350 kHz), is converted into dBµV using Equation 38.

$$V_{LISN\,(350\,kHz)} = 20 \times \log\left(\frac{166\ mA \times 50\ \Omega}{10^{-6}}\right) = 138.4\ dB\mu V \tag{38}$$

Then the noise magnitude is compared to the CISPR-25 limit to determine the required attenuation from the filter ($Att_{(350kHz)}$) in Equation 39:

$$Att_{(350\ kHz)} = V_{LISN\,(350\ kHz)} - M_{(350\ kHz)} = 138.4\ dB - 54\ dB = 84.4\ dB \tag{39}$$

where:

- $M_{(350kHz)}$ is the noise magnitude limit according to the CISPR-25 standard.

Therefore, the required attenuation is 84.4 dB. A four-order LCLC filter has been selected for this design. The corner frequency of the filter (f_c) can be calculated using Equation 40:

$$f_c = \frac{350\ \text{kHz}}{10^{\frac{\text{Att} + 3\ \text{dB}}{80\ \text{dB}}}} = \frac{350\ \text{kHz}}{10^{\frac{(84.4\ \text{dB} + 3\ \text{dB})}{80\ \text{dB}}}} = 28.2\ \text{kHz} \tag{40}$$

The corner frequency and filter inductor can be selected per the cost and size constraints. The filter inductance is selected as 150 µH. The required filter capacitance is calculated in Equation 41 as:

$$C_{DM} = \frac{1}{(2 \times \pi \times f_c)^2 \times L_{DM}} = \frac{1}{(2 \times \pi\, 28.2\ \text{kHz})^2 \times 150\ \mu\text{H}} = 212\ \text{nF} \tag{41}$$

A 4.7-µF DM capacitor is selected and the four-order filter is implemented as Figure 7 shows. The two DM inductors are implemented into the positive line and negative line, respectively. An AC analysis simulation is performed and Figure 10 shows the result. A 141-dB attenuation is achieved. Attenuation from the DM filter is realistic within the frequency range of 150 kHz to 500 kHz. A notable difference can be expected outside of this range due to the parasitic elements equivalent series resistance (ESR), equivalent series inductance (ESL), and equivalent parallel capacitance (EPC).

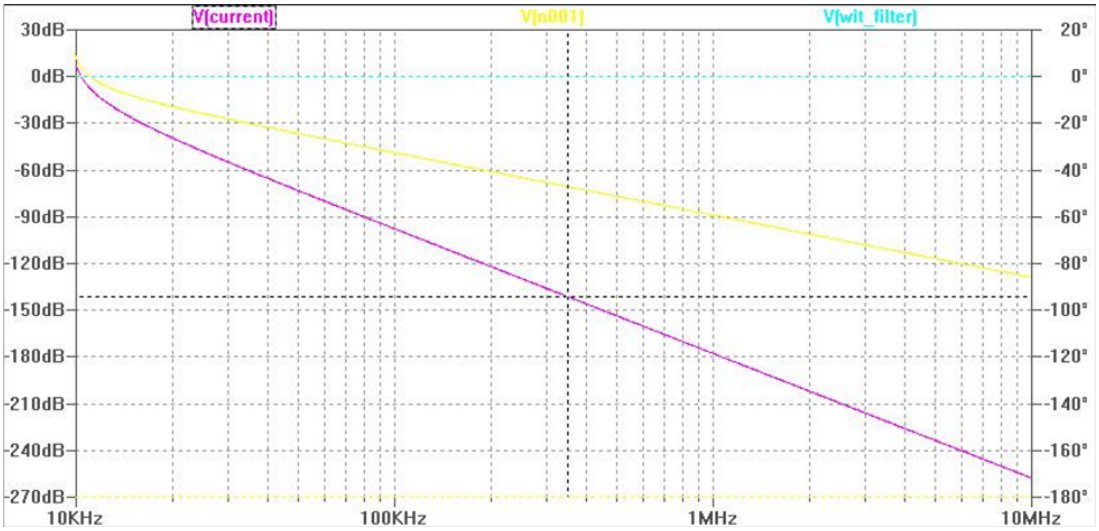


Figure 10. Simulated Frequency Response of Implemented Filter

3 Getting Started Hardware

3.1 Hardware

Figure 11 and Figure 12 show the PCB image of TIDA-01344 from the top side and bottom side, respectively. The board images indicate the input and output connectors and the PCB area of the main devices.

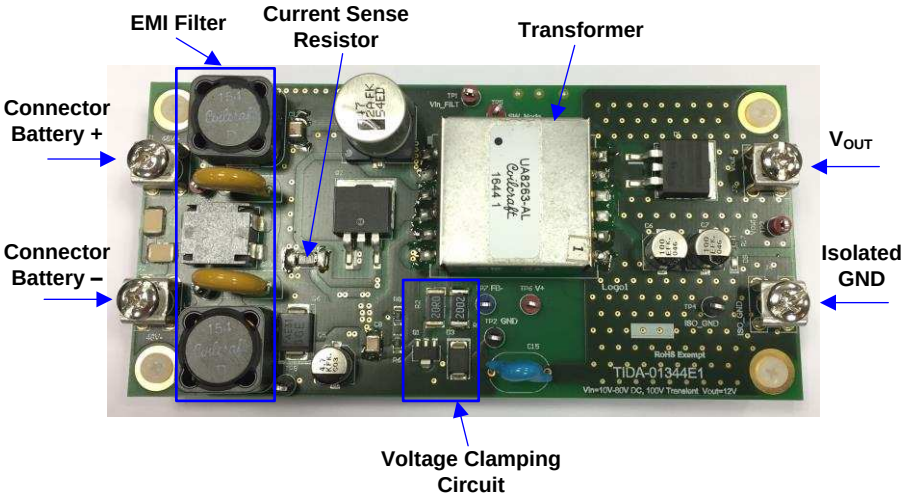


Figure 11. TIDA-01344 PCB Top Side

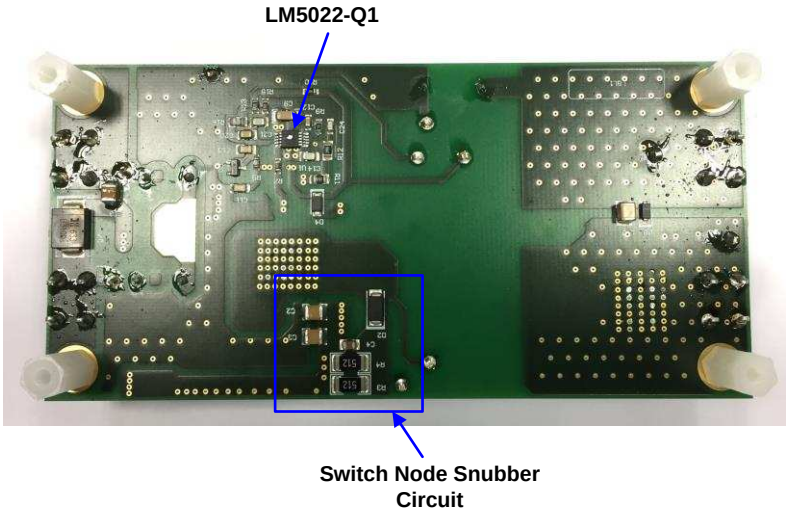


Figure 12. TIDA-01344 PCB Bottom Side

4 Testing and Results

4.1 Start-up Waveforms

4.1.1 Output Voltage and Switching Node

The startup waveforms of the flyback converter are measured under an 11-V input (see Figure 13) and 80-V input (see Figure 14), respectively. The corresponding soft-start times are measured as 10 ms and 5.6 ms.

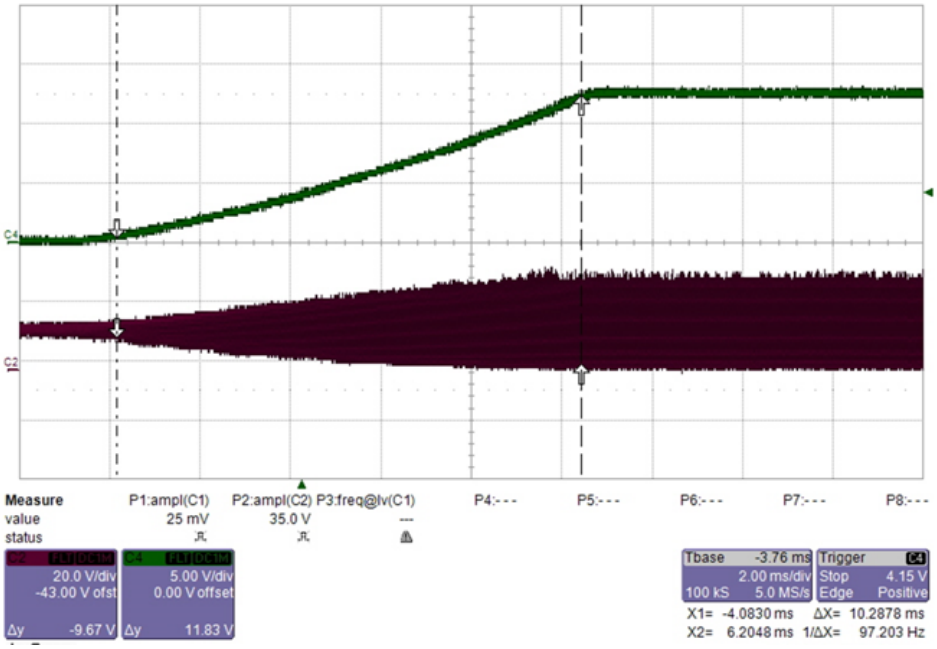


Figure 13. Start-up Waveform of Flyback Converter With V_{IN} = 11 V, I_{OUT} = 1.3 A

NOTE: CH1: Flyback output voltage, CH2: Flyback switch node

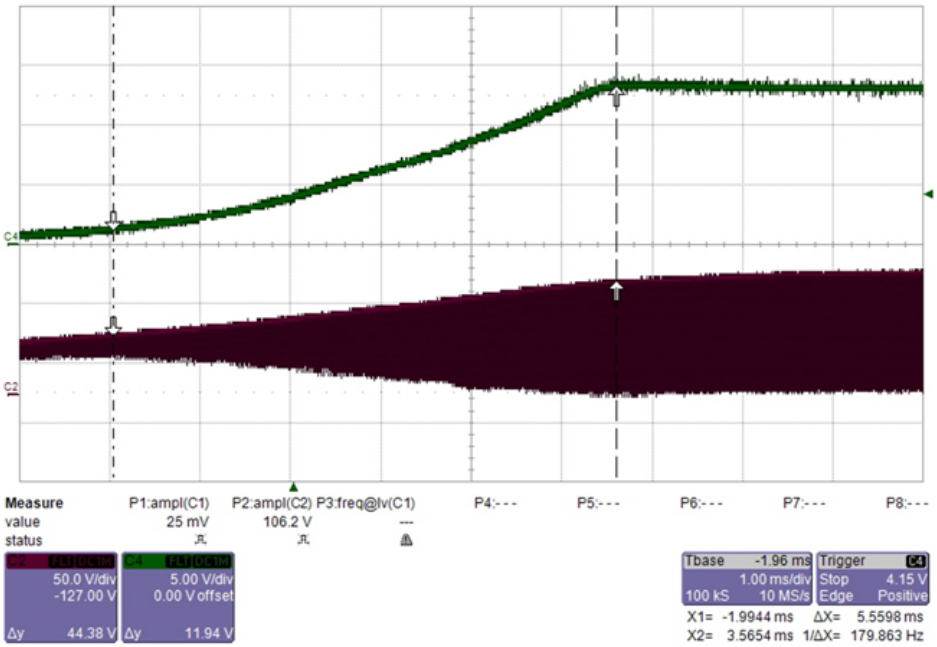


Figure 14. Start-up Waveform of Flyback Converter With V_{IN} = 80 V, I_{OUT} = 1.3 A

NOTE: CH1: Flyback output voltage, CH2: Flyback switch node

4.1.2 Clamping Circuit

Figure 15 shows the output waveform of the clamping circuit. The input voltage is 80 V and the load current is 1.7 A.

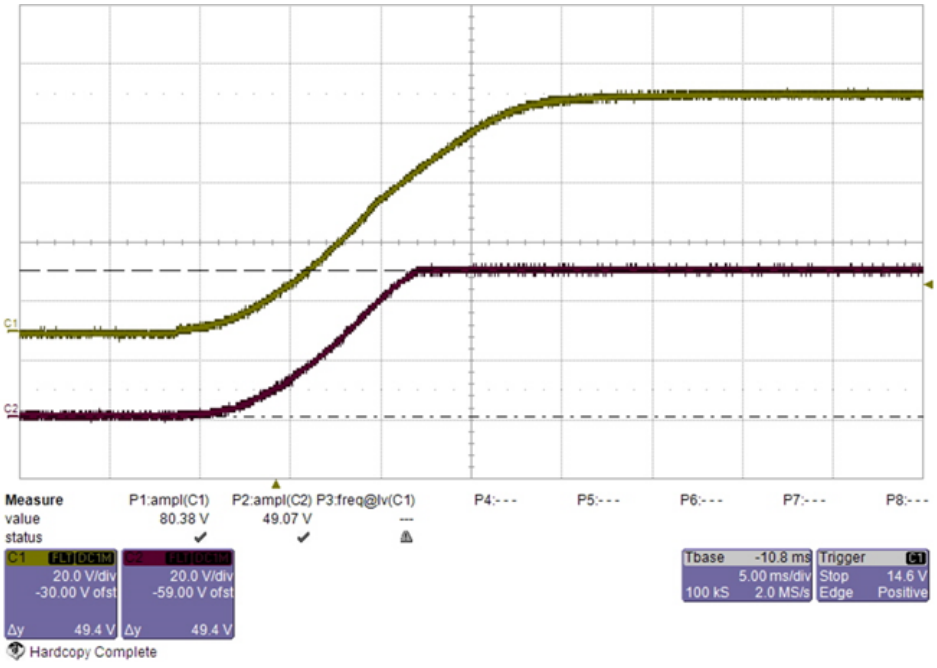


Figure 15. Output Waveform of Clamping Circuit During Start-up

NOTE: CH1: Input voltage, CH2: Pin V_{IN} of LM5022-Q1

4.1.3 Bias Supply

Figure 16 shows the start-up waveform of the LM5022-Q1 bias supply. The input voltage is 48 V and the load current is 1.7 A. The bias supply reduces the device power consumption upon powering up the converter. The bias supply rail comes from the bias winding of the transformer and is connected to the Vcc pin of the LM5022-Q1 device.

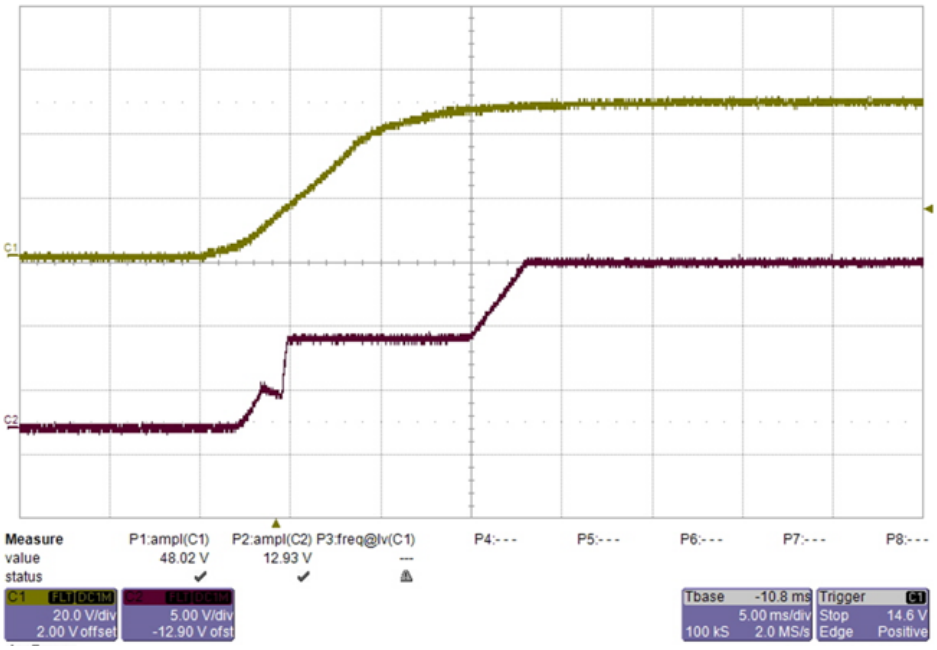


Figure 16. Start-up Waveform of LM5022-Q1 Bias Supply

4.2 Current Sense Waveform

Figure 17 shows the measured waveform across the current sense resistor and current sense pin (CS) of the LM5022-Q1 device, which have been measured respectively. As the figure shows, a clean waveform is obtained after the RC filtering and is received at the CS pin.

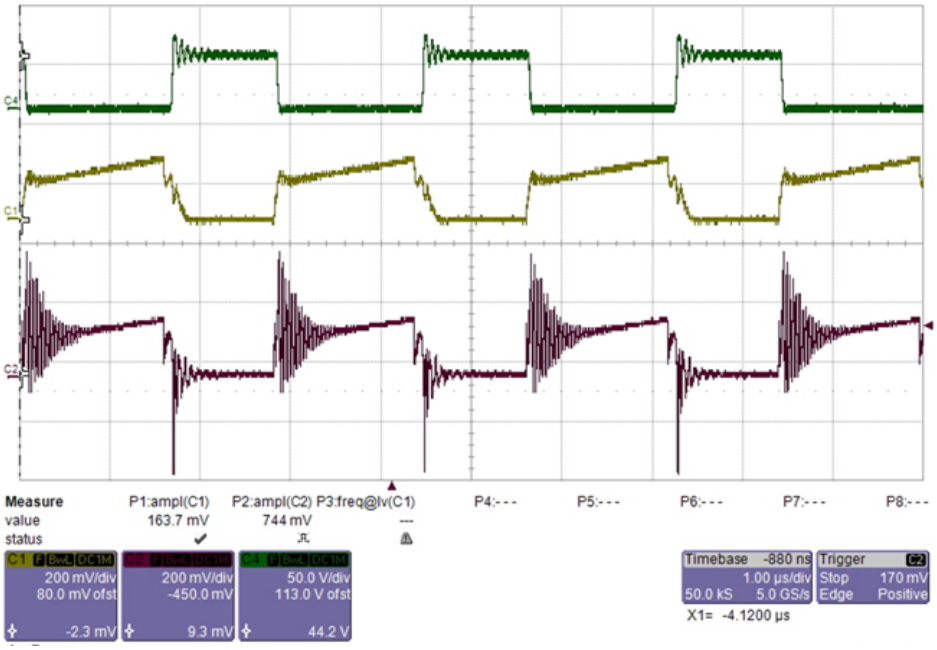


Figure 17. Comparison of Waveforms Across Current Sense Resistor and at LM5022-Q1 CS Pin

NOTE: From top to bottom – CH4: Switch node voltage, CH1: Pin CS of LM5022-Q1, CH2: Voltage across current sense resistor R15

4.3 Efficiency

The efficiency of the TIDA-01344 is measured under conditions of different input voltages. Figure 18 shows the measurement setup. Three digital multimeters are used to measure the input voltage, input current, and output voltage, respectively. The output current is measured through the electronic load.

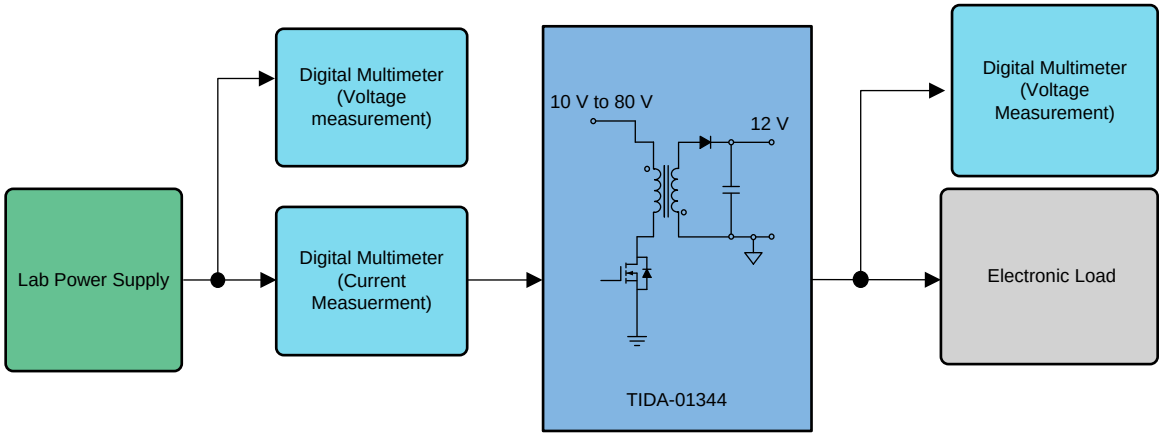


Figure 18. Experimental Setup for Measuring Efficiency of TIDA-01344

Figure 19 shows the measured efficiency of TIDA-01344. As the graph shows, an approximate 87% peak efficiency is achieved with the nominal input voltage of 48 V.

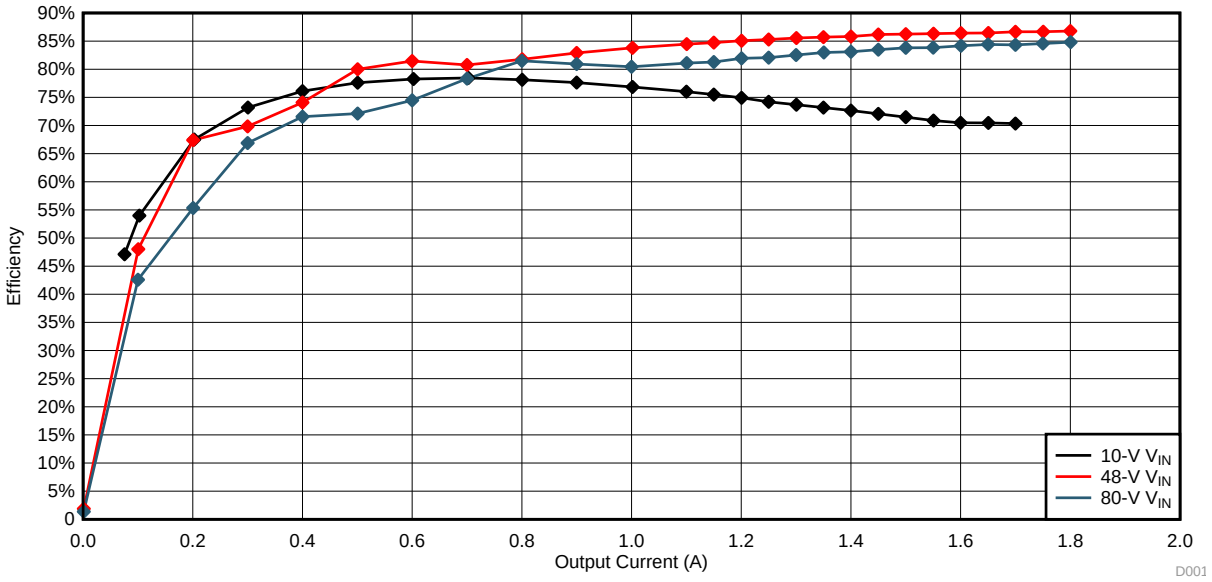


Figure 19. Measured Efficiency of TIDA-01344 Under Input Voltages of: 10 V, 48 V, and 80 V

4.4 Load Regulation

Load regulation measurements show the % of deviation from the nominal output voltage as a function of output current. The experimental setup is the same as that of the efficiency measurement shown in Figure 18. Figure 20 shows the measured result.

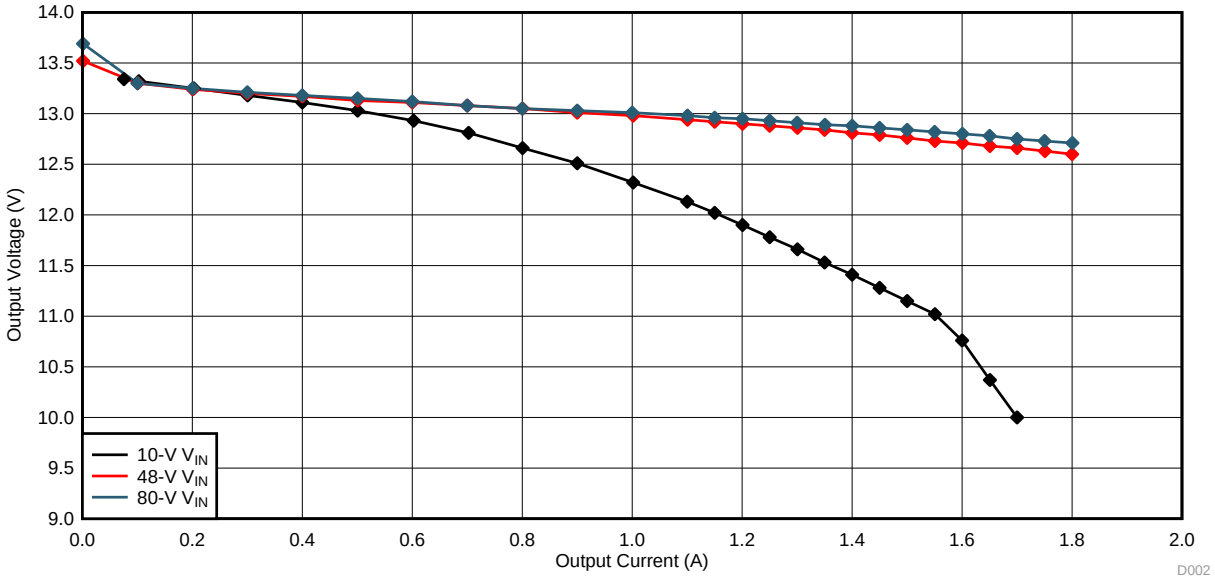


Figure 20. Load Regulation of TIDA-01344

4.5 Output Voltage Ripple

The output voltage ripple of the TIDA-01344 device is measured under light load and full conditions, respectively. The input voltage is kept constant at 48 V. Figure 21 and Figure 22 show the waveforms. As is evident from the waveforms, a 56.4-mV peak-to-peak ripple voltage is obtained at a 1.7-A load.

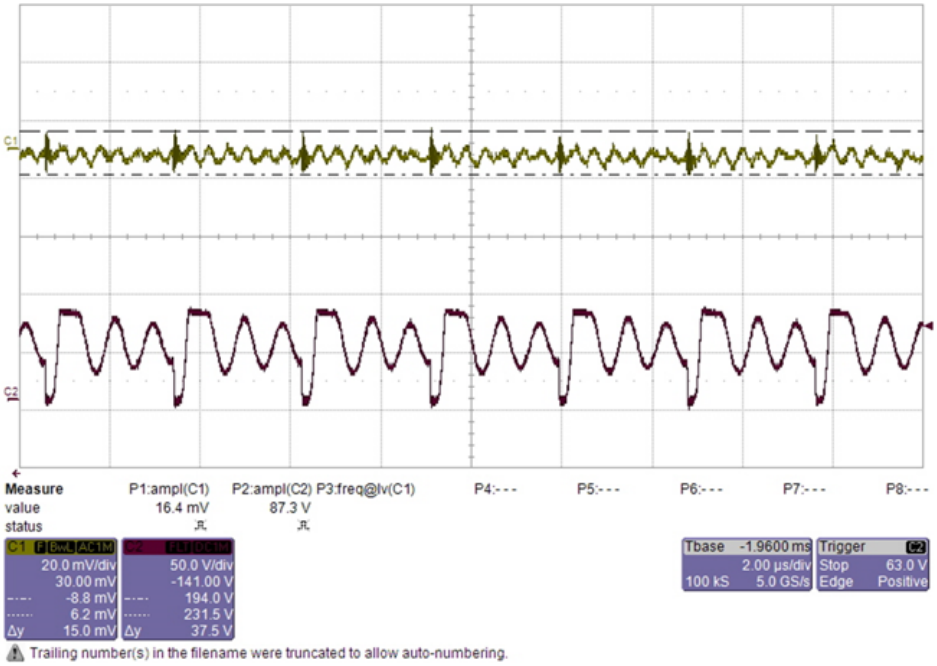


Figure 21. Output Voltage Ripple of Flyback Converter Under V_{IN} = 48 V and I_{OUT} = 0.1 A

NOTE: CH1: Output voltage ripple, CH2: Switch node

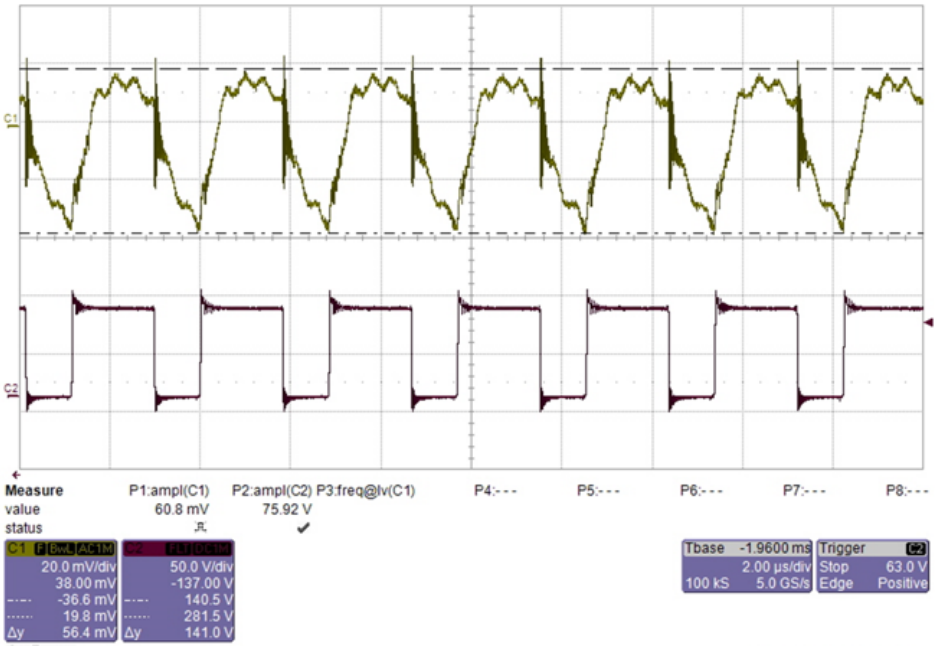


Figure 22. Output Voltage Ripple of Flyback Converter Under V_{IN} = 48 V and I_{OUT} = 1.7 A

NOTE: CH1: Output voltage ripple, CH2: Switch node

4.6 Load Transients

A load transient response presents how well a power supply copes with the changes in the load current demand. Figure 23 shows the load transient response of the TIDA-01344 device. The load is switching from 0.8 A to 1.7 A with a period of 60 ms and a 50% duty cycle. The input voltage is set to 10 V.

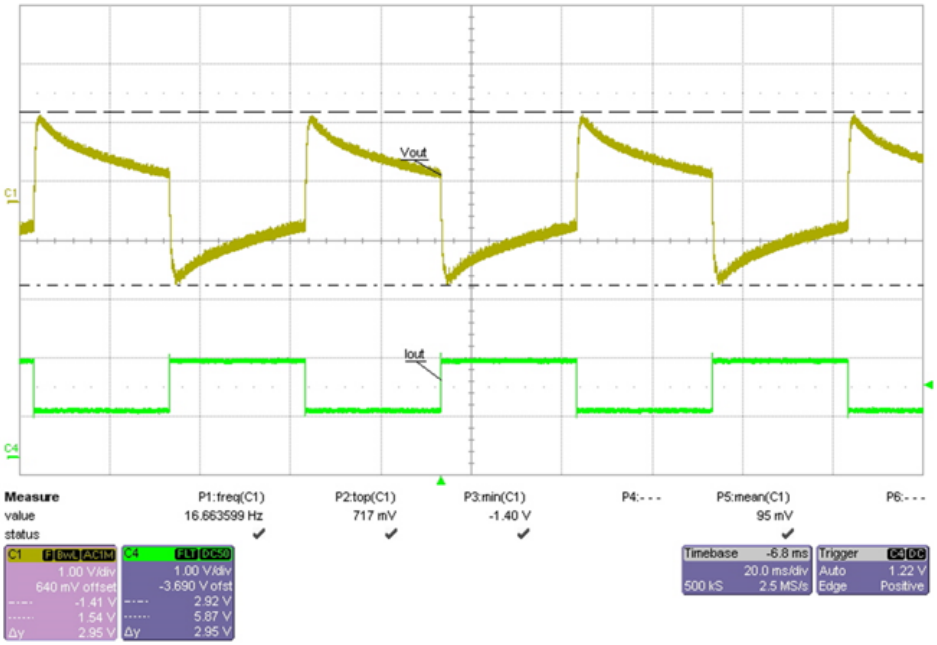


Figure 23. Load Transient Response Under V_{IN} = 10 V and I_{OUT} Switching Between 0.8 A and 1.7 A

NOTE: CH1: Output voltage ripple, CH3: Load current

Figure 24 shows the load transient response under the conditions of a load switching from 0.8 A to 1.7 A with a period of 60 ms and a 50% duty cycle. The input voltage is set to 48 V.

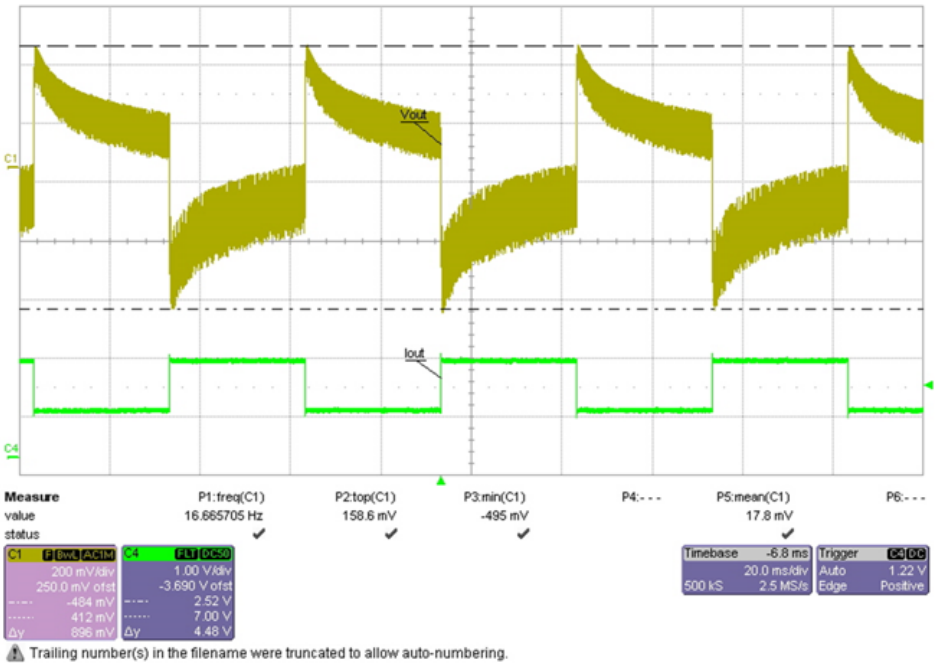


Figure 24. Load Transient Response Under V_{IN} = 48 V and I_{OUT} Switching Between 0.8 A and 1.7 A

NOTE: CH1: Output voltage ripple, CH3: Load current

Figure 25 shows the load transient response under the conditions of a load switching from 0.8 A to 1.7 A with a period of 60 ms and a 50% duty cycle. The input voltage is set to 80 V.

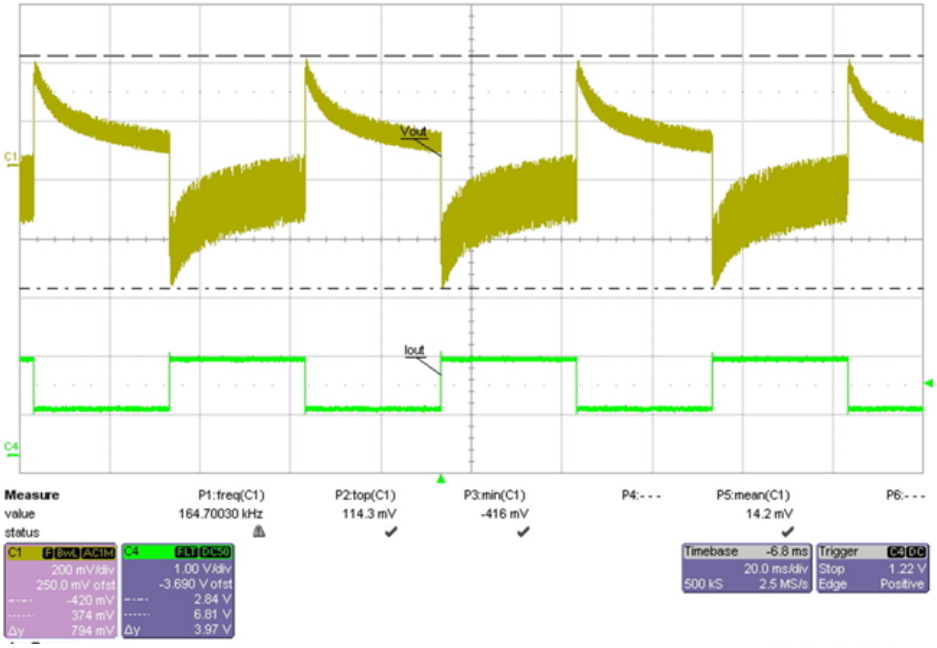


Figure 25. Load Transient Response Under V_{IN} = 80 V and I_{OUT} Switching Between 0.8 A and 1.7 A

NOTE: CH1: Output voltage ripple, CH3: Load current

4.7 Thermal Images

A thermal image of the design board has been measured under full load conditions. The circuit runs at the room temperature for 30 min and a nominal 48-V is applied. The converter is loaded with 1.7 A. The output power is 23.8 W. Figure 26 shows a thermal image of the top-side board and shows a thermal image of the bottom-side board.

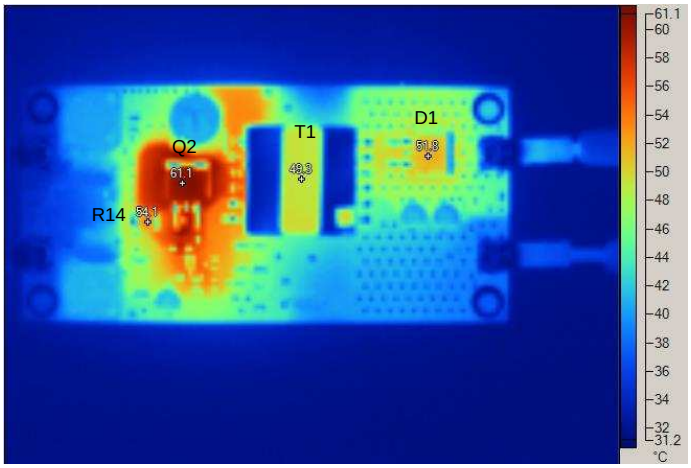


Figure 26. Thermal Image of TIDA-01344 With V_{IN} = 48 V and P_{OUT} = 23.8 W (PCB Top Side)

NOTE: Q2: MOSFET, R14: Current sense resistor, T1: Flyback transformer, D1: Secondary rectification diode

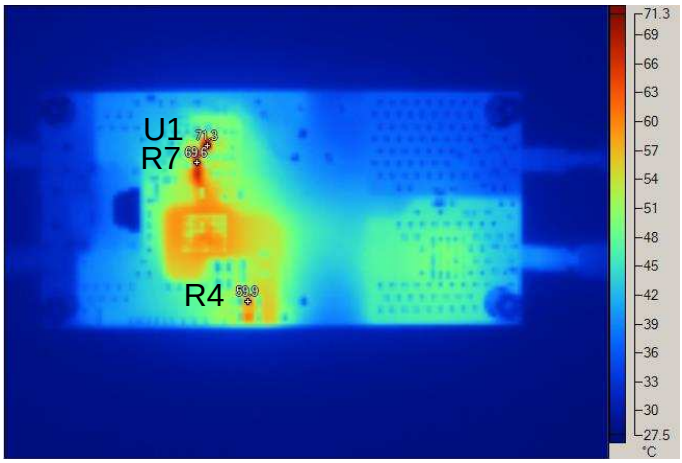


Figure 27. Thermal Image of TIDA-01344 With V_{IN} = 48 V and P_{OUT} = 23.8 W (PCB Bottom Side)

NOTE: U1: LM5022-Q1, R7: Gate resistor, R4: Snubber resistor

4.8 Control Loop Frequency Response

The control loop frequency response represents the stability of the power supply system. The TIDA-01344 loop-frequency response is measured under various loads and input voltages, respectively. Figure 28 shows the measurement setup. The output of the network analyzer is connected to the test points TP6 and TP7, which is located across the injection resistor R10. TP7 and TP6 are also connected to the input channel A and channel B, respectively.

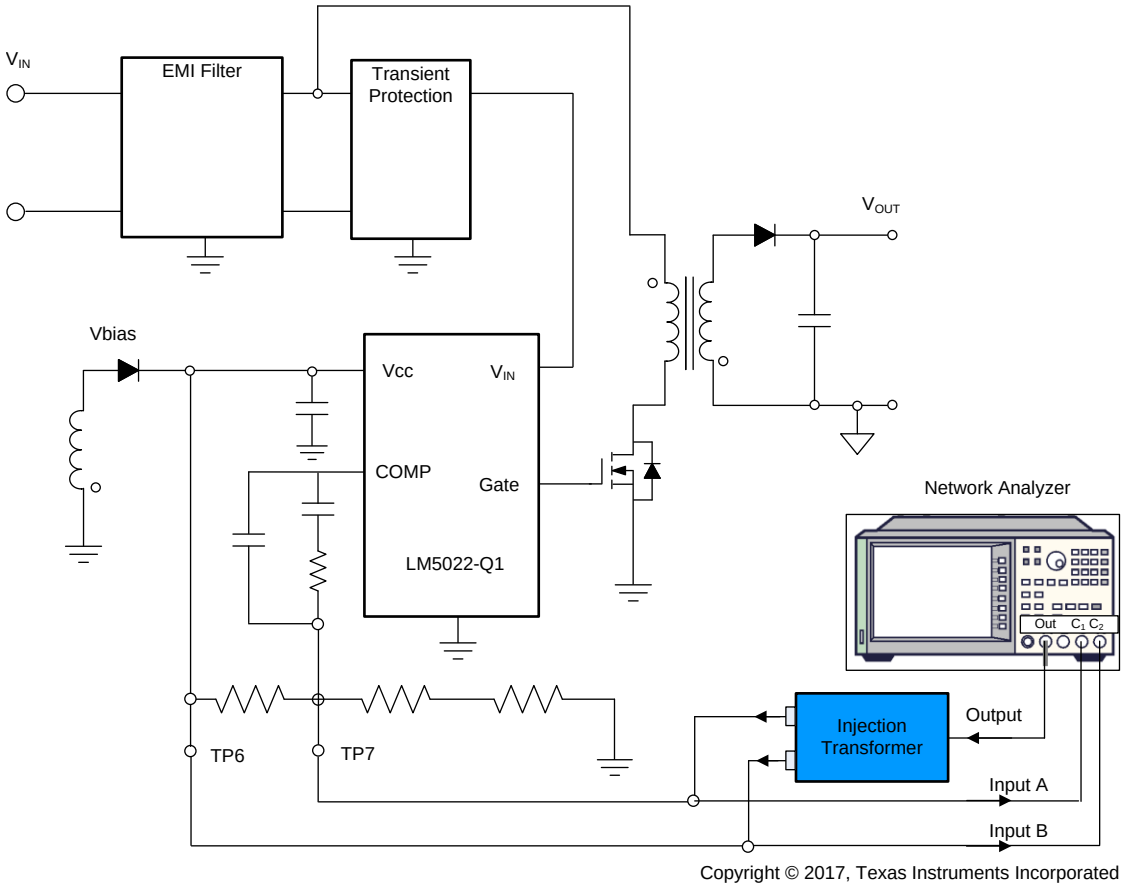


Figure 28. Measurement Setup for Control Loop Frequency Response

The loop frequency response of the buck converter is tested under various conditions as Table 5 shows. The measured results are shown from Figure 29 to Figure 31.

Table 5. Test Conditions and Results of TIDA-01344 Loop-Frequency Response

INPUT VOLTAGE	OUTPUT CURRENT I_{OUT}	OUTPUT POWER	ACHIEVED PHASE MARGIN	ACHIEVED GAIN MARGIN
10 V	1.7 A	23.8 W	48.54°	20 dB
48 V	1.7 A	23.8 W	63.59°	29 dB
80 V	1.7 A	23.8 W	66.31°	30 dB

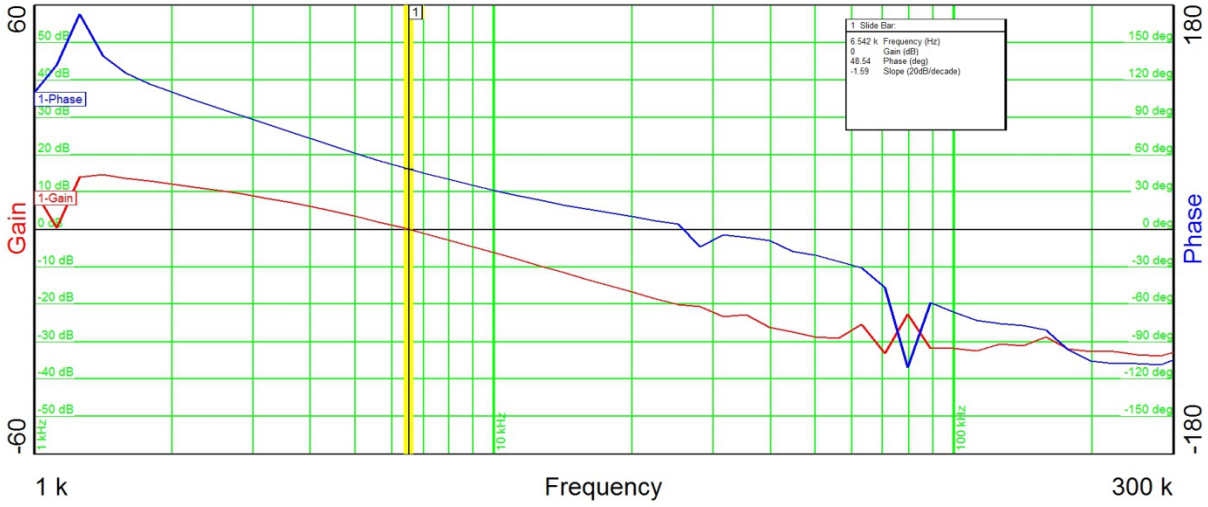


Figure 29. Loop Frequency Response of TIDA-01344 With V_{IN} = 10 V and I_{OUT} = 1.7 A

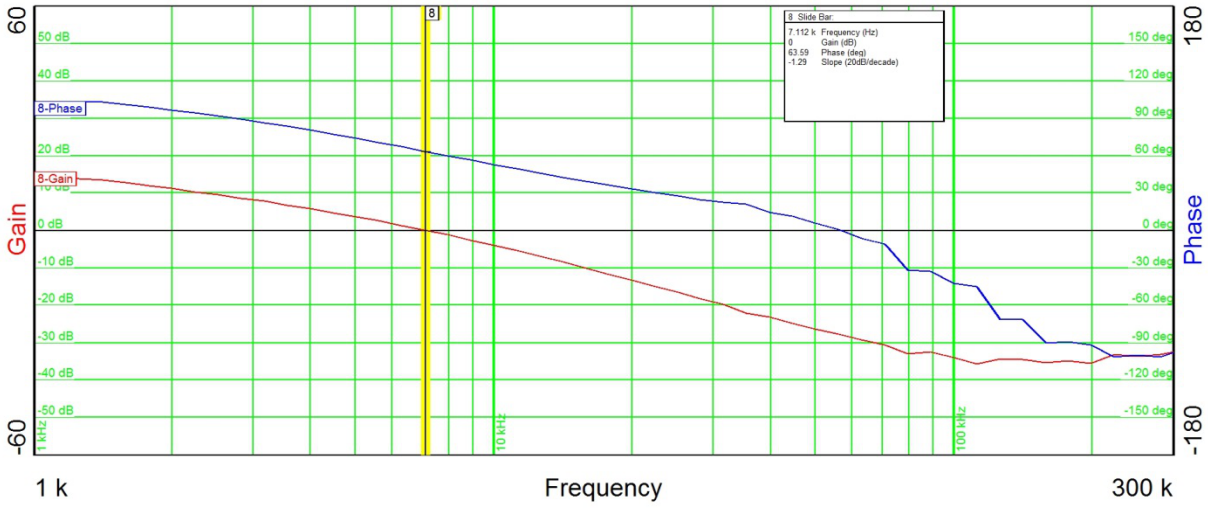


Figure 30. Loop Frequency Response of TIDA-01344 With V_{IN} = 48 V and I_{OUT} = 1.7 A

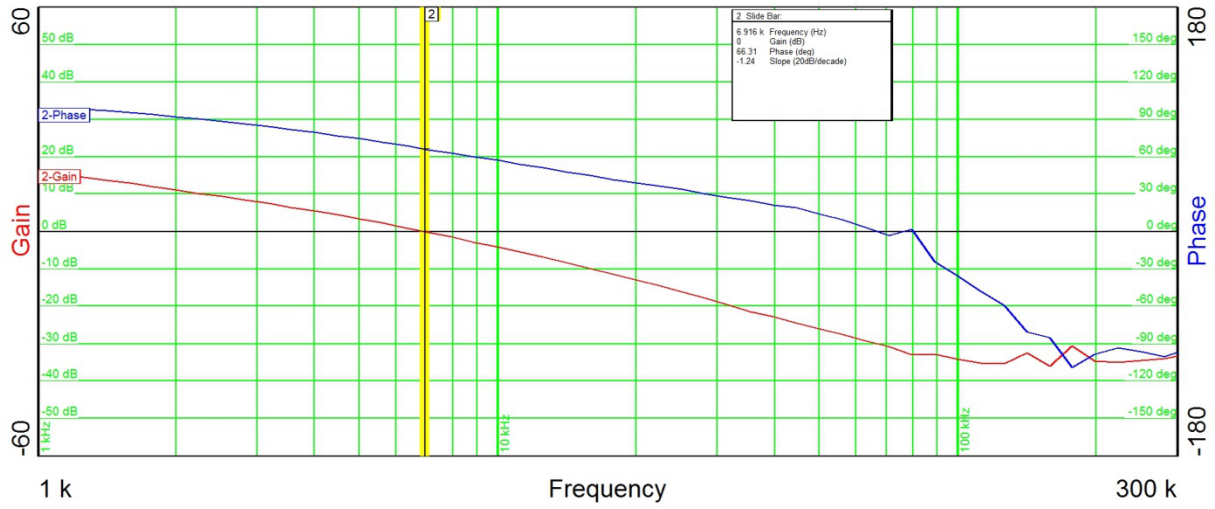


Figure 31. Loop Frequency Response of TIDA-01344 With V_{IN} = 80 V and I_{OUT} = 1.7 A

4.9 CISPR25 Conducted Emissions Testing

Conducted emission tests have been performed on the TIDA-01344 device. The CISPR-25 standard contains limits and procedures for the measurement of radio disturbances in the frequency range of 150 kHz to 2.5 GHz. The standard applies to any electronic or electrical component intended for use in vehicles, trailers, and devices. The emission standard consists of conducted emissions and radiated emissions, respectively, and TIDA-01344 focuses on the conducted emission tests. Radiated emissions are not of interest because this subsystem (as a part of the HEV and EV traction inverter system) is placed into an aluminum case where most the radiated emissions are shielded.

4.9.1 Conducted Emissions Test Setup and Conditions

The test setup for conducted emissions is outlined in the CISPR-25 standard documentation. The equipment under test (EUT) is powered through an artificial network or LISN and loaded. The EUT is placed on a non-conductive, low-relative permittivity material ($\varepsilon r \leq 1.4$), at 50 ±5 mm above the ground plane. The power supply lines between the connector of the artificial network and the connector of the EUT must a standard length of 200 mm. The load simulator is placed directly on the ground plane. A spectrum analyzer is connected to the artificial network through a Bayonet Neill-Concelman (BNC) cable to measure the conducted emissions of the EUT.

The peak and average ambient noise of different frequencies is measured and shown from Figure 32 to Figure 35.

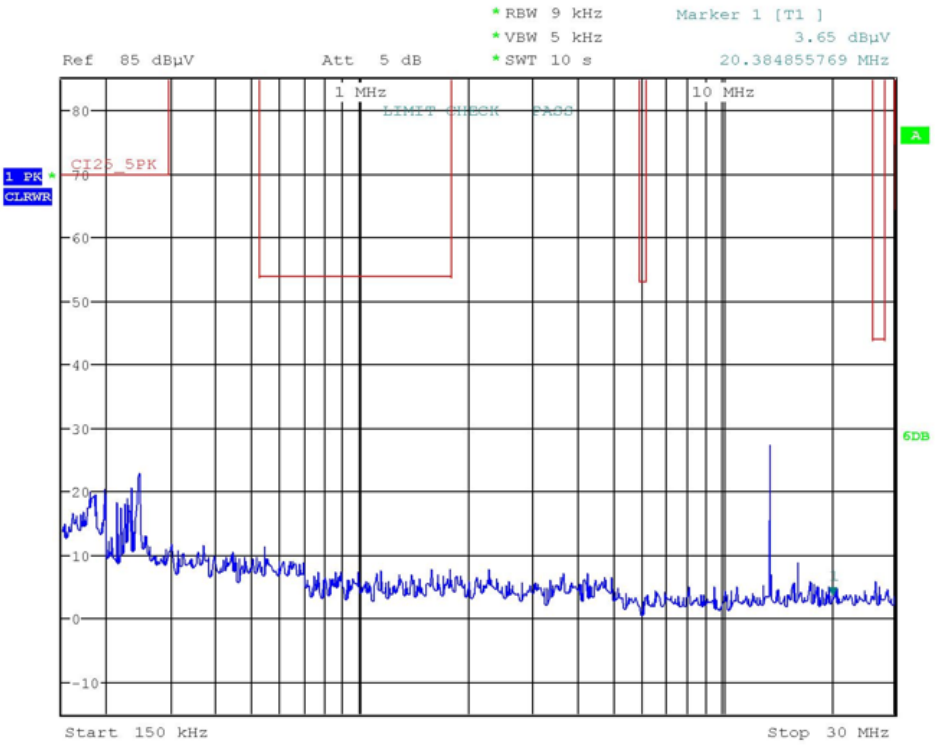


Figure 32. Ambient Noise (Peak Measurement: 150 kHz to 30 MHz)

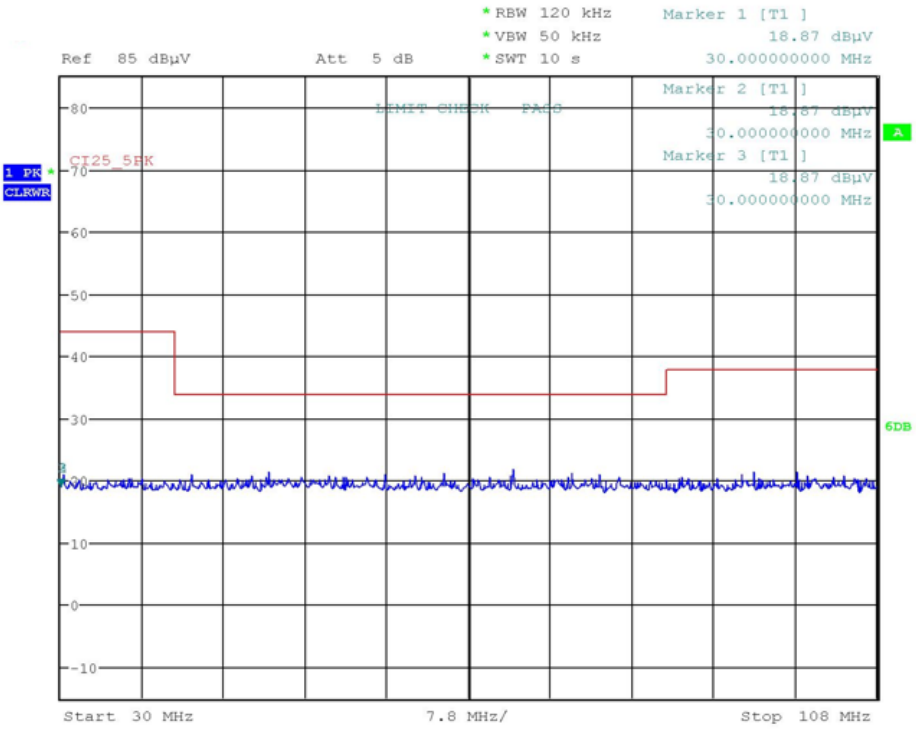


Figure 33. Ambient Noise (Peak Measurement: 30 MHz to 108 MHz)

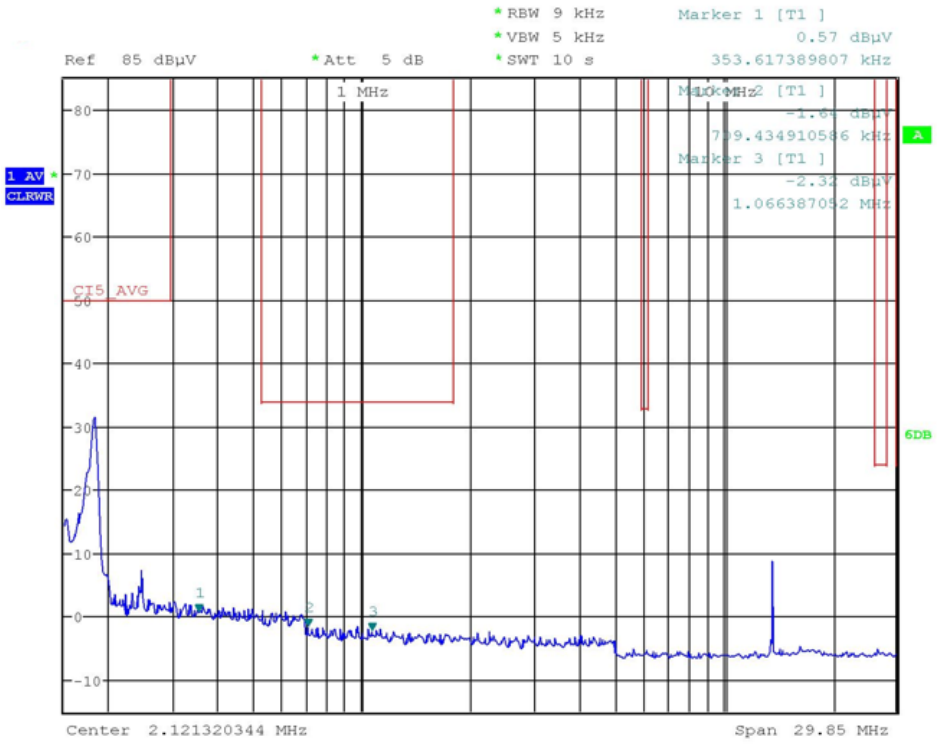


Figure 34. Ambient Noise (Average Measurement: 150 kHz to 30 MHz)

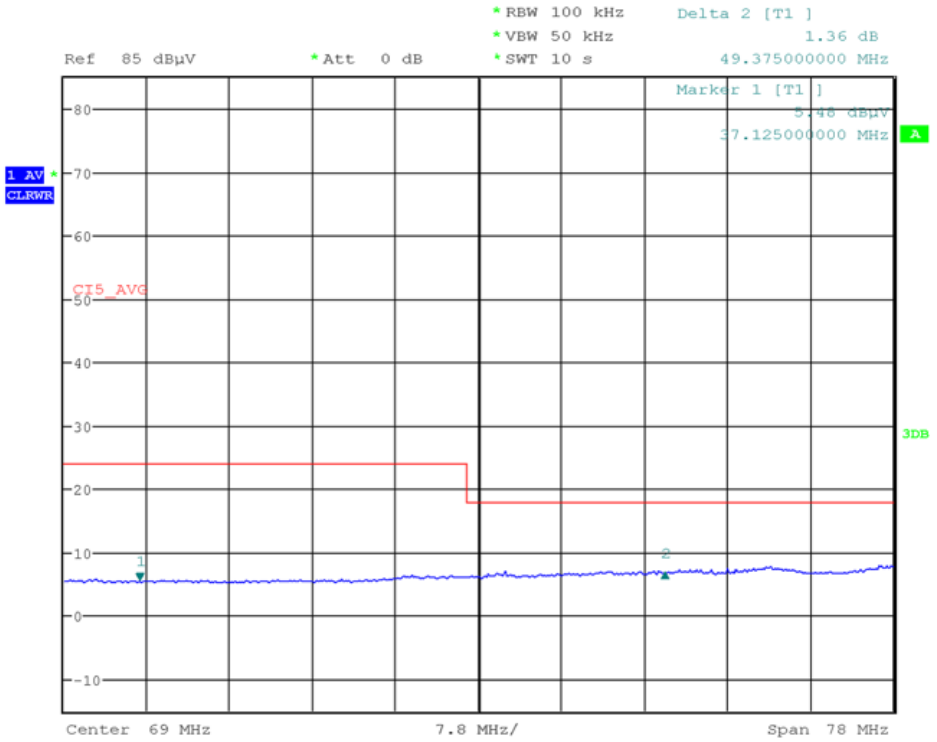


Figure 35. Ambient Noise (Average Measurement: 30 MHz to 108 MHz)

4.9.2 Peak Noise Measurement

The conducted emissions of the TIDA-01344 device is measured under different input voltages and a full load condition.

4.9.2.1 With 10-V Input at Full Load

The conducted emissions of the TIDA-01344 board is measured at a 10-V input voltage and under a 1.7-A output current. Figure 36 and Figure 37 show the measured peak noise within the different frequency ranges, respectively

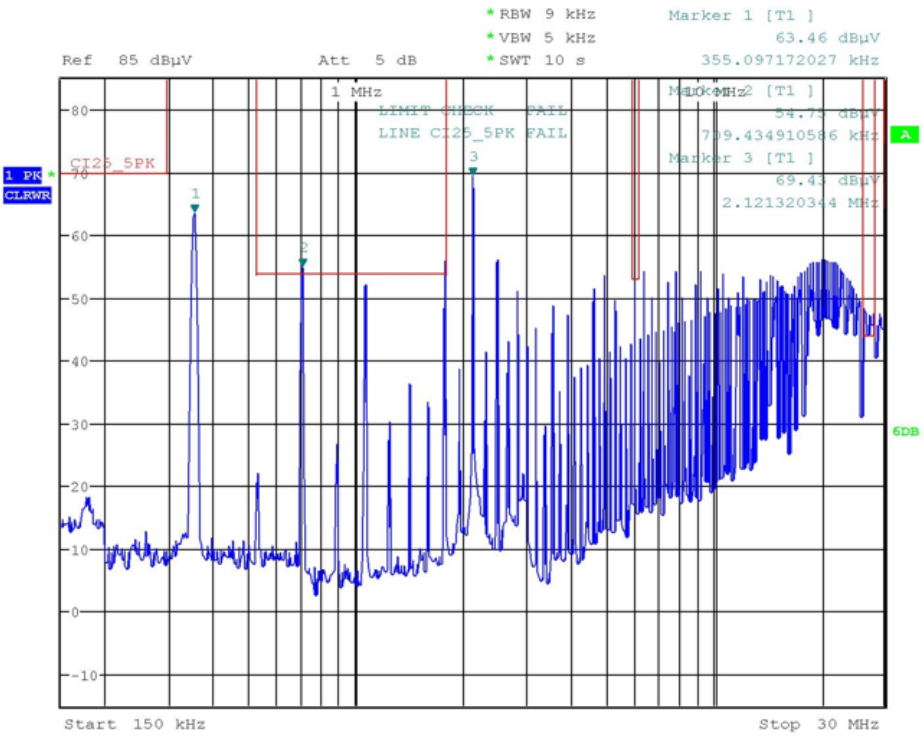


Figure 36. Peak Noise of TIDA-01344 With V_{IN} = 10 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 peak

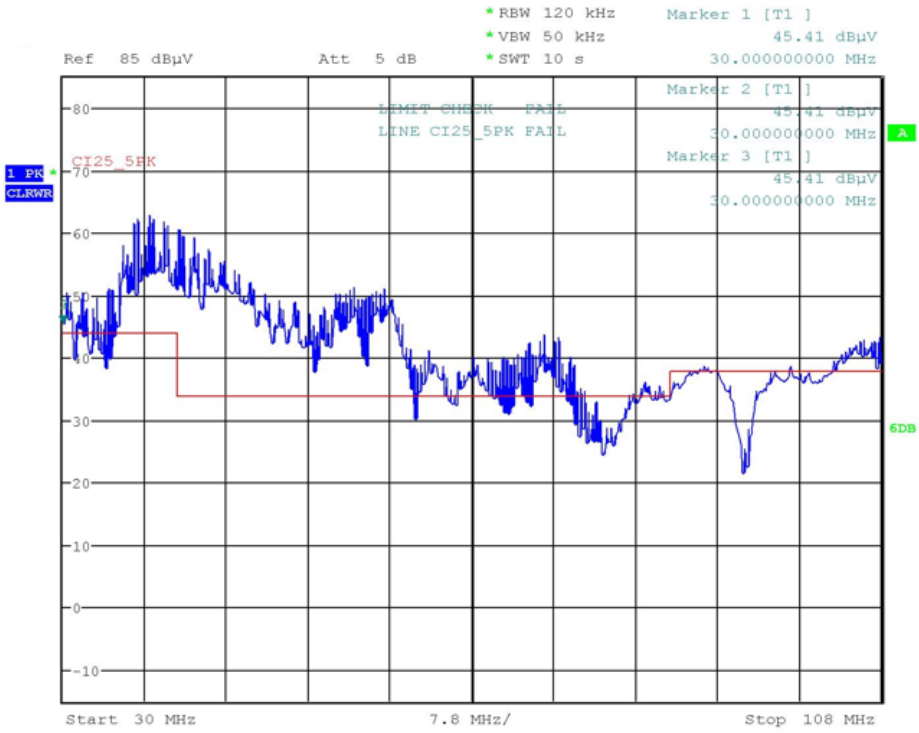


Figure 37. Peak Noise of TIDA-01344 With V_{IN} = 10 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 peak

4.9.2.2 With 48-V Input at Full Load

The conducted emissions of the TIDA-01344 board is measured at a 48-V input voltage and under a 1.7-A output current. Figure 38and Figure 39 show the measured peak noise within the different frequency ranges, respectively.

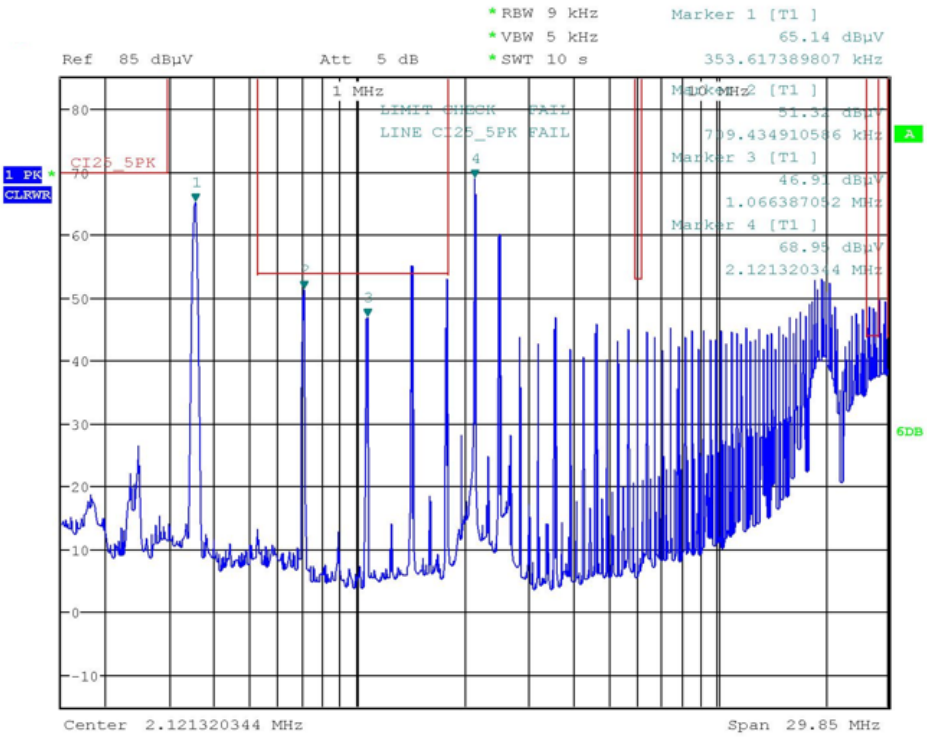


Figure 38. Peak Noise of TIDA-01344 With V_{IN} = 48 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 peak

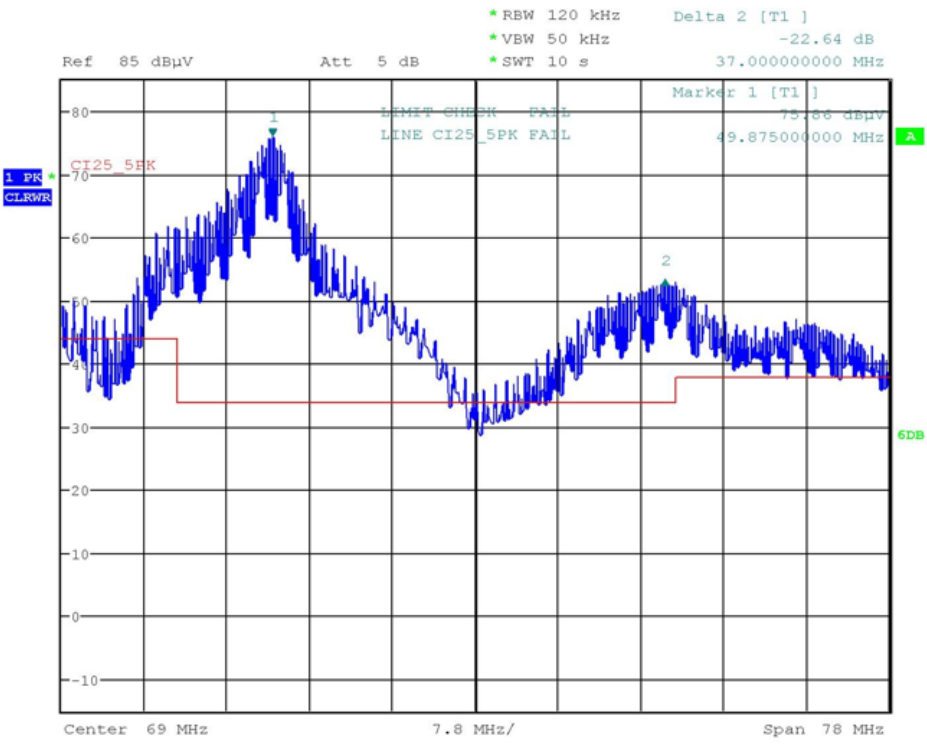


Figure 39. Peak Noise of TIDA-01344 With V_{IN} = 48 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 peak

4.9.2.3 With 80-V Input at Full Load

The conducted emissions of the TIDA-01344 board is measured at an 80-V input voltage and under a 1.7-A output current. Figure 40 and Figure 41 show the measured peak noise within the different frequency ranges, respectively.

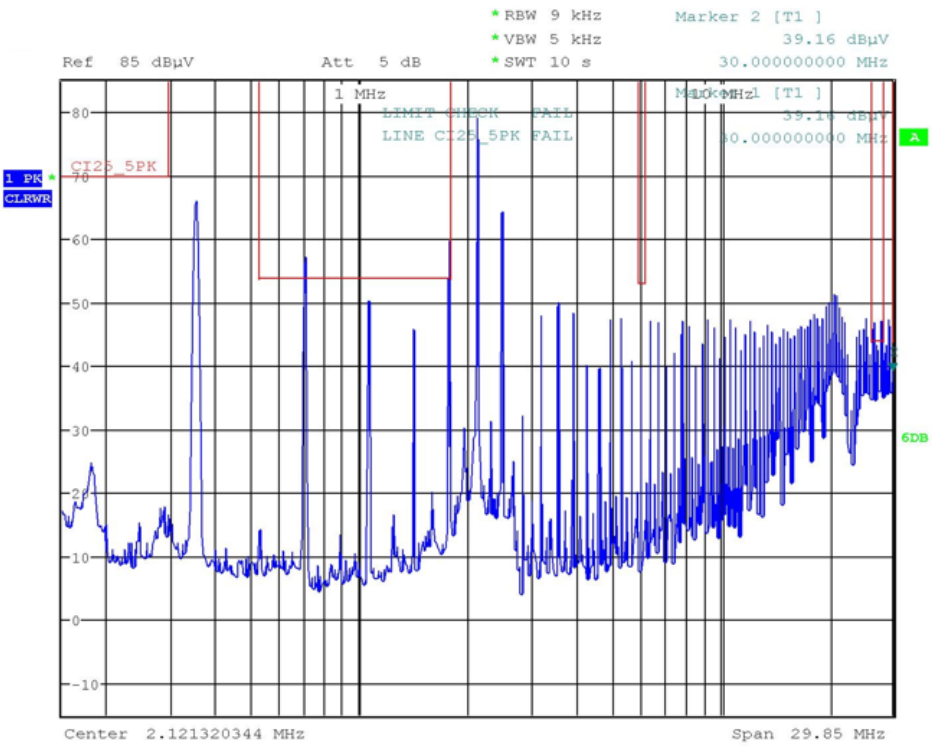


Figure 40. Peak Noise of TIDA-01344 With V_{IN} = 80 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 peak

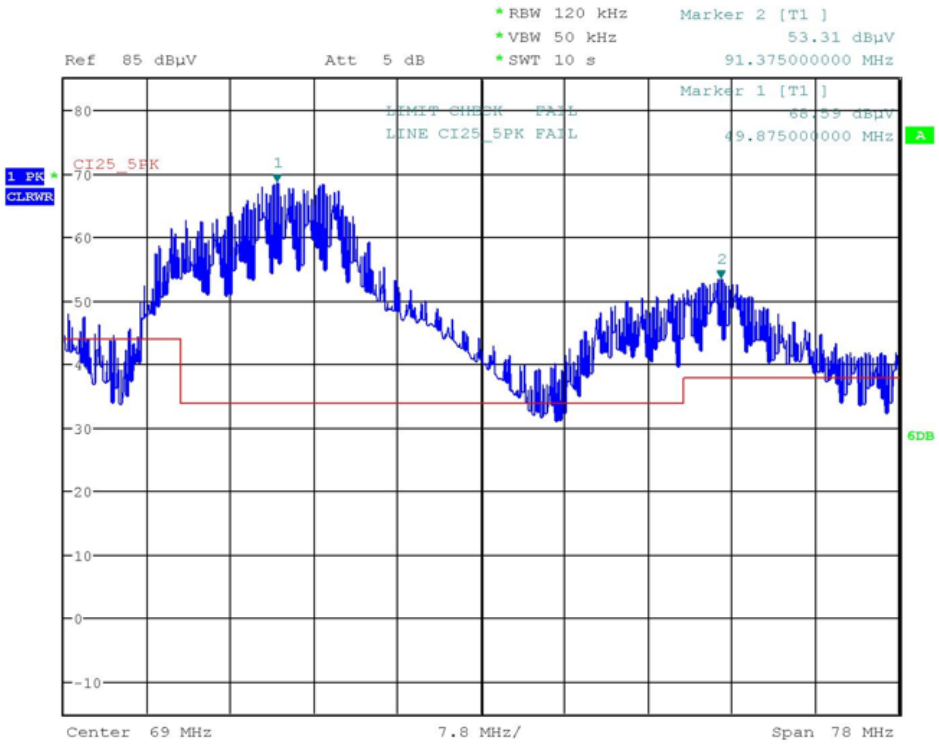


Figure 41. Peak Noise of TIDA-01344 With V_{IN} = 80 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 peak

4.9.3 With External Filter

An external EMI filter is applied to further reduce the EMI. Figure 42 shows the filter schematic. Both the peak and average noise is measured in comparison with the CISPR-25 standard class 5.

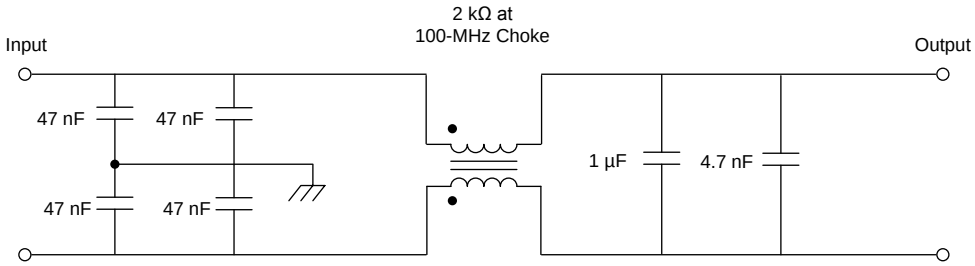


Figure 42. Implemented External CM Filter

4.9.3.1 With 10-V Input at Full Load

The conducted emissions of the TIDA-01344 board with the implemented external filter is measured at a 10-V input voltage and under a 1.7-A output current. Figure 43 to Figure 46 show the measured peak noise and average noise within the different frequencies.

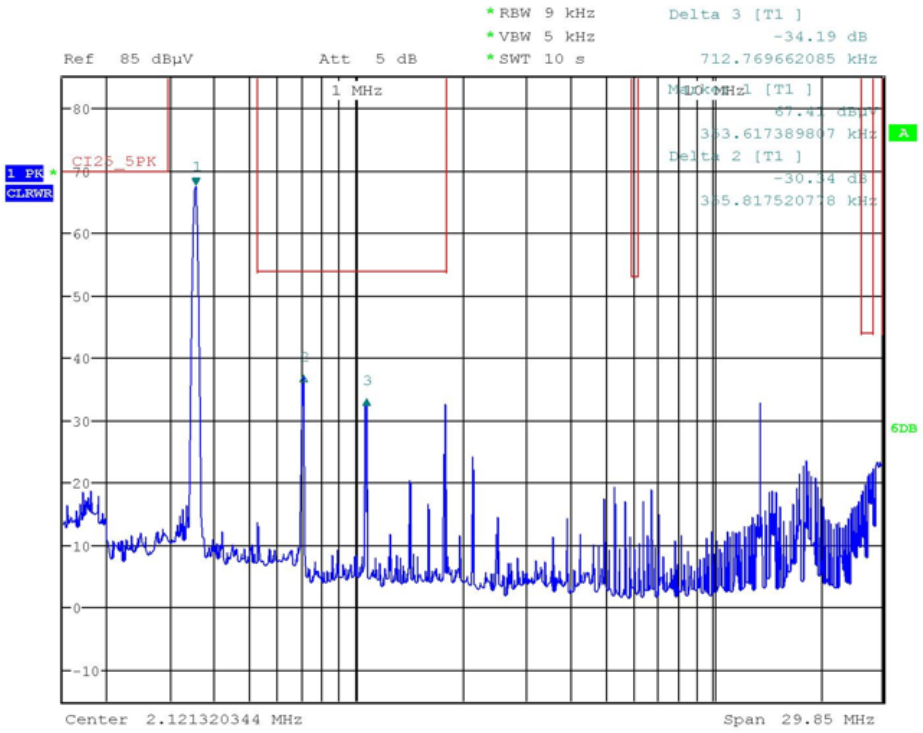


Figure 43. Peak Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 10 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 peak

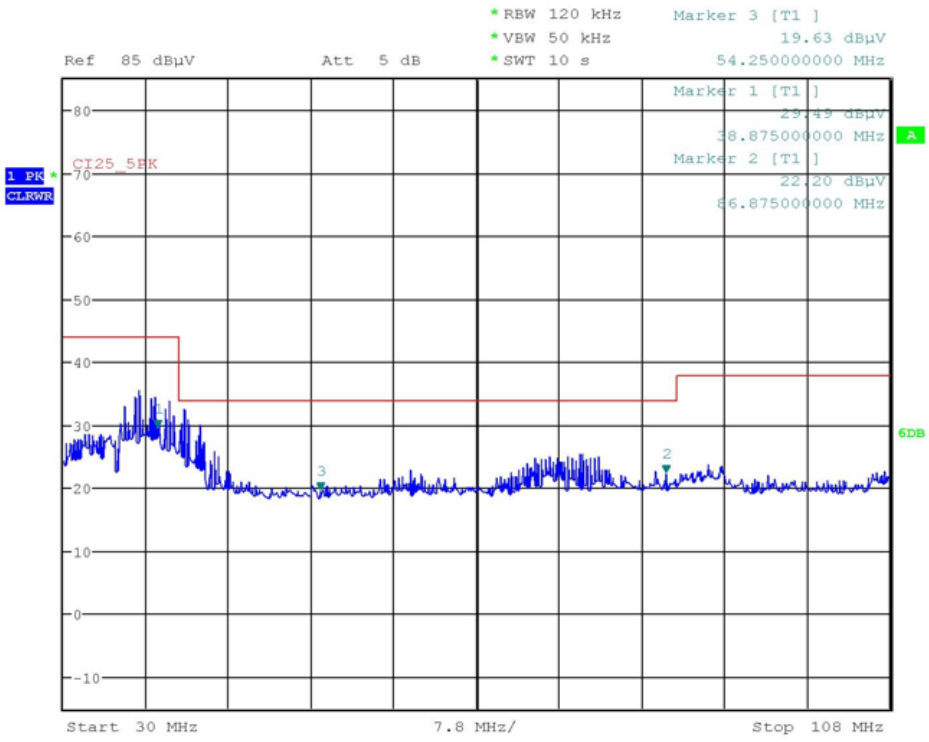


Figure 44. Peak Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 10 V and I_{OUT} = 1.7 A

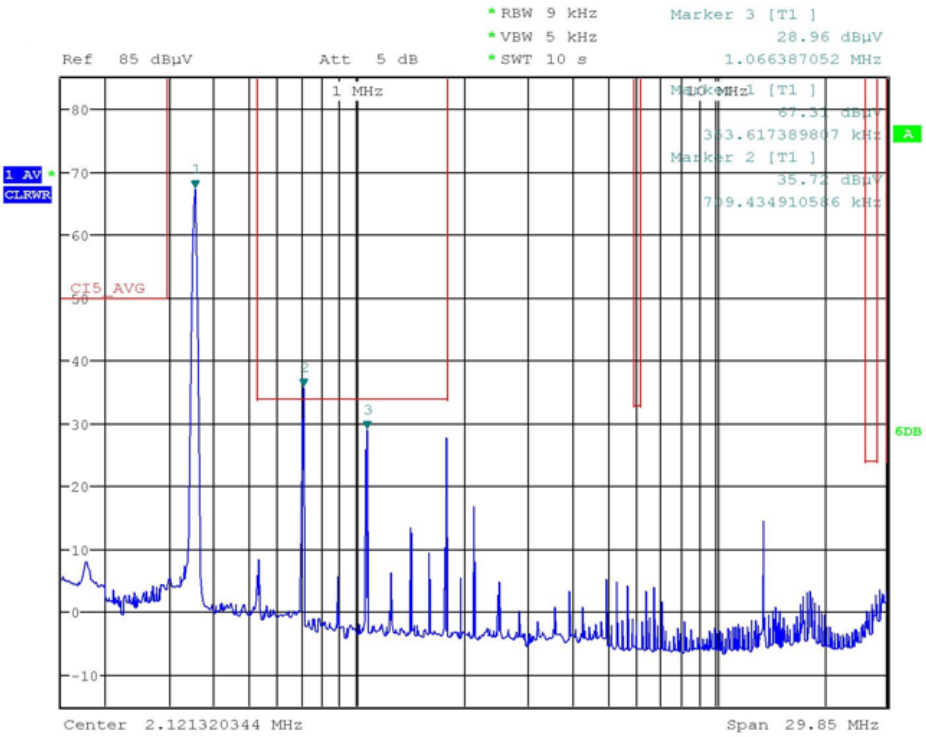


Figure 45. Frequency Range: 30 MHz to 108 MHz, Limit Line: CISPR 25, Class: 5 Peak

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 average

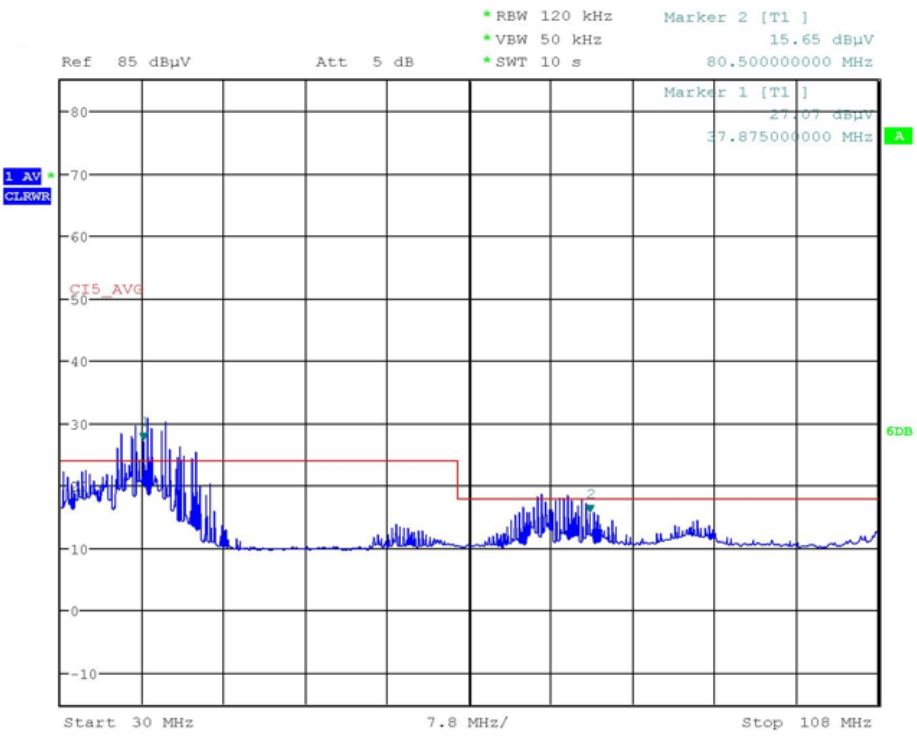


Figure 46. Average Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 10 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 average

4.9.3.2 With 48-V Input at Full Load

The conducted emissions of the TIDA-01344 board with the implemented external filter is measured at a 48-V input voltage and under a 1.7-A output current. Figure 47 to Figure 50 show the measured peak noise and average noise within the different frequencies.

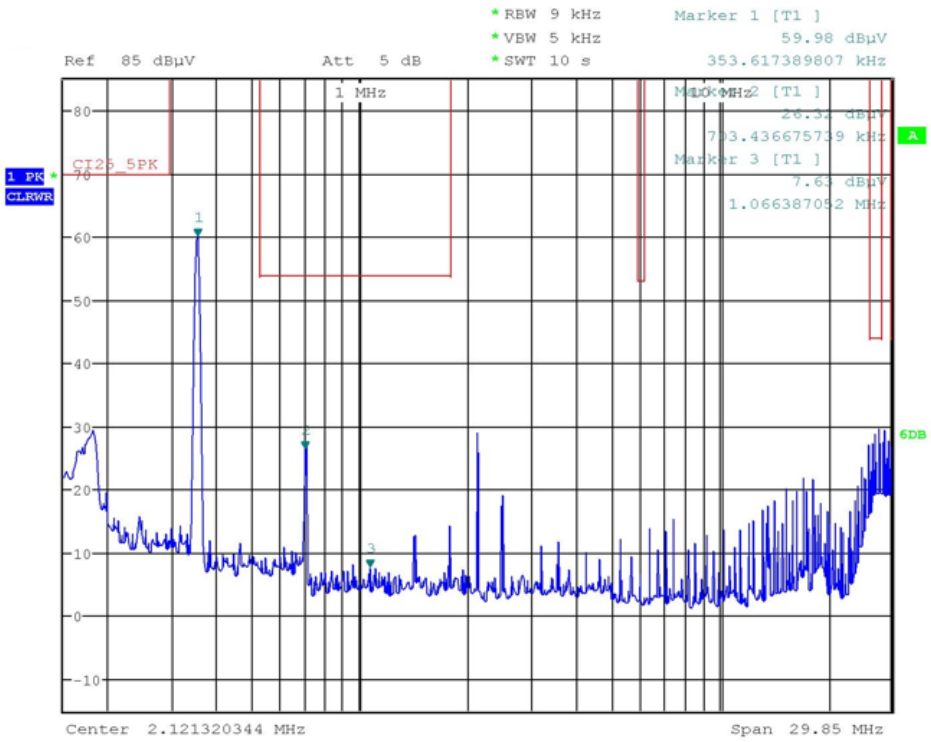


Figure 47. Peak Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 48 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz –to 30 MHz, Limit line: CISPR 25, Class: 5 peak

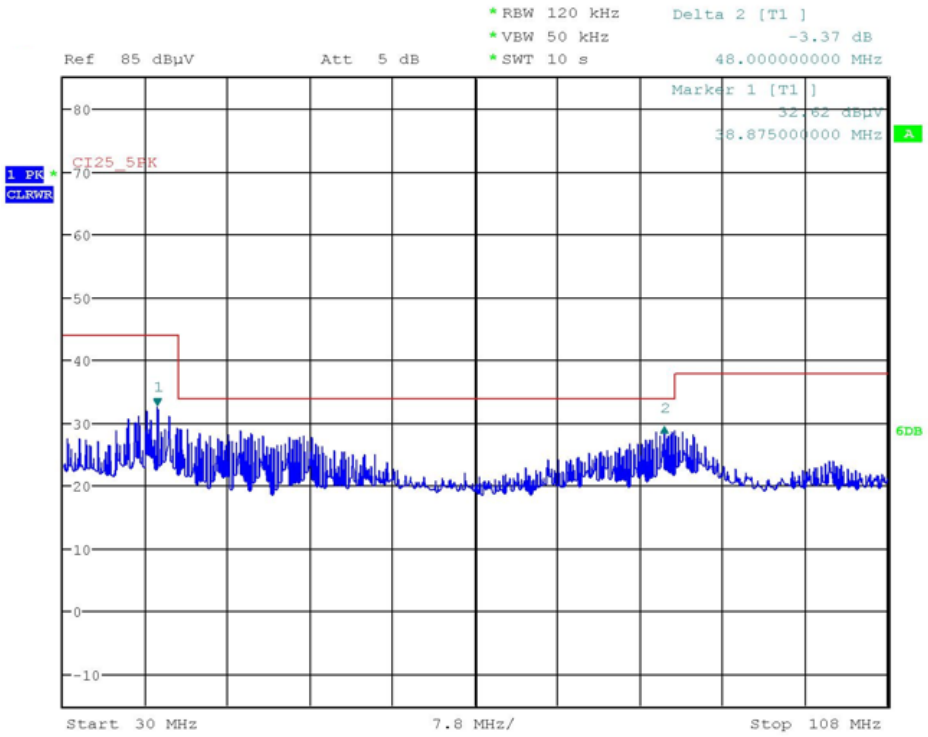


Figure 48. Peak Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 48 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 peak

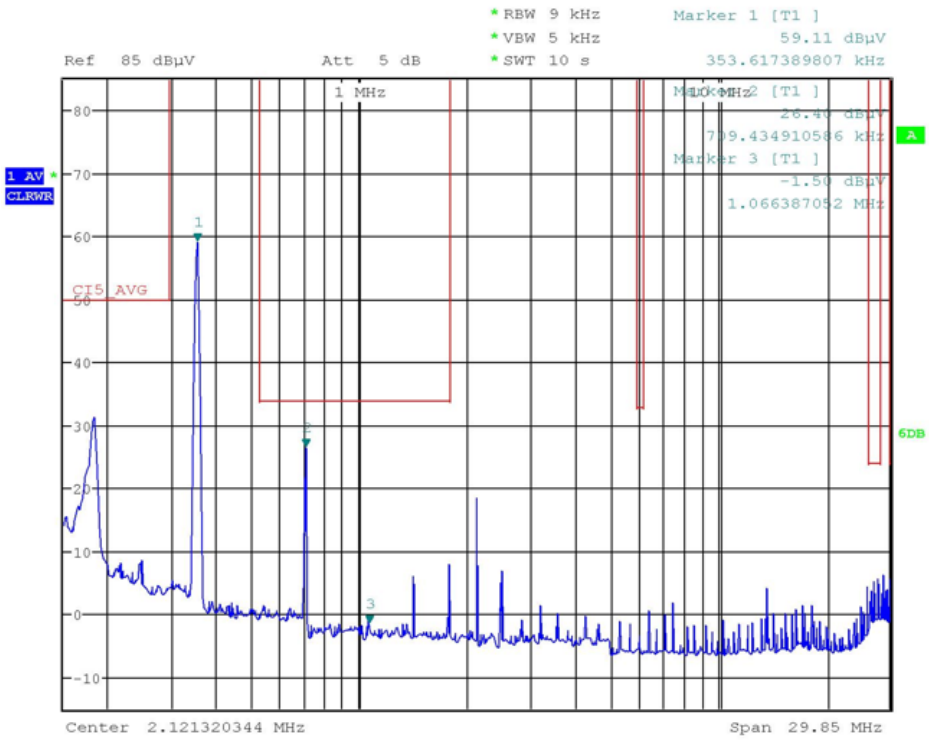


Figure 49. Average Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 48 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 average

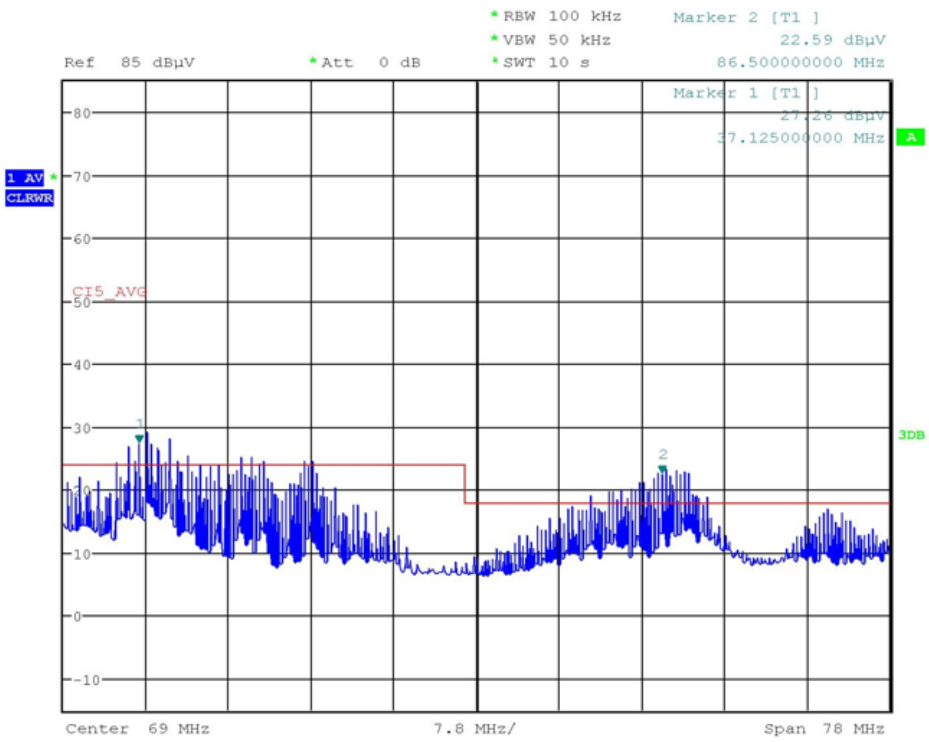


Figure 50. Average Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 80 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 average

4.9.3.3 With 80-V Input at Full Load

The conducted emissions of the TIDA-01344 board with the implemented external filter is measured at a 48-V input voltage and under a 1.7-A output current. Figure 51 to Figure 54 show the measured peak noise and average noise within the different frequencies.

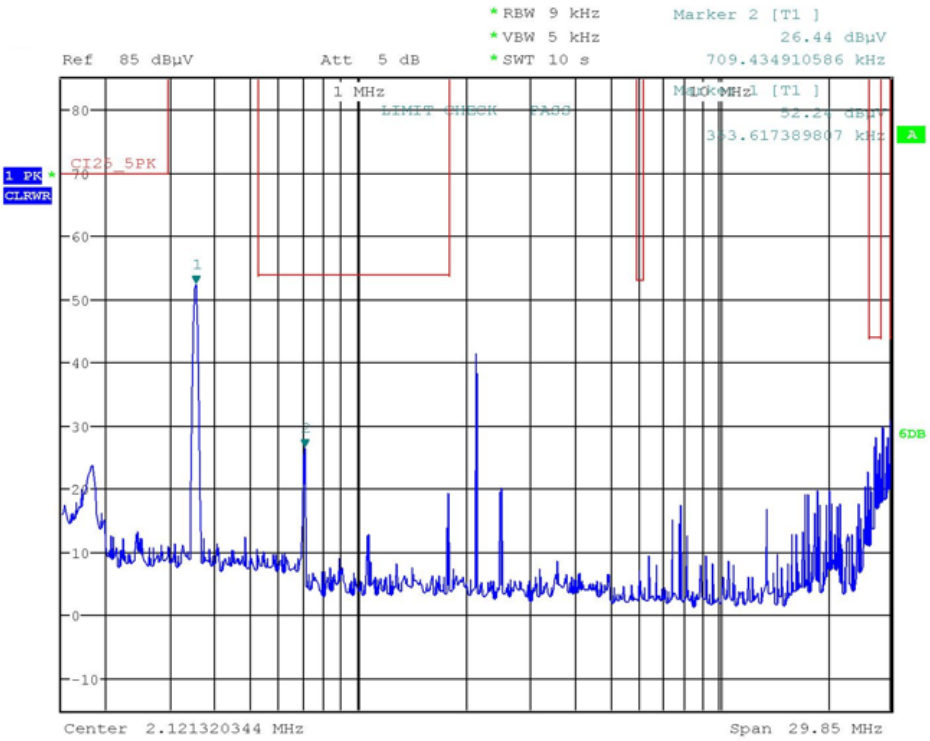


Figure 51. Peak Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 80 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 peak

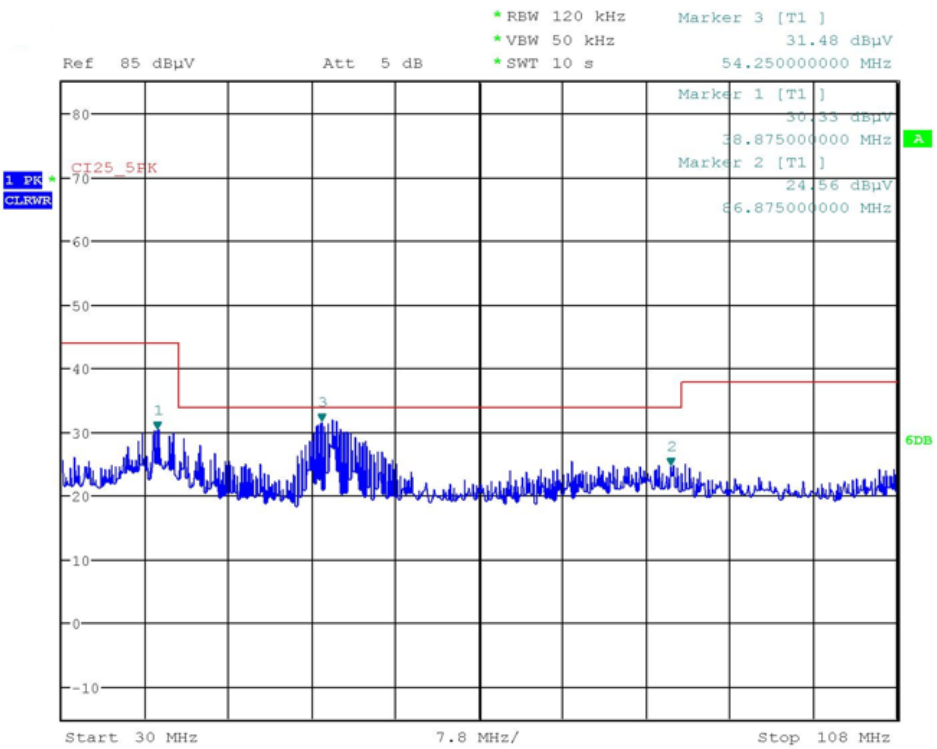


Figure 52. Peak Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 80 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 peak

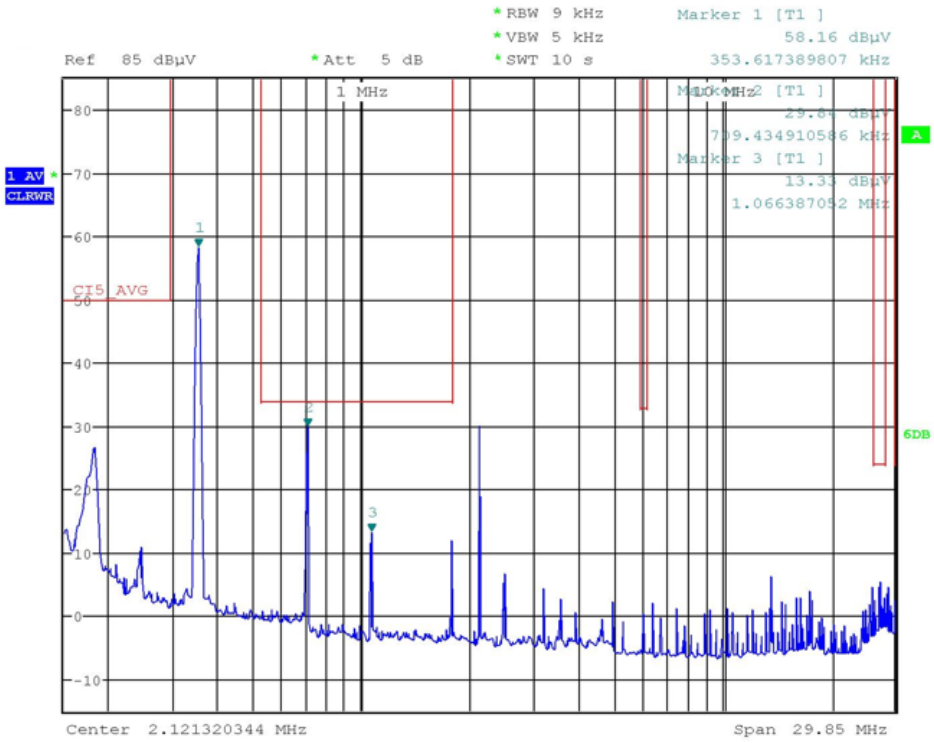


Figure 53. Average Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 80 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 150 kHz to 30 MHz, Limit line: CISPR 25, Class: 5 average

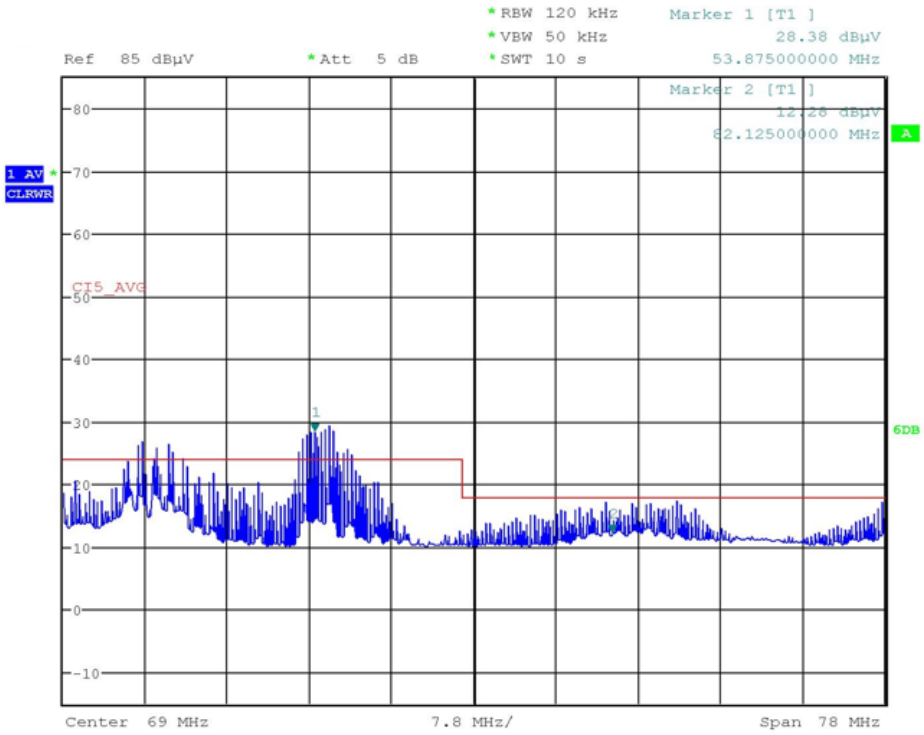


Figure 54. Average Noise of TIDA-01344 With External Filter Under Conditions: V_{IN} = 80 V and I_{OUT} = 1.7 A

NOTE: Frequency range: 30 MHz to 108 MHz, Limit line: CISPR 25, Class: 5 average

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01344.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01344.

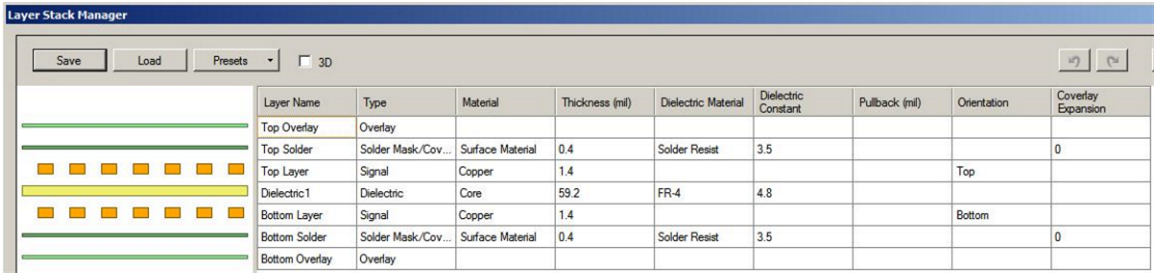
5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01344.

5.3.2 Layout Guidelines

TIDA-01344 implements a two-layer PCB. Figure 55 shows the board material, copper thickness, and the dielectric distance between the two layers.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric1	Dielectric	Core	59.2	FR-4	4.8			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask/Cov...	Surface Material	0.4	Solder Resist	3.5			0
Bottom Overlay	Overlay							

Figure 55. Layer Stack of TIDA-01344

Figure 56 shows the placement of the device input capacitor, which is placed as close as possible to the controller.

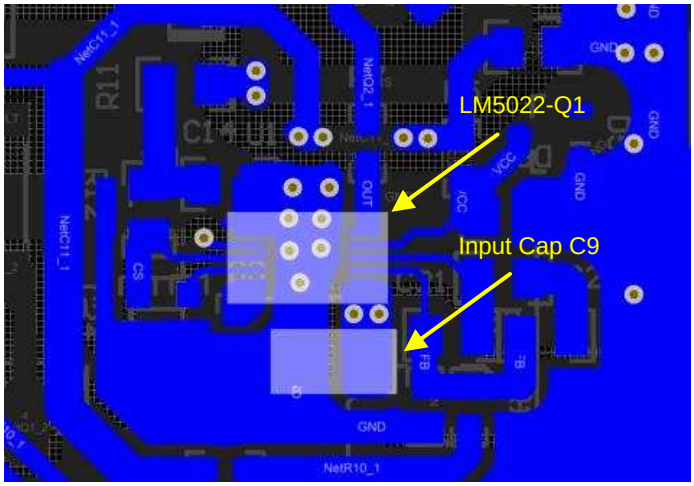


Figure 56. Placement of Input Capacitors of LM5022-Q1

Figure 57 shows the power stage and current sensing loop. The input capacitors of the power stage, MOSFET Q2, and current sense resistor R14 are placed as close as possible to the transformer primary winding to minimize the current loop.

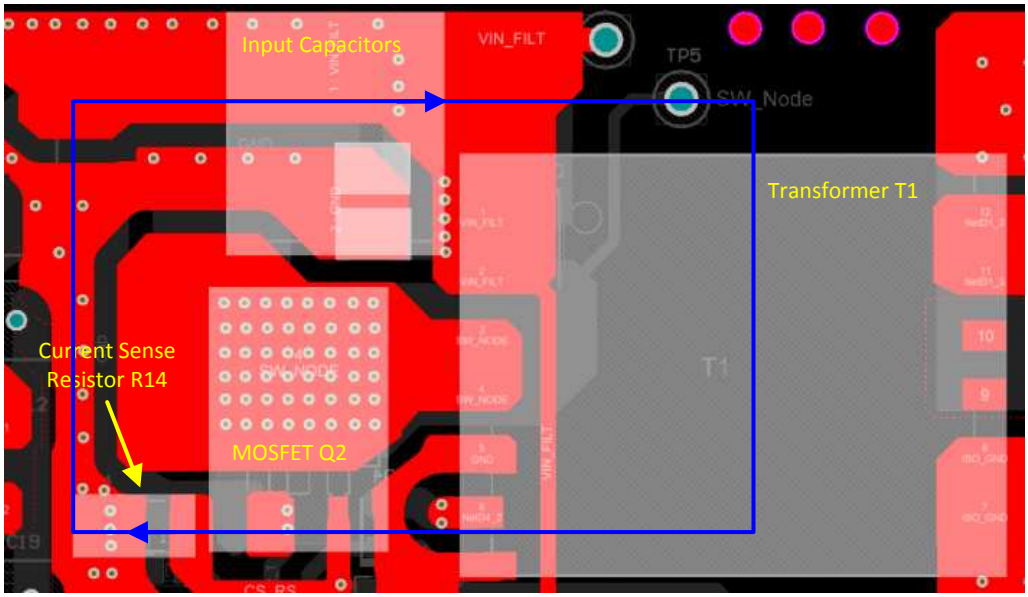


Figure 57. Current Flow Loop in Power Stage

Figure 58 shows the gate driving loop of the flyback converter. The loop starts from the Vcc capacitor C13, controller IC, gate resistor R7, MOSFET Q2, current sense resistor R14, ground plane, and then back to the Vcc capacitor C13.

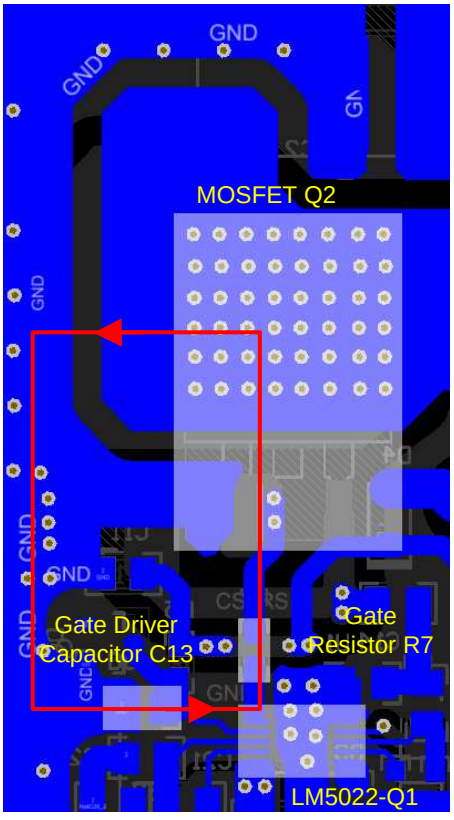


Figure 58. Gate Driver Current-Flowing Loop

Figure 59 shows the placement of the compensation network components. The components are placed at the same side of the controller and as close as possible to the controller.

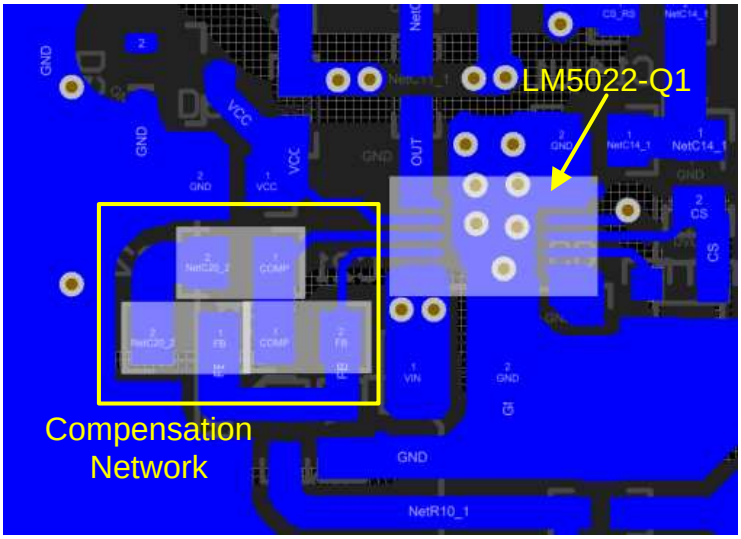


Figure 59. Compensation Network

Figure 60 and Figure 61 show the placement of the RC filtering network for the LM5022-Q1 current sense pin. The path is kept as short as possible and the filtering components are placed as close as possible to the chip.

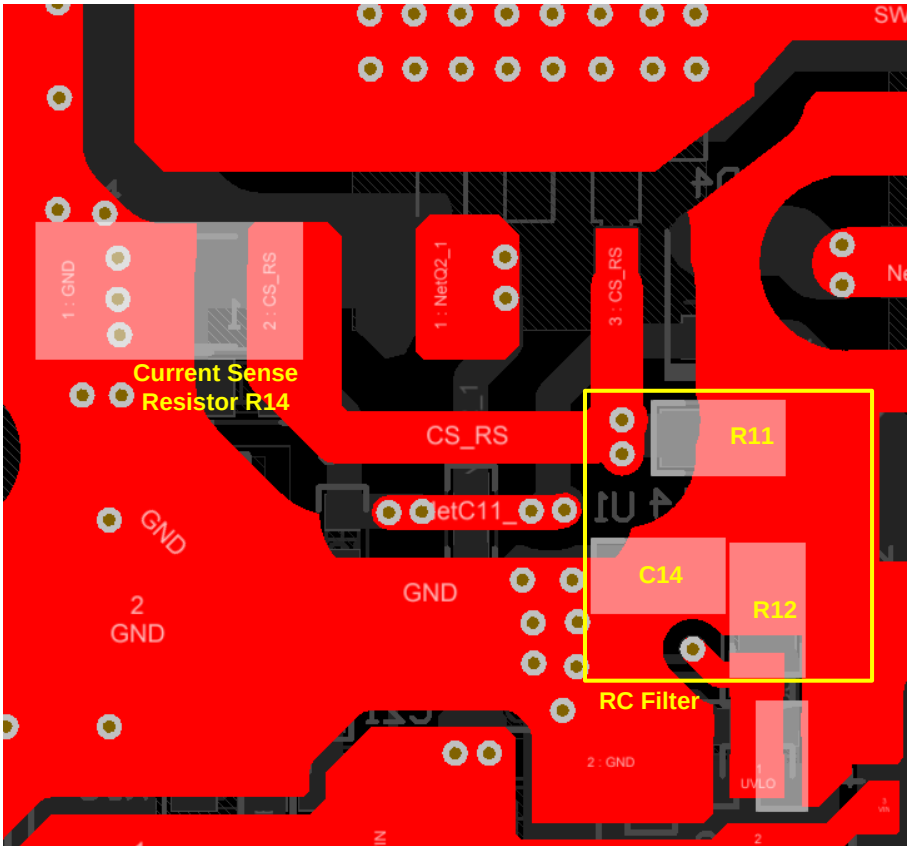


Figure 60. Placement of the RC Filtering Network for LM5022-Q1 Current Sense Pin (Top-Side PCB)

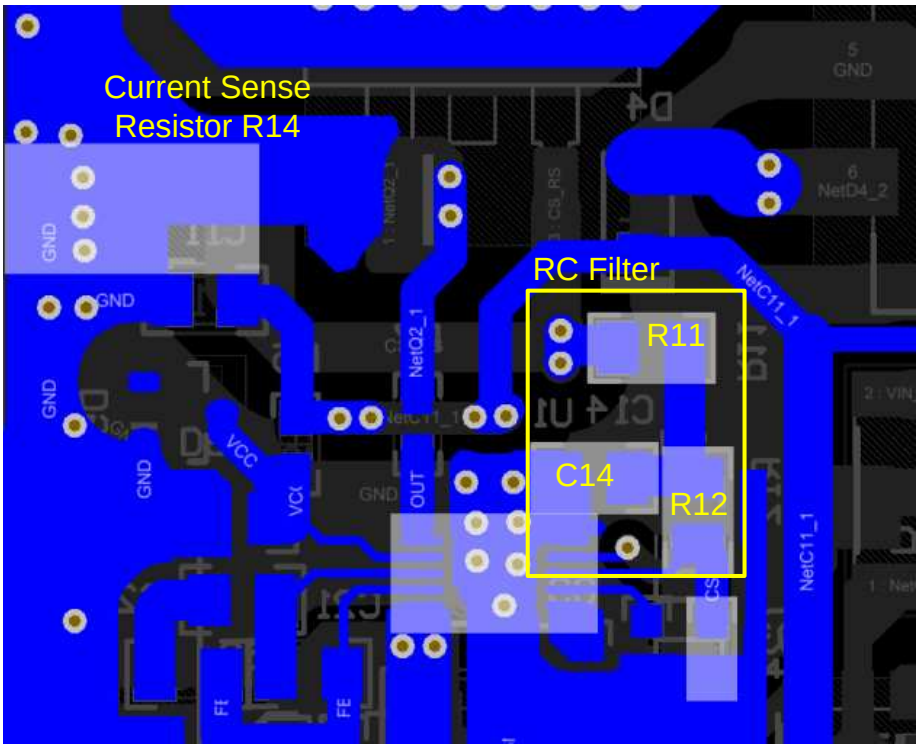


Figure 61. Placement of RC Filtering Network for LM5022-Q1 Current Sense Pin (Bottom-Side PCB)

5.4 Altium Project

To download the Altium project files, see the design CAD files at TIDA-01344.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01344.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01344.

6 Related Documentation

1. Texas Instruments, *Automotive VIN Front-End Power Reference Design With Cold Crank Operation and Transient Protections*, TIDA-01179 Reference Design (TIDUC53)
2. Texas Instruments, *AN-2162 Simple Success With Conducted EMI from DC-DC Converters*, Application Report (SNVA489)
3. Texas Instruments, *AN-2155 Layout Tips for EMI Reduction in DC / DC Converters*, Application Report (SNVA638)
4. IEC, CISPR 25: *Limits and methods of measurement of radio disturbance characteristics for protection of receivers used on board vehicles*, Second Edition 2002-2008

6.1 Trademarks

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7 Terminology

AFE – Analog front end

AEC – Automotive Electronics Council

ESR – Equivalent series resistance

EMI – Electromagnetic interference

EMC –Electromagnetic compatibility

DM – Differential mode

CM – Common mode

UVLO – Undervoltage Lockout

MOSFET – Metal-oxide semiconductor field-effect transistor

CISPR – International Special Committee on Radio Interference

PE – Protective earth

EMS – Root mean square

ISO – International Organization for Standardization

BOM –Bill of material

OEM –Original equipment manufacturer

AN –Artificial network

LISN – Line impedance stabilization network

EUT – Equipment under test

PCB – Printed-circuit board

HEV –Hybrid electric vehicle

EV –Electric vehicle

8 About the Author

XUN GONG is an Automotive Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the automotive segment in power train applications. Xun brings to this role his extensive experience in the field of IGBT and SiC (Silicon Carbide) power transistors, EMI and EMC in motor drives, and DC-DC converters. Xun achieved his Ph.D. in electrical engineering from Delft University of Technology in Delft, Netherlands. Xun Gong won the FirstPrize Paper Award of the IEEE Transactions on Power Electronics in the year of 2014.

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