TI Designs: TIDA-01410
Phase Synchronization of Multiple PLL Synthesizers Reference Design

Description

Many applications require two or more outputs of the same frequency with an adjustable phase relationship. Examples include clocking multiple data converters, beam steering, and smart antennas. The TIDA-01410 design uses two LMX2594 synthesizers to generate two phase-coherent outputs with very-fine phase adjustment capability. The LMX2594 allows a very wide range of adjustability in frequency from 10 MHz to 15 GHz. Having multiple devices is a good approach where the output signals may be far apart on the printed-circuit board (PCB) and when a designer wants to avoid routing high-frequency signals across long distances on the PCB.

Resources

TIDA-01410	Design Folder
LMX2594	Product Folder
PLLATINUMSIM-SW	PLLatinum Simulation Software
TICSPRO-SW	TICSPro Software

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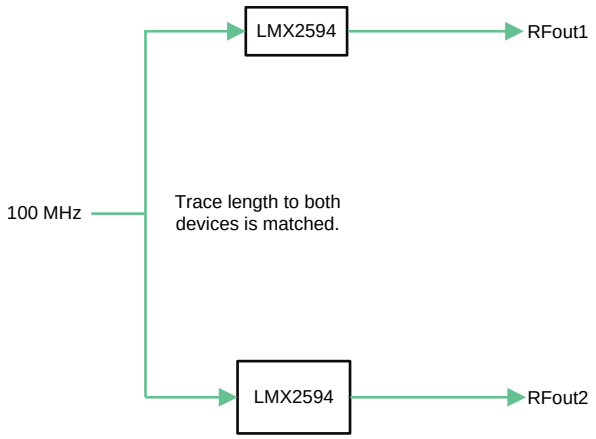
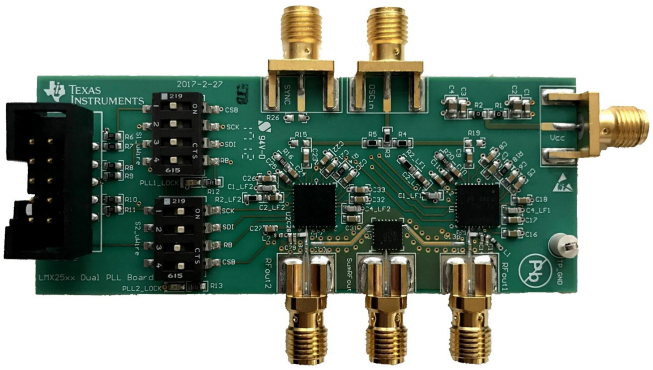
Features

- Output Frequency Range from 10 MHz to 15 GHz
- Input Clock Frequency from 5 MHz to 1400 MHz
- Coherent and Adjustable Output Phase

Applications

- Wireless Communications Tester
- Semiconductor Tester
- Signal Generators
- Functional/Arbitrary Waveform
- Oscilloscopes
- Spectrum Analyzers
- Vector Signal Analyzers
- Network Analyzers
- RADAR
- Munitions and Targeting





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1 System Description

The TIDA-01410 design uses two LMX2594 synthesizers to generate two phase coherent outputs locked to the same input reference. Both phase-locked loops (PLLs) have identical routing so that the phase can be controlled. The devices can be synchronized thorough software or pin. The synthesizers can be programmed independently or together by using the programming switches on the board.

Phase synchronization between two PLL synthesizers is very useful for many applications. One such application is test equipment that uses multiple data converters for higher performance. Having clocks with that are high frequency with coherent and adjustable phase are required to clock these converters and allows them to be interleaved for higher performance. This technique is relevant for wireless communication testers, semiconductor testers, functional and arbitrary waveform generators, oscilloscopes, spectrum analyzers, signal analyzers, and network analyzers. Other applications may use two or more elements with adjustable phases for beam steering, smart antennas, and RADAR.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Output frequency range	10 MHz to 15 GHz
Input frequency range	5 MHz to 1400 MHz
Input voltage range	3.15 V to 3.45 V; 3.3-V nominal

Table 2. Loop Filter

PARAMETER	VALUE
VCO frequency	7.5 MHz to 15 MHz
Phase detector frequency	200 MHz
Charge pump gain	15 mA
Loop bandwidth	250 kHz
C1_LF	0.39 nF
C2_LF	68 nF
C3_LF	1.8 nF
R2_LF	68 Ω
R3_LF	18 Ω

The loop filter is designed for a 200-kHz phase detector frequency for optimal jitter. If the phase detector frequency requires a significant change, such as in a case when the channel divider is used (due to the extra division in the input path), then the loop filter remains stable and demonstrates the phase relationship. However, the loop filter should be redesigned if the designer wishes to optimize jitter.

2 System Overview

2.1 Block Diagram

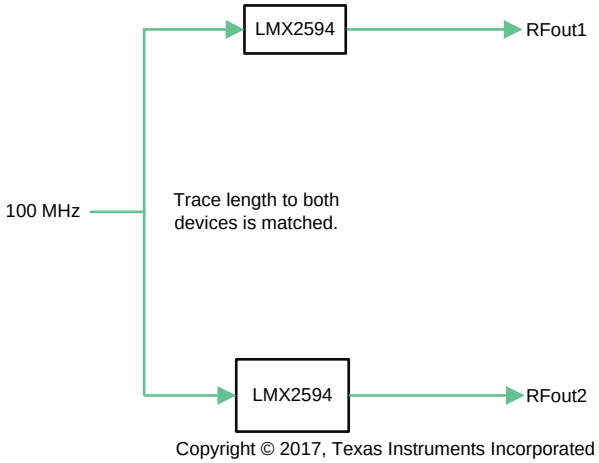

Figure 1. TIDA-01410 Block Diagram

2.2 System Design Theory

The TIDA-01410 reference design features two LMX2594 devices that are capable of demonstrating the use of two synthesizers to generate two outputs that are coherent but adjustable in phase. This design theory has two components: synchronization and phase adjustment. Synchronization involves setting up the devices to maintain the same phase relationship every time they are programmed or the power is cycled. Phase adjustment is the ability to adjust the phase, which is simply referred to as phase adjust.

One important consideration for synchronizing the LMX2594 device in phase is the treatment of the channel divider after the VCO. The approach of the LMX2594 is to include part of this divide inside the feedback loop (known as the IncludedChannelDivide) and then put the rest of the divide outside the loop. This included divide has implications to phase synchronization and phase shifting (see Table 3).

Table 3. IncludedChannelDivide

CHANNEL DIVIDER VALUE	IncludedChannelDivide
Bypass	1
6, 12, 48, 72, 96, 384, 768	6
All other values	4

2.2.1 Theory of Phase Synchronization

The first step in establishing two outputs to be phase coherent is to ensure that the phase relationship can be made to be the same every time. One thing that can cause the phase relationships to be different is if there are divides involved. For instance, whenever a signal is divide-by-two there are two possible output phases, which requires the designer to take action. If this divider is inside the PLL feedback loop (PLL_N), then the correct phase is always found by the PLL loop itself and no synchronization is required. However, if this divider is outside the loop, such as in the case of using the input divider (PLL_R), then the designer must provide a synchronization signal. This scenario also applies to the divider after the VCO (CHDIV). Synchronization may also be required when fractional circuitry is involved.

The key to synchronization is to provide a SYNC signal. This signal marks the specific edge of the input signal (OSCin) that is to be used. In some situations the timing of this signal is not critical, but it is still necessary to put the device in SYNC mode and send a pulse. This scenario is referred to as category 2. In other situations, the timing of this SYNC signal is critical. This scenario is referred to as category 3. Refer to the *LMX2594 High Performance, Wideband PLLatinum™ RF Synthesizer with Integrated VCO* datasheet[1] and the following Figure 2 for more details on the synchronization process.

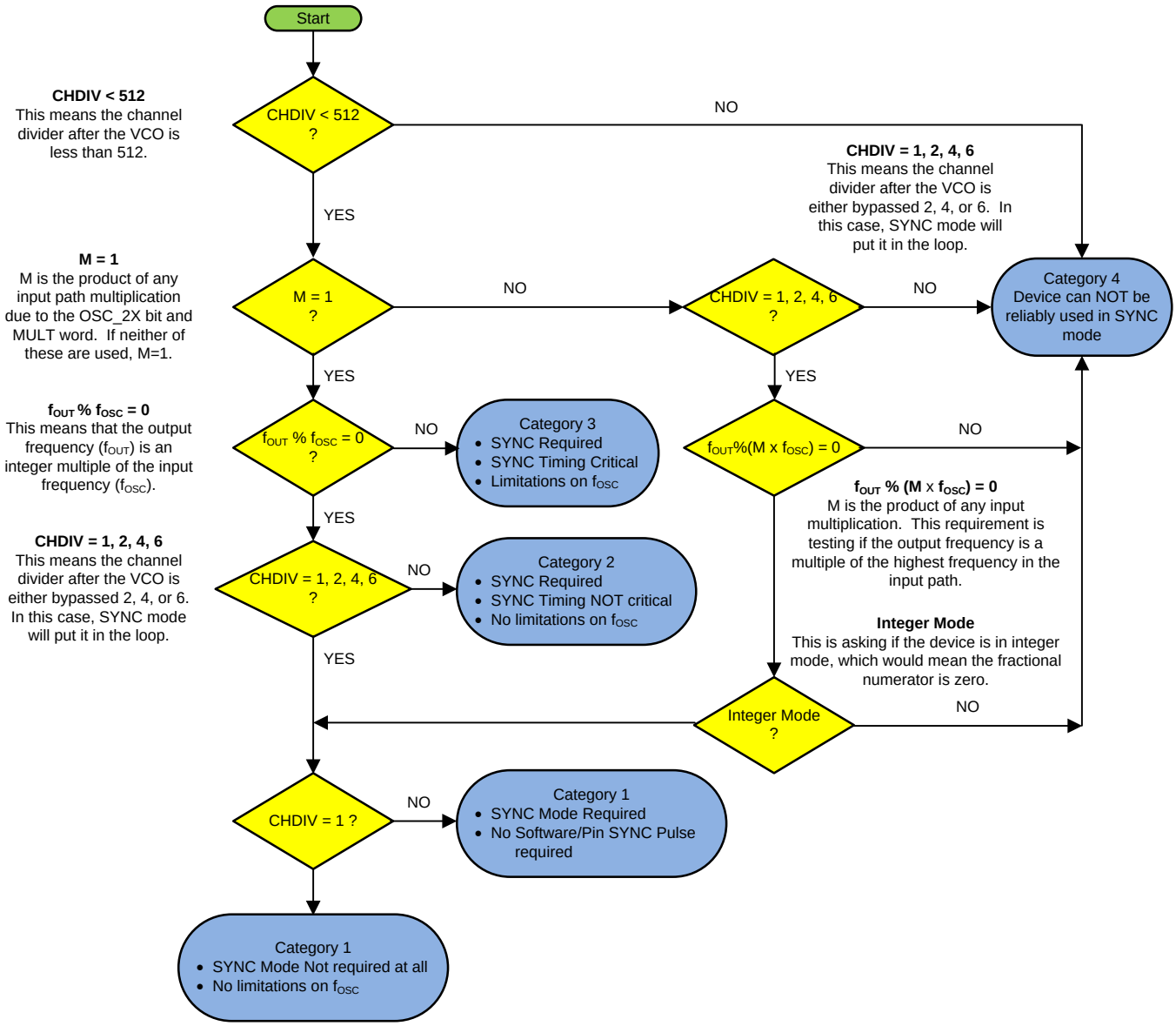

Figure 2. SYNC Categories Flow Chart

In the case that the output frequency is a multiple of the input frequency, the timing of this synchronization pulse is not critical, with the exception of where the fractional mode is used with MASH_SEED > 0. In the case of non-critical timing, sometimes no synchronization pulse is required and other times it is and can be done by toggling the VCO_PHASE_SYNC bit ("software sync"). In other cases of non-critical timing, the choice of which input clock rising edge is selected is important and this is referred to as a timing critical sync. The onboard SYNC SMA input can be used for a timing critical sync. This input can be driven with another device such as an LMK04828 or LMX2594 evaluation board to produce a SYNC signal that is far from the rising edge of the input reference clock. The board also allows connection of this SYNC input to the programmable header through resistor R26, which is good for debugging purposes. The SYNC pulse sent by the TICS Pro software is *not* synchronous to OSCin, but the setup is easy to proceed with as long as user is aware that TICS Pro may send the SYNC signal right on the rising edge of OSCin on rare occasions.

NOTE: If using the SYNC pin, be sure that the SYNC_IGNORE bit is disabled. If the SYNC_IGNORE bit is disabled, ensure that the SYNC input is not floating.

2.2.2 Theory of Phase Shift

After establishing the deterministic phase of the devices, the next task is enable phase shifting. The input and output traces are matched to reduce skew resulting from the board; however, there may still be some phase error introduced by differences in the delays through the components on these traces. The MASH_SEED word can be used to make fine adjustments for this phase error and remain the same for every power cycle. The phase adjustment due to this MASH_SEED is calculated using Equation 1:

$$\text{Delay (in degrees)} = \text{MASH\_SEED} \times \frac{(\text{IncludedChannelDivide})}{(\text{PLL\_DEN} \times \text{CHDIV})} \quad (1)$$

where,

- MASH_SEED is the programmed value for MASH_SEED
- IncludedChannelDivide is the portion of the channel divide that SYNC mode includes in the feedback loop (discussed further in the datasheet)
- PLL_DEN is the fractional denominator
- CHDIV is the channel divide value.

NOTE: If the SYNC pin or MASH_RST_N bit is toggled, the seed value in the accumulator is MASH_SEED. However, if the MASH_SEED value is programmed, this value is added to the value in the accumulator. For instance, if the user presses the ENTER key with the cursor in the MASH_SEED box in TICS Pro, the phase increments each time.

When the device is in SYNC mode (VCO_PHASE_SYNC = 1), part of the channel divider may be put in the feedback loop. The part of the divider that is included is the IncludedChannelDivide.

NOTE: The fractional denominator, PLL_DEN, must be a factor of the IncludedChannelDivide if MASH_SEED > 0.

Phase shifting *is* possible for integer values of N. In this case, the device is still in fractional mode, but the numerator is zero. Some freedom of choice exists for choosing the denominator, but there is a strategy. Programming non-zero seed values can actually produce fractional spurs with a numerator of zero. Therefore, optimal spurs are obtained when MASH_SEED is a multiple of IncludedChannelDivide and the fractional denominator is set to k × IncludedChannelDivide, where k is a positive integer that has no factors of 2 or 3. Sub-fractional spurs can be avoided using this strategy. For example, if the channel divide is 4 then IncludedChannelDivide would be 4. Good choices for the fractional denominator would be 4, 20, 28, 44, 52, 68, and so forth. If MASH_SEED is incremented in steps of IncludedChannelDivide, then there are no resulting sub-fractional spurs. MASH_SEED can still be incremented in smaller increments; however, the sub-fractional spurs are still present despite being minimal.

2.3 Highlighted Products

2.3.1 LMX2594

The LMX2594 is a high-performance, wideband PLL with integrated VCOs that can generate any frequency from 10 MHz to 15 GHz without using an internal doubler, which eliminates the requirement for sub-harmonic filters. The high performance PLL with a –236-dBc/Hz figure of merit and high phase detector frequency can attain very low in-band noise and integrated jitter. The high speed N-divider has no pre-divider, thus significantly reducing the amplitude and number of spurs. The device also has a programmable input multiplier to mitigate integer boundary spurs. The LMX2594 allows users to synchronize the output of multiple devices and also enables applications that require deterministic delay between input and output. A frequency ramp generator can synthesize up to two segments of ramp in an automatic ramp generation option or a manual option for maximum flexibility. The fast calibration algorithm allows changing frequencies faster than 20 μs. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard), which makes it an ideal low-noise clock source for high-speed data converters. Fine delay adjustment (9-ps resolution) is provided in this configuration to account for delay differences of board traces. The output drivers within LMX2594 deliver output power as high as 7 dBm at a 15-GHz carrier frequency. The device runs from a single 3.3-V supply and has integrated low-dropout (LDOs) regulators that eliminate the requirement for onboard LDOs.

3 Getting Started Hardware and Software

3.1 Hardware Setup

Figure 3 shows an outline of the hardware setup.

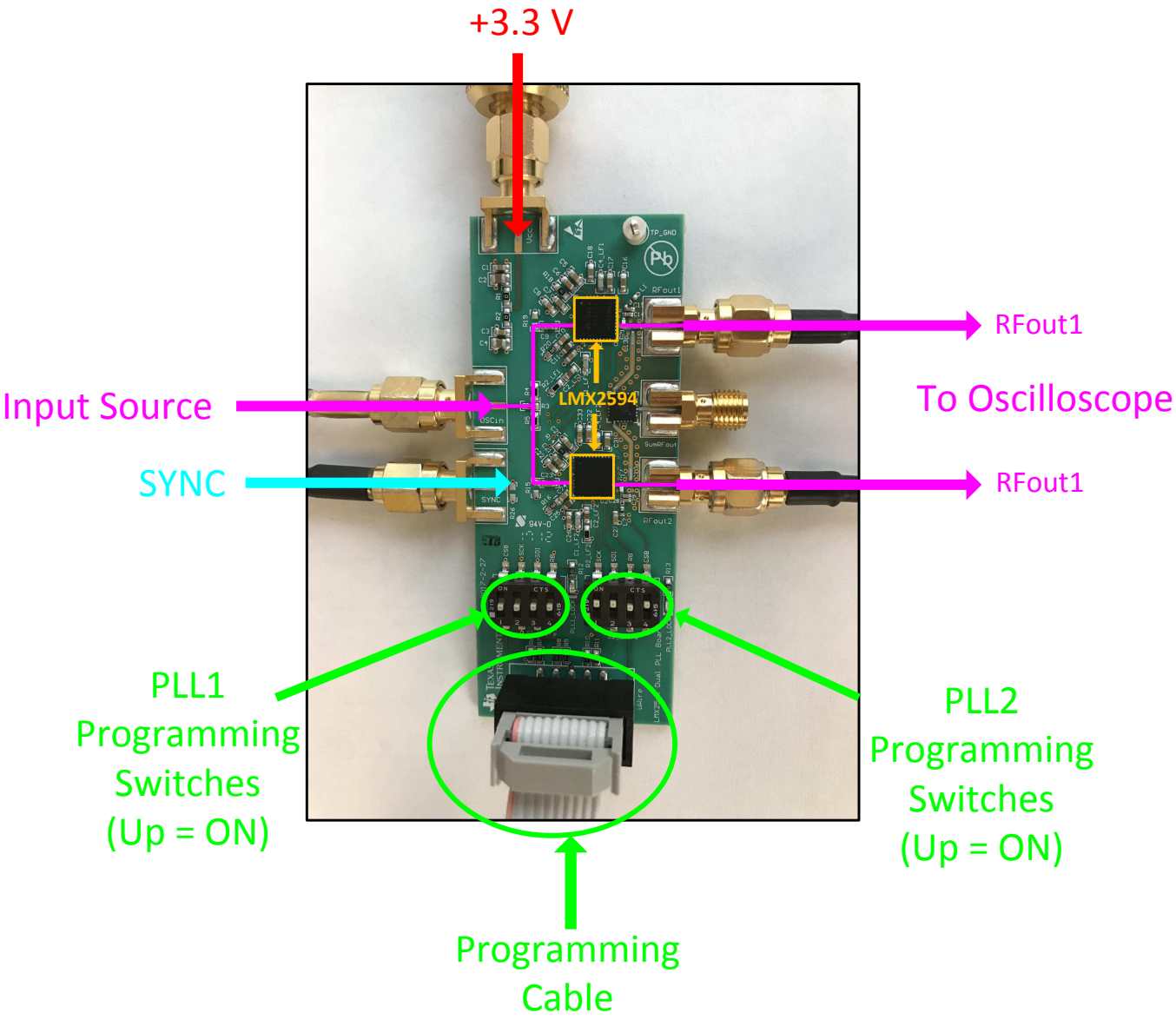

Figure 3. Hardware Setup

3.1.1 Power

Set the power supply to 3.3 V and connect this to the Vcc input SMA. Set the current limit to 1 A.

3.1.2 Input Signal

Connect the input signal to the OSCin SMA. A 100-MHz input signal has been used to obtain the test results in this reference design. Simply use a signal source if a timing critical SYNC is not required; however, if a timing SYNC is required, then consider using something that can produce a SYNC pulse that occurs on the rising edge of the input clock, such as the LMX2594 board (using RFoutB as SYSREF) or the LMK04828 EVM.

If using a noisy signal source, such as a signal generator, be aware that this can dominate close-in phase noise.

3.1.3 Output Signal

Connect the RFout1 and RFout2 outputs to an oscilloscope. Ensure that C13 and C30 are in place and that C13p and C30p are open.

3.1.4 Programming Interface

Connect the laptop to the board using the USB2ANY or ReferencePro interface. For more details, refer to the *LMX2594 EVM Instructions – 15-GHz Wideband Low Noise PLL With Integrated VCO* user's guide[2] to use the TICS Pro graphical user interface (GUI) for programming.

3.2 Programming Switches

This reference design has two banks of switches, one for each LMX2594 synthesizer. Each set of switches has four switches for CSB, SCK, SDA, and MUXout and all four switches in the set should be either ON or OFF altogether. If both sets of switches are ON, then both devices are programmed to the same setting. However, if the designer wants to program the synthesizers to different settings, as would be the case when using MASH_SEED, then the switches on one of the devices can be turned OFF so that the other device is not programmed. With this set of instructions using switches, a single programming interface can be used to program both devices.

3.3 Software

3.3.1 Download Texas Instruments Clock and Synthesizers (TICS) Pro Software

1. Download the TICS Pro Software from TI.com: http://www.ti.com/tool/TICSPRO-SW.
2. To start the software, open the *TICS PRO.exe* from the installed directory.

4 Testing and Results

4.1 Test Setup

The following test results were obtained using an 8-GHz oscilloscope and the test setup in Figure 4. The skew between channel 1 and channel 2 has been adjusted to de-skew the signals for the initial setup, but remain unchanged.

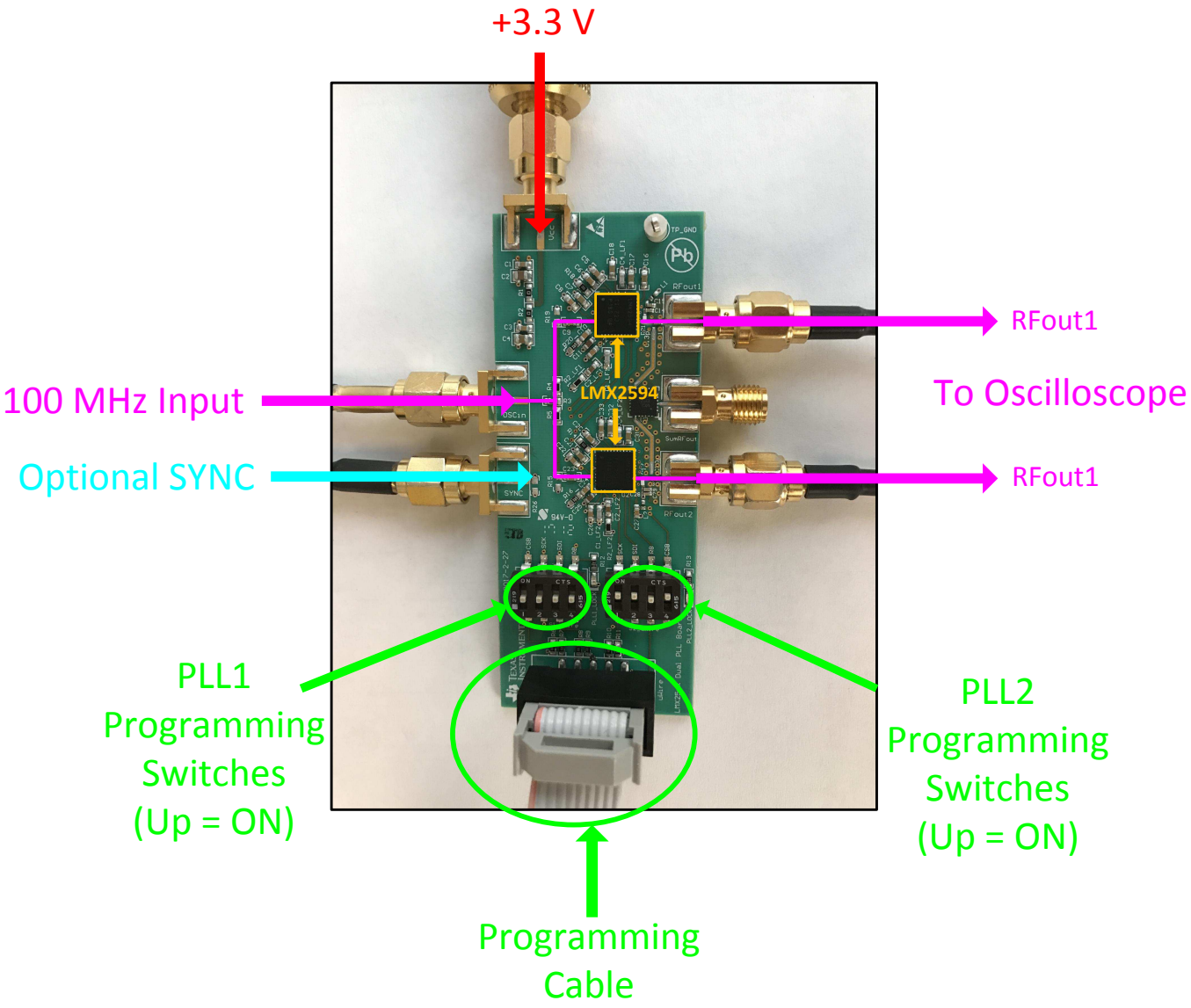

Figure 4. Test Setup

4.2 Test Data

4.2.1 Non-Critical TimingSYNC Example

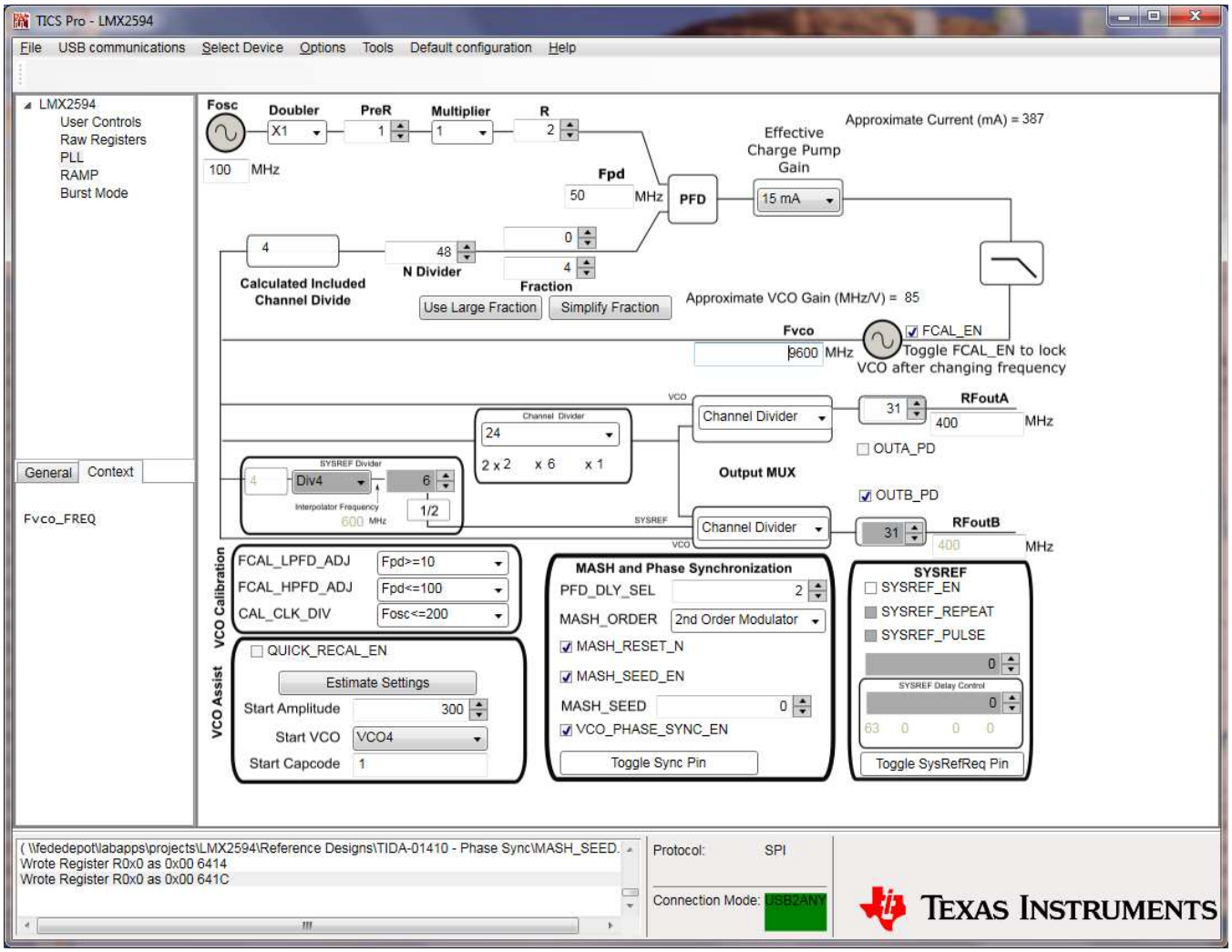

Figure 5. TICSPro Software Setup for Non-Critical Timing Case

The following figures show the results before (Figure 6) and after (Figure 7) VCO_PHASE_SYNC_EN is toggled.

Figure 6. Non-Timing Critical Example Before SYNC Pulse

Figure 7. Non-Critical SYNC Example After SYNC Pulse

4.2.2 Phase Shift Using MASH_SEED

Using the setup in Figure 5 a starting point, the MASH_SEED word can be used to shift the phase. In this case, the SYNC is not timing critical because the output frequency is a multiple of the input frequency. The fractional denominator is 4, the included channel divide is 4, and the channel divide is 24; therefore, the designer can determine that each increment in the MASH_SEED represents a phase shift of: 360 × 4 / (4 × 24) = 15º. So incrementing the MASH_SEED by 6 represents a 90° phase shift, which was the measured result. The oscilloscope was triggered on the PLL that was not shifted and the increment in the MASH_SEED caused a delay, which effectively causes a phase shift to the left. The MASH_RST_N bit was toggled each time the seed was changed, which can also be achieved with the SYNC pin. Note that when MASH_SEED = 6 or 18, there are sub-fractional spurs, but they are very low and far from the carrier (see Figure 8).

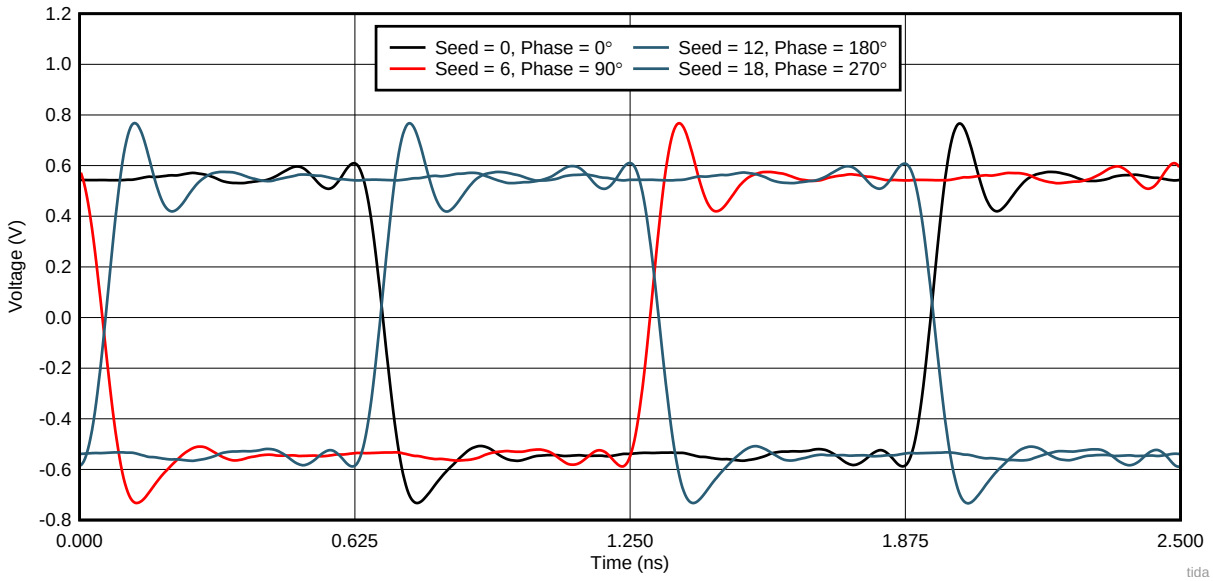

Figure 8. Phase Shift Using MASH_SEED

4.3 Timing Critical SYNC Example

In this example, the output frequency is clearly not a multiple of the input frequency, which means the timing of the SYNC pin is critical (see Figure 9).

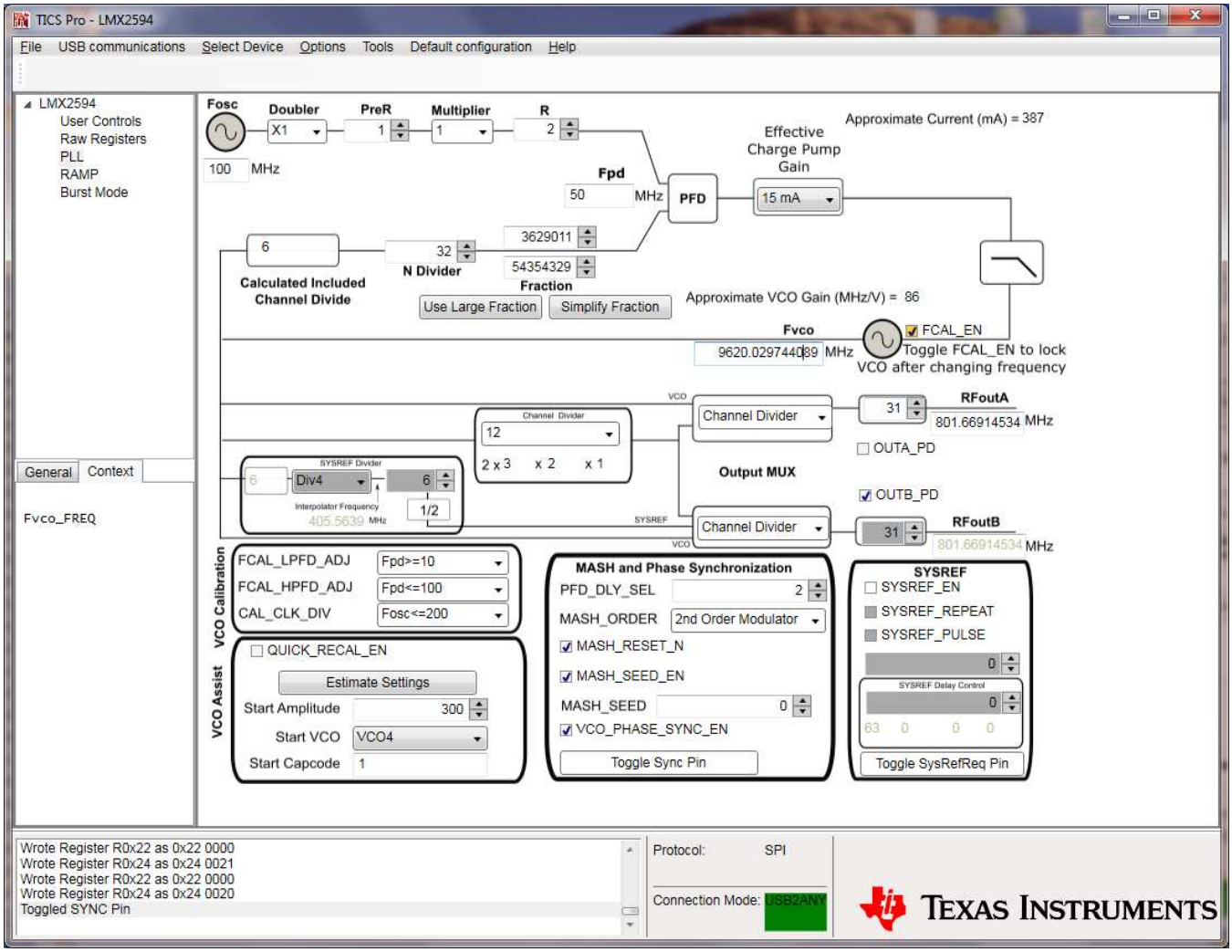

Figure 9. Timing Critical Setup Example

Figure 10. Timing Critical Example before SYNC

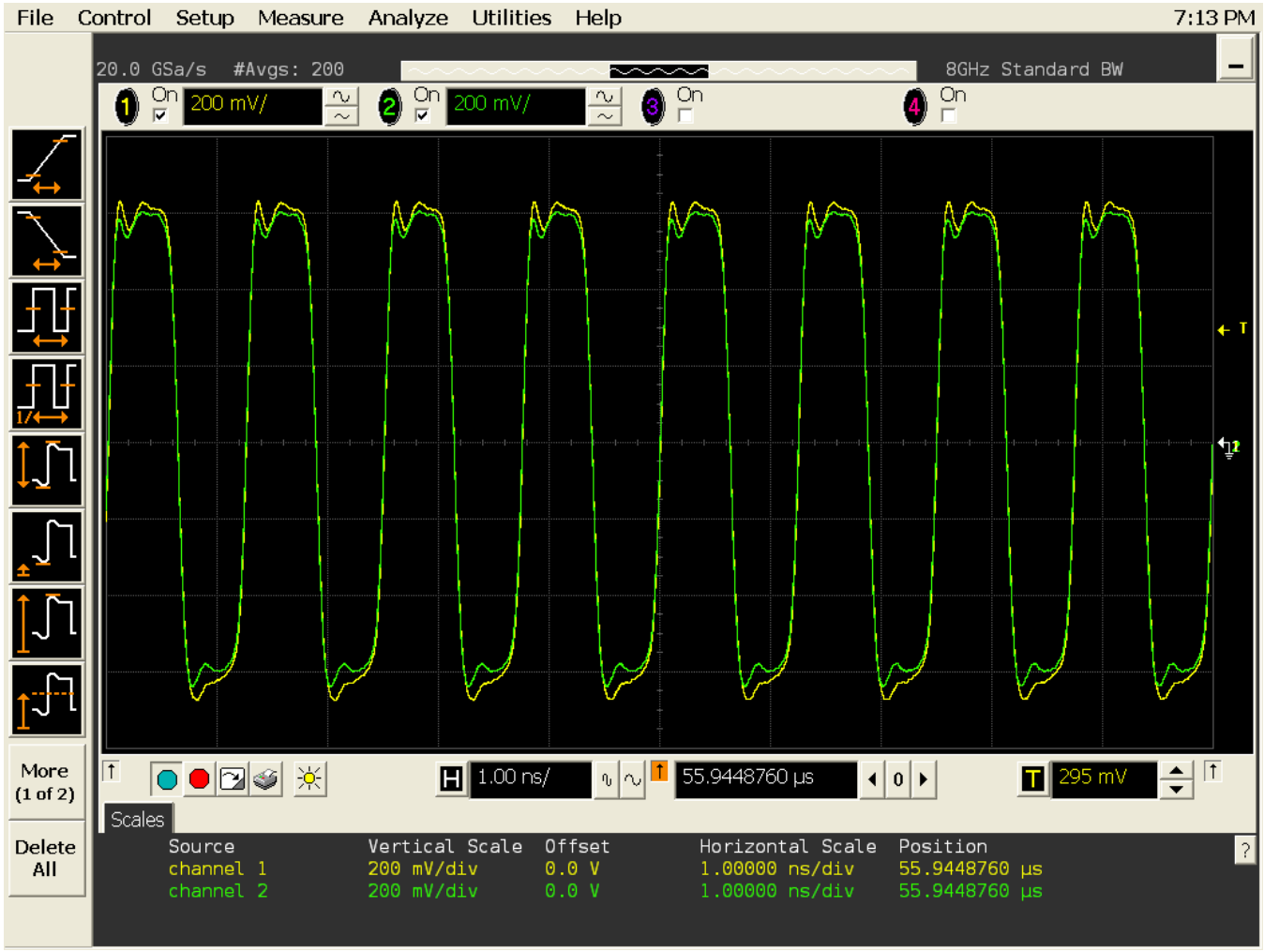

Figure 11. Timing Critical Example After SYNC

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01410.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01410.

5.3 PCB Layout Recommendations

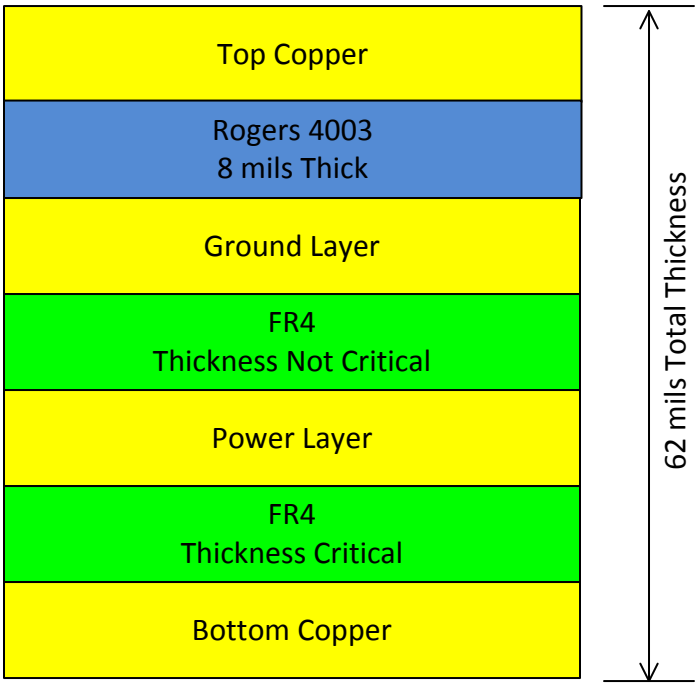

Figure 12. TIDA-01410 Layer Stack Up Information

Rogers 4003 was chosen for high-frequency performance.

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01410.

5.3.2 Layout Guidelines

Overall, the layout guidelines are similar to most other PLL devices. The following guidelines list the ideal layout:

- Place output pull-up components close to the pin.
- Ensure that the input signal trace is well-matched.
- For the routing of the outputs, single-ended is chosen so that trace lengths can be kept short and equal length. Pullup components should be as close to the pin as possible. The unused side was sent to the back side of the board through a via with the loading symmetrical to the used side.

Figure 13 shows an example layout of the LMX2594 board.

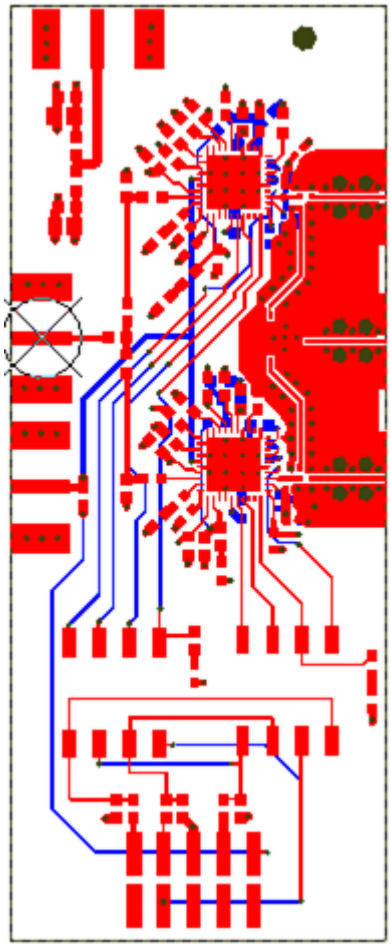

Figure 13. LMX2594 Layout Example

For more information, see the LMX2594 Datasheet[1] and the LMX2594EVM User's Guide[3].

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01410.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01410.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01410.

6 Software Files

To download the software files, see the design files at TIDA-01410.

7 Related Documentation

1. Texas Instruments, *LMX2594 High Performance, Wideband PLLatinum™ RF Synthesizer with Integrated VCO*, LMX2594 Datasheet (SNAS646)
2. Texas Instruments, *LMX2594 EVM Instructions – 15-GHz Wideband Low Noise PLL With Integrated VCO*, LMX5294EVM User's Guide (SNAU210)
3. Texas Instruments, *LMX2594EVM High Performance, Wideband PLLatinum™ RF Synthesizer Evaluation Board Operating Instructions*, LMX2594EVM User's Guide (SNAU195)
4. Texas Instruments, *WEBENCH® Design Center*, (http://www.ti.com/webench)

7.1 Trademarks

8 About the Author

DEAN BANERJEE is an applications engineer with Texas Instruments working with PLL synthesizers and is the author of *PLL Performance, Simulation, and Design*.

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