TI Designs: PMP20176

Four-Phase, 140-A Reference Design for Intel® Stratix® 10 GX FPGAs Using TPS53647

Description

This reference design focuses on providing a compact, high-performance, multiphase solution suitable for powering Intel®Stratix® 10 GX FPGAs with a specific focus on the 1SG280-1IV variant. Integrated PMBus™ allows for easy output voltage setting and telemetry of key design parameters. The design enables programming, configuration, smart VID adjustment, and control of the power supply, while providing monitoring of input and output voltage, current, power, and temperature. TI's Fusion Digital Power™ Designer is used for programming, monitoring, validation, and characterization of the FPGA power design.

Resources

PMP20176	Design Folder
TPS53647	Product Folder
CSD95472Q5MC	Product Folder
Fusion Digital Power Designer	Product Folder

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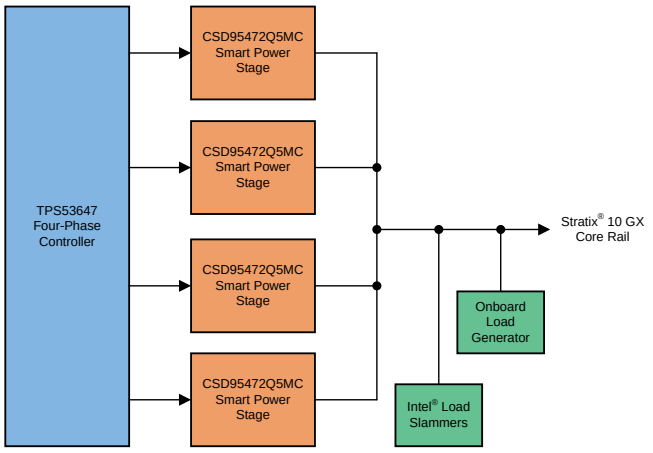
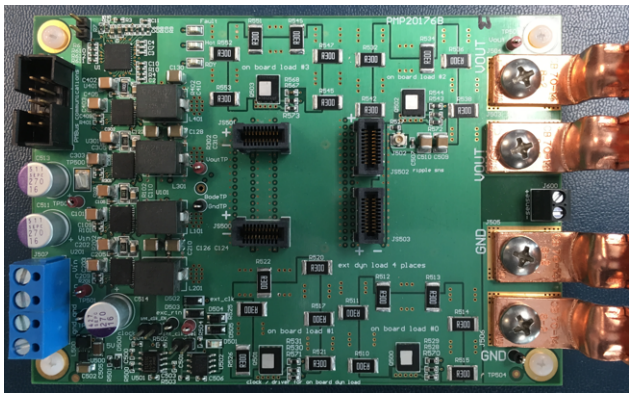
Features

- All Ceramic Output Capacitors
- D-CAP+™ Modulator for Superior Current-Sharing Capabilities and Transient Response
- Peak Efficiency of 91.5% at 400 kHz, V_{IN} = 12 V, V_{OUT} = 0.9 V, I_{OUT} = 60 A
- Excellent Thermal Performance Under No Airflow Conditions
- Overvoltage, Overcurrent, and Overtemperature Protection
- PMBus Compatibility for Output Voltage Setting and Telemetry for V_{IN}, V_{OUT}, I_{OUT}, and Temperature
- PMBus and Pinstrapping Programming Options

Applications

- FPGA Core Rail Power
- Ethernet Switches
- Firewalls and Routers
- Telecom and Base Band Units
- Test and Measurement





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

The PMP20176 is a high-efficiency, power-dense design featuring a four-phase buck controller and TI's proprietary Smart Power Stages optimized for use in Intel® Stratix® 10 GX FPGA core rail applications. These FPGAs are typically used in enterprise switching, telecom infrastructure, test and measurement, and cloud computing infrastructure environments with high utilization percentages that call for the high current and fast transient response that this design provides.

A 400-kHz switching frequency maintains a thermal design current efficiency of 90.1% while a high crossover frequency of 149 kHz produces a fast transient response with no stability issues. The TPS53647 controller uses the D-CAP+™ multiphase modulator for fast transient response capabilities and tight regulation of the output voltage. The D-CAP+ modulator offers reliable current balancing between the four phases of the design that provide stability over a wide range of operating conditions and simple type-II compensation of the control loop. Additionally, the TPS53647 is compatible with TI's Smart Power Stages, such as the CSD95472 used in this design, which offer optimized driver-FET solutions for high efficiency and integrated current-monitoring circuitry. These smart power stages are responsible for saving layout area and eliminating the requirement for external current-sensing components.

Design modifications can be made in the WEBENCH® Designer if a lower-power Stratix 10 GX FPGA is used, or a different output capacitor mix is desired.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input supply	12 V ±10%
Nominal output voltage	0.9 V
DC regulation	<1.2%
DC ripple	2% max
AC ripple	±5%
Maximum output current	140 A
Thermal design current	100 A
Maximum load step	75 A at 500 A/µs
Number of phases	Four
Switching frequency	400 kHz

2 System Overview

2.1 Block Diagram

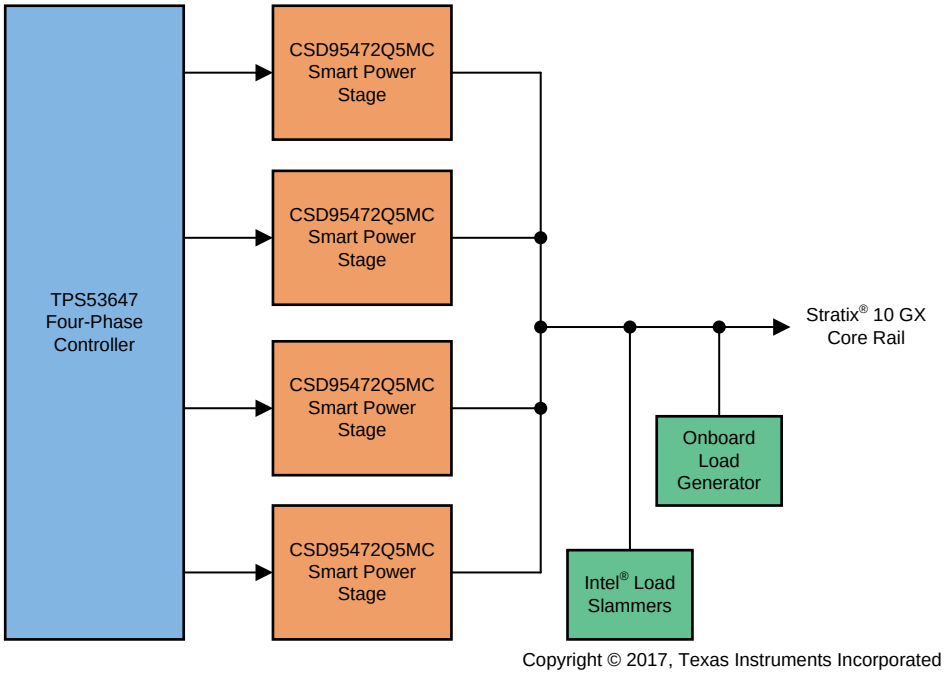


Figure 1. PMP20176 Block Diagram

2.2 Highlighted Products

2.2.1 TPS53647 – Four-Phase, D-CAP+™ Step-Down Buck Controller With NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load

Features:

- 8-bit selectable boot voltage through pinstrap or non-volatile memory (NVM)
- One-, two-, three-, or four-phase operation
- 1.8-V or 3.3-V compatible PMBus™ system interface for fault monitoring and voltage, current, power, and temperature telemetry
- D-CAP+ modulator and eight independent levels of overshoot and undershoot reduction for excellent transient response
- Adjustable voltage positioning
- Dynamic phase shedding with programmable current threshold
- 6×6-mm, 40-pin, QFN PowerPAD™ integrated circuit package

2.2.2 CSD95472Q5MC – 60-A Synchronous Buck NexFET™ Smart Power Stage With DualCool™Package

Features:

- 60-A continuous current capability
- Low power loss of 2.3 W at 30 A
- High-frequency operation up to 1.25 MHz
- 3.3-V and 5-V pulse-width modulation (PWM) compatible
- Temperature-compensated bidirectional current sense
- Analog temperature output
- Integrated bootstrap diode and optimized deadtime
- 5-mm × 6-mm SON, low inductance, DualCool™ packaging

3 Getting Started Hardware and Software

3.1 Hardware

The hardware for the design is as follows:

- 12-V supply capable of 20 A
- 5-V supply capable of 1 A
- Function generator capable of pulses with < 1-µs rise times (optional)
- Oscilloscope with differential and passive probes
- Digital multimeter
- Three 25-A Intel Mini Load Slammers and associated control board (optional)

The function generator must be used if the onboard clock generator is not used to drive the onboard load transient generator. Intel mini load slammers can be used in place of the entire onboard load circuitry if desired.

3.2 Software

This design uses TI's Digital Fusion Power Designer software.

3.3 Test Setup

Figure 2 shows the PMP20176 test setup.

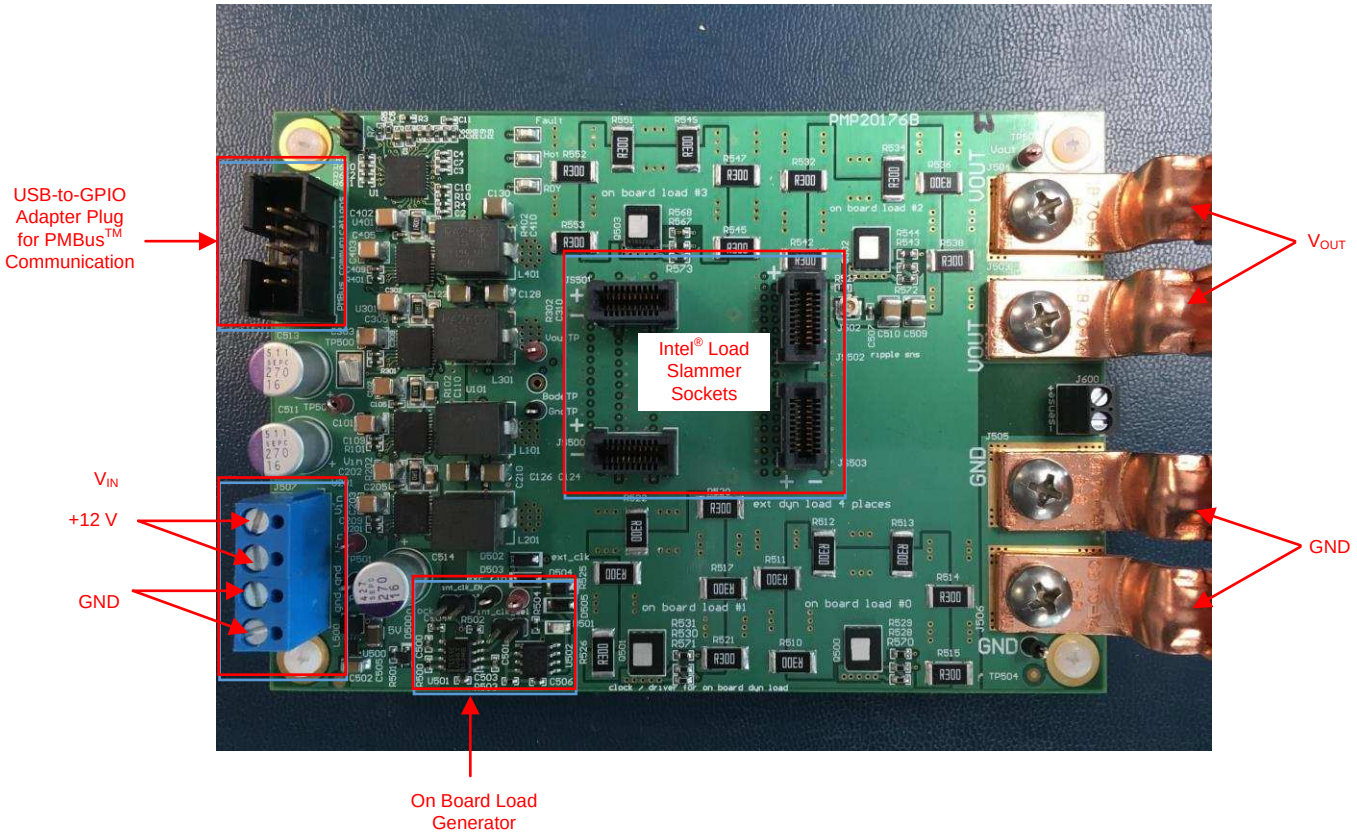


Figure 2. PMP20176 Test Setup

4 Test Results

4.1 Efficiency and Power Loss

Peak efficiencies of 91.9% (V_{IN} = 10.8 V), 91.5% (V_{IN} = 12 V), and 91.1% (V_{IN} = 13.2 V) have been measured for this design, as Figure 3 shows. At a thermal design current (TDC) of 100 A, the efficiencies were 90.3%, 90.1%, and 89.9% for V_{IN} = 10.8 V, 12 V, and 13.2 V, respectively. When the load current is set to the maximum current of 140 A, the efficiency is 87.8% for V_{IN} = 10.8 V, 87.7% for V_{IN} = 12 V, and 87.6% for V_{IN} = 13.2 V. The curve in Figure 3 and Figure 4 includes the losses associated with the 5-V power stage VDD rail as well as the power losses associated with the inductors of each phase.

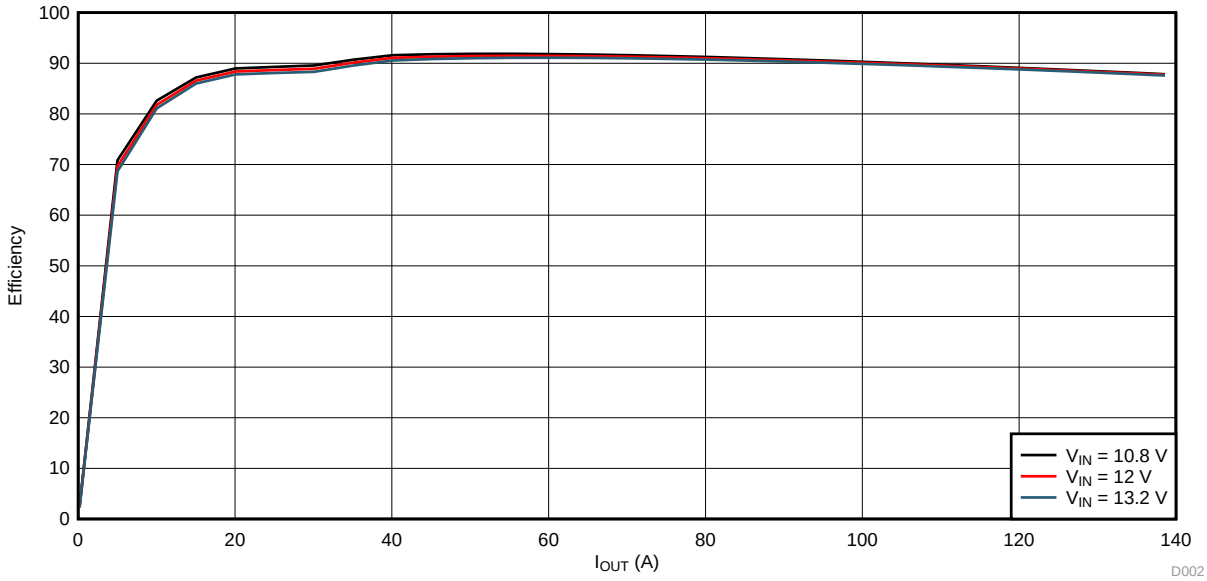


Figure 3. PMP20176 Efficiency Curves: V_{OUT} = 0.9 V, 400 kHz

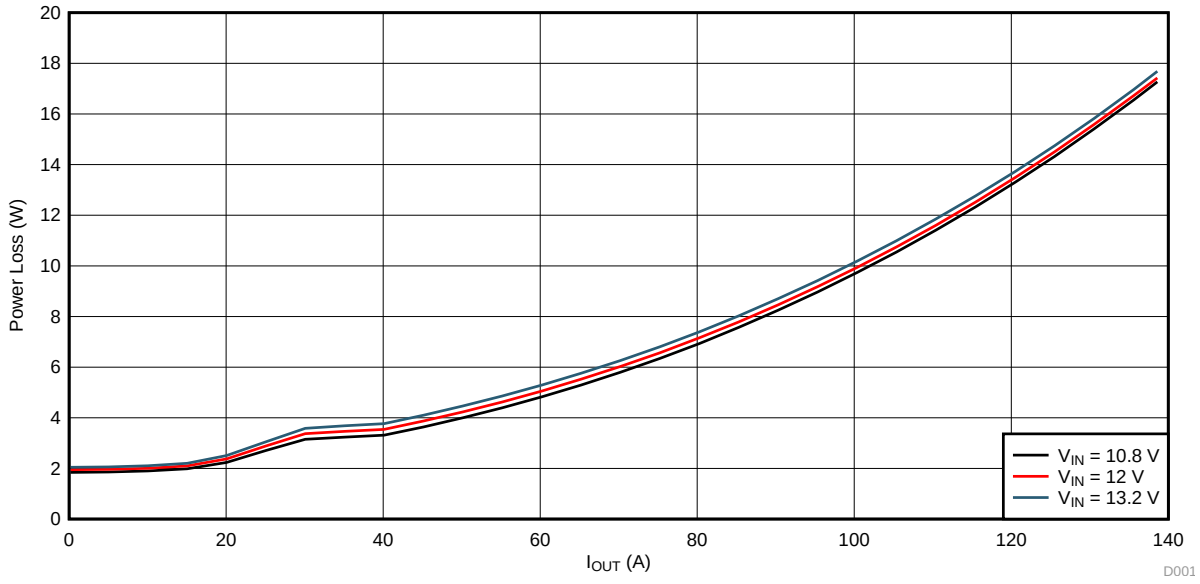


Figure 4. PMP20176 Power Loss Curves: V_{OUT} = 0.9 V, 400 kHz

4.2 Phase Ringing and Loop Stability

To ensure that the power MOSFETs inside the CSD95472 are not being damaged during normal operation, the phase nodes are probed at various output currents to ensure that any ringing is safely within the data sheet limits. No anomalies were observed during testing and Figure 5 shows one such measurement with the load current set to 40 A. A peak voltage of 20.7 V with a duration of < 10 ns is measured, which places the ringing safely within the data sheet limits. Figure 6 provides the results for measuring the switching frequency and shows it to be within the data sheet limits with no double pulsing or excessive jitter, which indicate that the system is stable.

To check the stability further, the control loop bode plot is obtained using a network analyzer with 49° of phase margin being measured at the 149-kHz unity gain frequency (see Figure 7).

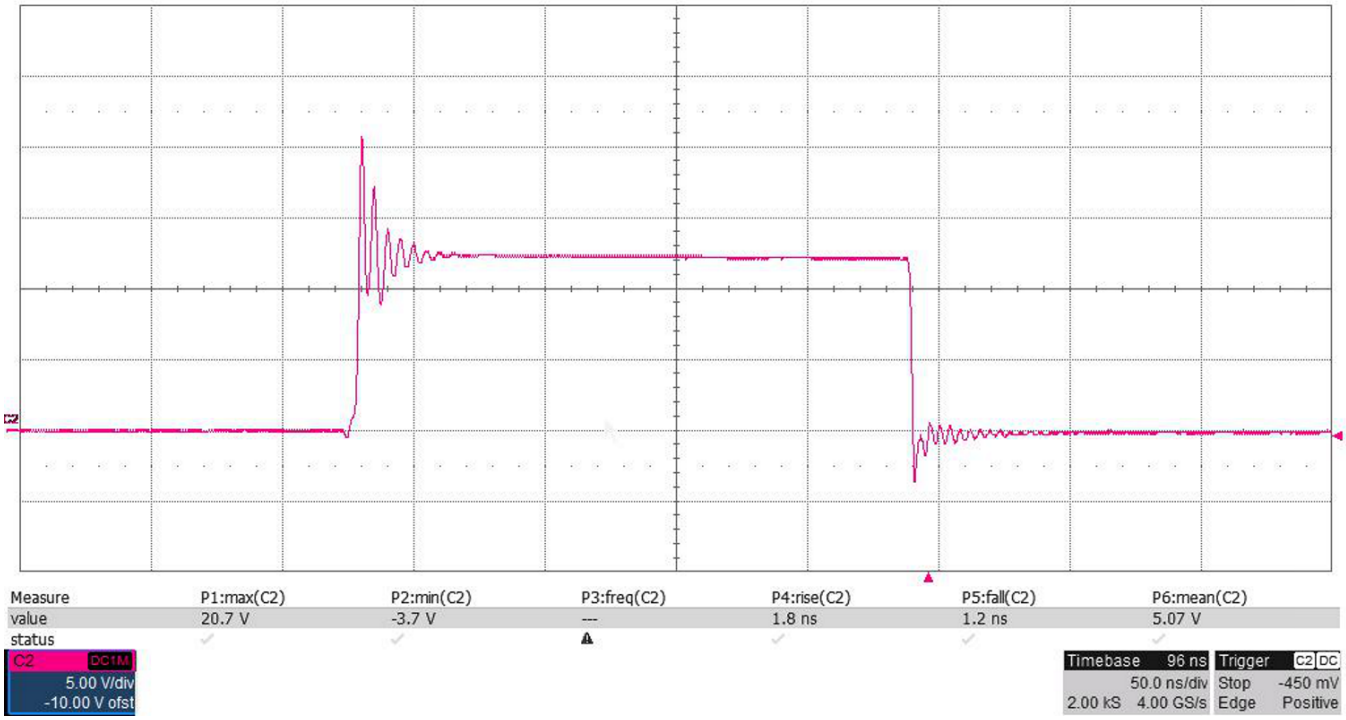


Figure 5. Phase Node Ringing With 40-A Load

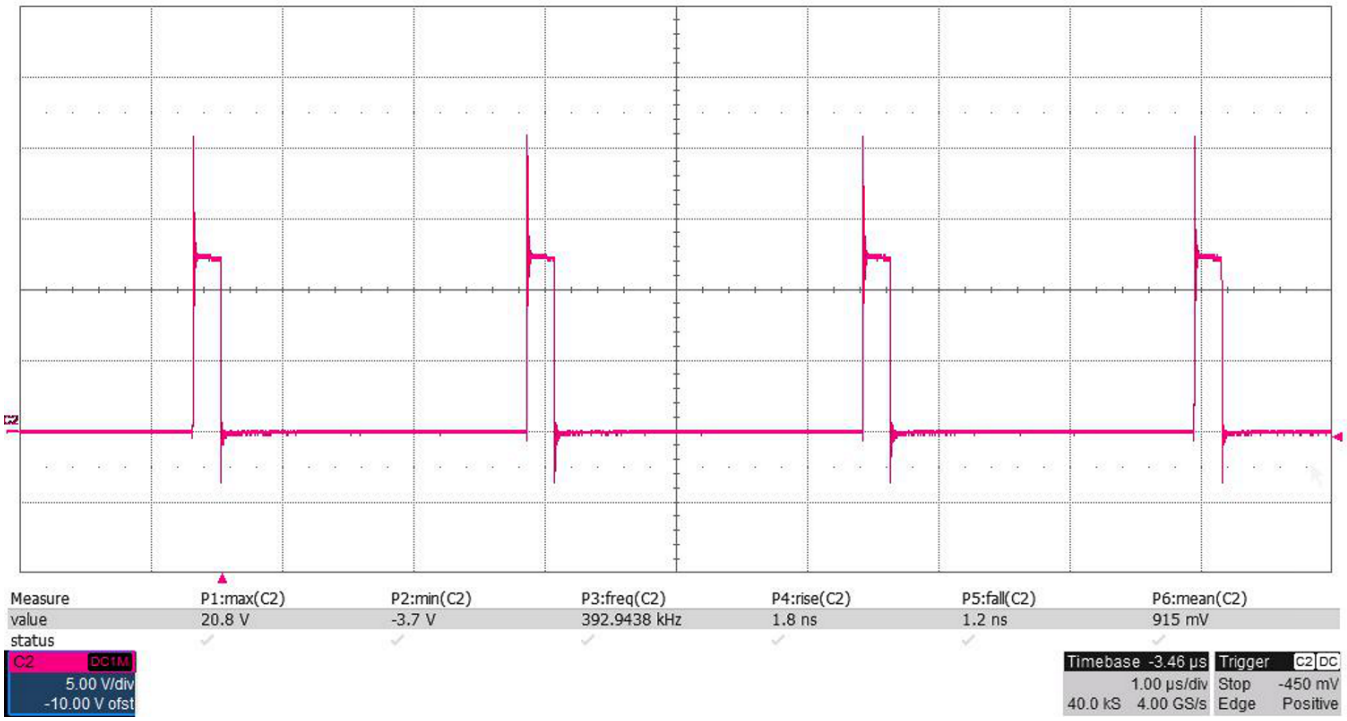


Figure 6. Phase Node Pulses

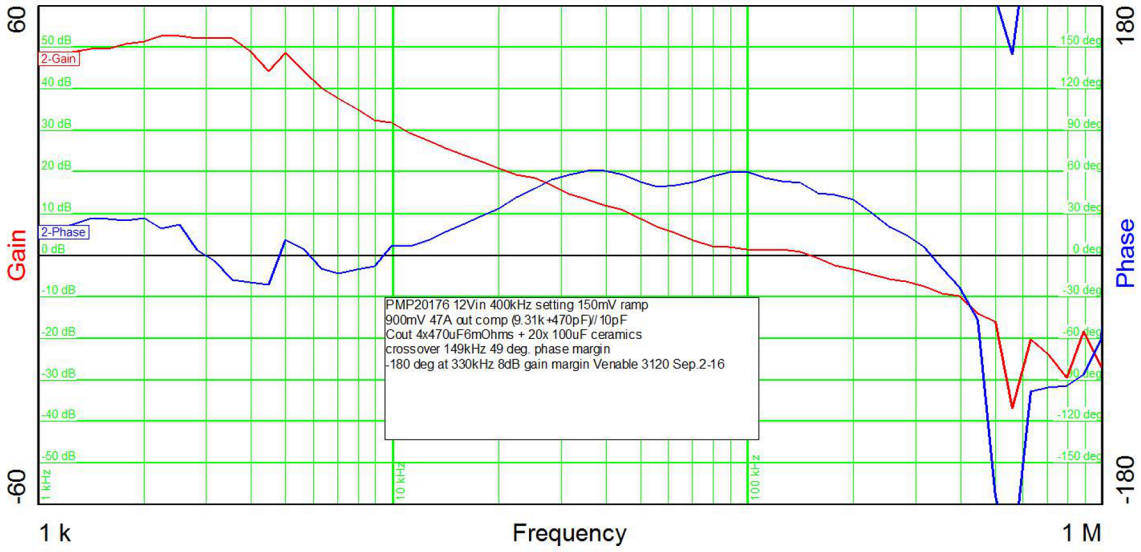


Figure 7. Bode Plot: 50-A Load, V_{IN} = 12 V

4.3 Thermal Performance

The design was placed in a 25°C environment under 100-A and 140-A loads at an output voltage of 0.9 V until it reached thermal equilibrium before taking measurements of the power stages and inductors using an infrared camera. Neither airflow or heatsinks are used at the TDC current to test a worst-case scenario. A setup more closely mimicking an end application was used when the 140-A current was applied.

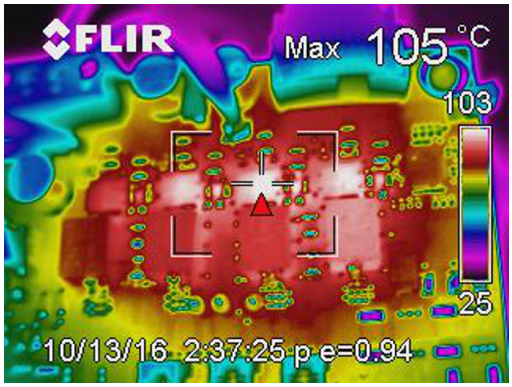


Figure 8. 100-A Load Thermal Performance, No Airflow

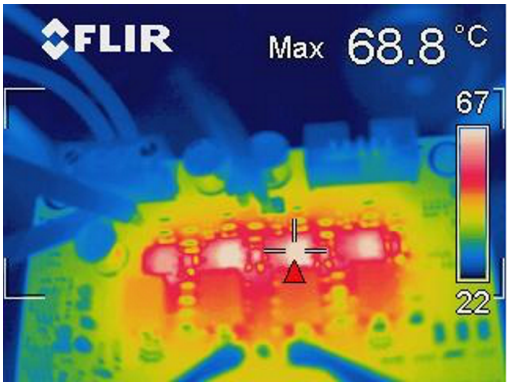


Figure 9. 140-A Load Thermal Performance, ≈350 LFM

4.4 Transient Response

A load step of 75 A was applied to the TPS53647 regulator under two test conditions. The first test condition is from 4 A to 79 A and the second test condition is from 65 A to the maximum load of 140 A. Under both conditions the load frequency was swept from 1 kHz to 1 MHz to check the stability under a wider range of operational corners. With no DC load line and an AC tolerance of ±5%, a peak-to-peak voltage swing of 90 mVpp is allowed at the nominal output voltage of 0.9 V. No stability issues were observed during testing and the output voltage remained within the regulation window.

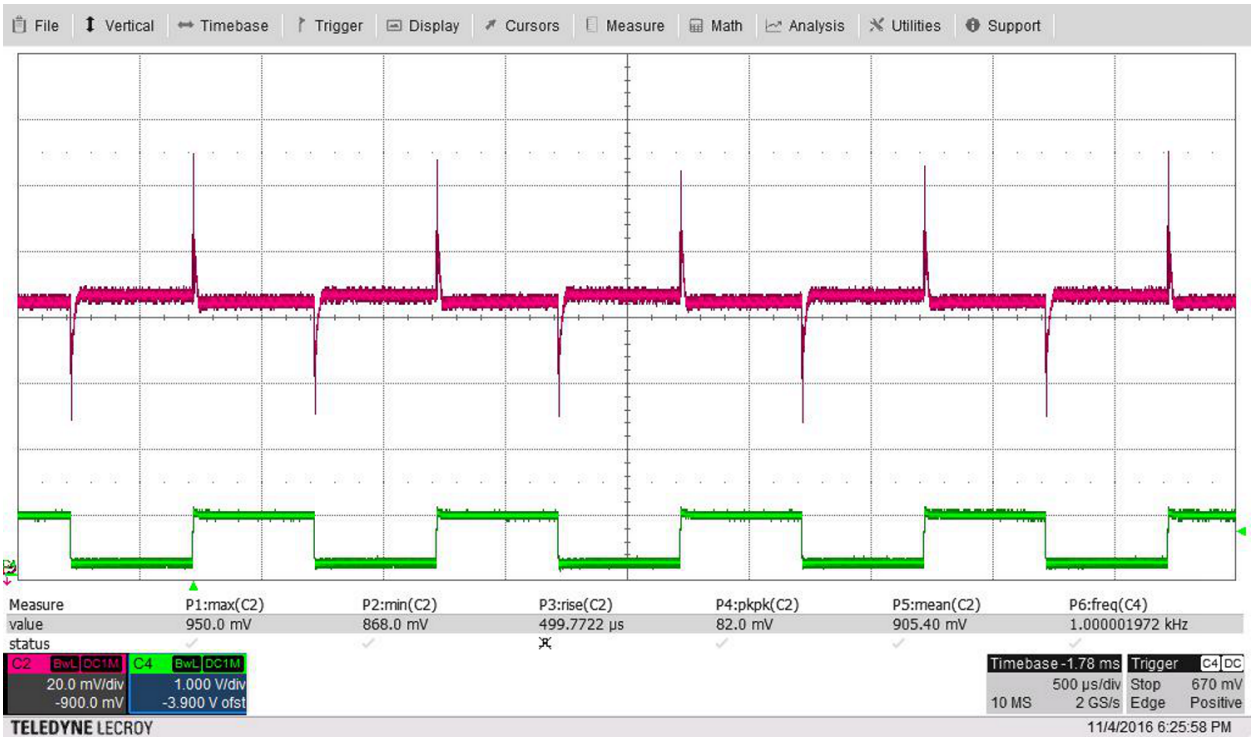


Figure 10. 4-A to 79-A Transient, 1-kHz Load Frequency

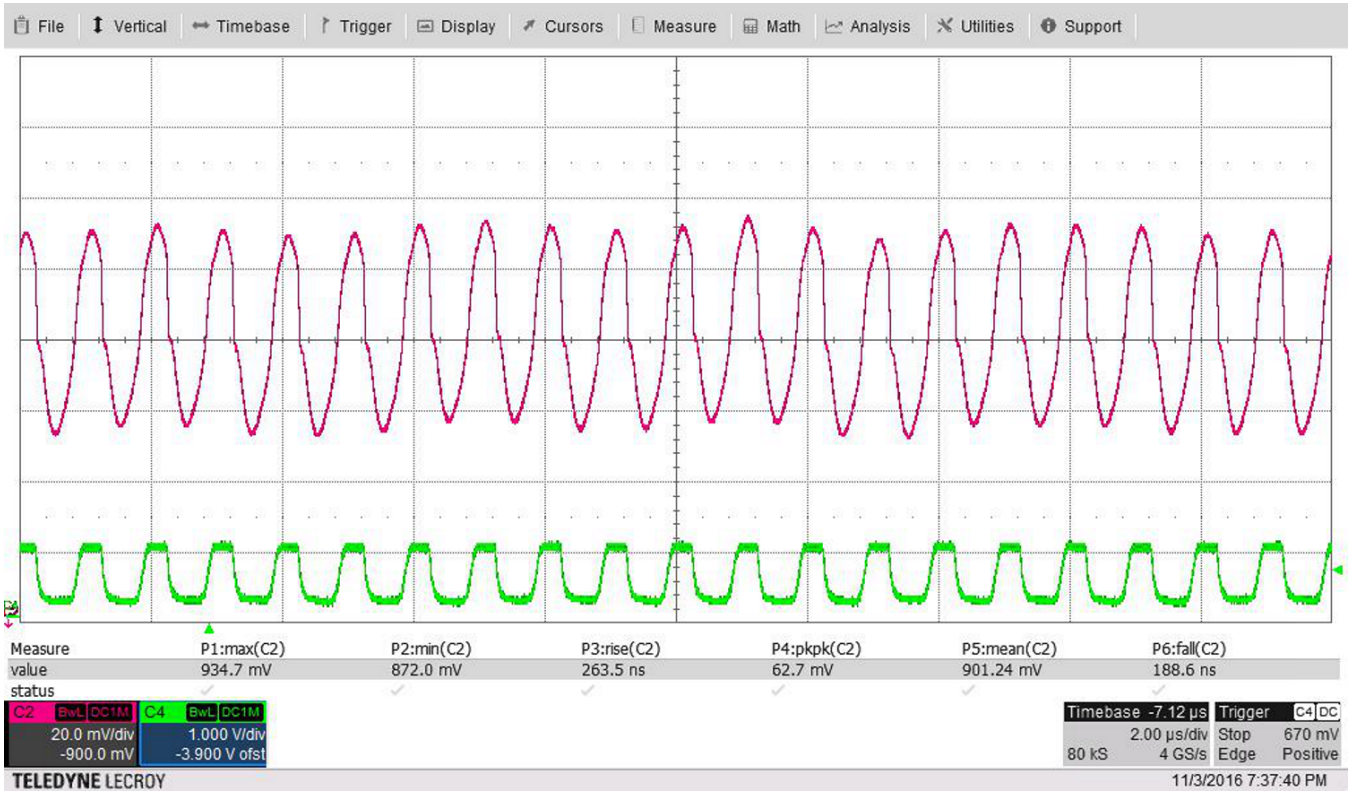


Figure 11. 4-A to 79-A Transient, 1-MHz Load Frequency

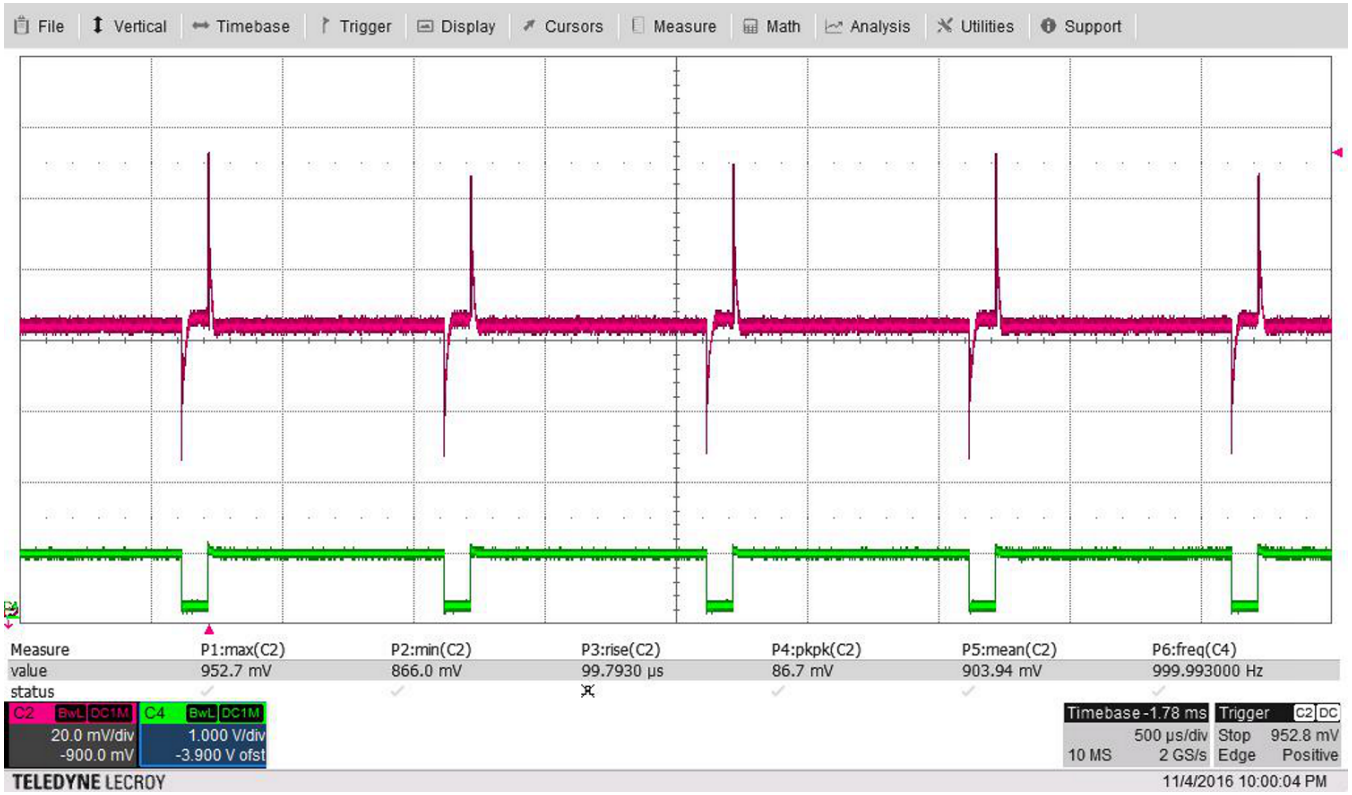


Figure 12. 65-A to 140-A Transient, 1-kHz Load Frequency

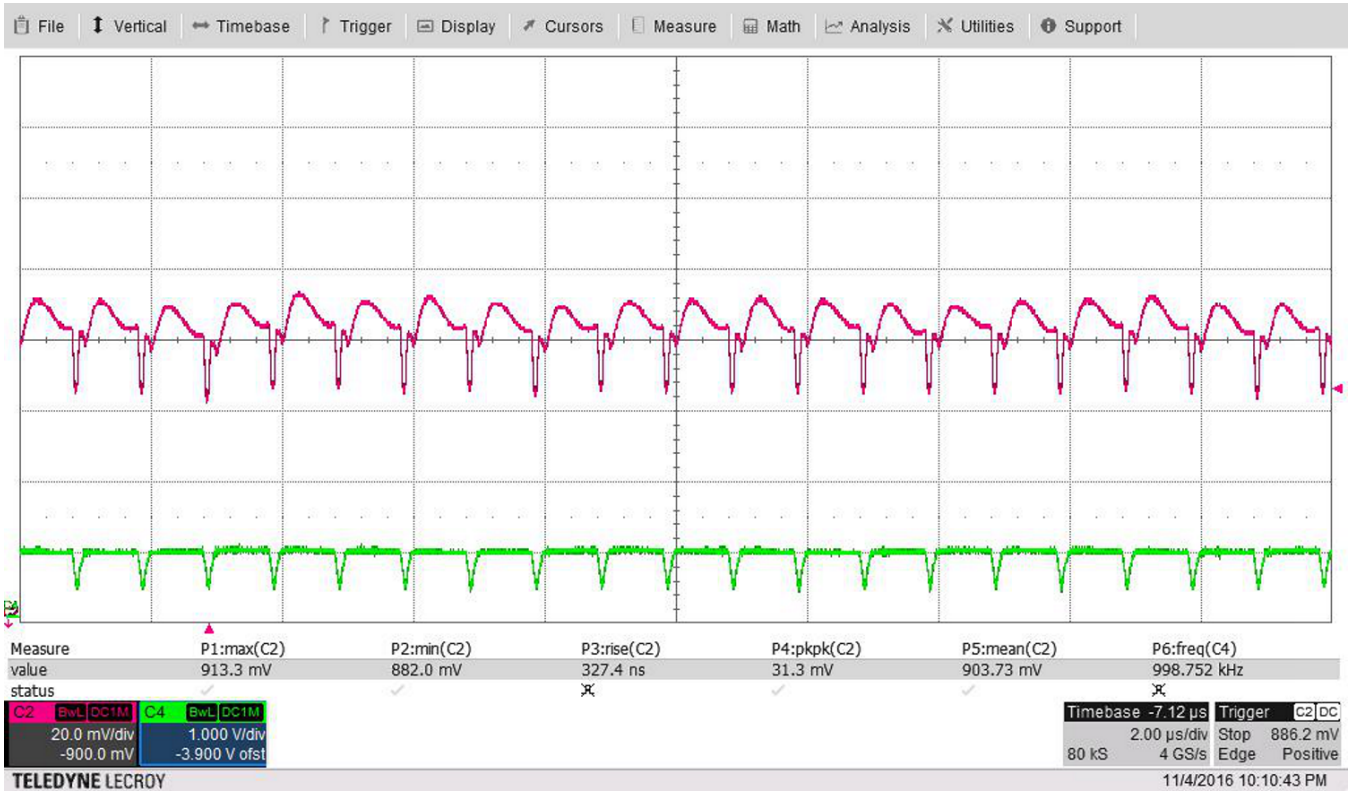


Figure 13. 65-A to 140-A Transient, 1-MHz Load Frequency

Table 2. Transient Response Validation Results

LOAD STEP	TRANSIENT SPECIFICATION AT NOMINAL OUTPUT VOLTAGE	MEASURED RESULTS
4 A to 79 A, 1 kHz	90 mV_{PP}	82 mV_{PP}
4 A to 79 A, 1 MHz	90 mV_{PP}	62 mV_{PP}
65 A to 140 A, 1 kHz	90 mV_{PP}	86.7 mV_{PP}
65 A to 140 A, 1 MHz	90 mV_{PP}	31.3 mV_{PP}

4.5 Start-Up and Shutdown

Start-up and shutdown waveforms were taken at 4-A and 100-A loads while monitoring the enable, output voltage, and power good signals. For the high-current shutdown scenario, V_{OUT} is dragged below ground because the electronic load attached to the output of the regulator tries to maintain the 100-A load. Such behavior does not occur in real applications.

In the following scopeshots, C2 is the Enable signal, C3 is the V_{OUT} signal, and C4 is the PGOOD signal.

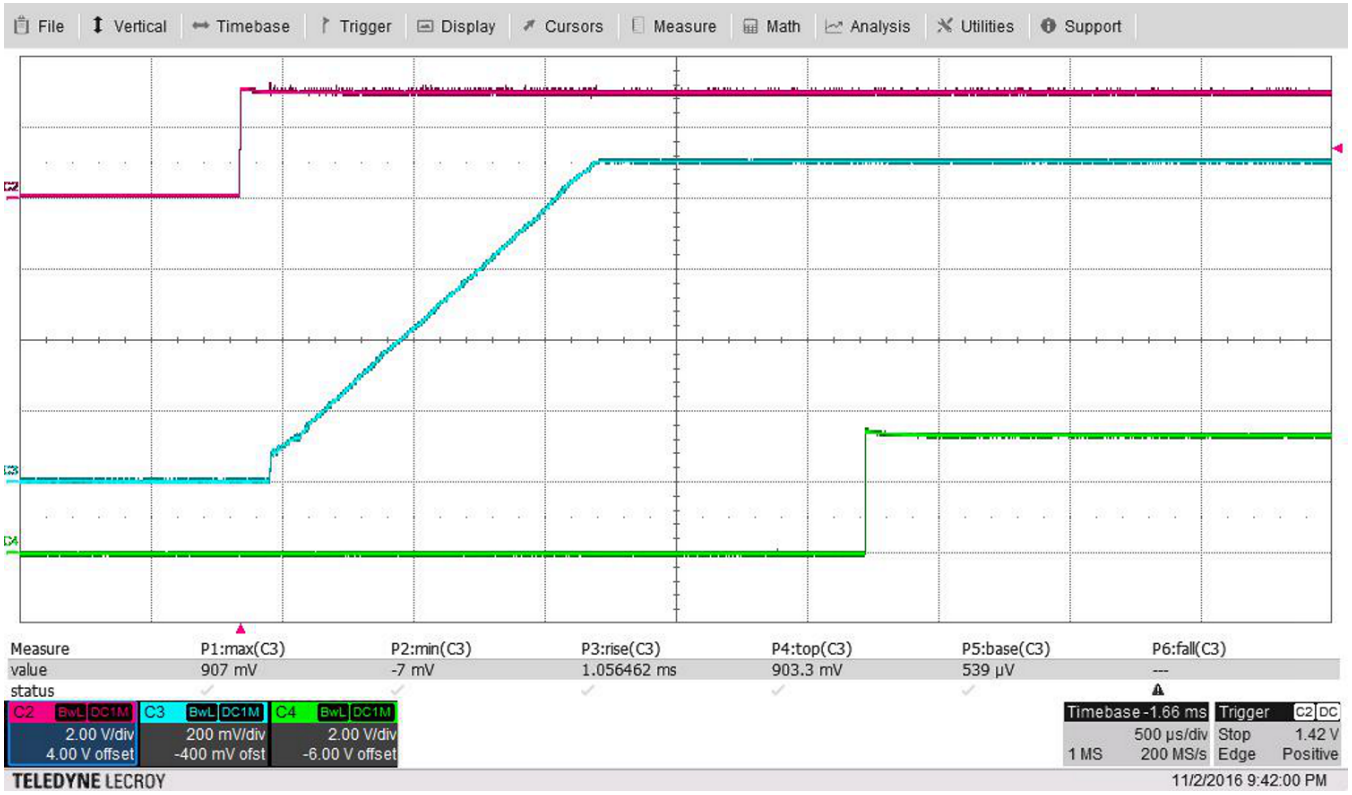


Figure 14. 4-A Start-Up

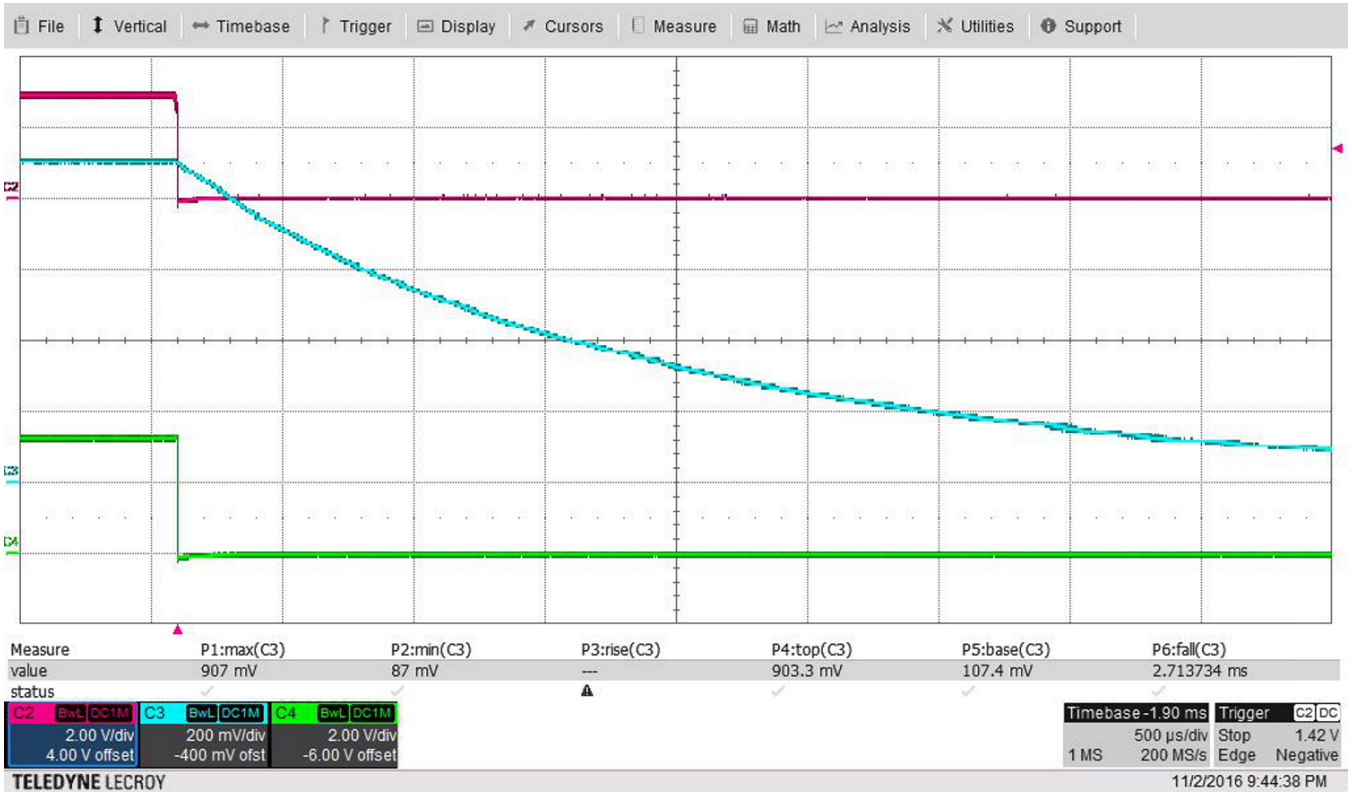


Figure 15. 4-A Shutdown

Figure 16. 100-A Start-Up

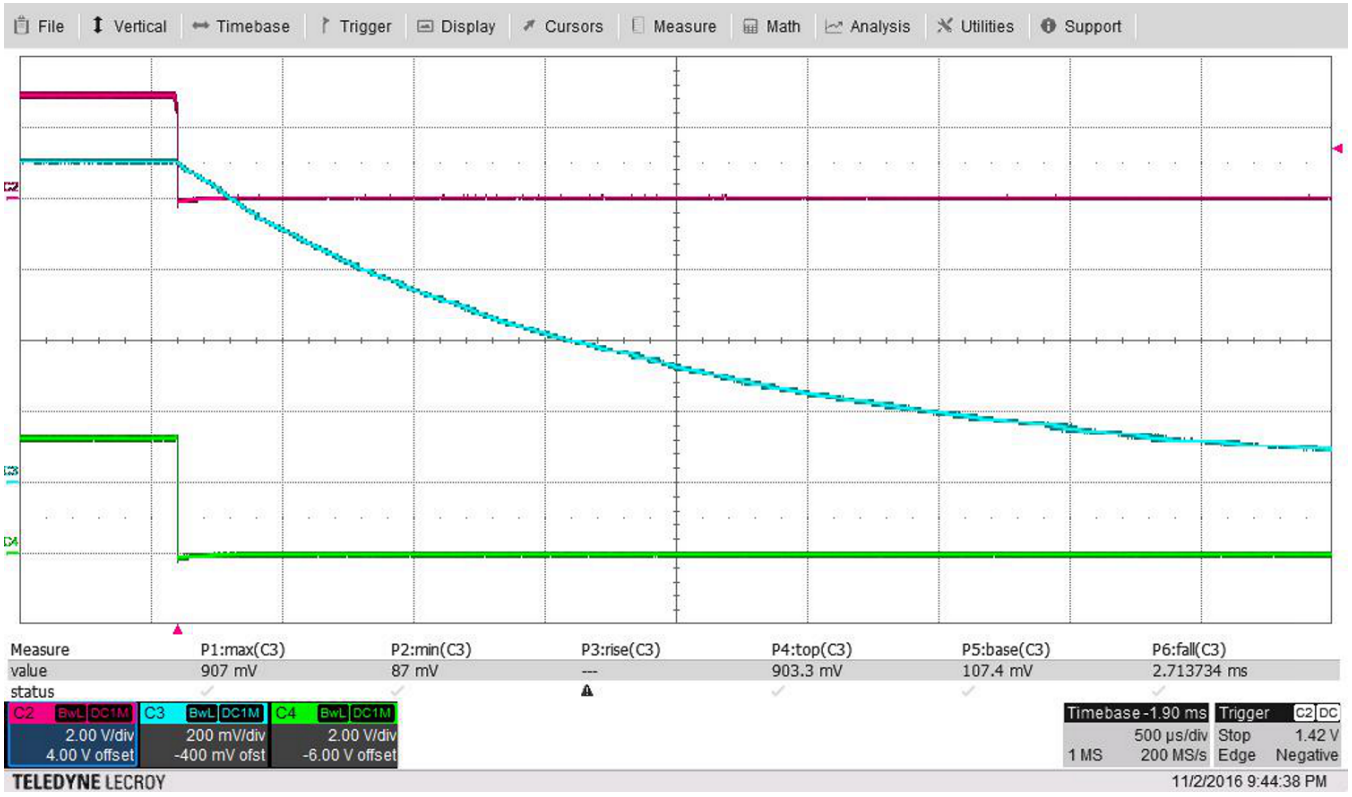


Figure 17. 100-A Shutdown

4.6 Protection Circuitry

The TPS53647 device also performed admirably when testing the on-chip protection mechanisms for this application. The overcurrent and overtemperature protection features work as intended when triggered and prevent the load and power stages from damage. Upon hitting the overcurrent limit, the controller enters hiccup mode and attempts to restart. Figure 18 shows a single shutdown and Figure 19 shows the hiccup mode. A successful power-up only occurred after removing the high current. After the overtemperature threshold was crossed, the output voltage decayed to 0 V (according to the load current) until the part had cooled off and a restart was triggered. In Figure 20 and Figure 21, a recovery time of 12 seconds was observed after the overtemperature fault occurred. For all testing, the PGOOD signal toggles low when the event occurs to signal a fault until V_{OUT} is brought back into regulation.

During overcurrent events, V_{OUT} is dragged below ground because the electronic load attached to the output of the regulator tries to maintain the load. Such behavior does not occur in real applications.

In the following scopeshots, C2 is the V_{OUT} signal and C4 is the PGOOD signal.

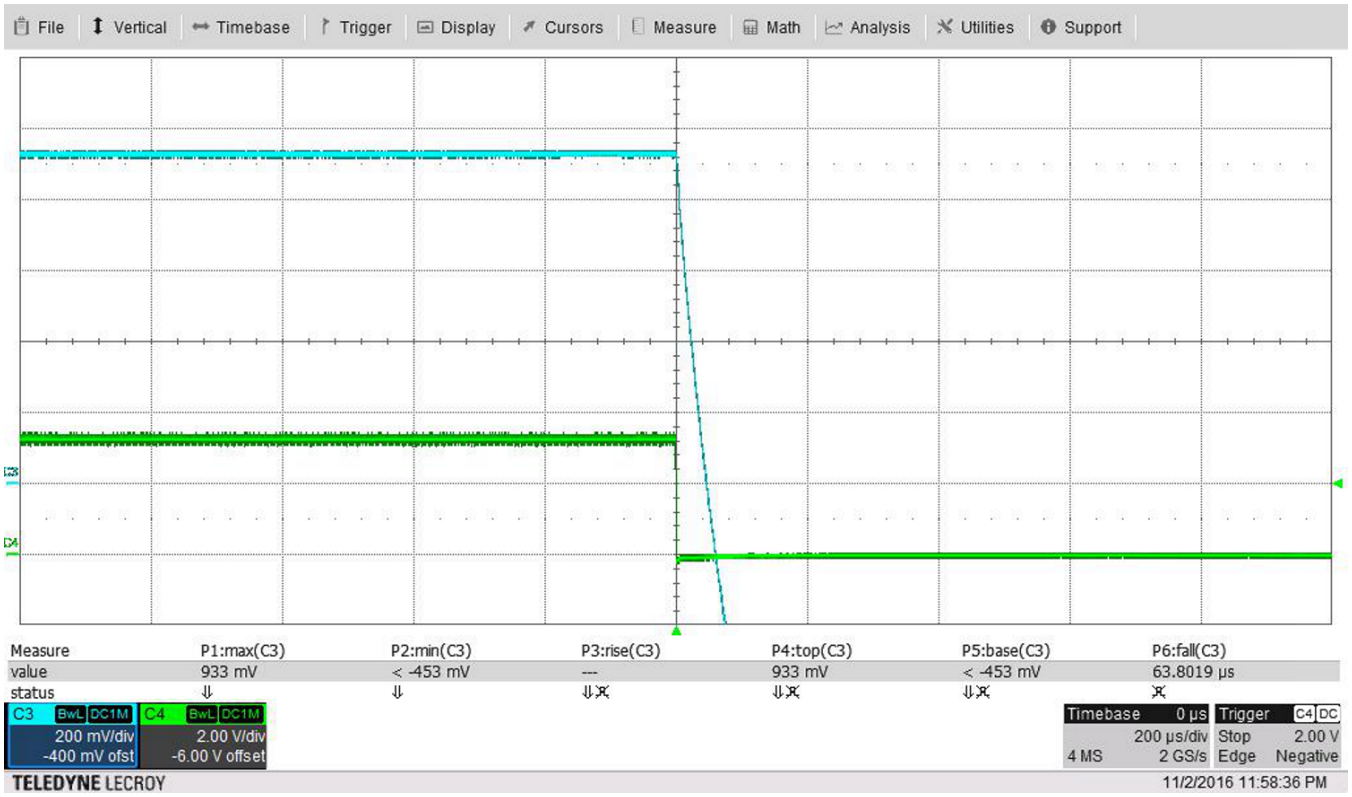


Figure 18. Single Overcurrent Shutdown

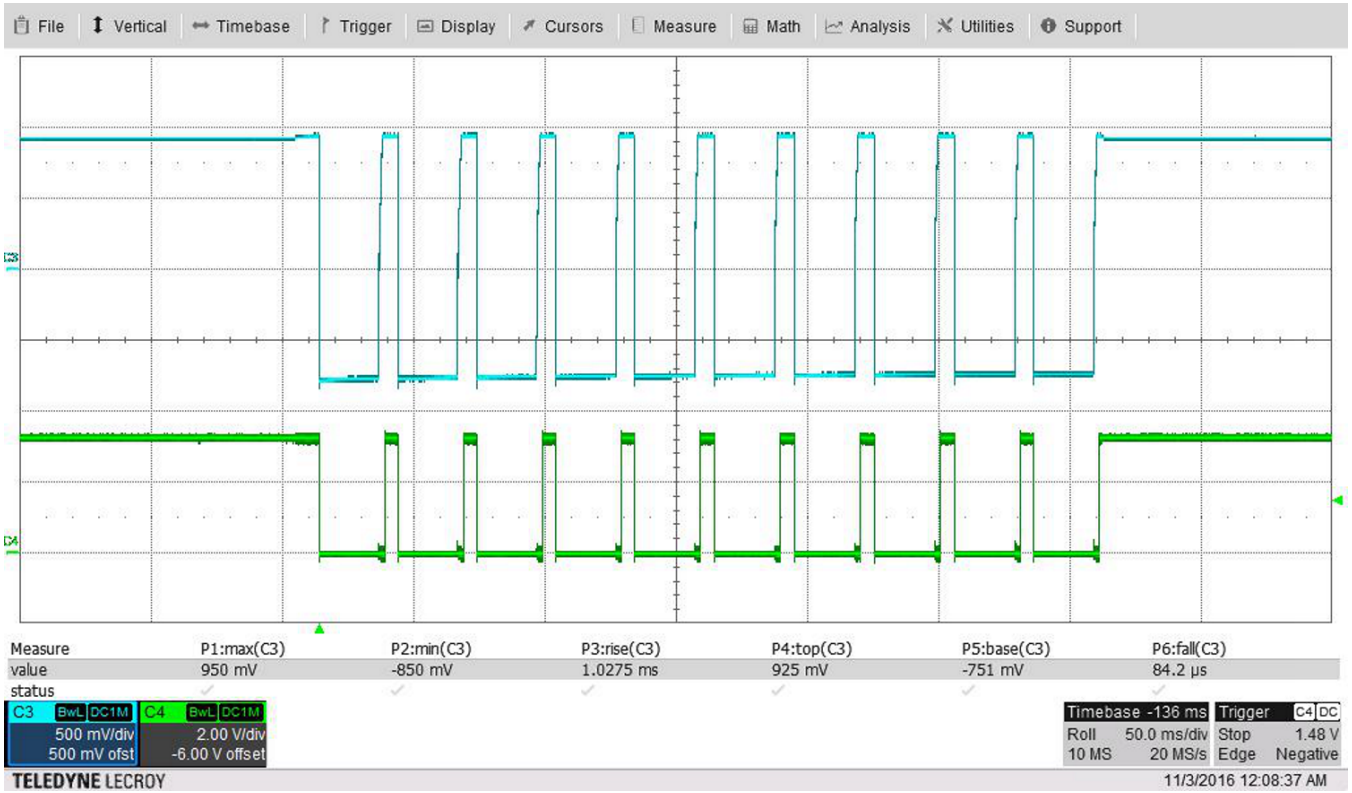


Figure 19. Overcurrent Shutdown With Hiccup Mode

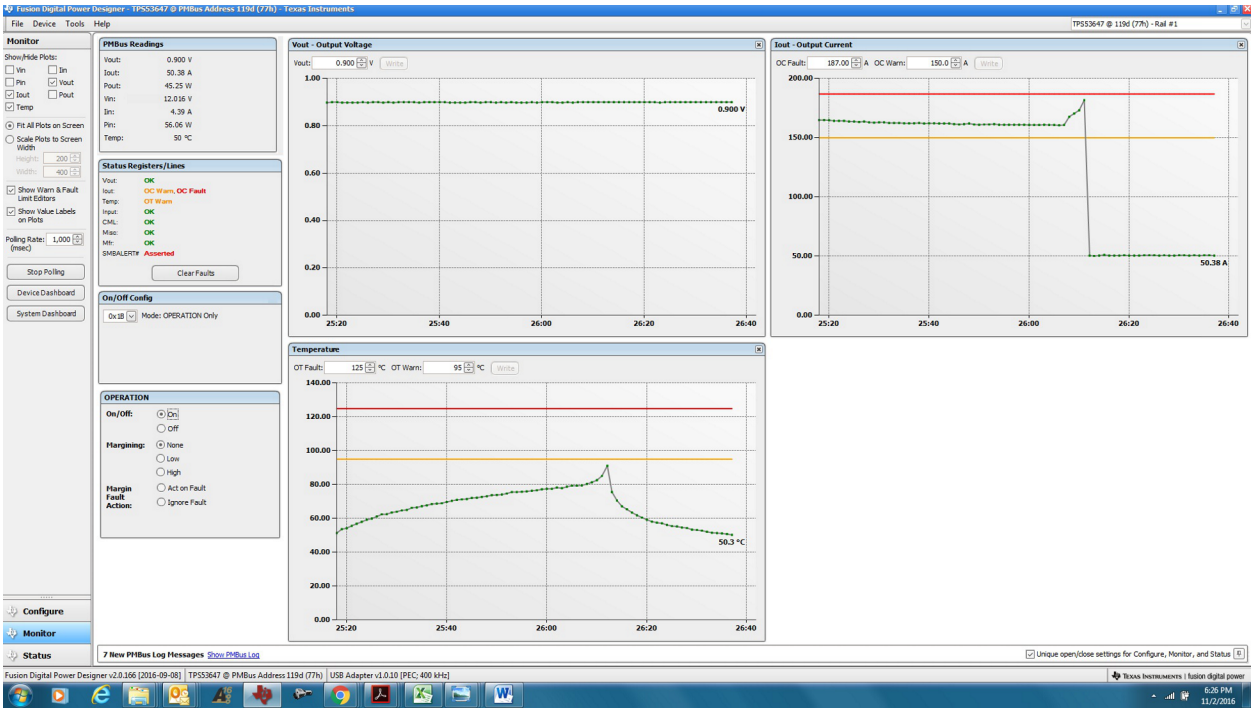


Figure 20. Single Overcurrent Shutdown as Seen in Fusion GUI

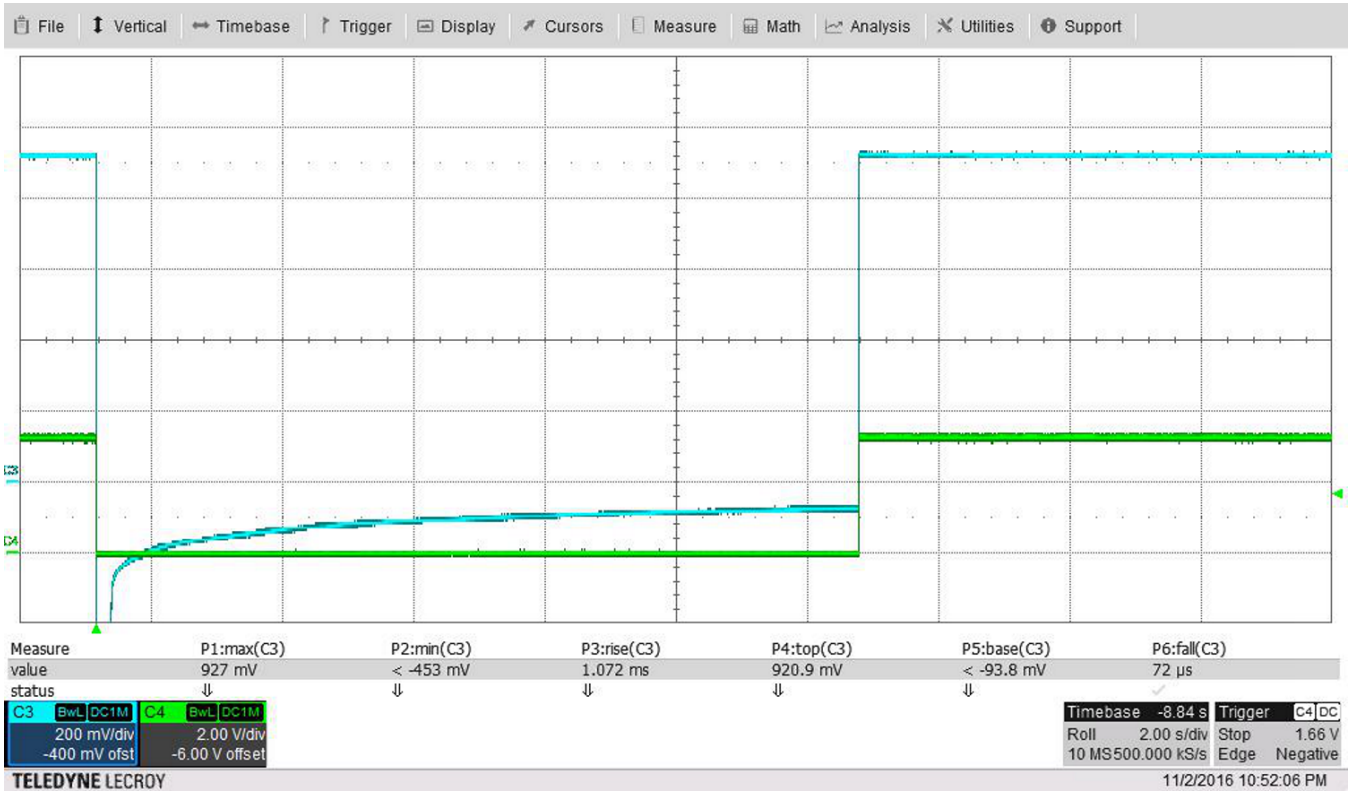


Figure 21. Overtemperature Shutdown With Recovery

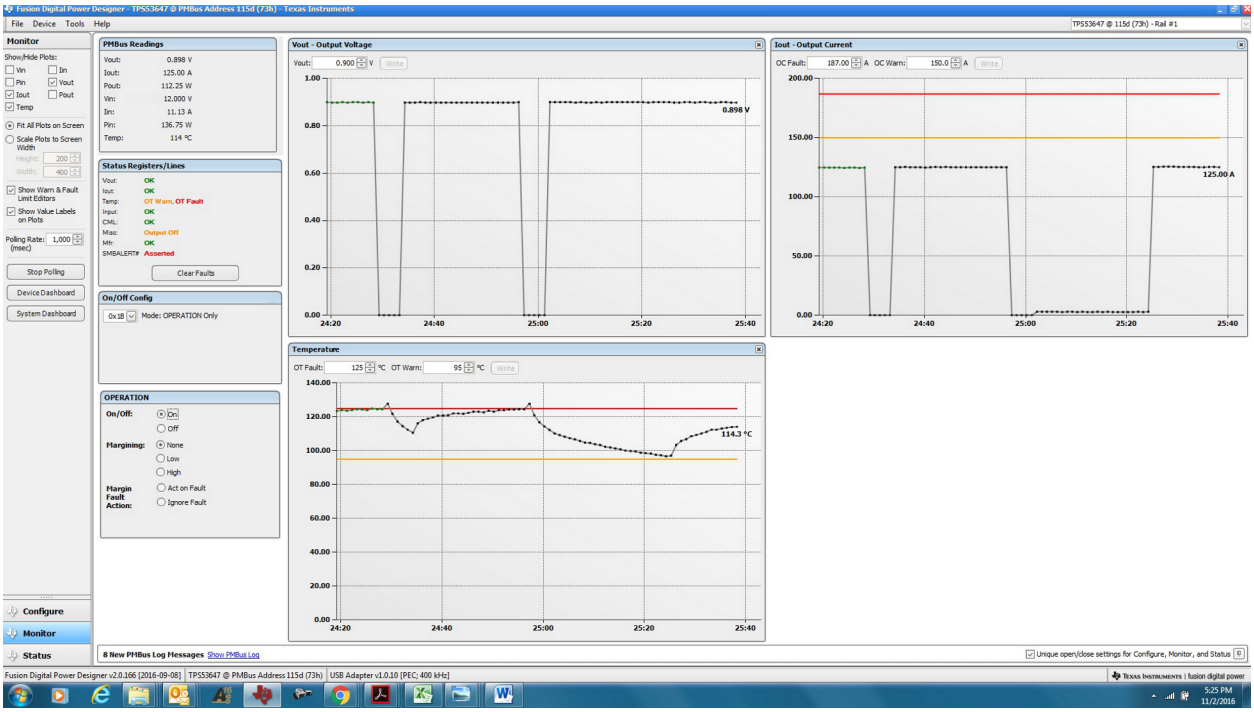


Figure 22. Overtemperature Shutdown and Recovery as Seen in Fusion GUI

5 VOUT_COMMAND Alignment Procedure Between FPGA and TPS53647

The TPS53647 supports Intel's VR12.0/12.5 VID (Voltage Identification) tables while Stratix 10 chips support the SmartVID 10-mV step VID table. With the FPGA default settings its VID codes don't match those of the TPS53647. For the testing in this report TI's software and USB-TO-GPIO cable were used so there was no conflict. In a real application however, the FPGA and TPS53647 must be configured properly in order to enable correct output voltage positioning between devices.

1. Ensure the TPS53647 is set up to use the Intel VR12.5 VID Table through either the correct pin-strap resistor or via NVM programming
   a. See Section 7.5 on page 31 of the controller datasheet for more information on programming the TPS53647
2. Using Intel's Quartus Prime Software, configure the FPGA to use the PMBus Direct Format
   a. Contact Intel support for the procedure if exact steps are needed
3. Set the proper Direct Coefficients (M, B, and R) to select the correct scaling and offset values such that the SmartVID block of the FPGA follows the VR12.5 VID Table
   a. M = 0x0064 (100d), B = 0xFFCF (-49d), R = 0x0000 (0d)
   b. Note VID Code 0 (0.00V) is not supported
   c. Refer to Table 1 on page 25 of the TPS53647 datasheet for the VR12.5 VID Table

6 Design Files

6.1 Schematics

To download the schematics, see the design files at PMP20176.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at PMP20176.

6.3 PCB Layout Recommendations

Follow all the layout instructions as specified in the respective data sheet for each part when laying out a design using the TPS53647 controller and CSD95472 Smart Power Stage. Some other guidelines to consider include:

- Keep the layout for all four phases identical to ensure optimal current balancing and thermal performance between phases.
- Route noisy traces such as PWM and the PMBus lines on a separate layer than the sensitive analog sense lines such as VSP, VSN, COMP, IMON, and so forth.
- Use quality capacitors for both the input and output decoupling to obtain the maximum performance possible with respect to DC ripple and transient response. Capacitors must be voltage rated to at least 16 V on V_{IN} and 2.5 V on V_{OUT} with a dielectric rating of X5R or better.
- Ensure that the VOUT and GND nodes are routed on multiple layers of copper and connected with enough vias to handle the current requirements for the best thermal performance. Following this guideline allows for the maximum amount of heat to flow out of the power stages and inductors into the board.

6.3.1 Layout Prints

To download the layer plots, see the design files at PMP20176.

6.4 Gerber Files

To download the Gerber files, see the design files at PMP20176.

6.5 Assembly Drawings

To download the assembly drawings, see the design files at PMP20176.

7 Software Files

To download the Fusion Digital Power Designer software, see the following tool folder.

8 Related Documentation

1. Texas Instruments, *TPS53647 4-Phase, D-CAP+, Step-Down, Buck Controller with NVM and PMBus™ Interface for ASIC Power and High-Current Point-of-Load*, TPS53647 Data Sheet (SLUSC39)
2. Texas Instruments, *CSD95472Q5MC Synchronous Buck NexFET™ Smart Power Stage*, CSD95472Q5MC Data Sheet (SLPS599)
3. Intel, *Intel® Arria® 10 GX, GT, and SX Device Family Pin Connection Guidelines*, PCG-01017 (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/dp/arria-10/pcg-01017.pdf)
4. Intel, *Power Reduction Features in Arria 10 Devices*, AN-711 (https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an711.pdf)
5. Intel, *SmartVID Controller IP Core User Guide*, UG-SVID (https://www.altera.com/content/dam/alterawww/global/en_US/pdfs/literature/ug/ug_smartvid.pdf)
6. Intel, *25A Mini Slammer*, Product Page (https://designintools.intel.com/25A_Mini_Slammer_p/q6uj9a00ms25.htm)

8.1 Trademarks

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2017) to B Revision	Page
• Added Section 5	17

Changes from Original (August 2017) to A Revision	Page
• Updated to specify Stratix® 10 FPGAs with 1SG280-1IV variant instead of SG2800-I1V	1

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