*TI Designs: TIDA-01473*

# *Ultra-Mobile, Low Power nHD Display Reference Design Using TI DLP® Technology for Low-Cost Processors*

## Description

This display reference design is created for a wide array of ultra-mobile and ultra-portable display applications in consumer, wearables, industrial, medical, and internet of things (IoT) markets. The design includes the DLP2000 chipset comprising of the DLP2000 0.2 nHD DMD, DLPC2607 display controller, and DLPA1000 PMIC and LED driver. This reference design can be used with production-ready optical engines and low-cost application processors that support 8/16/24-bit RGB parallel video interface in small form factors.

## Resources

| | |
|---|---|
| TIDA-01473 | Design Folder |
| DLPC2607 | Product Folder |
| DLPA1000 | Product Folder |
| DLP2000 (DMD) | Product Folder |

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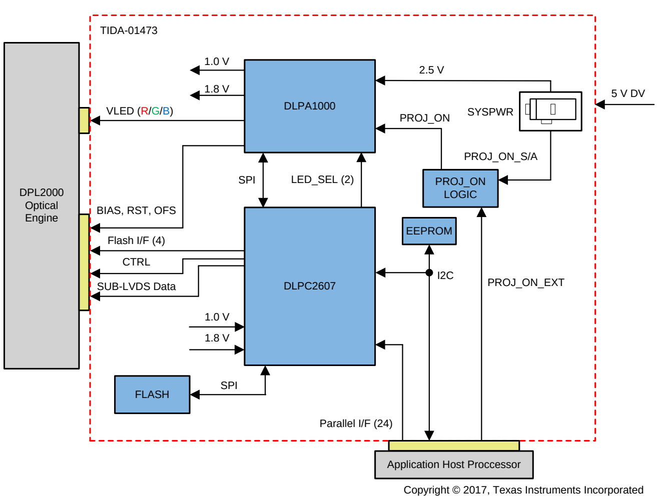
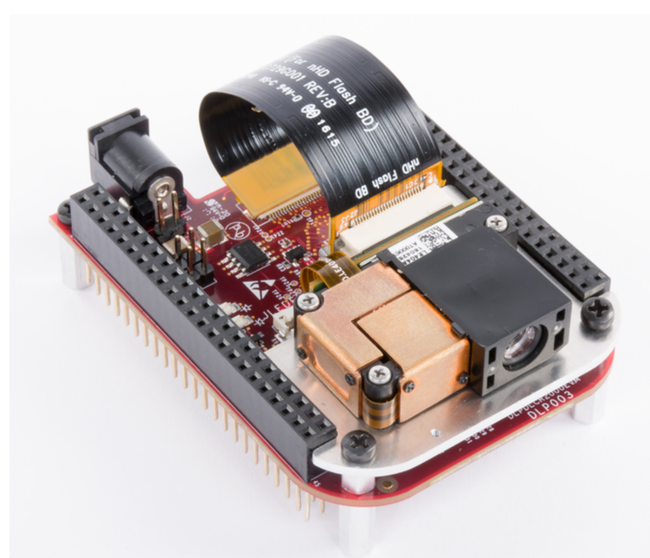
## Features

- Most affordable way for developers to incorporate DLP technology in their display applications
- $I^2C$ and 8/16/24-bit parallel RGB video interfaces to support virtually any low-cost host processor
- Affordable and compact PCB layout supporting nHD (DLP2000) Optical Engine
- Used in DLPDLCR2000EVM layout
- 5-V input and LED current drive up to 1 A
- Part of an established eco-system to help you accelerate the design cycle

## Applications

- Industrial
  - Building automation
  - Appliances
  - Display
  - EPOS
- Personal electronics
  - Mobile phones
  - PC & notebooks
  - Portable electronics (main EE)
  - Tablets
- Internet of things



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# 1 System Description

The 0.2 nHD DLP chipset is a low-cost platform enabling the use of DLP technology with embedded host processors such as the BeagleBone Black. This chipset enables one to quickly implement display capability in embedded Smart Home and Internet of Things (IoT) settings.

## *1.1 Applications for Smart Home and IoT*

*Smart home* is a broad category of products and services that bring automation and interconnectivity to a variety of devices in the home, such as lighting, thermostats, appliances, and entertainment devices.

Bringing smart displays based on DLP Pico™ technology into the home can offer many benefits such as interactive, adaptive, and reconfigurable interfaces that can replace buttons, tablets, LCD panels, and mechanical knobs in virtually every room of the house. DLP technology-based smart displays offer advantages in brightness, resolution, small form factor, low power consumption, throw ratio, and interactivity.

Find more about smart home displays using DLP technology in the white paper *TI DLP Pico technology for smart home applications* (DLPC101).

**Table 1. DLP Features and Design Benefits for Smart Home Applications**

| DLP FEATURE | DESIGN BENEFIT |
| --- | --- |
| Displays of any shape on virtually any surface | Smart displays using DLP chips can project directly onto existing surfaces in the home, delivering convenient information just about anywhere. |
| On-demand display | Smart home projection can instantly provide a display without the intrusion of a permanent display panel. In addition, DLP Pico technology enables small optical module designs that can be tucked out of sight or be integrated into existing home devices. |
| High optical efficiency | Digital micromirror devices (DMDs) incorporate highly reflective and polarization agnostic aluminum micromirrors, which enable bright, power-efficient, compact smart home display systems. |
| High resolution | DLP Pico DMDs enable high-resolution projected images—up to Full HD 1080p resolution. |
| Solid-state illumination compatible | DLP chips are compatible with solid-state illumination, such as LEDs and lasers, which further enables compact sizes and long illumination lifetimes. |

## *1.2 Applications in Wearable Displays*

Wearable displays are devices that are worn as a helmet, headset, or glasses by the user and create an image in the user's field of view. The display can either be see-through (augmented reality) or opaque (immersive or virtual reality).

The DLP Pico chip is a reflective microdisplay technology used in the optical module in a wearable display. It is typically illuminated by RGB LEDs and intelligently reflects light through pupil forming optics into a final optical element such as a waveguide or curved combiner, which relays the image into the eye. DLP Pico technology enables bright, high-contrast, low-power HMDs and NEDs with fast refresh rates, providing ideal qualities for small form factor, lightweight wearable display products.

Find more about wearable displays in the white paper *DLP Technology for Near Eye Display (NED)*.

## *1.3 Applications in Factory Automation Human Machine Interfaces (HMI)*

Interactive displays used in factory automation environment need to be easy to use and robust to withstand a manufacturing environment. Projection-based HMIs provide a flexibility beyond most other display technologies. Incorporating DLP projection technology can provide a hamper-free display surface using a front projected image on virtually any surface.

# 2 System Overview

## 2.1 Block Diagram

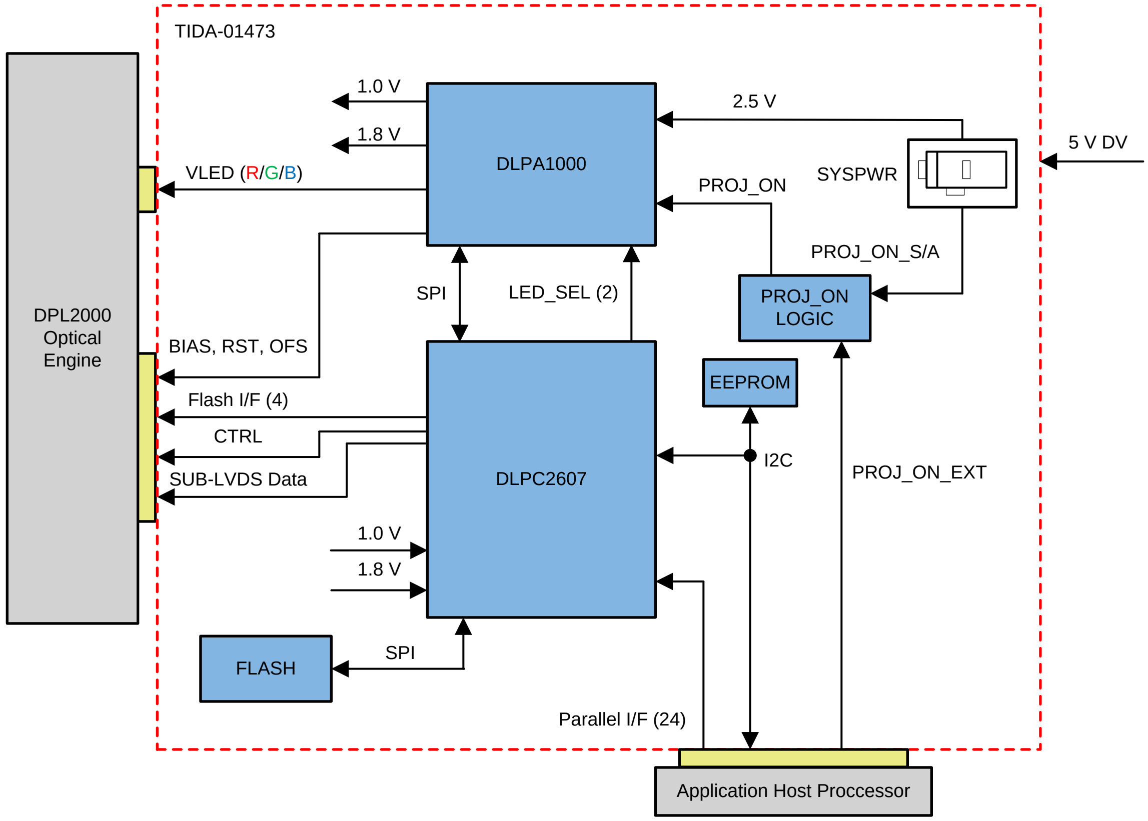


**Figure 1. TIDA-01473 Block Diagram**

## 2.2 Design Considerations

See the following documents for considerations in DLP system design:

- TI DLP Pico System Design: Optical Module Specifications
- TI DLP System Design: Brightness Requirements and Tradeoffs

## 2.3 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the 0.2 nHD DLP chipset. See Section 6 for a list of these documents.

# 3 Hardware, Software, Testing Requirements, and Test Results

## 3.1 Required Hardware and Software

### 3.1.1 Hardware

Assuming default conditions are shipped:

1. Ensure that the optical engine is properly connected to the DLP LightCrafter™ Display 2000 evaluation module (EVM) board.
   (a) Align "pin 1" of the optical engine with "pin 1" of the DMD data flex cable (female side).
   (b) Align "pin 1" of the DMD data flex cable (male side) to the DLP LightCrafter Display 2000 board (at connector J1). Figure 2 through Figure 4 are provided to assist in proper assembly of the board with the optical engine.

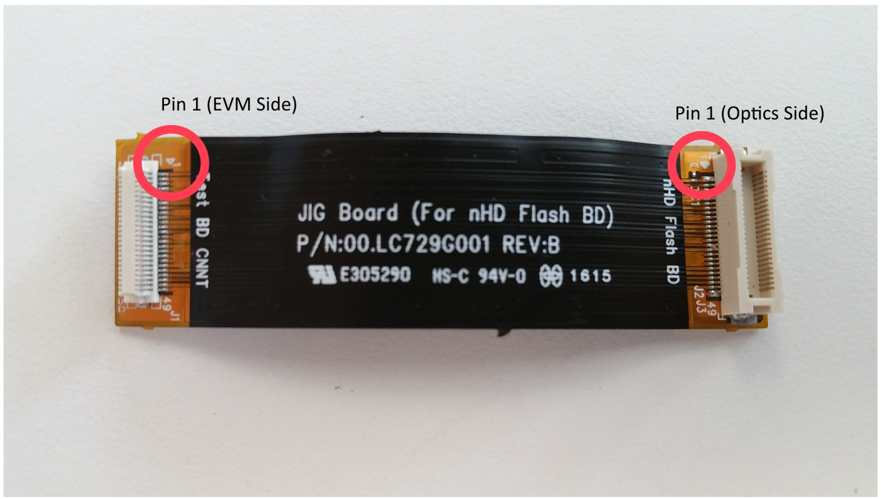


**Figure 2. Overview of Flex Cable Pinout for 0.2 nHD Optical Engine**

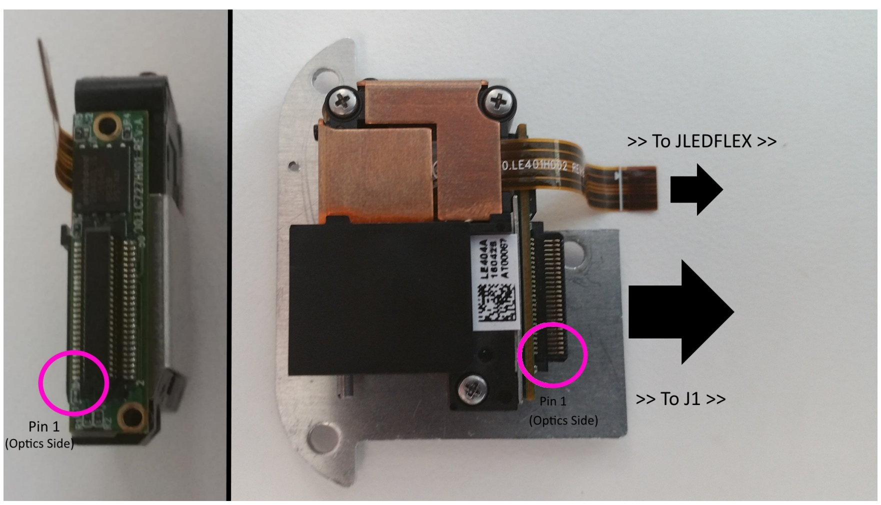


**Figure 3. Overview of Connection for 0.2 nHD Optical Engine**

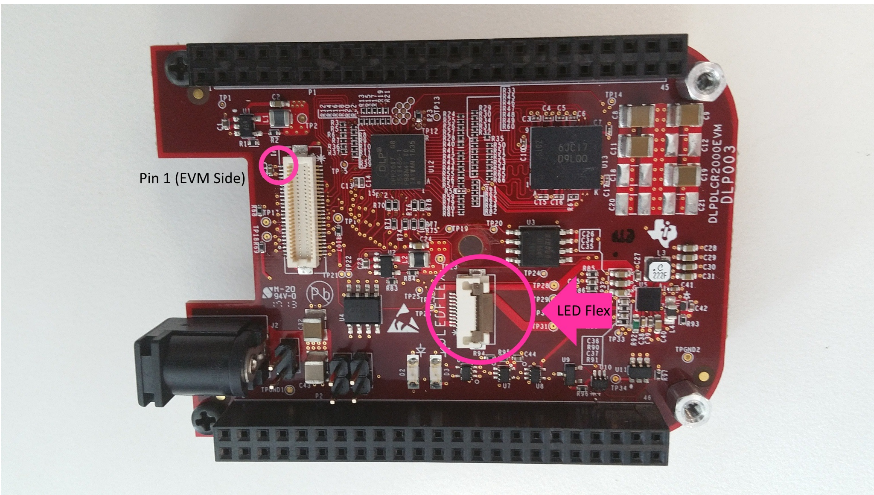


**Figure 4. Overview of Board Pinout**

2. Power up the DLP LightCrafter Display 2000 board by applying an external DC power supply (5-V DC, 3.0 A) to the J2 connector.
   (a) Use an AC-DC switching power supply that accepts 50 to 60 Hz, 100- to 240-V AC inputs, and outputs a nominal 5-V DC at maximum a 3-A output current. For this purpose, this design team recommends the PW172KB0503F01 ITE Switch Mode Power Supply (or equivalent), which can be purchased from retailers such as Mouser or Digikey. The DC power supply jack has a 0.1-inch inner diameter and a 0.218-inch outer diameter.
   (b) If the host processor used supports it, the system can be made to consume power through the attached host. Power and ground need to be supplied through header J3 on the board. See the user's guide for the respective host processor to determine if enough current can be supplied to drive the DLP LightCrafter Display 2000 board. A minimum of 320 mA is recommended for the board to run at typical brightness settings.
3. After the DLP LightCrafter Display 2000 board is turned on, the projector defaults to a DLP LightCrafter Display splash screen. See Figure 5 for an example:


**Figure 5. 0.2 nHD Board Splash Screen**

4. Adjust the focus of the image with the focus wheel on the optical engine.

From this point, the system will need to be supplied with a video source (using a host processor such as the BeagleBone Black) and given instructions through the supplied $I^2C$ bus. Methods for doing this are provided in the following subsections.

#### 3.1.1.1 Use With Host Processor

To control the system through a host processor, the selected host must possess the necessary GPIO pinouts to drive the inputs to the board. This can be accomplished using a customized video and $I^2C$ output driver. For the BeagleBone Black, a driver to use with the DLP LightCrafter Display 2000 board has been provided such that the pinouts of the BeagleBone Black match the footprint of the board I/O ports. This driver also works with the BeagleBone Green. This design guide assumes the user is interfacing with a BeagleBone Black as an example (see Figure 6).

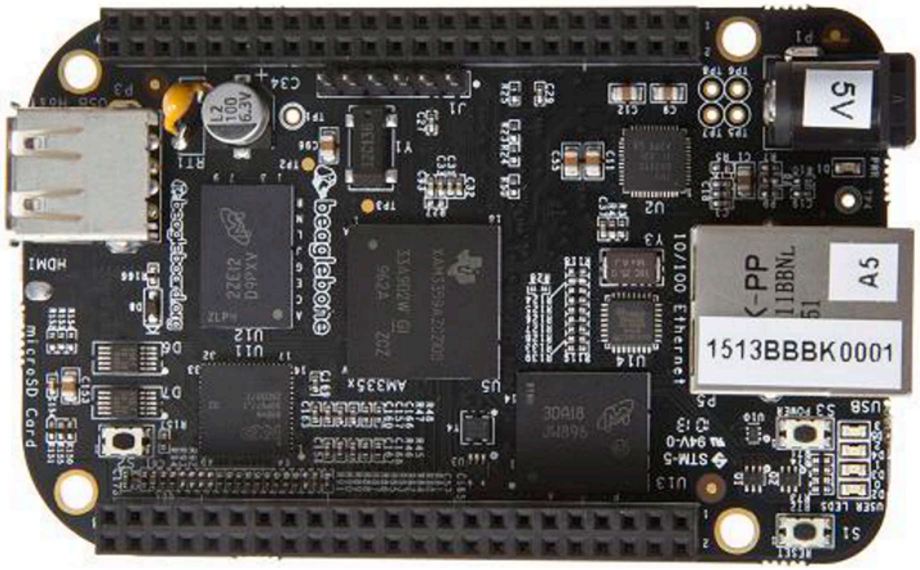


**Figure 6. BeagleBone Black Host Processor**

After installing the BeagleBone-compatible Debian image, an interface between the host processor and the user must be established. There are two ways to establish this interface:

- Onboard mini-HDMI video output with USB keyboard and mouse connection
- Remote connection through an SSH terminal application (such as PuTTY for Windows® users)

Once the system is set up properly, the BeagleBone Black communicates with the EEPROM on the DLP LightCrafter Display 2000 board on boot. This signals the BeagleBone Black to load the appropriate daughter card (or cape) overlay to configure the GPIO ports on the host processor. Once the cape overlay is loaded, the host processor has three ways to interact with the board:

- Parallel I/F video data (through RGB888)
- Issuing I2C commands (through I2C commands)
- Enabling or disabling the board (through PROJ_ON_EXT)

Support for use of these features with the DLP LightCrafter Display 2000 board is included in the BeagleBone Black support scripts, which can be found in the "opt/scripts" directory and executed from the terminal command line. To access the BeagleBone Black terminal, follow the networking access guide at http://elinux.org/Beagleboard:Terminal_Shells.

$I^2C$ commands can be issued by using the aforementioned shell scripts but can also be issued manually using the $I^2C$ terminal commands "i2cdetect", "i2cget", "i2cset". These commands use the onboard $I^2C$ bus to communicate with peripheral devices attached to the host processor. Using these commands is documented at http://elinux.org/Interfacing_with_I2C_Devices. For further information, the "man" command in Linux can also be used to access internal manuals for "i2cdetect", "i2cget", and "i2cset". See Figure 7 and Figure 8 for examples of using these commands within a Linux SSH terminal interfacing with the BeagleBone Black. Typically, the DLPC2607 is located at address 0x1b, and the EEPROM is located at address 0x54, 0x55, 0x56, or 0x57, depending on the configuration of jumpers J4 and J5 on the board. By default, the EEPROM device address is 0x54.


**Figure 7. "i2cdetect" Example Use (in Bash)**

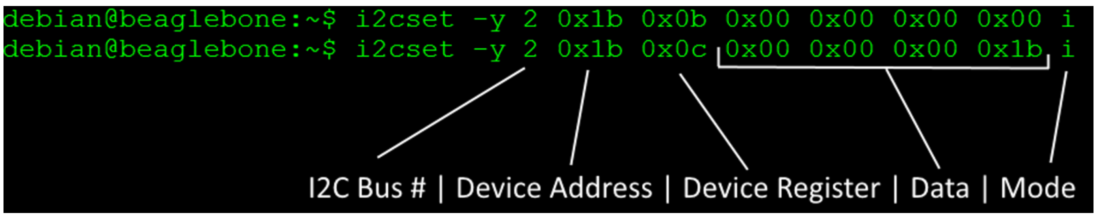


**Figure 8. "i2cset" Example Use (in Bash)**

#### *3.1.1.2 Use Without Host Processor*

If the system is to be controlled without the use of a host processor, an external $I^2C$ driver is necessary to issue commands to control the system. In this case, a USB-$I^2C$ compatible dongle can be employed to enable communication between the PC and the DLP LightCrafter Display 2000 board. When choosing to use this method to interact with the system, see the documentation of the specific dongle for help in setting up the system. Once it is connected and set up, follow the *DLPC2607 Software Programmer's Guide* (DLPU013) for help in issuing commands to the system.

### 3.1.2 Suggested Third-Party Software

To begin, an appropriate operating system image must be installed onto the board. An SD card with the latest Debian image designed for the BeagleBone is necessary to use the most up-to-date board drivers. For help with this step, consult the getting started page located at http://beagleboard.org/getting-started.

Using a remote SSH connection is recommended for its flexibility and ease of use. Before continuing, download PuTTY (or see another preferred SSH terminal application) from the creator's website located at http://www.putty.org/. Included on the website are documentation links to provide more detailed information on how to use PuTTY.

### 3.2 Testing and Results

The results of a successful test of this system is the appearance on the display of the splash screen, as shown in Figure 9.


**Figure 9. 0.2 nHD Board Splash Screen**

There are two LEDs on the system. D2 must flash on then turn off. D3 must stay on during operation. D2 corresponds to HOST_IRQ and D3 is the PROJ_ON LED. See the DLPDLCR2000EVM user's guide for more information.

# 4 Design Files

## 4.1 Schematics

To download the schematics, see the design files at TIDA-01473.

## 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01473.

## 4.3 PCB Layout Recommendations

### 4.3.1 Internal ASIC PLL Power

TI recommends the following guidelines to achieve the desired ASIC performance relative to the internal PLL. The DLPC2607 device contains one internal PLL, which has a dedicated analog supply (VDD_PLL and VSS_PLL). At a minimum, VDD_PLL power and VSS_PLL ground pins must be isolated using an RC filter consisting of two 50-Ω series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). TI recommends using one 0.1-µF capacitor and a 0.01-µF capacitor. Place all four components as close to the ASIC as possible; it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that the user must connect both capacitors across VDD_PLL and VSS_PLL on the ASIC side of the ferrites.

The PCB layout is critical to PLL performance. It is important that the quiet ground and power are treated like analog signals. Therefore, VDD_PLL must be a single trace from the DLPC2607 device to both capacitors and then through the series ferrites to the power source. The power and ground traces must be as short as possible, parallel to each other, and as close as possible to each other.

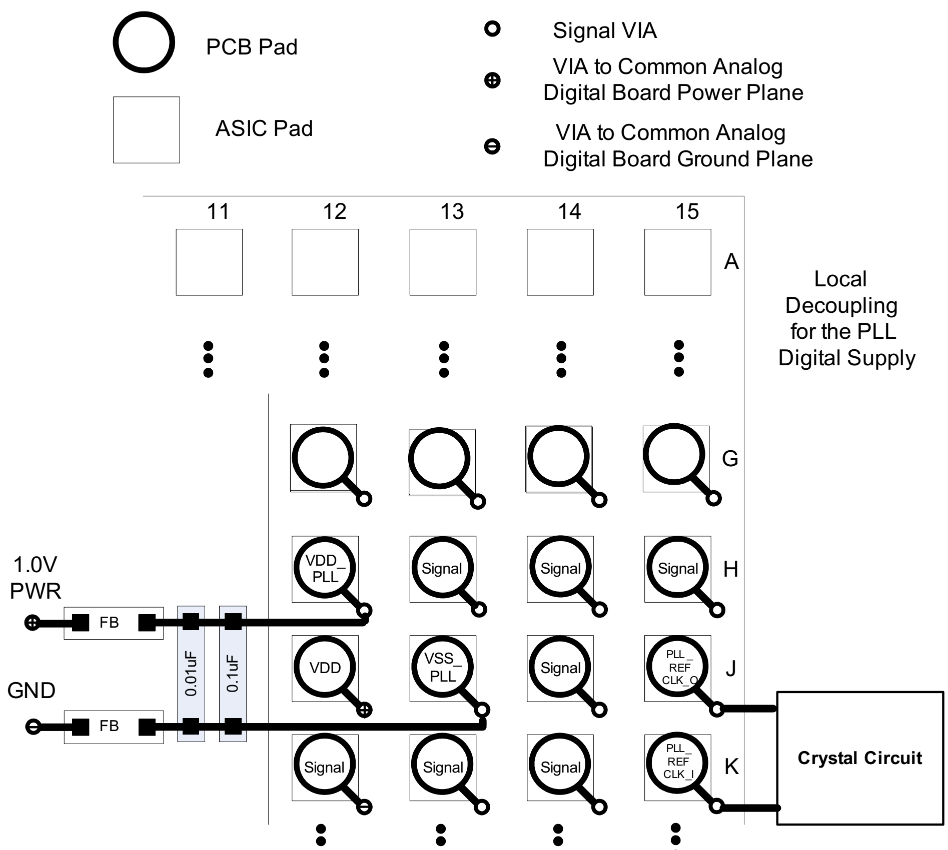


Figure 10. PLL Filter Layout

### 4.3.2 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends to tie unused ASIC input pins through a pullup resistor to their associated power supply or a pulldown resistor to ground. For ASIC inputs with internal pullup or pulldown resistors, do not add an external pullup or pulldown unless specifically recommended.

**NOTE:** Internal pullup and pulldown resistors are weak and must not be expected to drive the external line. The DLPC2607 device implements very few internal resistors, and these are noted in the pin list.

Never tie unused output-only pins directly to power or ground. These pins can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they must be pulled up (or pulled down) using an appropriate, dedicated resistor.

### 4.3.3 SPI Signal Routing

The DLPC2607 device is designed to support two SPI slave devices: a serial flash and the PMD1000. This requires routing associated SPI signals to two locations while attempting to operate at 33.3 MHz. Ensure that reflections do not compromise signal integrity. TI recommends the following:

- The SPICLK PCB signal trace from the DLPC2607 source to each slave device must be split into separate routes as close to the DLPC2607 device as possible. In addition, the SPICLK trace length to each device must be equal in total length.
- The SPIDOUT PCB signal trace from the DLPC2607 source to each slave device must be split into separate routes as close to the DLPC2607 device as possible. In addition, the SPIDOUT trace length to each device must be equal in total length (that is, use the same strategy as SPICLK).
- The SPIDIN PCB signal trace from each slave device to the point where they intersect on their way back to the DLPC2607 device must be made equal in length and as short as possible. They must then share a common trace back to the DLPC2607 device.
- SPICSZ0 and SPICSZ1 do not require special treatment because they are dedicated signals that drive only one device.

### 4.3.4 mDDR Memory and DMD Interface Considerations

High-speed interface waveform quality and timing on the DLPC2607 ASIC (that is, the mDDR memory I/F and the DMD interface) depend on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, the timing margin of the DMD interface system can be calculated as follows:

Setup margin = (DLPC2607 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (1)

Hold-time margin = (DLPC2607 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

where

- PCB SI degradation is signal integrity degradation due to PCB effects. This includes things such as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interference (ISI) noise. (2)

The DLPC2607 device I/O timing parameters, as well as mDDR and DMD I/O timing parameters, can be found in their corresponding datasheets. Similarly, PCB routing mismatch can be easily budgeted and met by controlled PCB routing. However, PCB SI degradation is not so straight forward.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations may also work, but must be confirmed with PCB signal integrity analysis or lab measurements.

#### 4.3.5 PCB Design

- Configuration: Asymmetric dual stripline
- Etch thickness (T): 0.5-oz copper
- Single-ended signal impedance: 50 Ω (±10%)
- Differential signal impedance: 100-Ω differential (±10%)

- Reference plane 1 is assumed to be a ground plane for proper return path.
- Reference plane 2 is assumed to be the I/O power plane or ground.
- Dielectric FR4, (Er): 4.2 (nominal)
- Signal trace distance to reference plane 1 (H1): 5 mil (nominal)
- Signal trace distance to reference plane 2 (H2): 34.2 mil (nominal)

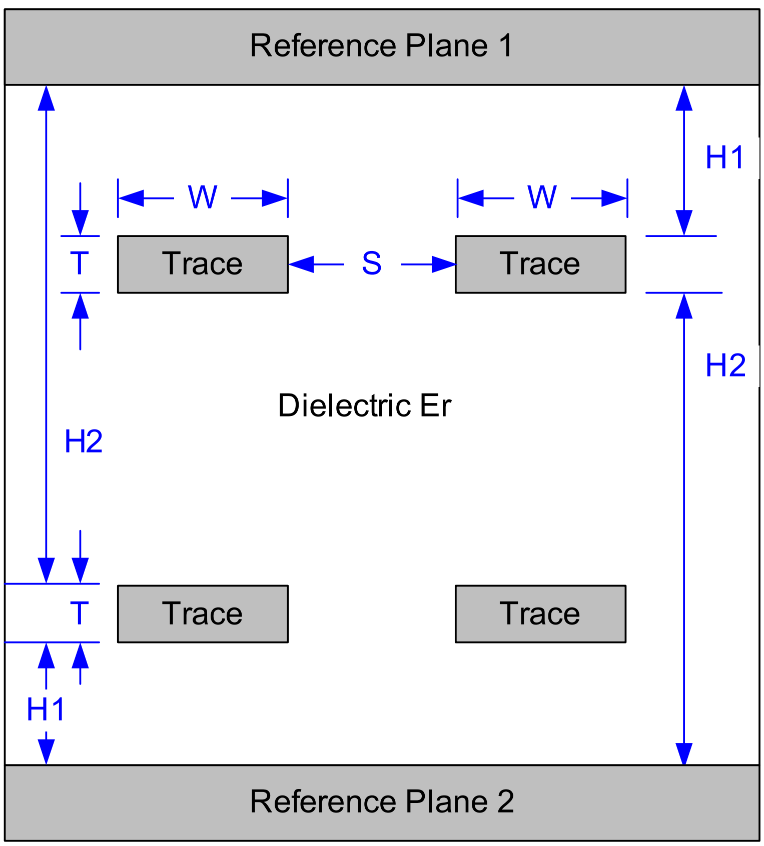


**Figure 11. PCB Stacking Geometries**

### 4.3.6 General PCB Routing (Applies to All Corresponding PCB Signals)

**Table 2. PCB Line and Spacing Recommendations[(1)] [(2)] [(3)]**

| PARAMETER | APPLICATION | SINGLE-ENDED SIGNALS | DIFFERENTIAL PAIRS | UNIT |
|---|---|---|---|---|
| Line width (W) | Escape routing in ball field | 3 (0.762) | 3 (0.762) | mil (mm) |
| | PCB etch: Outer layer data or control | 7.25 (0.184) | 4.5 (0.114) | mil (mm) |
| | PCB etch: Inner layer data or control | 4.5 (0.114) | 4.5 (0.114) | mil (mm) |
| | PCB etch clocks | 4.5 (0.114) | 4.5 (0.114) | mil (mm) |
| Differential signal pair spacing (S) | PCB etch data or control | N/A | 7.75 [1] (0.305) | mil (mm) |
| | PCB etch clocks | N/A | 7.75 [1] (0.305) | mil (mm) |
| Minimum line spacing to other signals (S) | Escape routing in ball field | 3 (0.762) | 3 (0.762) | mil (mm) |
| | PCB etch: Outer layer data or control | 7.25 (0.184) | 4.5 (0.114) | mil (mm) |
| | PCB etch: Inner layer data or control | 4.5 (0.114) | 4.5 (0.114) | mil (mm) |
| | PCB etch clocks | 11 (0.279) | 11 (0.279) | mil (mm) |
| Maximum differential pair P-to-N length mismatch | Total clock | N/A | 25 (0.635) | mil (mm) |

(1) Spacing may vary to maintain differential impedance requirements.
(2) The DLPC2607 device only includes one differential signal pair: MEM0_CK_P and MEM0_CK_N.
(3) These values are merely recommendations to achieve good signal integrity. The OEM is free to apply their own rules as long as they maintain good signal integrity.

These PCB design guidelines are purposefully conservative to minimize potential signal integrity issues. Given this device is targeted for low-cost, handheld application, be more aggressive with these best practices. TI highly recommends to perform a full board-level signal integrity analysis if these guidelines cannot be followed. The DLPC2607 IBIS models are available for such analysis.

### 4.3.7 Maximum, Pin-to-Pin, PCB Interconnects Etch Lengths

**Table 3. Max Pin-to-Pin PCB Interconnect Recommendations[(1)] [(2)]**

| BUS | SIGNAL INTERCONNECT TOPOLOGY | | UNIT |
|---|---|---|---|
| | SINGLE BOARD SIGNAL ROUTING LENGTH | MULTI-BOARD SIGNAL ROUTING LENGTH | |
| **DMD** | | | |
| DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK and DMD_SAC_BUS | 4 max (101.5 max) | 3.5 max (88.91 max) | inch (mm) |
| **mDDR** | | | |
| MEM0_DQ(15:8), MEM0_UDM and MEM0_UDQS | 1.5 max 38.1 max | N/A | inch (mm) |
| **mDDR** | | | |
| MEM0_DQ(7:0), MEM0_LDM and MEM0_LDQS | 1.5 max (38.1 max) | N/A | inch (mm) |

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.

**Table 3. Max Pin-to-Pin PCB Interconnect Recommendations[(1)] [(2)] (continued)**

| BUS | SIGNAL INTERCONNECT TOPOLOGY | | UNIT |
|---|---|---|---|
| | SINGLE BOARD SIGNAL ROUTING LENGTH | MULTI-BOARD SIGNAL ROUTING LENGTH | |
| **mDDR** | | | |
| MEM0_CK_P, MEM0_CK_N, MEM0_A(12:0), MEM0_BA(1:0), MEM0_CKE, MEM0_CSZ, MEM0_RASZ, MEM0_CASZ and MEM0_WEZ | 2.5 max (63.5 max) | N/A | inch (mm) |

### 4.3.8 I/F Specific PCB Routing

**Table 4. High-Speed PCB Signal Routing Matching Requirements[(1)] [(2)] [(3)]**

| SIGNAL INTERCONNECT TOPOLOGY | | | | |
|---|---|---|---|---|
| IF | SINGLE GROUP | REFERENCE SIGNAL | MAX MISMATCH | UNIT |
| DMD | DMD_D(14:0), DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_OEZ | DMD_DCLK | ±500 (±12.7) | mil (mm) |
| | DMD_DAD_STRB, DMD_DAD_BUS | DMD_DCLK | ±750 (±19.05) | mil (mm) |
| | DMD_SAC_BUS | DMD_SAC_CLK | ±750 (±19.05) | mil (mm) |
| | DMD_SAC_CLK | DMD_DCLK | ±500 (±12.7) | mil (mm) |
| mDDR: | MEM0_CLK_P | MEM0_CLK_N | ±150 (±3.81) | mil (mm) |
| | Read/ Write Data Lower Byte: MEM0_LDM and MEM0_DQ(7:0) 38.1 max | MEM0_LDQS | ±300 (±7.62) | mil (mm) |
| | Read/ Write Data Upper Byte: MEM0_UDM and MEM0_DQ(15:8) | MEM0_UDQS | ±300 (±7.62) | mil (mm) |
| | Address and control: MEM0_A(12:0), MEM0_BA(1:0), MEM0_RASZ , MEM0_CASZ, MEM0_WEZ, MEM0_CSZ, MEM0_CKE | MEM0_CLK_P/ MEM0_CLK_N | ±1000 (±25.4) | mil (mm) |
| | Data strobes: MEM0_LDQS and MEM0_UDQS | MEM0_CLK_P/ MEM0_CLK_N | ±300 (±7.62) | mil (mm) |

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC2607 device, DMD, or mDDR memory.

(2) DMD data and control lines are DDR, whereas DMD_SAC and DMD_DAD lines are a single data rate. Matching the DDR lines is more critical and must take precedence over matching single data rate lines.

(3) mDDR data, mask, and strobe lines are DDR, whereas address and control are a single data rate. Matching the DDR lines is more critical and must take precedence over matching single data rate lines.

### 4.3.9 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.

### 4.3.10 Stubs

Avoid stubs.

### 4.3.11 Termination Requirements

| | |
|---|---|
| DMD I/F | Terminate all DMD I/F signals, with the exception of DMD_OEZ (specifically DMD_D(14:0), DMD_DCLK, DMD_TRC, DMD_SCTRL, DMD_LOADB, DMD_DAD_STRB, DMD_DAD_BUS, DMD_SAC_CLK, and DMD_SAC_BUS), at the source with a 10- to 30-Ω series resistor. TI recommends a 30-Ω series resistor for most applications because this minimizes overshoot, undershoot, and reduces EMI; however, for systems that must operate below –20°C, it may be necessary to reduce this series resistance to avoid narrowing the data eye too much under worse-case PVT conditions. TI recommends IBIS simulations for this worse-case scenario. |
| mDDR memory I/F | |
| mDDR differential clock | Terminate each line, specifically MEM0_CK(P:N), at the source with a 30-Ω series resistor. The pair must also be terminated with an external 100-Ω differential termination across the two signals as close to the DRAM as possible. (It may be possible to use a 200-Ω differential termination at the DRAM to save power while still providing sufficient signal integrity, but this has not been validated.) |
| mDDR data, strobe, and mask | Specifically MEM0_DQ(15:0), MEM0_LDM, MEM0_UDM, MEM0_LDQS, and MEM0_UDQS must be terminated with a 30-Ω series resistor located midway between the two devices. |
| mDDR address and control | Specifically MEM0_A(12:0), MEM0_BA(1:0), MEM0_CKE, MEM0_CSZ, MEM0_RASZ, MEM0_CASZ, and MEM0_WEZ should be terminated at the source with a 30-Ω series resistor. |

For applications where the routed distance of the mDDR or DMD signal can be kept to less than 0.75 inches, this signal is short enough not to be considered a transmission line and does not need a series terminating resistor.

### 4.3.12 DMD Flex Cable Interface Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board-to-board connector with a flex cable. The tlex cable provided the interface of data and control signals between the DLPC2607 controller and the DLP2000 DMD. For detailed layout guidelines, see the DLPC2607 controller layout guidelines under Section 4.3.5 and Section 4.3.4.

Follow these layout guidelines for the flex cable interface with the DMD:

- Minimize the number of layer changes for DMD data and control signals.
- DMD data and control lines are DDR, whereas DMD_SAC and DMD_DRC lines are a single data rate. Matching the DDR lines is more critical and must take precedence over matching single data rate lines.

Figure 12 and Figure 13 show the top and bottom layers of the DMD flex cable connections.

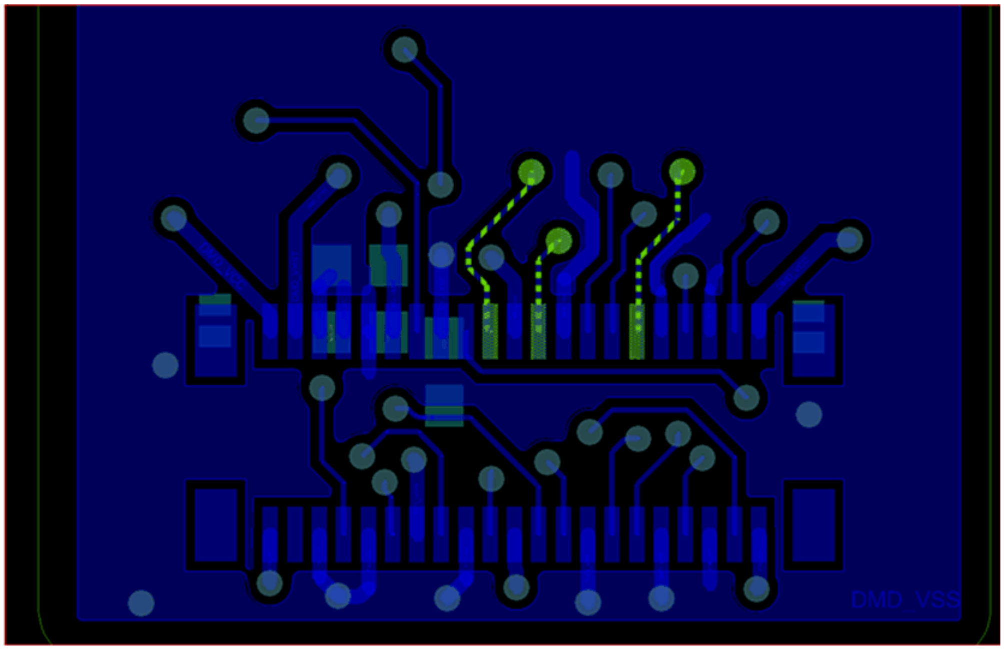

Figure 12. DMD Flex Cable—Top Layer

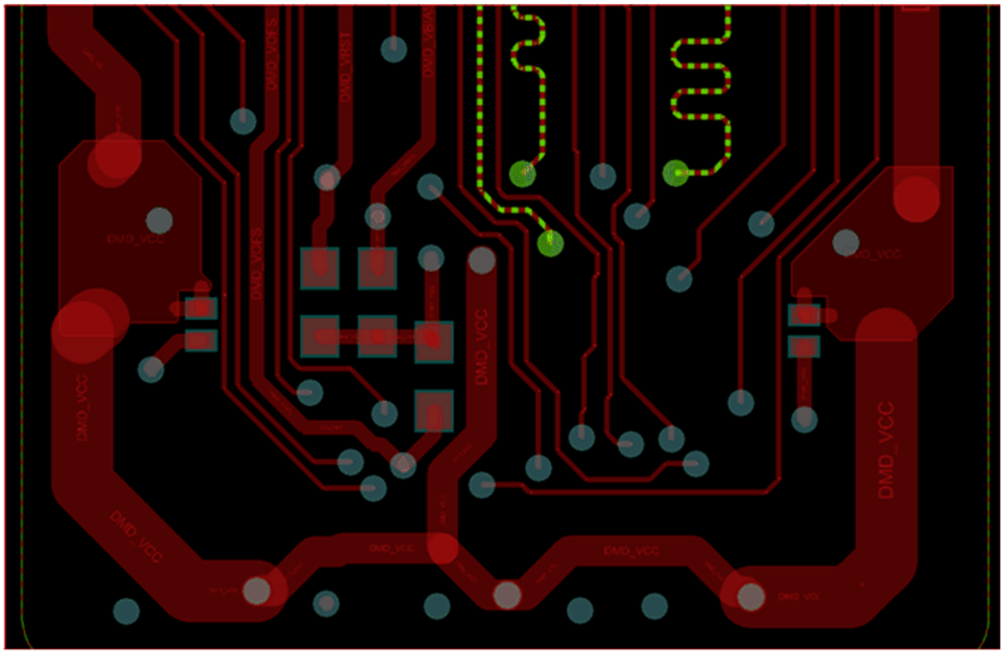

Figure 13. DMD Flex Cable—Bottom Layer

### 4.3.13 Layout Guidelines for Switching Power Supply

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulators could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. Input capacitors, output capacitors, and inductors must be placed as close as possible to the device.

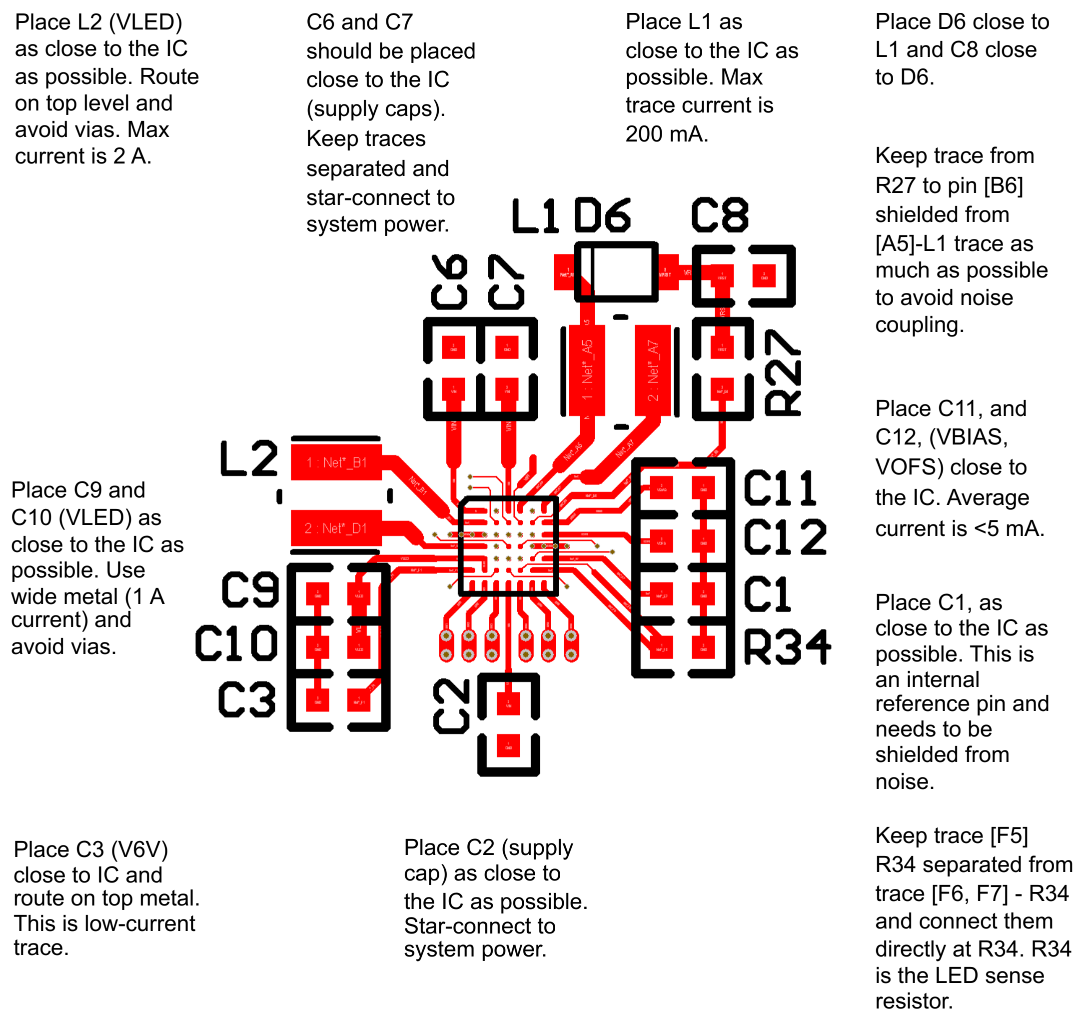


**Figure 14. Layout Example for Switching Power Supply**

**Table 5. Layout Components for Switching Power Supply**

| LABEL | DESCRIPTION |
|---|---|
| C1 | V2V5 output filter cap |
| C2 | VINA input cap |
| C3 | V6V output filter cap |
| C6 | VINL input cap |
| C7 | VINR input cap |
| C8 | VRST output filter cap |
| C9 | VLED output filter cap |
| C10 | VLED output filter cap |
| C11 | VBIAS output filter cap |
| C12 | VOFS output filter cap |
| D6 | VRST rectifying diode |
| L1 | DMD supply inductor |
| L2 | VLED buck-boost inductor |
| R27 | 100k VRST feedback resistor |
| R34 | 100m RLIM sense resistor |

#### 4.3.14 Layout Prints

To download the layer plots, see the design files at TIDA-01473.

### *4.4 Altium Project*

To download the Altium project files, see the design files at TIDA-01473.

### *4.5 Gerber Files*

To download the Gerber files, see the design files at TIDA-01473.

### *4.6 Assembly Drawings*

To download the assembly drawings, see the design files at TIDA-01473.

## 5 Software Files

To download the software files, see the design files at TIDA-01473.

## 6 Related Documentation


1. Texas Instruments, *TI DLP® LightCrafter™ Display 2000 EVM User's Guide*, DLPDLCR2000EVM User's Guide (DLPU049)
2. Texas Instruments, *DLPC2607 Software Programmer's Guide* (DLPU013)
3. Texas Instruments, *DLPC2607 DLP PICO Processor 2607 ASIC*, DLPC2607 Datasheet (DLPS030)
4. Texas Instruments, DLP2000 DMD Datasheet (DLPS078)
5. Texas Instruments, DLPA1000 Power Management and LED Driver IC, DLPA1000 Datasheet (SLVSDP7)


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