TI Designs: TIDA-01512

PMBus™ Voltage Regulator Reference Design for NXP QorIQ® LS2085A/LS2088A Processors

Description

This reference design uses the TPS53681 multiphase controller and CSD95490Q5MC smart power stages to implement a high-performance design suitable for powering NXP QorIQ® communication processors, specifically the LS2085A and LS2088A variants. The dual outputs of the controller target a four-phase 60-A_{TDC}, 1.0-V core rail (VDD) and a two-phase 30-A_{TDC}, 1.2-V auxiliary rail (GVDD). The smart power stages and integrated PMBus™ allow for easy output voltage setting and telemetry of key design parameters. The design enables configuration, smart VID adjustment, and compensation adjustment of the power supply, while providing monitoring of input and output voltage, current, power, and temperature. TI's Fusion Digital Power™ Designer is used for programming, monitoring, validation, and characterization of the system. Additionally, the D-CAP+™ modulator of the TPS53681 coupled with the optimized gate driver and FETs of the CSD95490Q5MC greatly reduces the amount of output capacitance required for both rails by over 50% of the NXP evaluation boards.

Features

- Dual Rail 4+2 Design—Targeting LS2085A/LS2088A VDD and GVDD Rails
- Peak Efficiencies of 92% and 94% for VDD and GVDD Rails
- D-CAP+ Modulator for Superior Current-Sharing Capabilities and Transient Response
- PMBus Compatibility for Output Voltage Setting and Telemetry for V_{IN}, V_{OUT}, I_{OUT}, and Temperature
- Dual Rail Temperature Monitoring for Independent Tracking of Thermal Performance
- Full Compensation Tuning Through PMBus
- Minimal Output Capacitance Required for 50-mV and –30-mV Overshoot and Undershoot Targets Under Maximum Transient Conditions

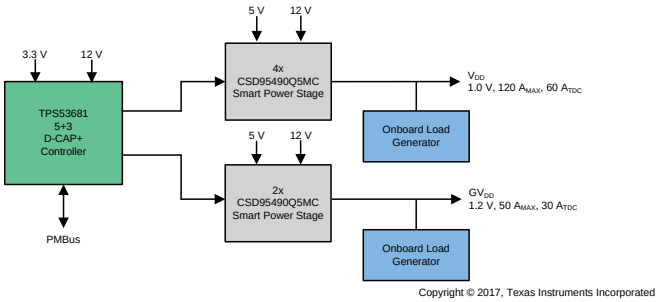
Applications

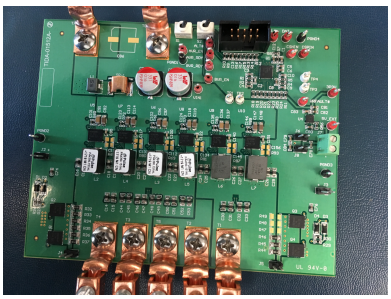
- Campus and Branch Switches
- Data Center Switches
- Small Cells Base Station

Resources

TIDA-01512	Design Folder
TPS53819	Product Folder
CSD95490Q5MC	Product Folder
Fusion Digital Power™ Designer	Product Folder

TI E2E™ Community — ASK Our E2E Experts





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Description

This is a power-dense, high-performance design targeted at powering NXP QorIQ communications processors commonly found in wireless infrastructure and base station applications. The dual-output multiphase controller and TI's proprietary smart power stages allow for an integrated design, which, when compared to more traditional discrete designs, eliminates a number of passive components and reduces the printed-circuit board (PCB) layout area. These processors require excellent thermal performance, efficiency, and a fast transient response from their voltage regulators while also requiring on-the-fly optimization through PMBus. This design meets all the criteria with a simple thermal solution and minimal number of output capacitors when compared to the regulator solution on the NXP processor evaluation board. The total capacitance on each output and number of capacitors has been reduced by approximately half.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input supply	12 V, ±5%
DC tolerance	± 0.5%
AC tolerance	50 mV and –30 mV
Switching frequency	600 kHz
Nominal output voltage – VDD	1.0 V
Max output current – VDD	120 A
TDC current – VDD	60 A
DC load line – VDD	—
Max load step – VDD	60 A at 12 A/µs
Number of phases – VDD	4
Nominal output voltage – GVDD	1.2 V
Max output current – GVDD	50 A
TDC current – GVDD	30 A
DC load line – GVDD	—
Max load step – GVDD	20 A at 12 A/µs
Number of phases – GVDD	2

2 System Overview

2.1 Block Diagram

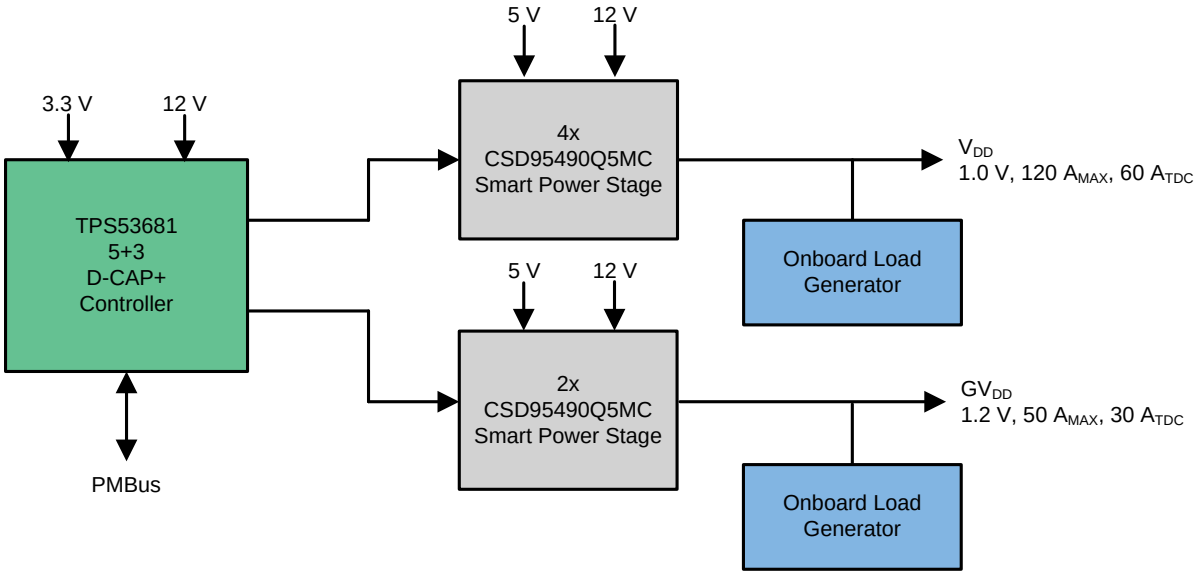


Figure 1. Block Diagram

2.2 Highlighted Products

2.2.1 TPS53681—Dual-Channel (6-Phase + 2-Phase) or (5-Phase + 3-Phase) D-CAP+™ Step-Down Multiphase Controller with NVM and PMBus™

- Easily configurable for a wide range of dual-output voltage scenarios
- Programmable loop compensation through PMBus
- Configurable with non-volatile memory (NVM) for low external component counts
- Dynamic phase shedding with programmable current threshold for optimizing efficiency at light and heavy loads
- PMBus system interface for telemetry of voltage, current, power, temperature, and fault conditions
- Dual-rail temperature monitoring
- 5-mm × 5-mm, 40-pin, QFN PowerPad™ package

2.2.2 CSD95490Q5MC—75-A Synchronous Buck NexFET™ Power Stage With DualCool™ Packaging

- 75-A continuous current capability
- 95% system efficiency at 25 A
- Up to 1.25-MHz switching frequencies supported
- Temperature-compensated bidirectional current sense signal
- Analog temperature output and fault monitoring
- High-density, low-inductance, SON 5-mm × 6-mm package

2.3 System Design Theory

The D-CAP+ modulator of the TPS53681 controller is integral to the high-performance of this reference design. This modulator allows the control loops of both rails to remain stable over a wide range of operating conditions because the transfer function is insensitive to variations in input voltage, load current, and phase number. Phase margins of 67° and 86° were measured for the VDD and GVDD rails, respectively, with crossover frequencies of 83 kHz and 159 kHz. Placing the unity gain frequencies higher than 1/10 the switching frequencies allows for a faster transient response that can keep V_{OUT} within its regulation limits during large load steps, such as the 60-A step on the core rail. Stability is maintained even as the load current duty cycle and frequency are varied. A faster transient response also directly leads to the significant reduction of output capacitors over the processor reference design for both rails.

Loop compensation can easily be adjusted through the PMBus using TI's Fusion graphical user interface (GUI), which allows the user to tune the design for a wide range of output filters, including using all ceramic output capacitors should the design requirements change. At high load currents, the D-CAP+ modulator can keep all phase currents evenly balanced to avoid thermally stressing or damaging either the field-effect transistors (FETs), inductors, or processor while maintaining tight output voltage regulation.

The CSD95490Q5MC smart power stage features an optimized driver-FET solution in a thermally-efficient package that provides high efficiency up to 75 A of DC load current. Higher efficiency leads to lower power loss and thus excellent thermal performance, allowing for smaller heat sinks and less airflow, making thermal design simpler than less efficient power stages. Integrated fault monitoring and temperature reports back to the TPS53681 controller and complements the PMBus functionality, which allows for operational telemetry, painless debug, validation, and configuration of the design. On-chip, temperature compensated, bidirectional current sensing offers increased accuracy over operational corners compared to the simple, un-temperature compensated, DCR sense method used on the NXP reference design.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The hardware for this design is as follows:

- 12-V, 20-A power supply
- 5-V, 1-A power supply
- 500-MHz oscilloscope with differential and passive probes
- Function generator capable of pulse with < 1-µs rise times (hook to J2 or J3 on load transient circuits)
- Digital multimeter
- USB interface adapter EVM

3.1.2 Software

This design uses TI's Digital Fusion Power Designer software.

3.2 Testing and Results

3.2.1 Test Setup

Figure 2 shows the test setup of this reference design.

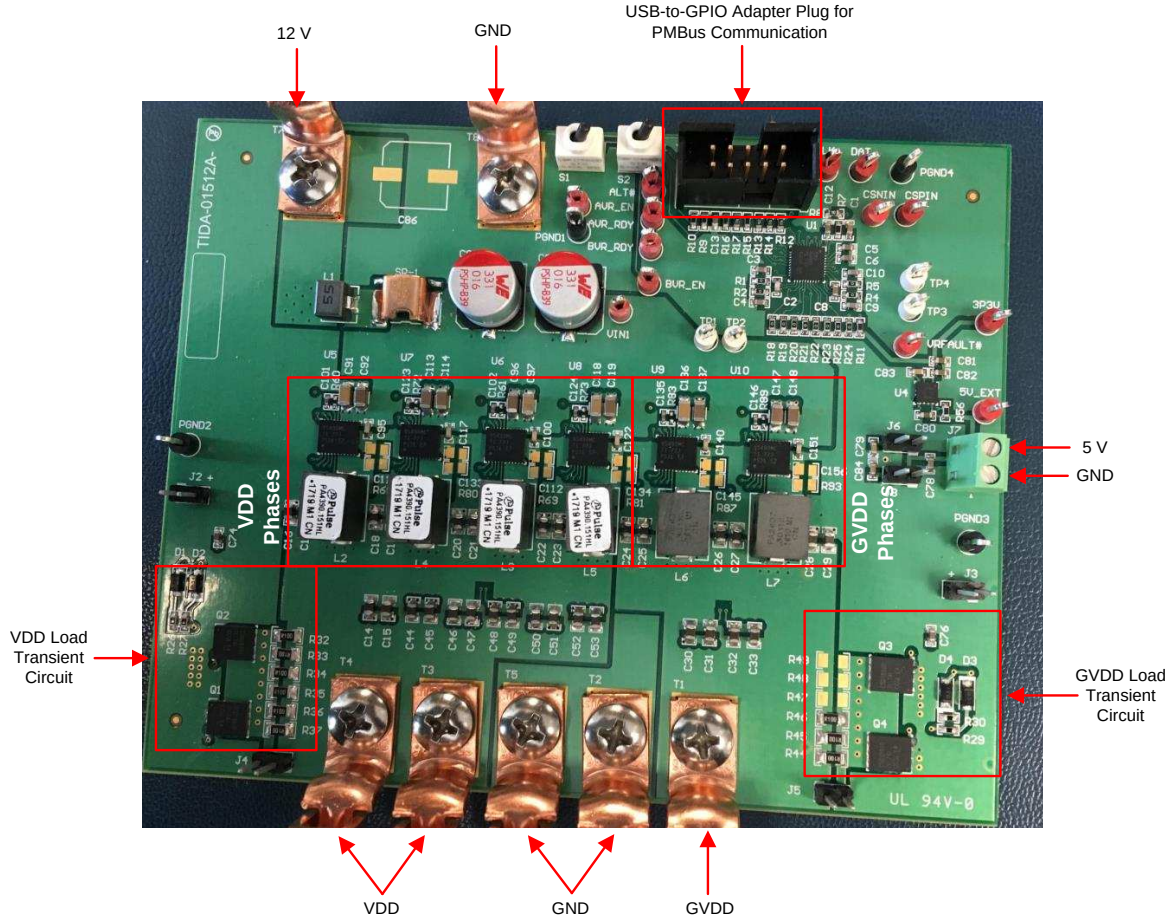


Figure 2. TIDA-01512 Test Setup

3.2.2 Test Results

3.2.2.1 Efficiency and Power Loss

For the VDD rail, a peak efficiency of 92.4% was measured at the target output voltage of 1.0 V at 17.5 A of load current (see Figure 3, Figure 4). A 91.3% efficiency was measured at the 60-A thermal design current (TDC). Both the efficiency and loss curves include the inductor losses and 5-V rail losses of the CSD95490Q5MC power stages.

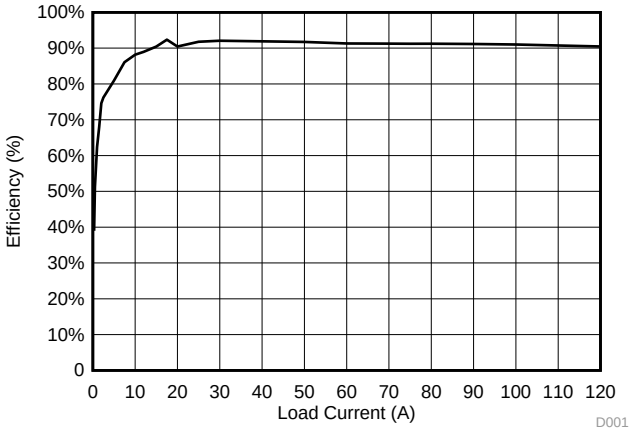


Figure 3. VDD Rail 12-V to 1-V Efficiency

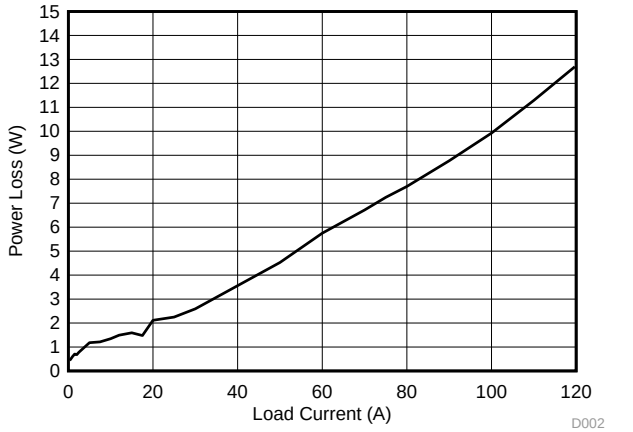


Figure 4. VDD Rail 12-V to 1-V Power Loss

Efficiency measurements on the dual-phase GVDD rail were taken with the inductor, and 5-V power stage loss are also included in the results (see Figure 5, Figure 6). A peak efficiency of 93.8% was measured at 15 A while the 30-A TDC efficiency was 93.5%. Because of the high currents and low voltages of this application, care was taken during the measurements to sense the input voltage cross the power stage ceramic capacitors and the output voltage from the output side of the inductors, to minimize the influence of parasitic losses of the test setup.

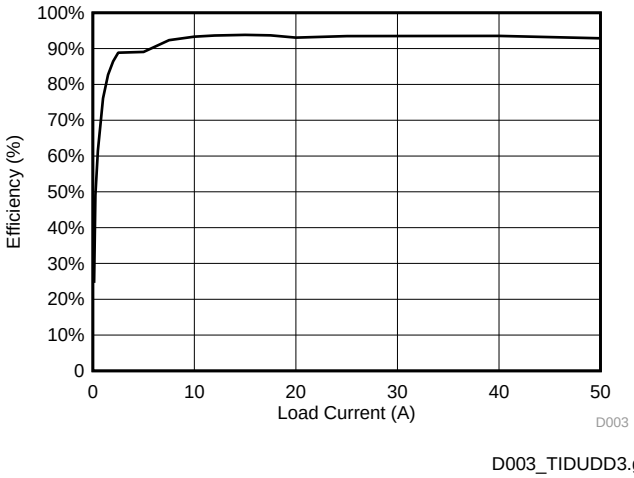


Figure 5. GVDD 12-V to 1.2-V Efficiency

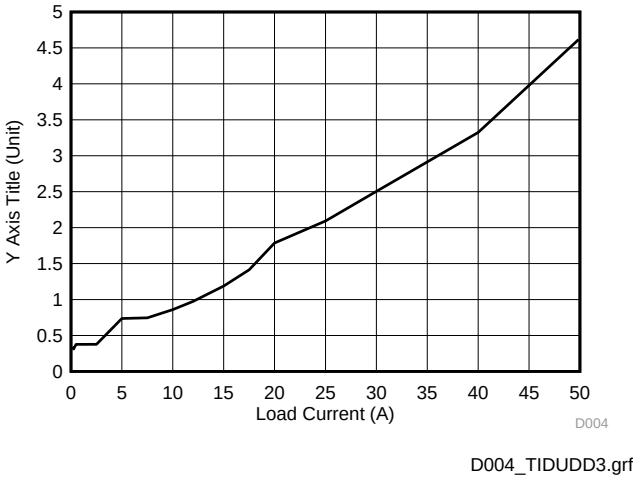


Figure 6. GVDD 12-V to 1.2-V Power Loss

3.2.2.2 Steady-State Regulation and DC Accuracy

Both rails of this design were tested for steady-state stability across their entire load ranges without recording any failures or anomalies. DC ripple remained within 2% or less of the output voltage, and the measured switching frequency was within the data sheet limits. Care was taken to ensure that the noise floor of the output voltage differential probe did not impact the results to cause false failures in output ripple or stability. TI recommends probing a phase node during testing to check against any possible questions regarding stability that may be attributed to a noisy differential probe. The design is likely stable if the switching frequency is consistent between phase pulses, and varies within the TPS53681 data sheet limits. If an adequate differential probe is not available, a passive probe with tight ground connection should be used instead to verify the design.

Figure 7, Figure 8, and Figure 9 show the results from the VDD rail at 10 A, 60 A, and 200 A.

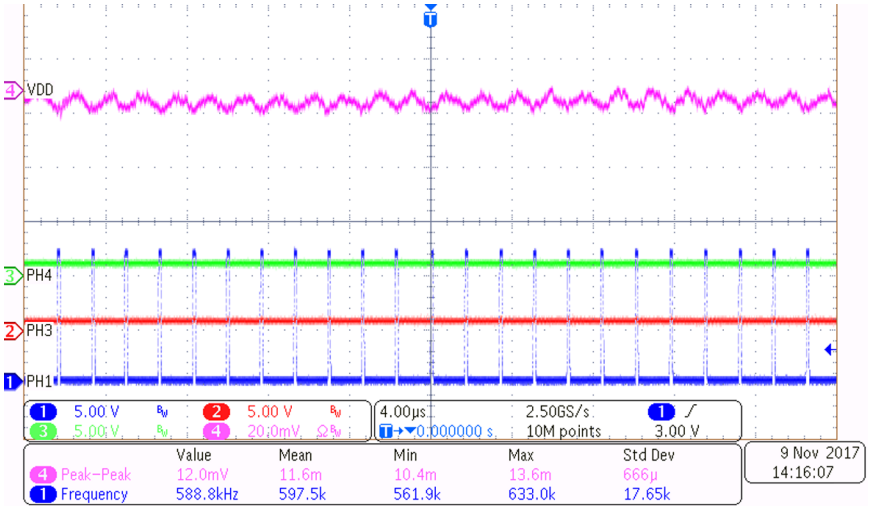


Figure 7. VDD Rail—Steady State, 10 A

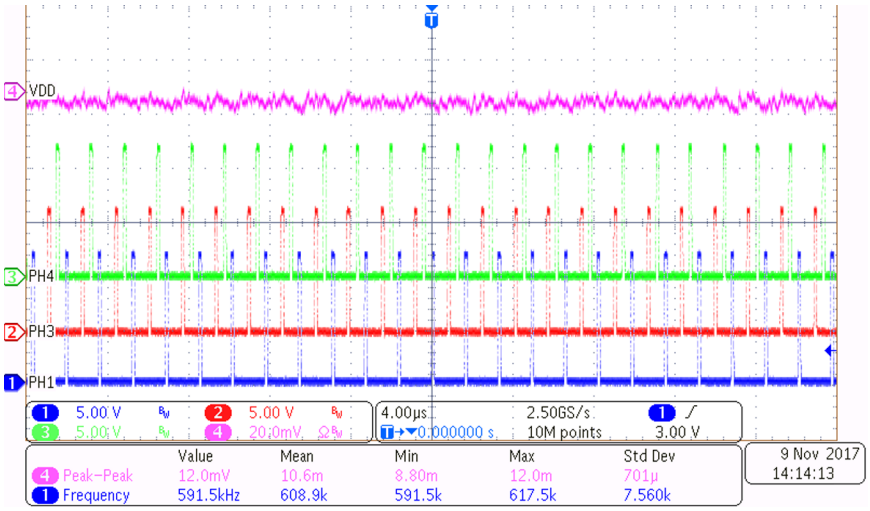


Figure 8. VDD Rail—Steady State, 60 A

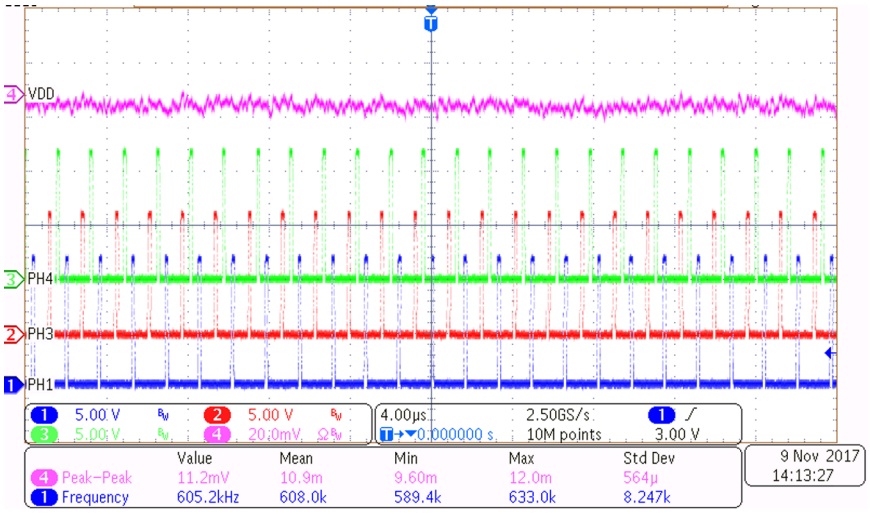


Figure 9. VDD Rail—Steady State, 120 A

Figure 10 and Figure 11 show the auxiliary rail results at 10 A and 30 A. These figures also show multiple phase nodes at each load current to demonstrate the dynamic add/drop capabilities of the controller properly balancing the phase currents while maintaining output and switching frequency stability.

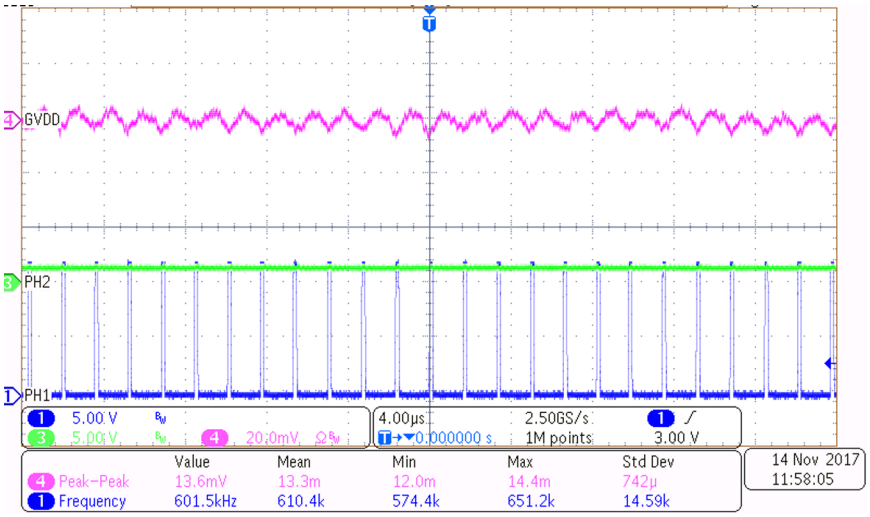


Figure 10. GVDD Rail—Steady State, 10 A

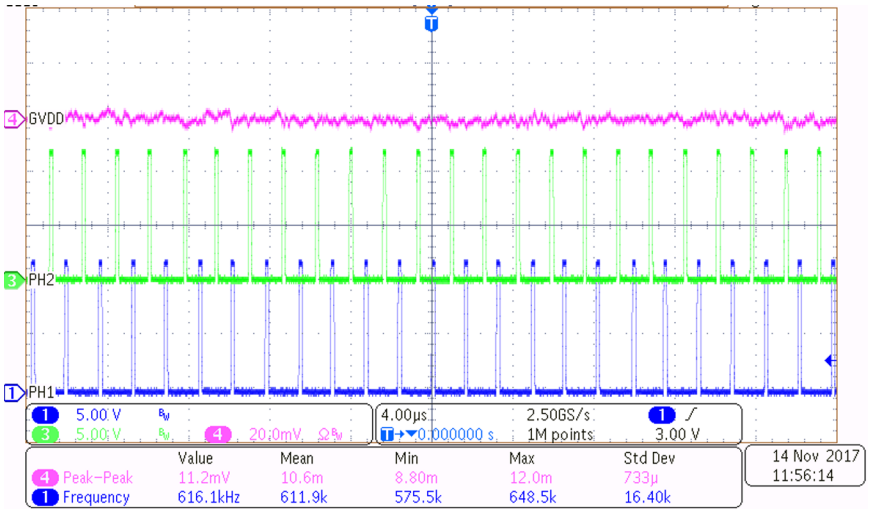


Figure 11. GVDD Rail—Steady State, 30 A

The DC accuracy on both rails of the system was measured across their entire load ranges to ensure that each output remained within the ±5% allowable window. Figure 12 and Figure 13 show that both rails fall well within the allowable limits by over a factor of 10. This leaves plenty of margin for any additional variations such temperature, PCB layout, and output capacitor mix.

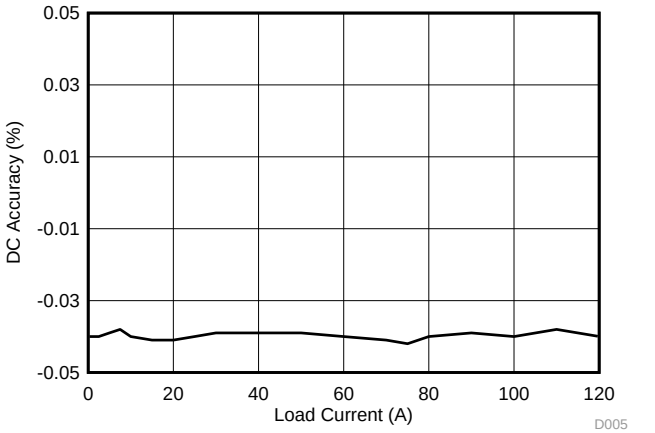


Figure 12. VDD Rail DC Accuracy

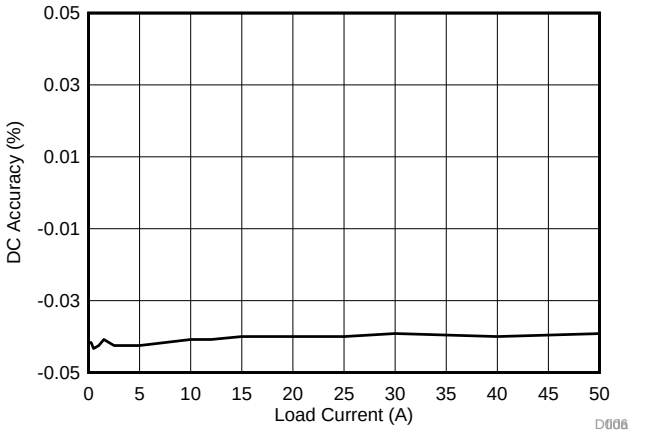


Figure 13. GVDD Rail DC Accuracy

3.2.2.3 Transient Response

Load transient circuits were placed on the board close to the output of both rails to generate the 60-A and 20-A steps at the target slew rate of 12 A/µs. Because of the slower load step slew rate compared to other processors, a transient frequency sweep was not performed on either rail. Any frequencies that could be tested were well within the bandwidth of the control loop and posed no issue to stability. At higher frequencies, the load current did not have time to reach its target before the transient event ended, resulting in less overshoot and undershoot than what was measured for the single-step responses. Overall the responses of both the VDD and GVDD rails looked excellent and the measured over- and undershoots were less than NXP's allowable targets with output capacitances of less than half.

For the main processor rail, the single-step response Figure 14 shows only 19.6 mV of undershoot, which is over 10 mV less than the 30-mV target. Figure 15 shows the overshoot at 26.4 mV, which is just over half of the 50 mV allowed. The output voltage remained stable and within the target window as the load duty cycle was swept from 10% to 80%, as shown in Figure 16.

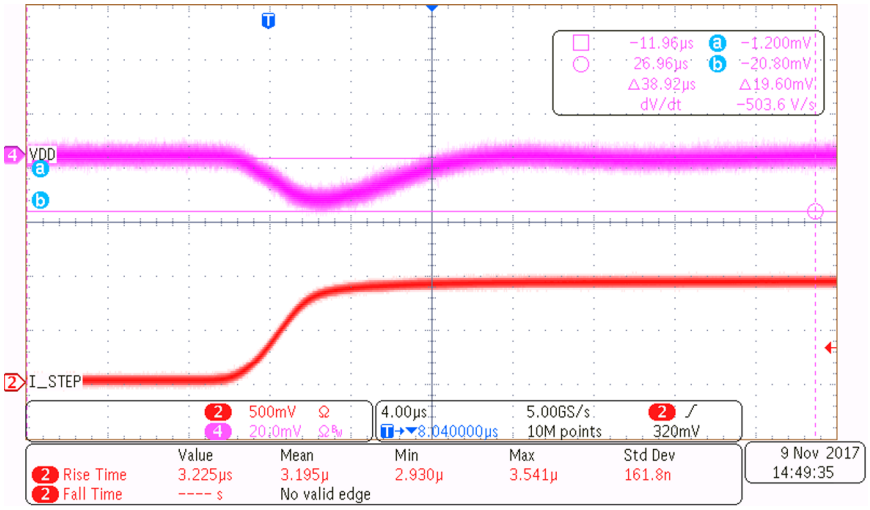


Figure 14. VDD Rail—60-A to 120-A Transient Undershoot, 10% Duty Cycle

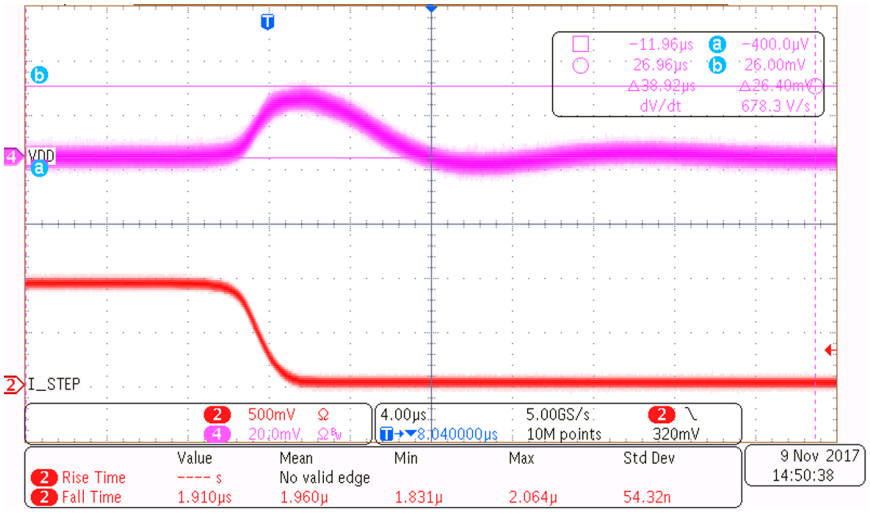


Figure 15. VDD Rail—60-A to 120-A Transient Overshoot, 10% Duty Cycle

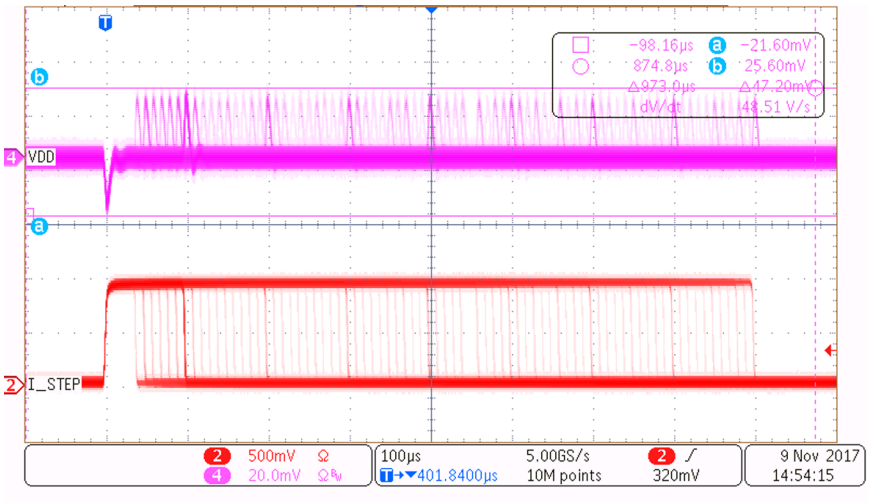


Figure 16. VDD Rail—60-A to 120-A Transient, 10% to 80% Duty Cycle Sweep

A 20-A current step was applied to the auxiliary rail using an onboard load circuit and the undershoot, as shown in Figure 17, measuring under half of the allowable swing at just 13.2 mV. The measured overshoot is 22.8 mV, which is less than the target of 50 mV (see Figure 18). The transient response was also tested as the load duty cycle (see Figure 19) was swept from 10% to 80%, with no observed issues.

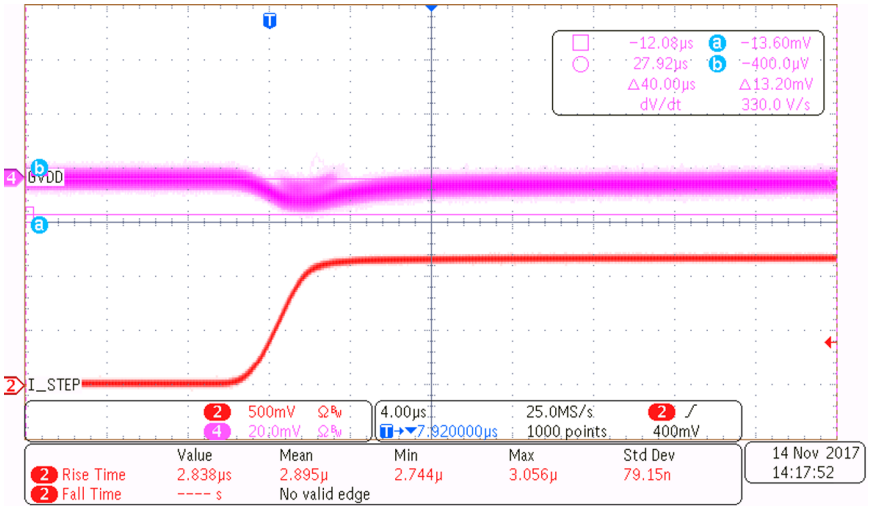


Figure 17. GVDD Rail—30-A to 50-A Transient Undershoot, 10% Duty Cycle

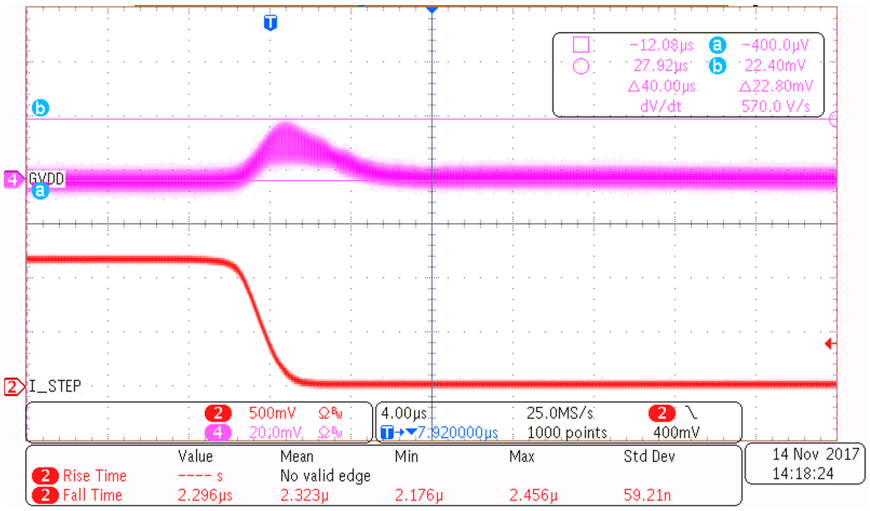


Figure 18. GVDD Rail—30-A to 50-A Transient Overshoot, 10% Duty Cycle

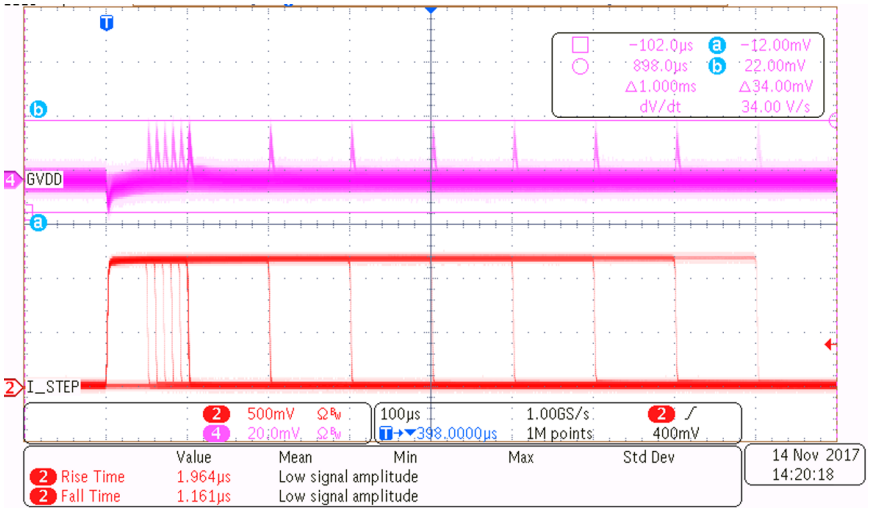


Figure 19. GVDD Rail—10-A to 20-A Transient, 10% to 80% Duty Cycle Sweep

3.2.2.4 Additional Small Signal Stability Testing

Because transient frequency sweeps were unfeasible for this design, Bode plots for each rail were taken using a network analyzer to determine the transfer function, and to further check the stability of the control loop for each one. For VDD (see Figure 20) a unity gain frequency of 83.6 kHz is measured with a phase margin of 66.9°, which indicates stability. The GVDD rail is also stable with a phase margin of 86.5° at a crossover of 160 kHz (see Figure 21).

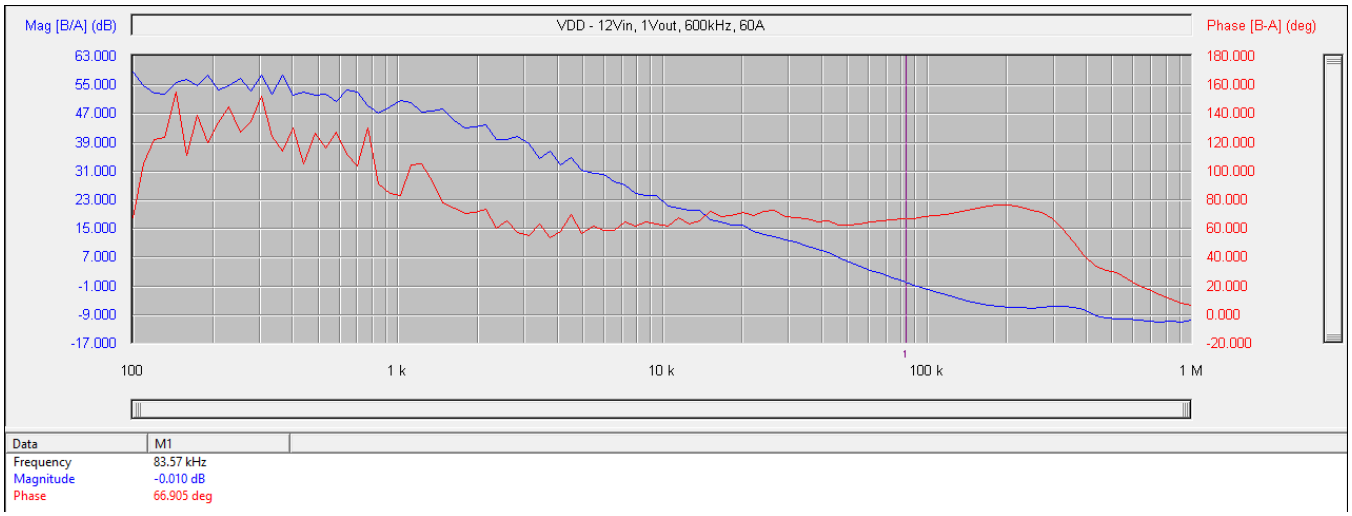


Figure 20. VDD—Bode Plot

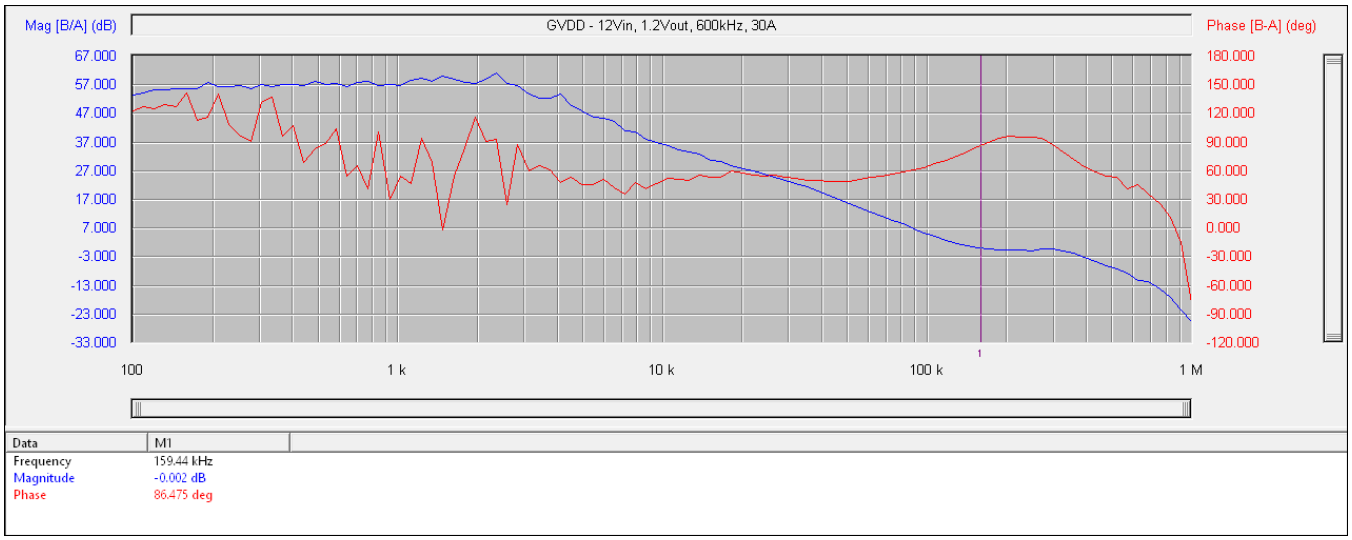


Figure 21. GVDD Rail—Bode Plot

Both Bode plots indicate stability, but the flattening of the gain curves above the unity frequency is troubling. The rails may only be conditionally stable, which can lead to issues when the design has gone to production. Nyquist plots must be used to definitely prove stability. As a reminder, the Nyquist plot is stable if no encirclements of the point (–1, 0) occur as the test frequency is swept during testing. The gain and phase margins can also be checked again from these results.

Looking at Figure 22, no encirclements of (–1, 0) occur and at nowhere does the plot approach the point which indicates proper stability and margin in the design. The phase margin matches the Bode plot results at 66.9M °, and on this plot there is infinite gain margin because the loop phase never reaches 180°—at least not up to 1 MHz. For the GVDD rail (see Figure 23), no encirclements of (–1, 0) are seen and again there is plenty of margin. The Nyquist and Bode phase margins are also matching, and here there is 19 dB of gain margin in the system. Between the Bode plots, Nyquist plots, and the transient results, it is safe to conclude that both the VDD and GVDD control loops are stable.

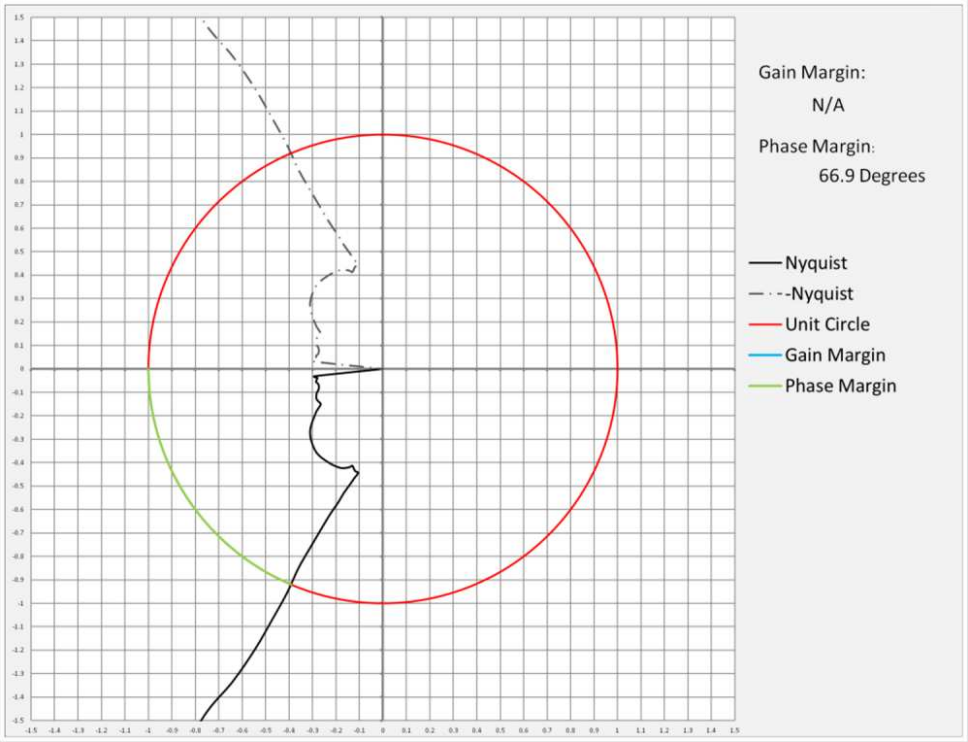


Figure 22. VDD Rail—Nyquist Plot

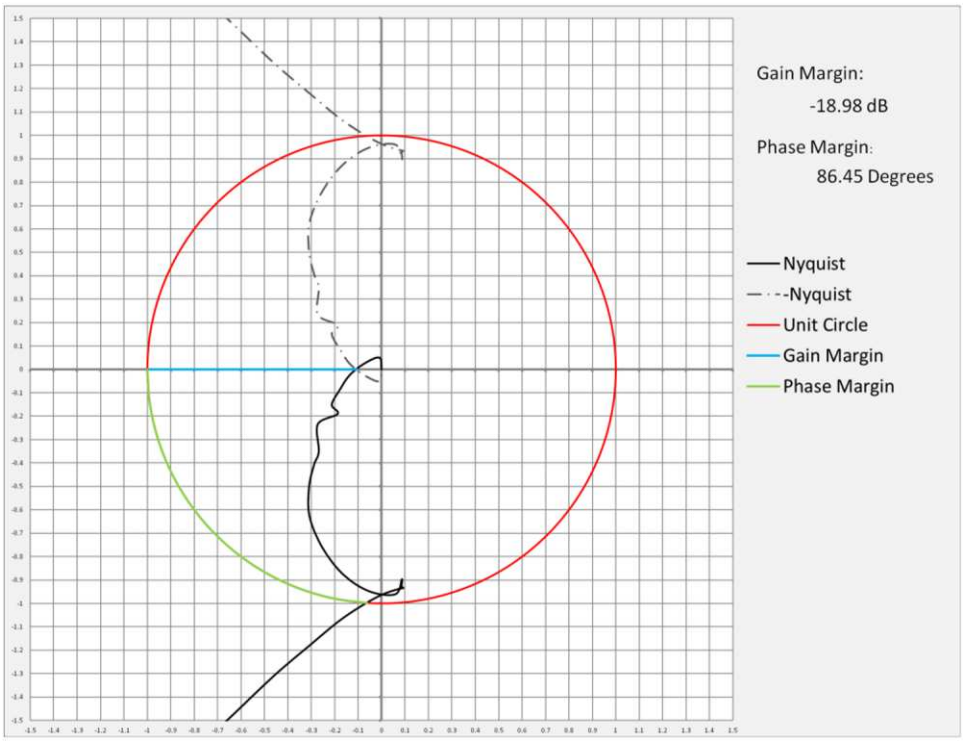


Figure 23. GVDD Rail—Nyquist Plot

Special thanks to former TI intern Mark Chounlakone for his hard work developing the Nyquist Plot tool over the summer of 2017.

3.2.2.5 Thermal Performance

The thermal performance of each rail was tested both separately and together to check the design's performance. During testing, the ambient temperature was 23°C for each test case, and the design was allowed to soak for 5 minutes under load to reach thermal equilibrium. A fan providing 500 ft/min (200 Lfm) of airflow across the board was also used. In a real application, however, any airflow would likely be used in conjunction with heat sinks on the power stages, so this test is slightly worse than a typical operating environment.

Both the standalone and combined measurements were done with the rails loaded to their thermal design currents of 60 A and 30 A. Simultaneous loading only increased the hottest recorded temperature, marginally making it easier to implement a full thermal solution later in the design process.

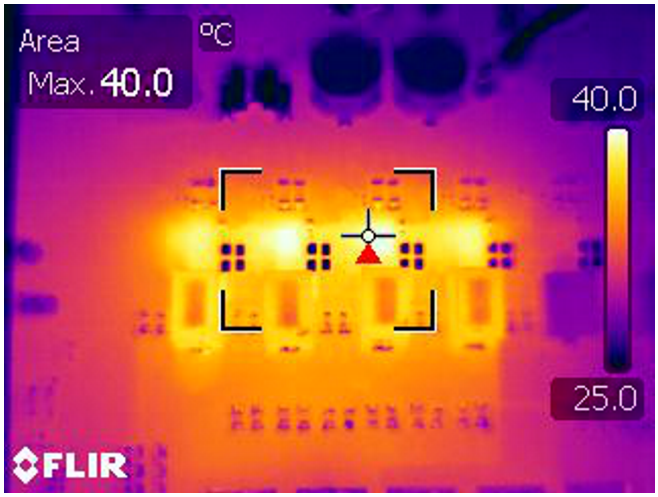


Figure 24. VDD Rail Power Stage Temperatures, 60-A Load

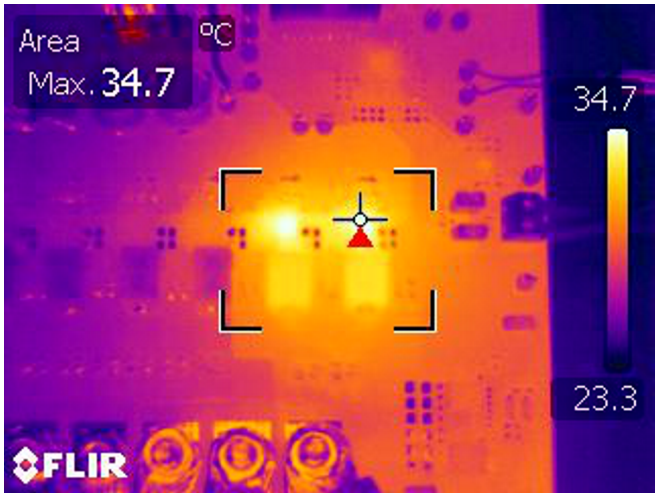


Figure 25. GVDD Rail Power Stage Temperatures, 30-A Load

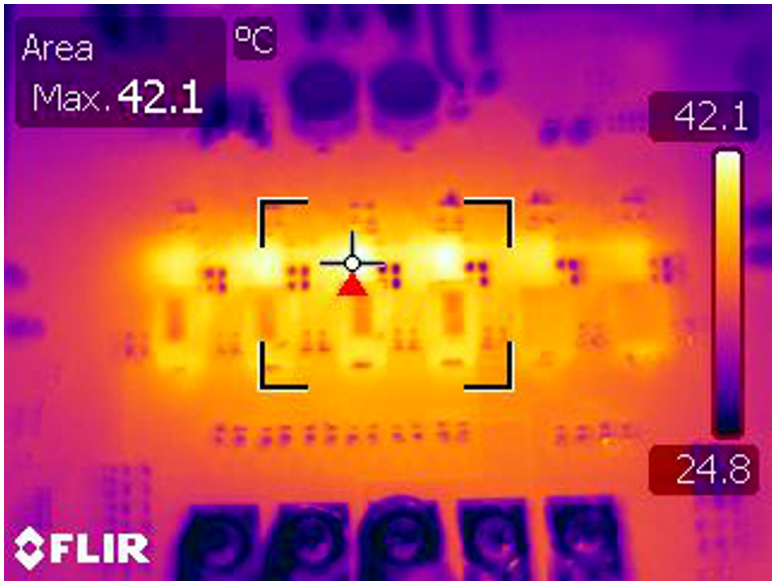


Figure 26. Dual-Rail Power Stage Temperatures

3.2.2.6 Start-up and Shutdown Performance

The VDD and GVDD rails were powered both up and down under heavy and light loads to check for proper operation. During this time, the output voltage was probed to look for monotonic behavior, and investigate the potential for overshoot. Additionally, the first and final phase nodes were also probed to ensure the TPS53681 could properly add and remove phases as conditions dictated.

During a voltage transition, such as at start-up, all phases of a rail are activated to quickly slew the output to the correct voltage. At light loads, when fewer phases are required (possible only one), the controller turns off any unnecessary phases after determining the output voltage has settled once, and the appropriate ready signal goes high (see Figure 27 and Figure 31). When high currents are required after start-up (Figure 28 and Figure 32) all phases remain active to maintain regulation when the output settles to its proper setting. No matter the output current, when a rail is disabled and its ready signal falls low, the TPS53681 tri-states each active phase and lets the output voltage decay according to the load current (Figure 29, Figure 30, Figure 33, Figure 34).

No issues were seen during the validation of this design during start-up or shutdown. VDD and GVDD exhibited no overshoot nor any abnormal dips during transition. Any ringing seen below ground on shutdown is solely due to the electronic load on the output trying to maintain the set current. In a real application, this ringing would not be present.

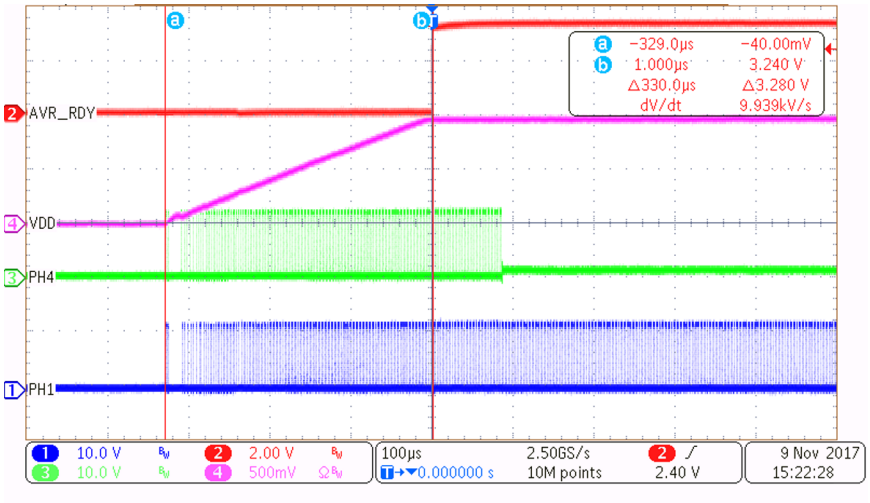


Figure 27. VDD Rail—10-A Start-up

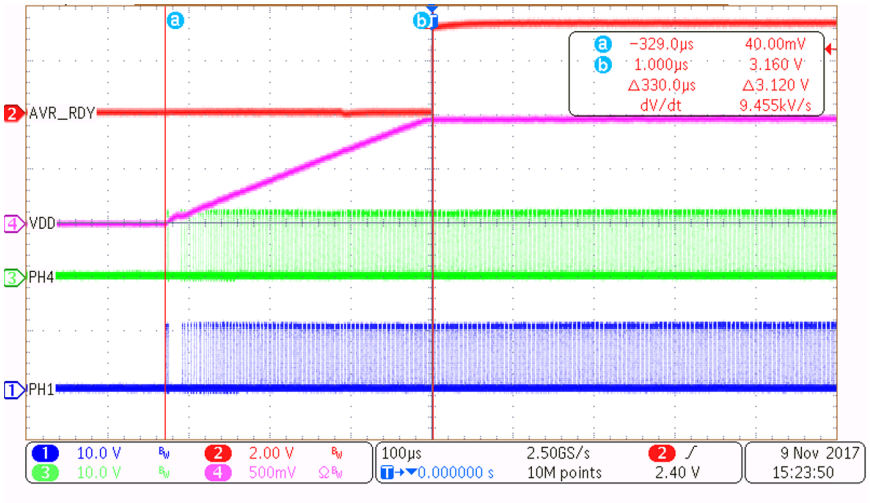


Figure 28. VDD Rail—60-A Start-up

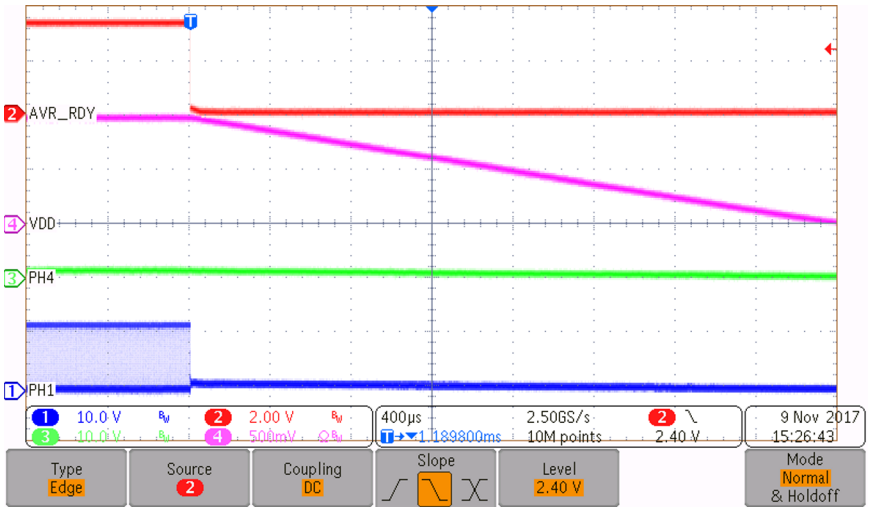


Figure 29. VDD Rail—10-A Shutdown

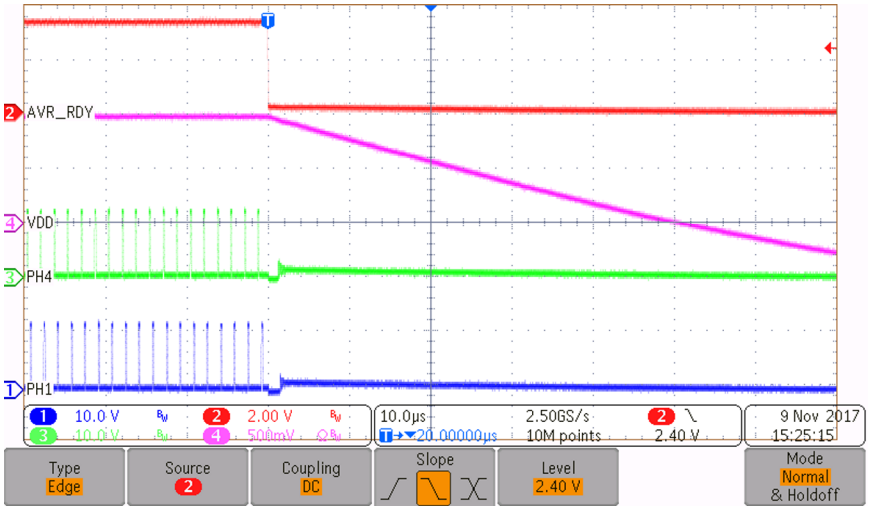


Figure 30. VDD Rail—60-A Shutdown

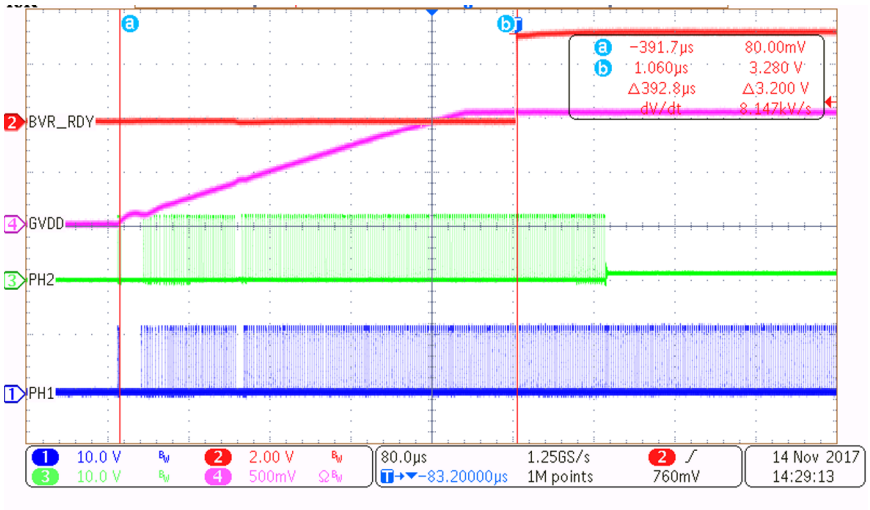


Figure 31. GVDD Rail—10-A Start-up

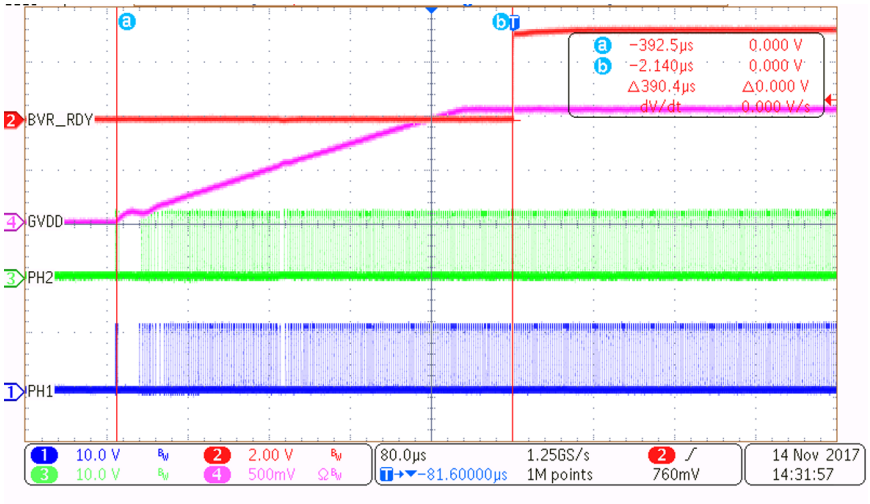


Figure 32. GVDD Rail—30-A Start-up

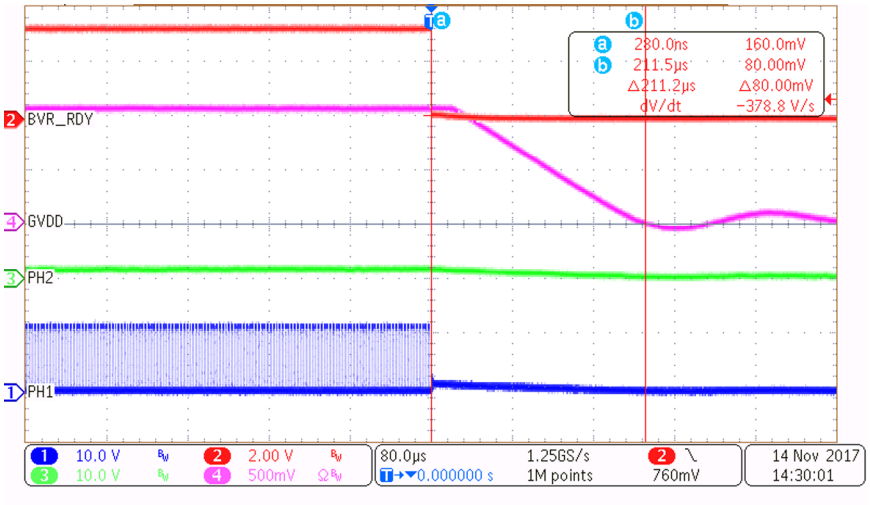


Figure 33. GVDD Rail—10-A Shutdown

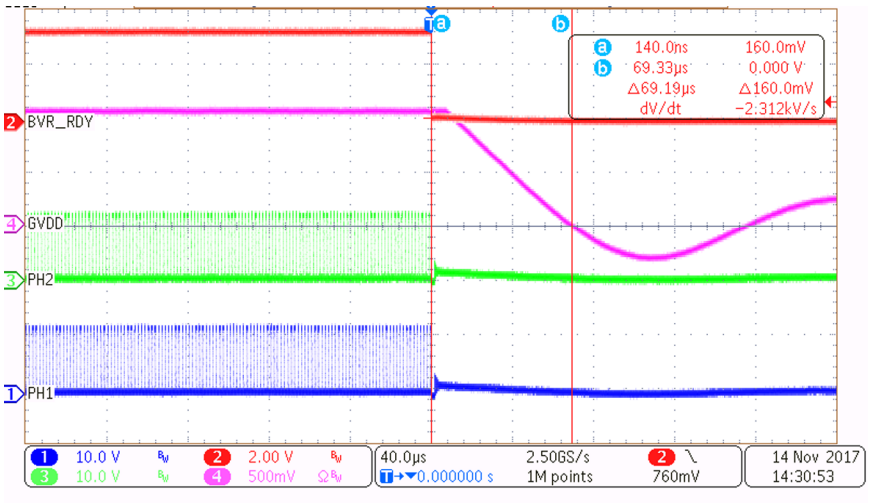


Figure 34. GVDD Rail—30-A Shutdown

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01512.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01512.

4.3 PCB Layout Recommendations

Follow all the layout instructions as specified in the respective data sheet for each part when laying out a design using the TPS53681 controller and CSD95490 smart power stage. Some other guidelines to consider include:

- Keep the layout for all six phases on the core rail identical to ensure optimal current balancing and thermal performance between phases.
- Route noisy traces such as pulse-width modulation (PWM) and the PMBus lines on a separate layer than the sensitive analog sense lines such as VSP, VSN, CSP, VREF, and so forth.
- Use quality capacitors for both the input and output decoupling to obtain the maximum performance possible with respect to DC ripple and transient response. Ceramic capacitors must be rated to at least 16 V on V_{IN} and 2.5 V on V_{OUT}, with a dielectric rating of X5R or better.
- Ensure that the V_{OUT} and GND nodes are routed on multiple layers of copper and connected with enough vias to handle the current requirements for the best thermal performance. Following this guideline allows for a maximum amount of heat to flow out of the power stages and inductors into the board.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01512 .

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01512.

5 Software Files

To download the Fusion Digital Power Designer software, see the following tool folder.

6 Related Documentation

1. Texas Instruments, *TPS53681 Dual-Channel (6-Phase + 2-Phase) or (5-Phase + 3-Phase) D-CAP+™ Step-Down Multiphase Controller with NVM and PMBus™ Data Sheet*
2. Texas Instruments, *CSD95490Q5MC Synchronous Buck NexFET™ Smart Power Stage Data Sheet*
3. NXP, *LS2088A-RDB: QorIQ® LS2088A Reference Design Board*
4. NXP LS2088A Data Sheet LS2088AEC
5. NXP QorIQ LS2088A/LS2048A Design Checklist AN4977

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7 About the Author

CARMEN PARISI is a Senior Applications Engineer working in the Multiphase and Control Solutions (MCS) group at TI developing reference designs and application notes. He has six years of experience in power electronics working on mobile, desktop, and server V_{CORE} applications; battery chargers; and system PMICs. Carmen earned a combined BS/MS degree in electrical engineering from the Rochester Institute of Technology.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2018) to A Revision	Page
• Changed Applications	1

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