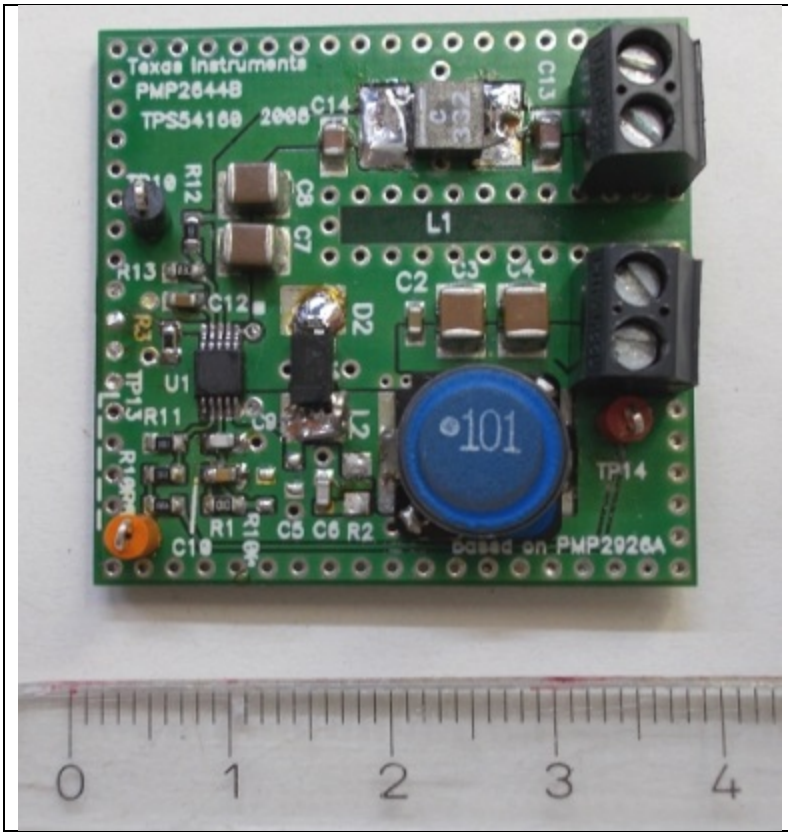
PMP30370RevB Test Results

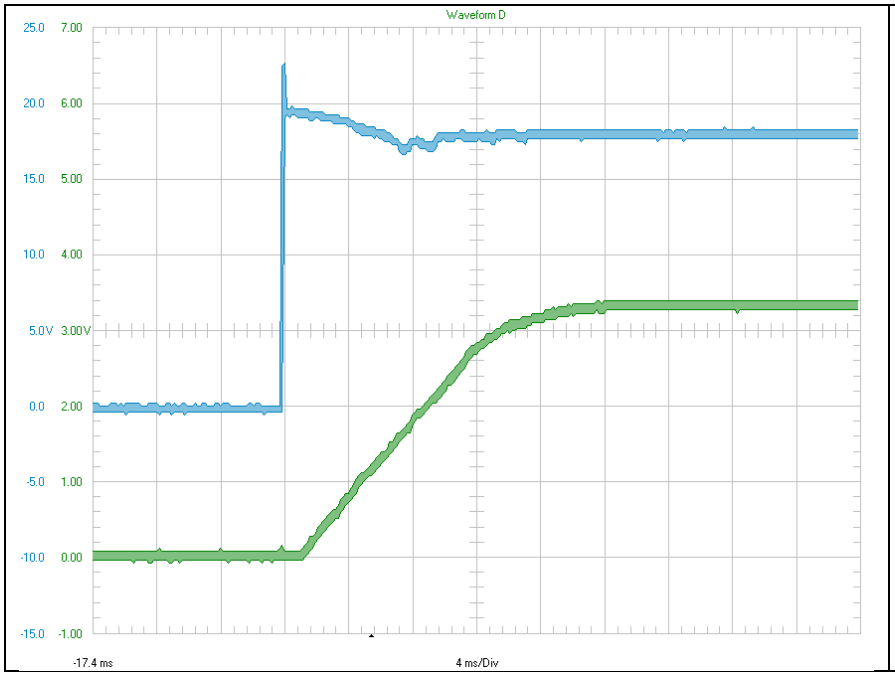
Topology: Non-Synchronous Buck Converter
TI-Device: TPS57060-q1, Fsw approx.. 300kHz, measured Fsw 292kHz
UVLO: circuit switches OFF at 13.82V, ON at 17.38V (load current 500mA).

Unless otherwise mentioned circuit was measured with a resistive load at 0.5A output current.



1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set to 18V.



Ch1=> input voltage 5V/div

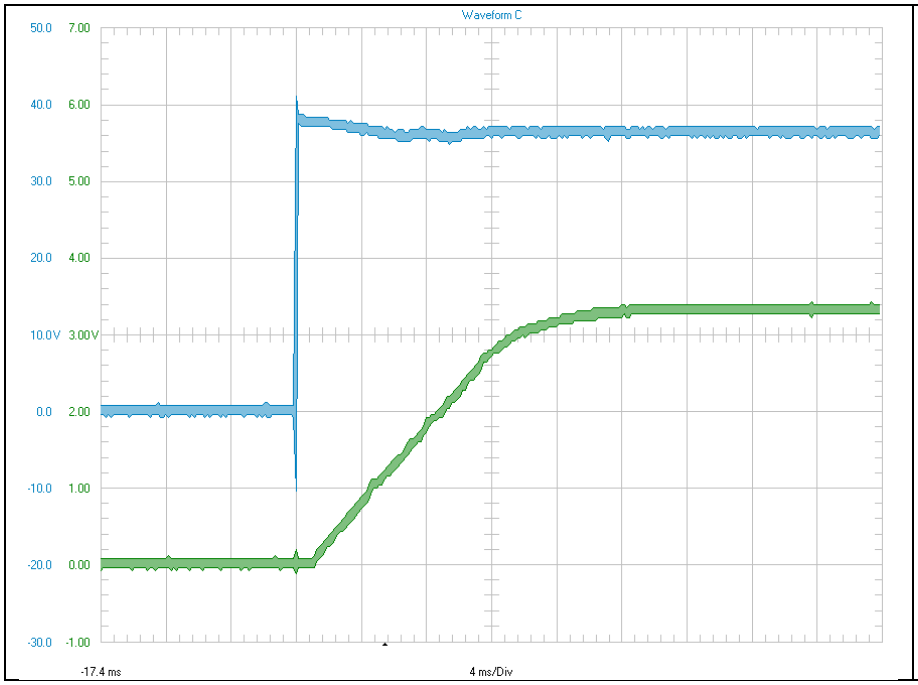
Ch2=> output voltage 1V/div

4ms/div

20MHz bw

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set to 36V.



Ch1=> input voltage 10V/div

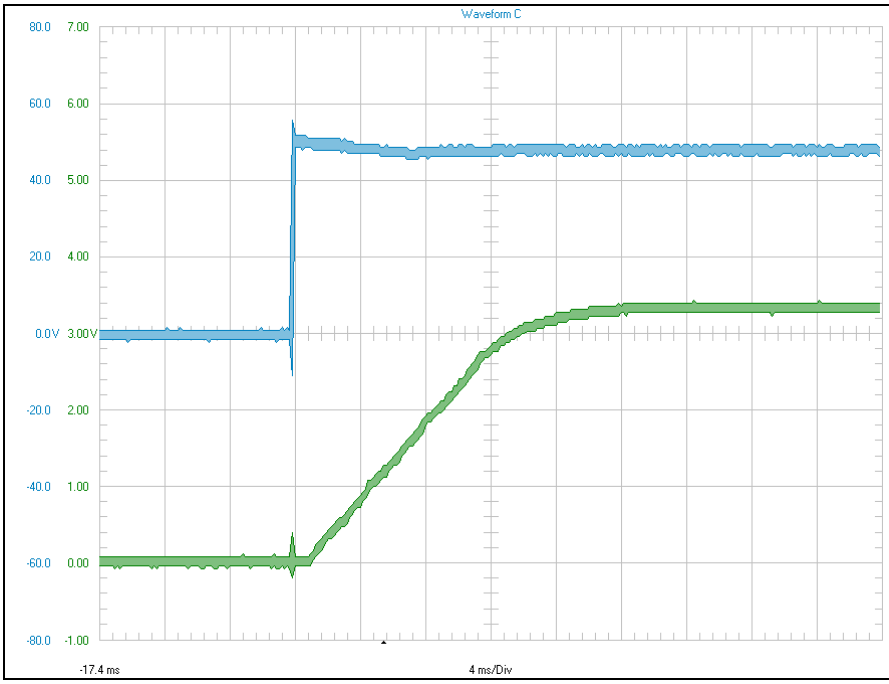
Ch2=> output voltage 1V/div

4ms/div

20MHz bw

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set to 48V.



Ch1=> input voltage
20V/div

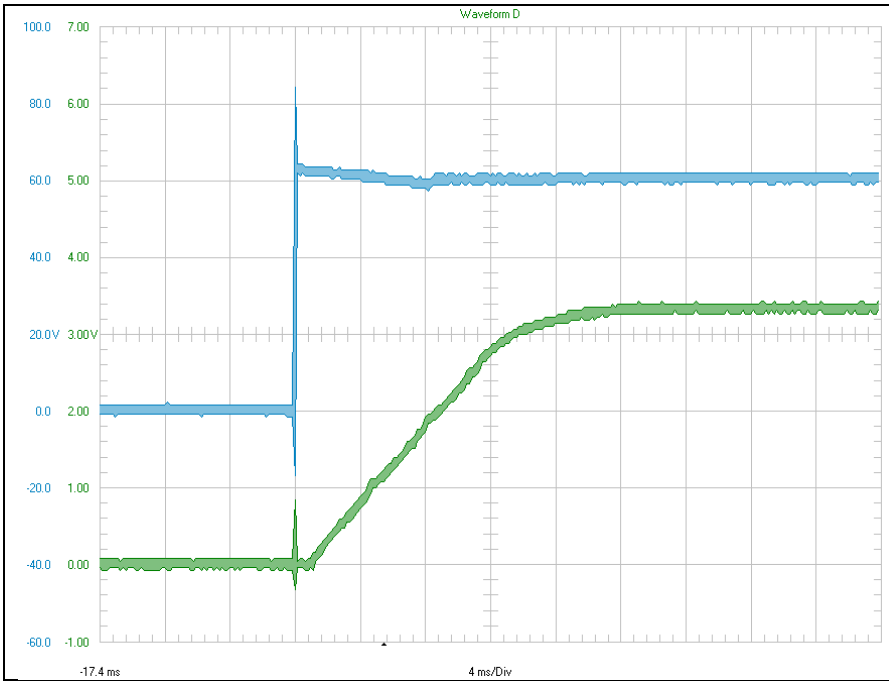
Ch2=> output voltage
1V/div

4ms/div

20MHz bw

Figure 3

The startup waveform is shown in the Figure 4. The input voltage was set to 60V.



Ch1=> input voltage
10V/div

Ch2=> output voltage
1V/div

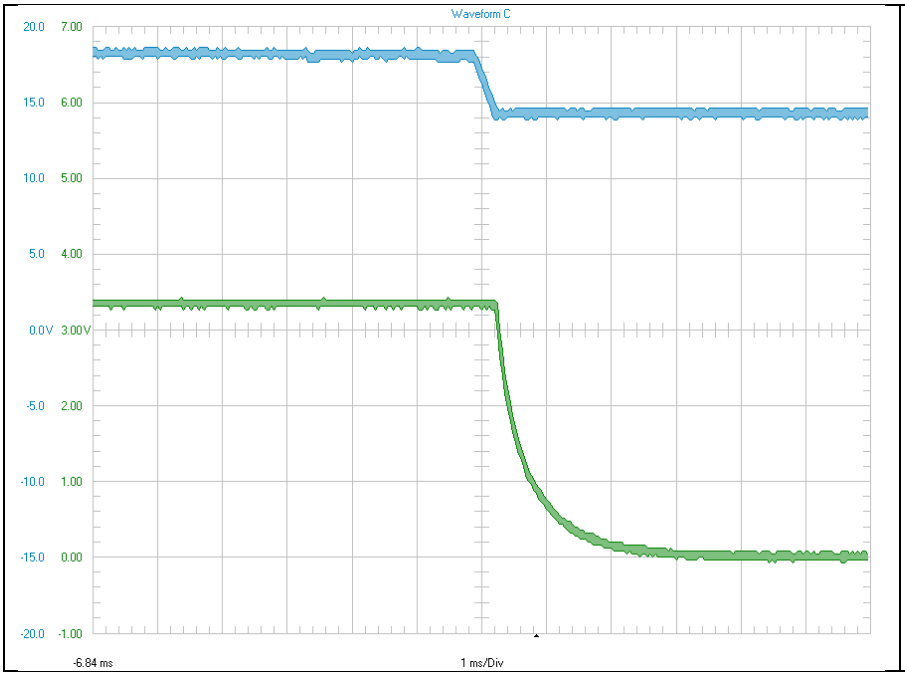
4ms/div

20MHz bw

Figure 4

2 Shutdown

The shutdown waveform is shown in the Figure 5. The input voltage was set to 18V.
The power supply was disconnected**.**



Ch1=> input voltage
5V/div

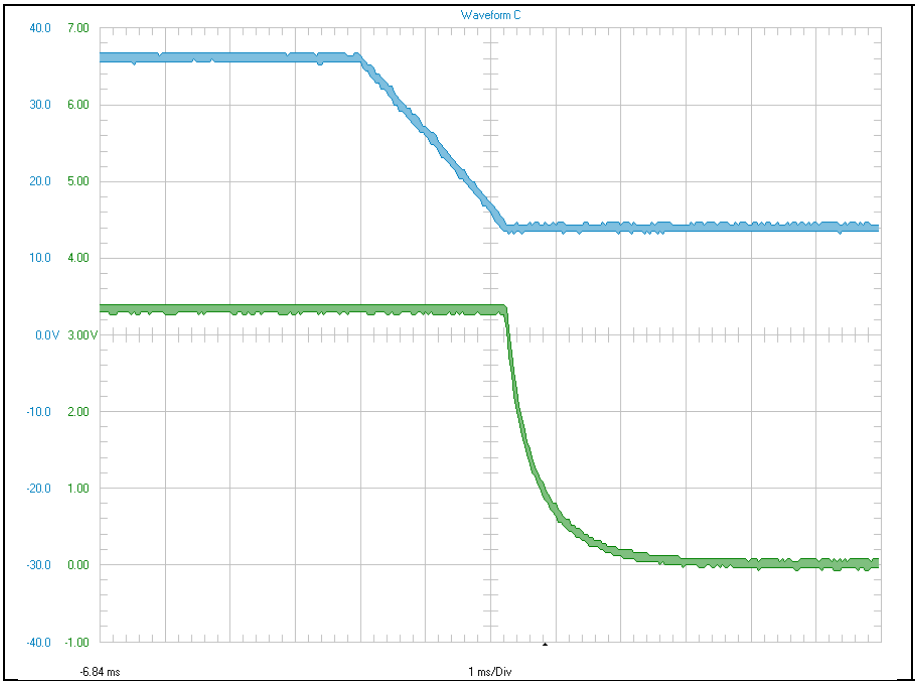
Ch2=> output voltage
1V/div

1ms/div

20MHz bw

Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set to 36V.
The power supply was disconnected.



Ch1=> input voltage
10V/div

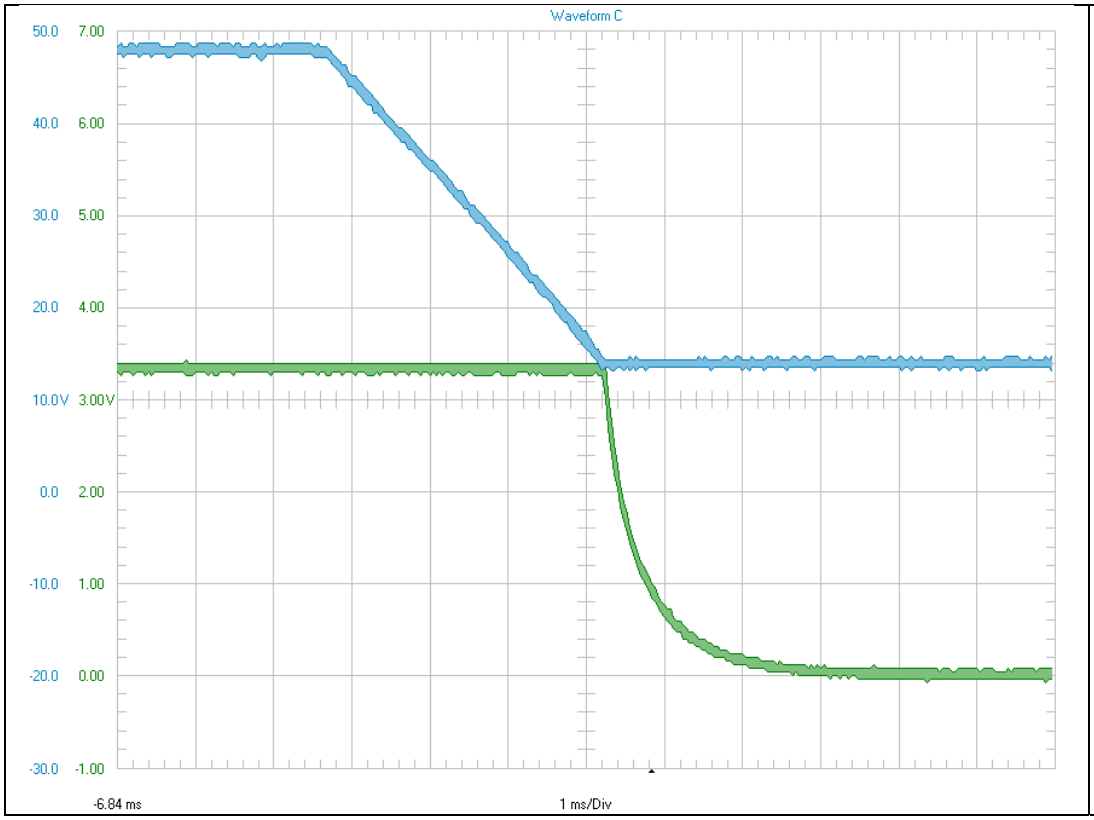
Ch2=> output voltage
1V/div

1ms/div

20MHz bw

Figure 6

The shutdown waveform is shown in the Figure 7. The input voltage was set to 48V.
The power supply was disconnected.



Ch1=> input voltage 10V/div

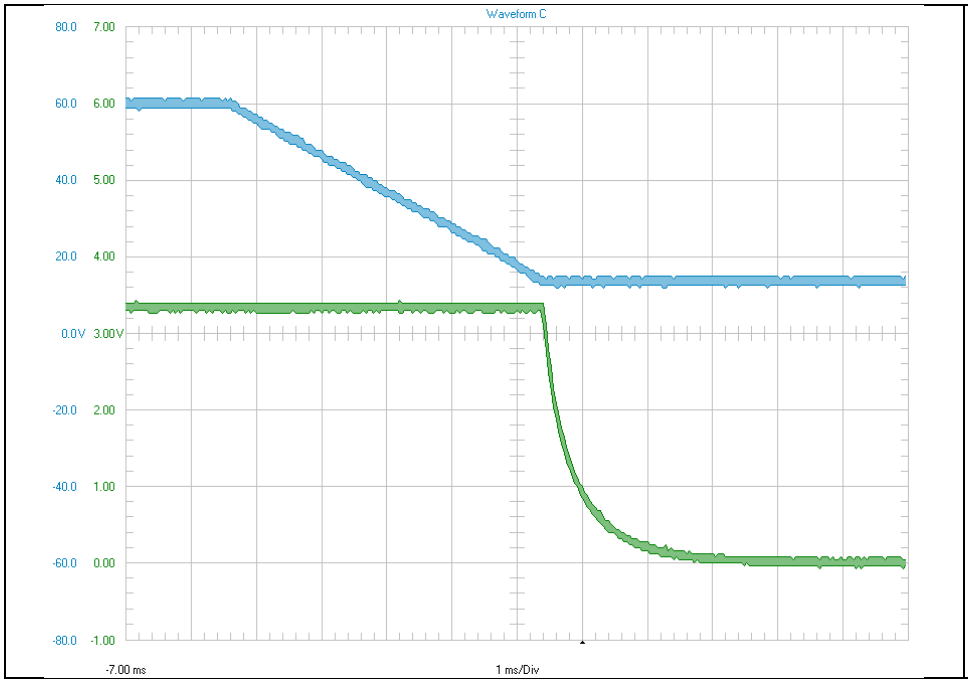
Ch2=> output voltage 1V/div

1ms/div

20MHz bw

Figure 7

The shutdown waveform is shown in the Figure 8. The input voltage was set to 60V.
The power supply was disconnected.



Ch1=> input voltage 20V/div

Ch2=> output voltage 1V/div

1ms/div

20MHz bw

Figure 8

3 Efficiency

The efficiency is shown in the Figure 9 below.
The input voltage was set to 18V, 36V, 48V and 60V.

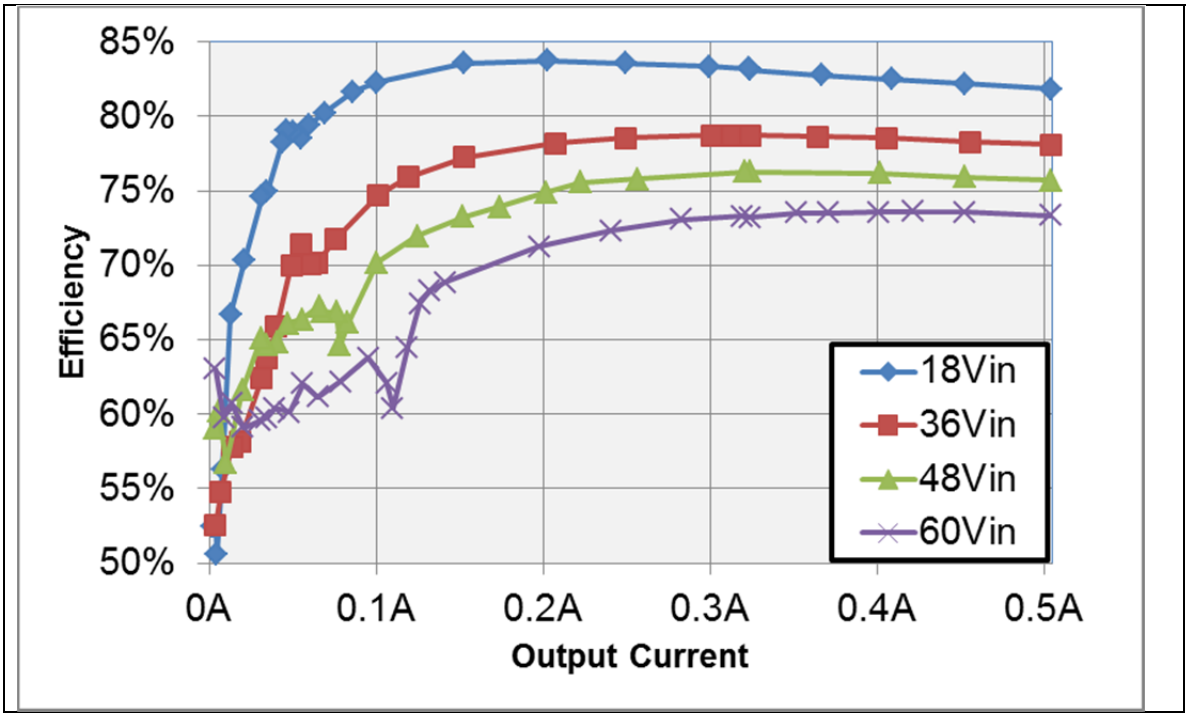


Figure 9

Figure 10 show the losses (Pin - Pout) with input voltage 18V, 36V, 48 and 60V

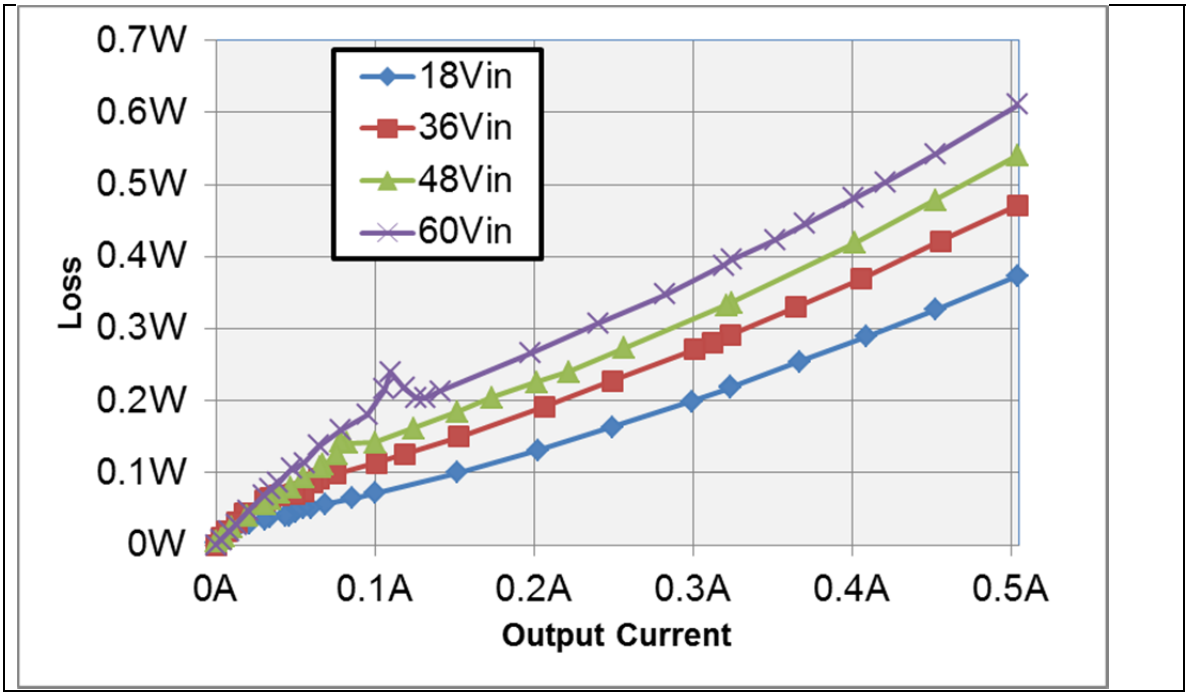


Figure 10

4 Load Regulation

The load regulation of the output is shown in the Figure 11 below.
The input voltage was set to 18V, 36V, 48 and 60V.

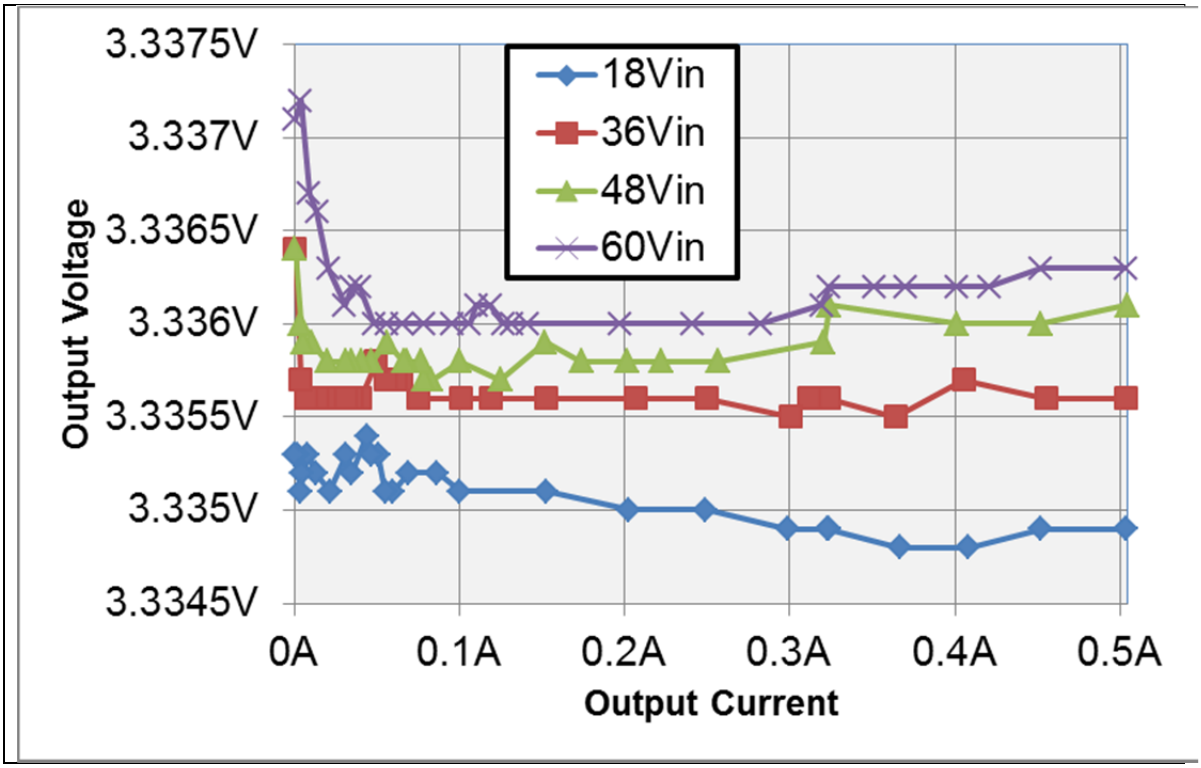


Figure 11

The load regulation is less than 3mV despite device works in burst mode at 60Vin and zero load !

5 Line Regulation

The line regulation is shown in Figure 12. The output current was set to 0.5A.

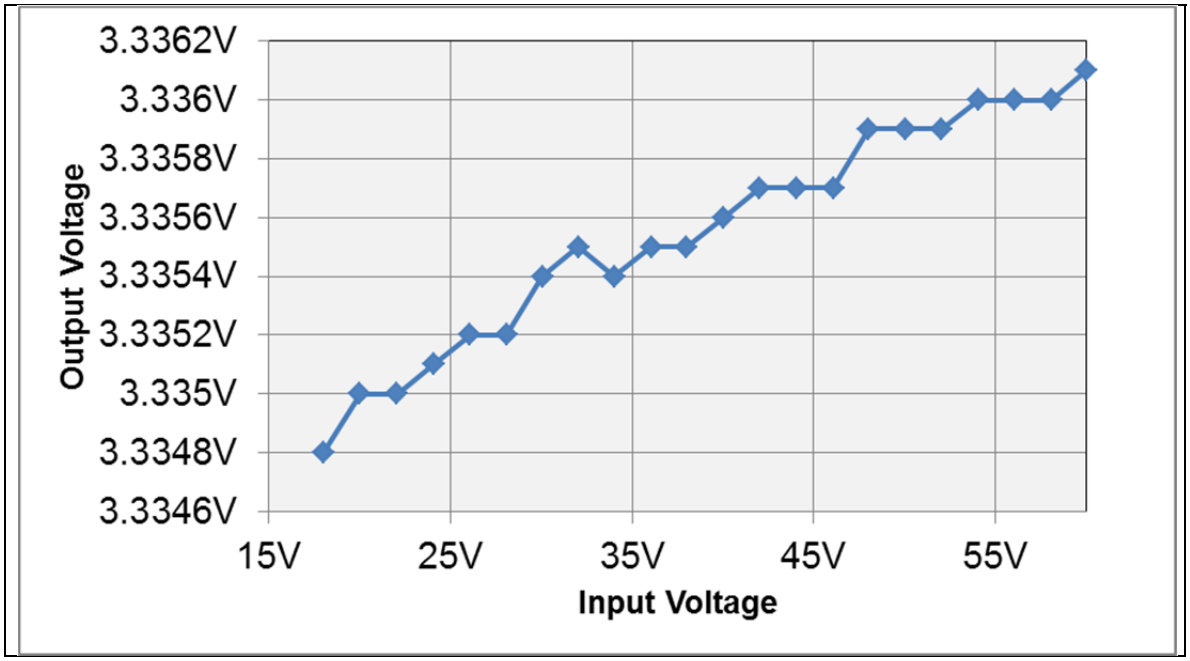


Figure 12

The line regulation is less than 1.5mV at full load current 500mA !

With the same setup efficiencies and losses were calculated. This is shown in Figure 13

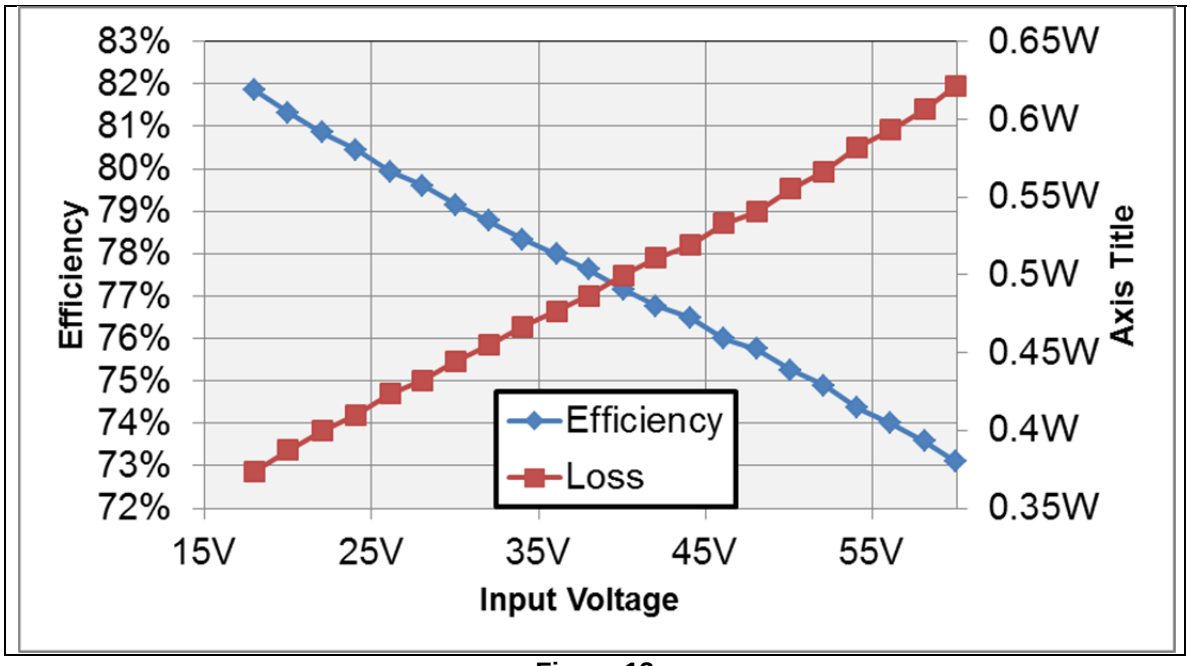
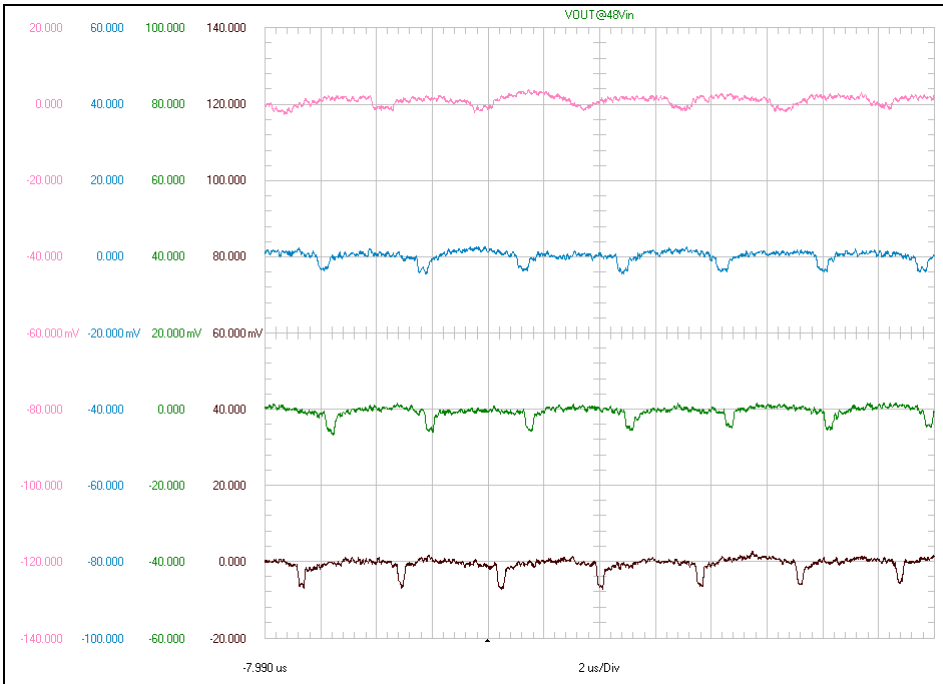


Figure 13

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 14.



Ch1 => output ripple with 18V Vin

Ch2 => output ripple with 36V Vin

Ch3 => output ripple with 48V Vin

Ch4 => output ripple with 60V Vin

20mV/div

AC coupled

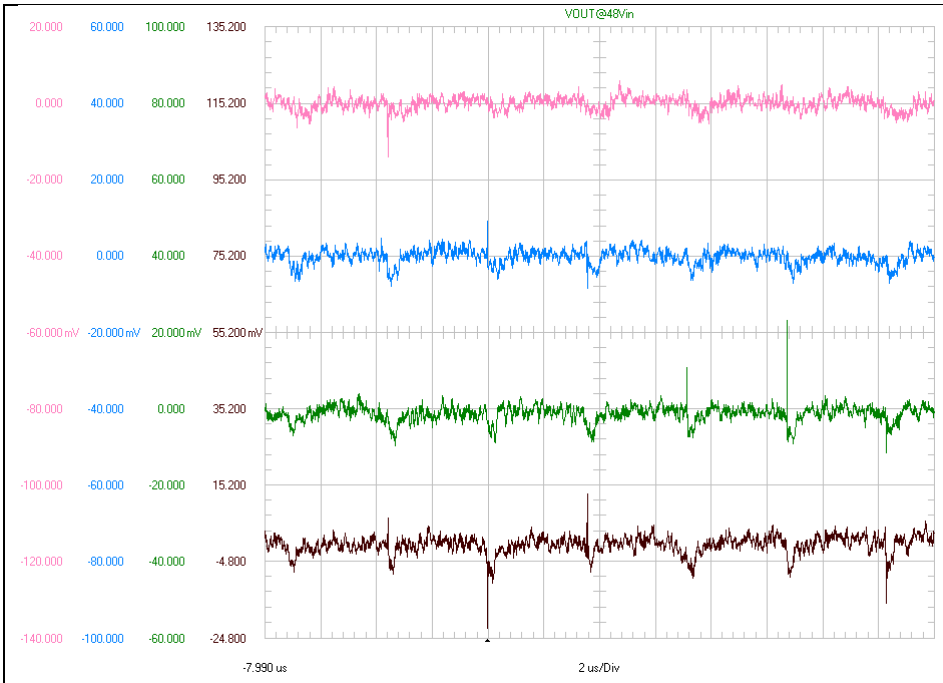
20MHz bw

2µs/div

Figure 14

The output ripple is less than 10mV across input voltage range !

The output ripple voltage is shown in Figure 15.



Ch1 => output ripple with 18V Vin

Ch2 => output ripple with 36V Vin

Ch3 => output ripple with 48V Vin

Ch4 => output ripple with 60V Vin

20mV/div

AC coupled

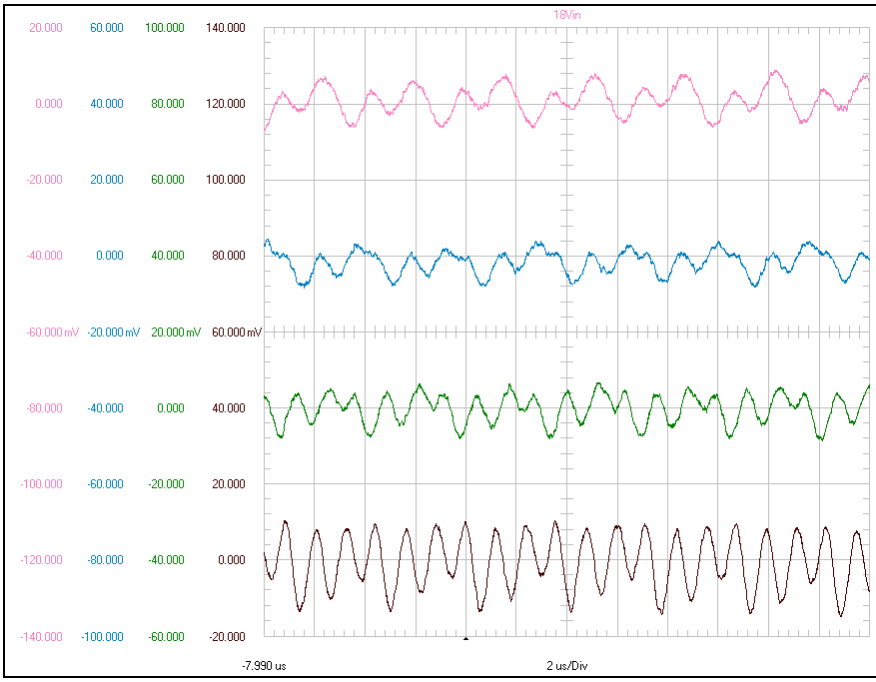
full bw

2µs/div

Figure 15

7 Input Ripple Voltage

The input ripple voltage measured near C13 (with input filter) is shown in Figure 16.



Ch1 => input ripple with 18V Vin

Ch2 => input ripple with 36V Vin

Ch3 => input ripple with 48V Vin

Ch4 => input ripple with 60V Vin

20mV/div

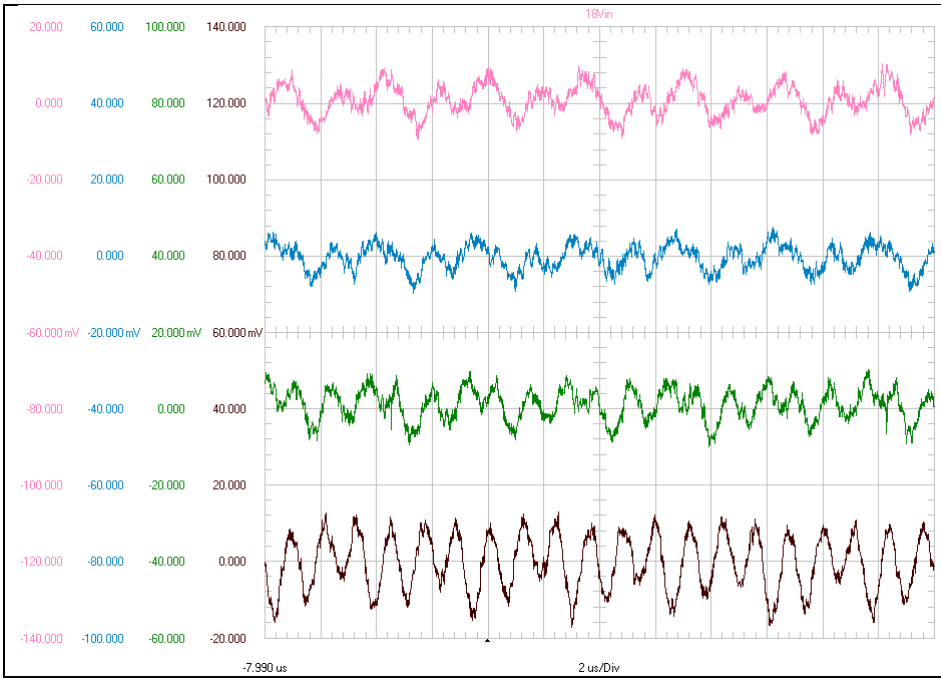
AC coupled

20MHz bw

2µs/div

Figure 16

The input ripple voltage measured near C13 is shown in Figure 17.



Ch1 => input ripple with 18V Vin

Ch2 => input ripple with 36V Vin

Ch3 => input ripple with 48V Vin

Ch4 => input ripple with 60V Vin

20mV/div

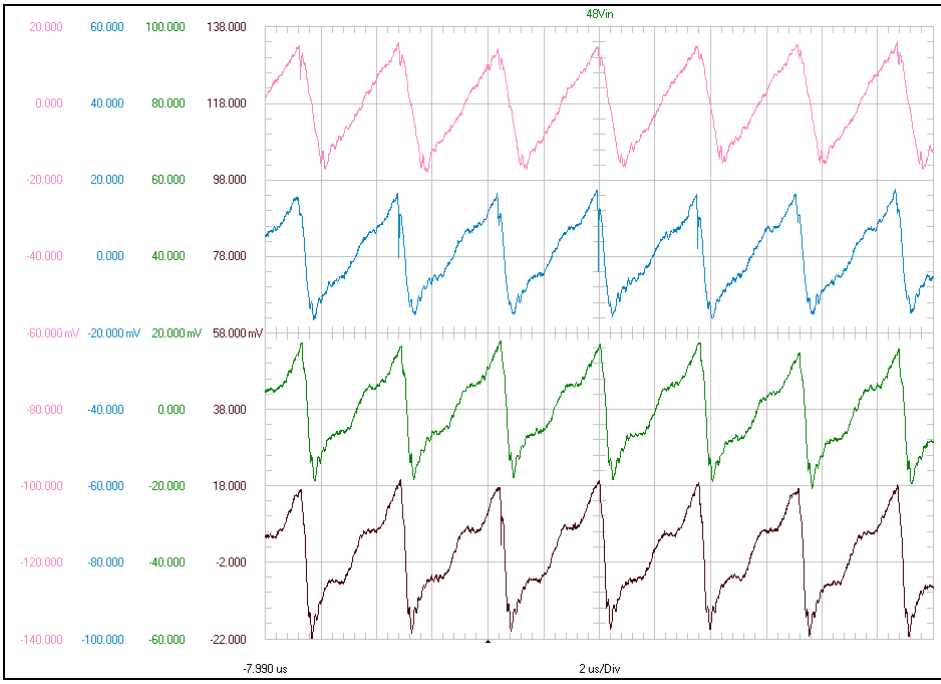
AC coupled

full bw

2µs/div

Figure 17

The input ripple voltage measured near C14 (no input filter) is shown in Figure 18.



Ch1 => input ripple with 18V Vin

Ch2 => input ripple with 36V Vin

Ch3 => input ripple with 48V Vin

Ch4 => input ripple with 60V Vin

20mV/div

AC coupled

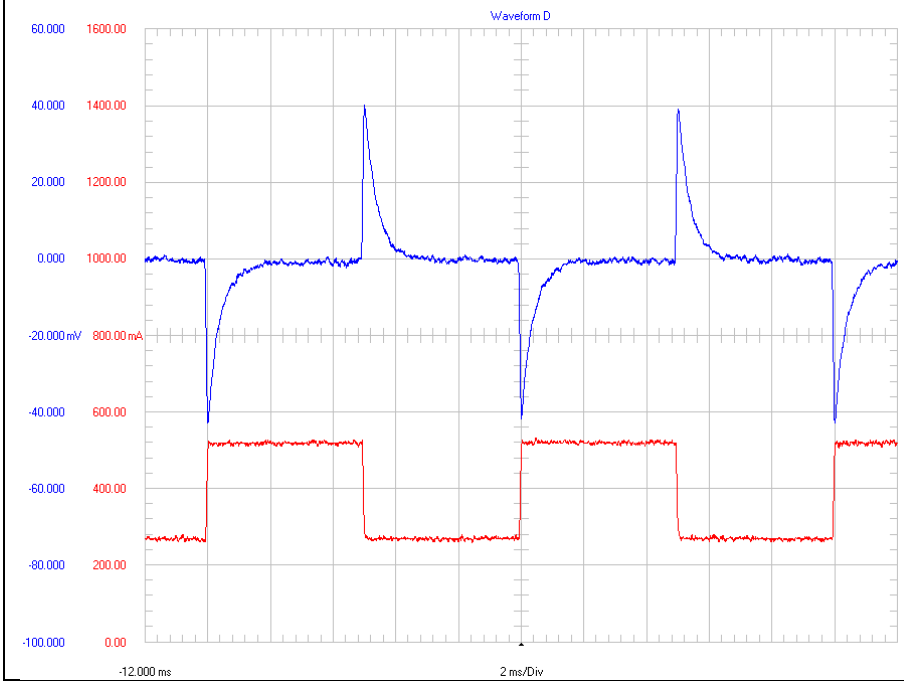
20MHz bw

2µs/div

Figure 18

8 Load Transients

The Figure 19 shows the response to load transients at 18V input voltage.
The electronic load is switching from 0.25A to 0.5A (100Hz).



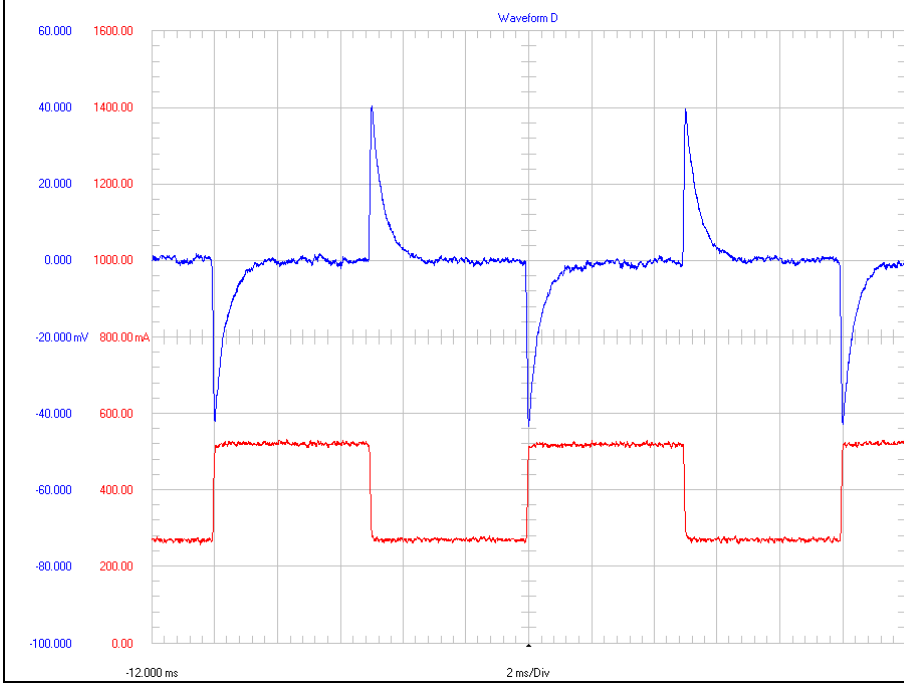
Ch1 => output voltage
20mV/div
AC coupling
20MHz bw

Ch2 => output current 200mA/div
10kHz bw

2ms/div

Figure 19

The Figure 20 shows the response to load transients at 36V input voltage.
The load is switching from 0.25A to 0.5A (100Hz).



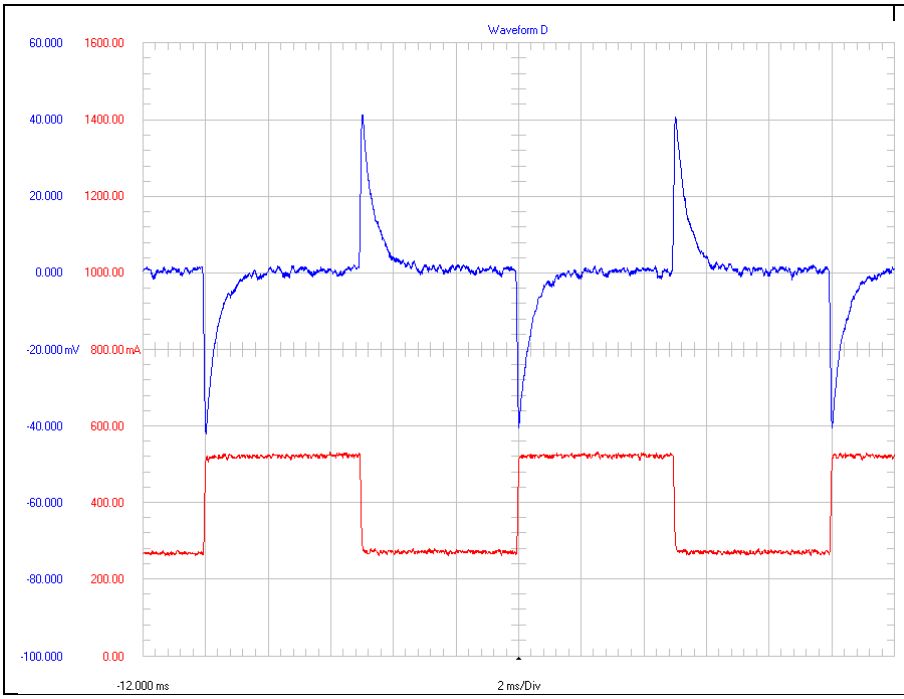
Ch1 => output voltage
20mV/div
AC coupling
20MHz bw

Ch2 => output current
200mA/div
10kHz bw

2ms/div

Figure 20

The Figure 21 shows the response to load transients at 48V input voltage.
The load is switching from 0.25A to 0.5A (100Hz).



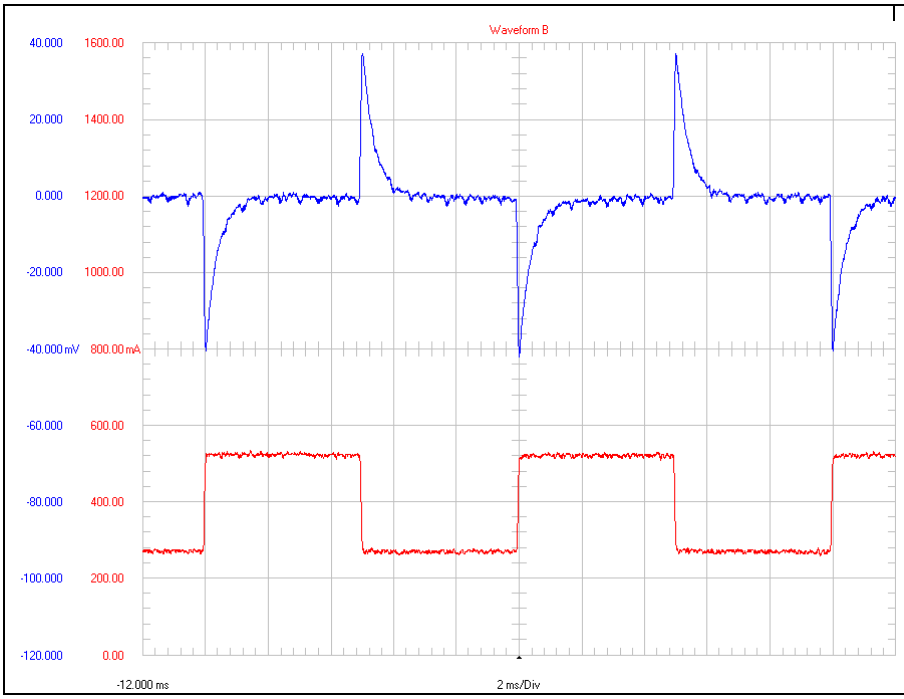
Ch1 => output voltage
20mV/div
AC coupling
20MHz bw

Ch2 => output current
200mA/div
10kHz bw

2ms/div

Figure 21

The Figure 22 shows the response to load transients at 60V input voltage.
The load is switching from 0.25A to 0.5A (100Hz).



Ch1 => output voltage
20mV/div
AC coupling
20MHz bw

Ch2 => output current
200mA/div
10kHz bw

2ms/div

Figure 22

output voltage deviation at 50% load transient is around 40mV peak, so around 1.2%.

9 Control Loop Frequency Response

Figure 23 shows the loop response for 18Vin. Load is 0.5A.

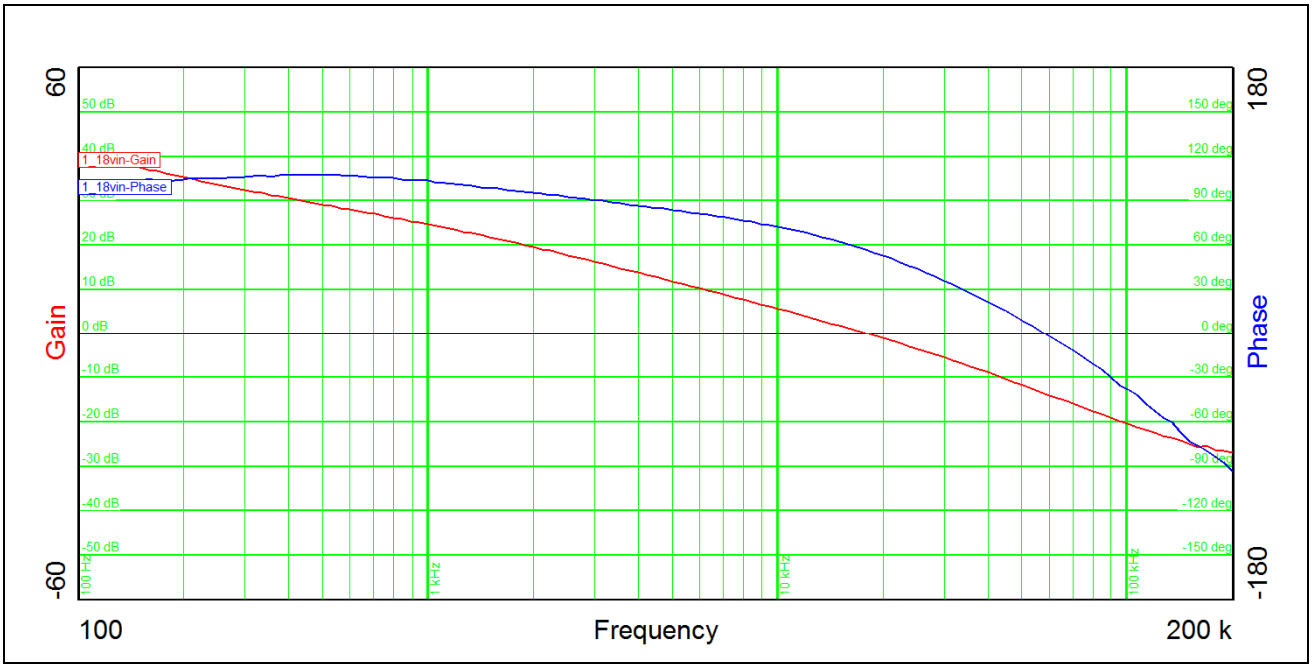


Figure 23

Figure 24 shows the loop response for 36Vin. Load is 0.5A.

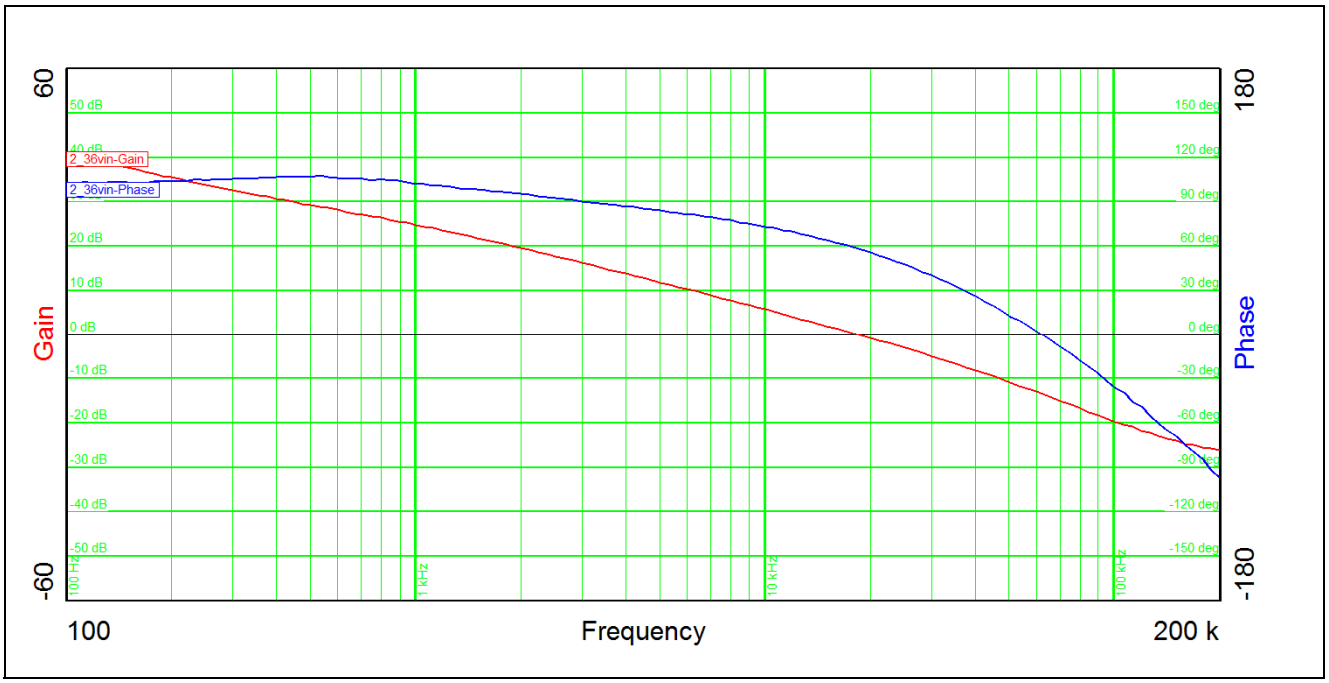


Figure 24

Figure 25 shows the loop response for 48Vin. Load is 0.5A.

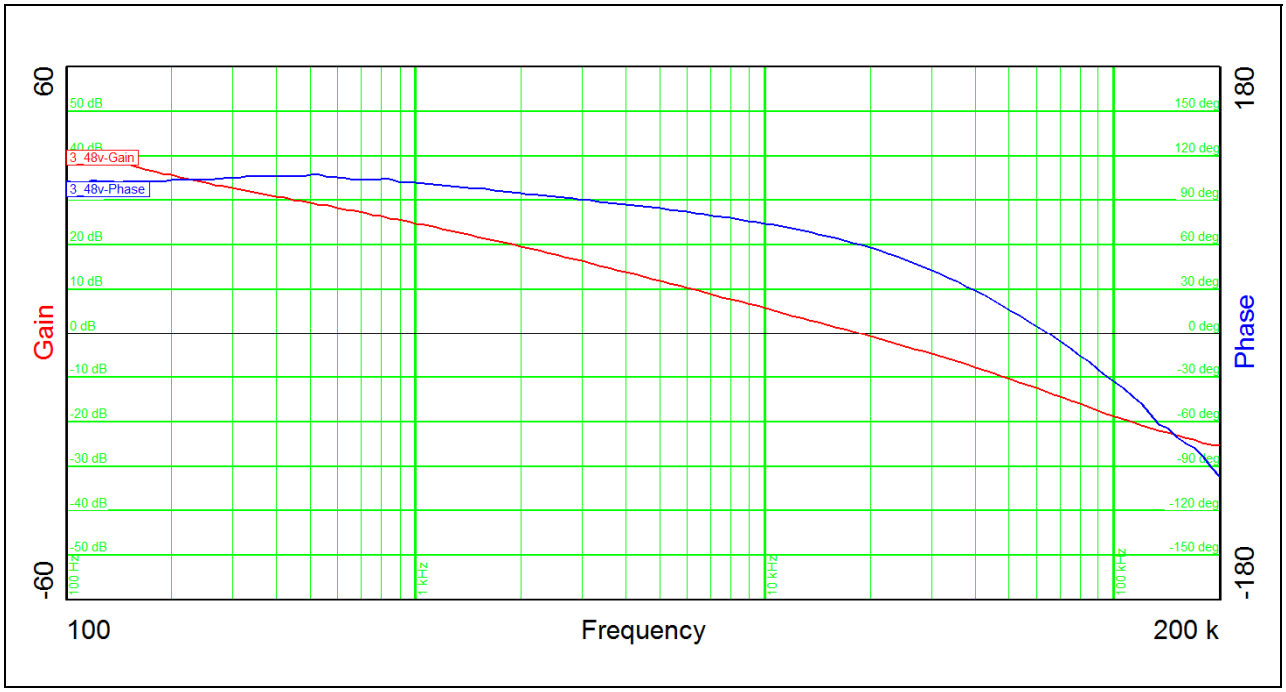


Figure 25

Figure 26 shows the loop response for 60Vin. Load is 0.5A.

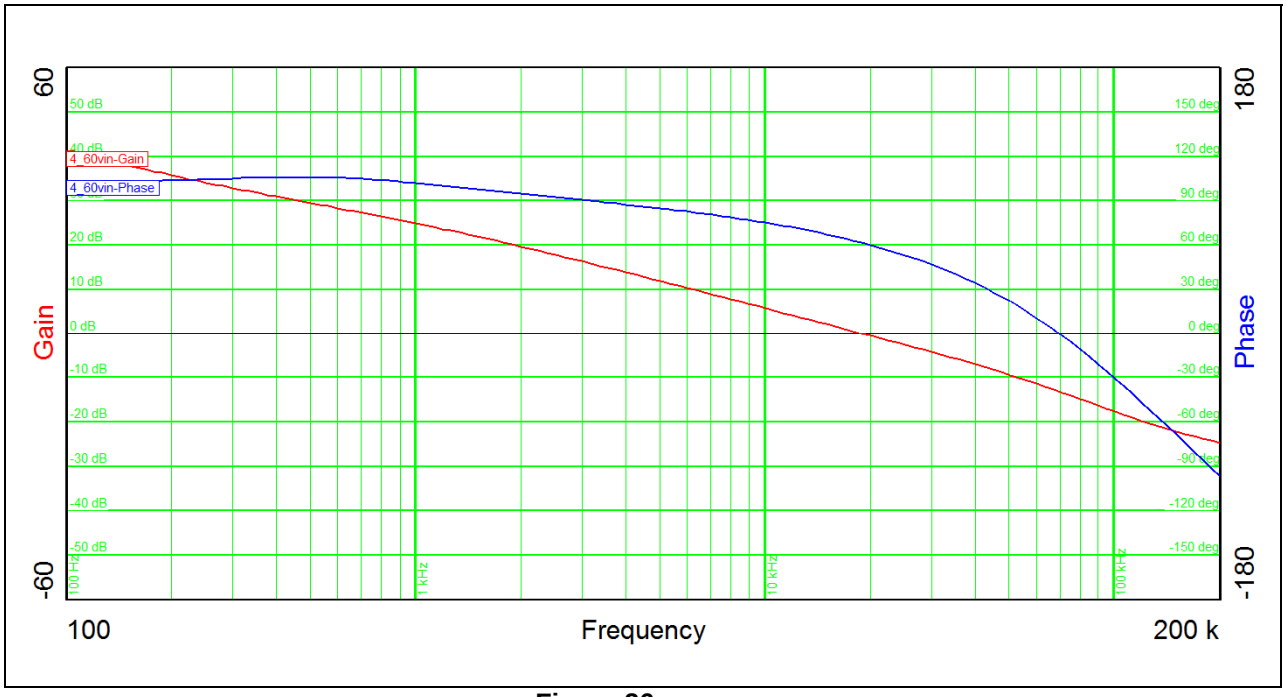


Figure 26

For best dynamics the transconductance error amplifier has been set close to 20kHz loop bandwidth; phase margin is still around 60 degrees.

Table 1 summarizes the results of the above measurements

Vin	18V	36V	48V	60V
Bandwidth (kHz)	18.0	18.3	18.6	18.9
Phase margin	56.6°	58.5°	60°	61.5°
slope (20dB/decade)	-1.2	-1.1	-1.1	-1.1
gain margin (dB)	-13.7	-13.5	-13.4	-13.2
slope (20dB/decade)	-1.5	-1.5	-1.4	-1.4
freq (kHz)	58	62	65	69

Table 1

10 Miscellaneous Waveforms

10.1 Switch Node

The waveform of the voltage on switch node is shown in Figure 27.
Input voltage was set to 18V.

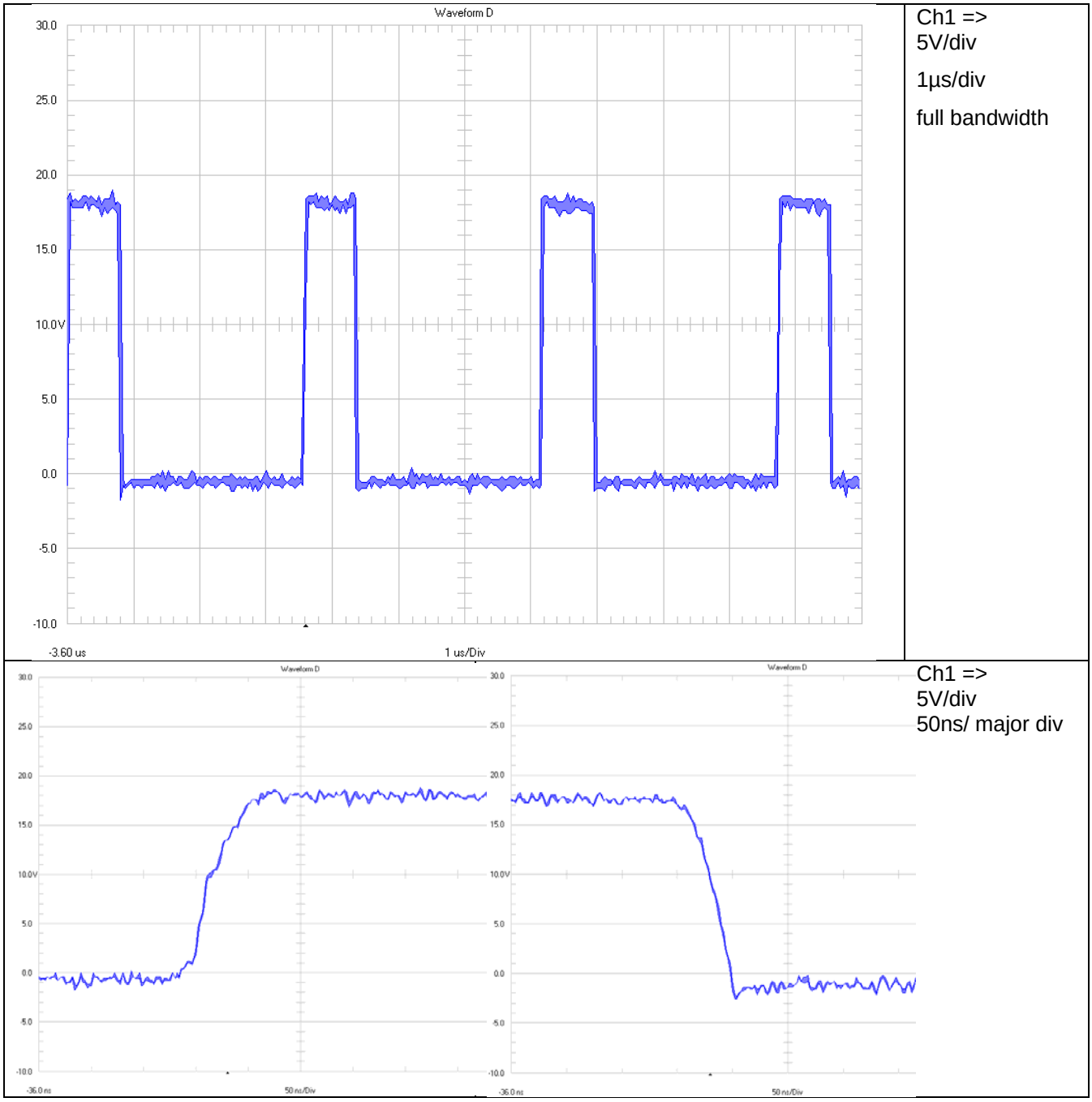


Figure 27

The waveform of the voltage on the switch node is shown in Figure 28.
Input voltage was set to 36V.

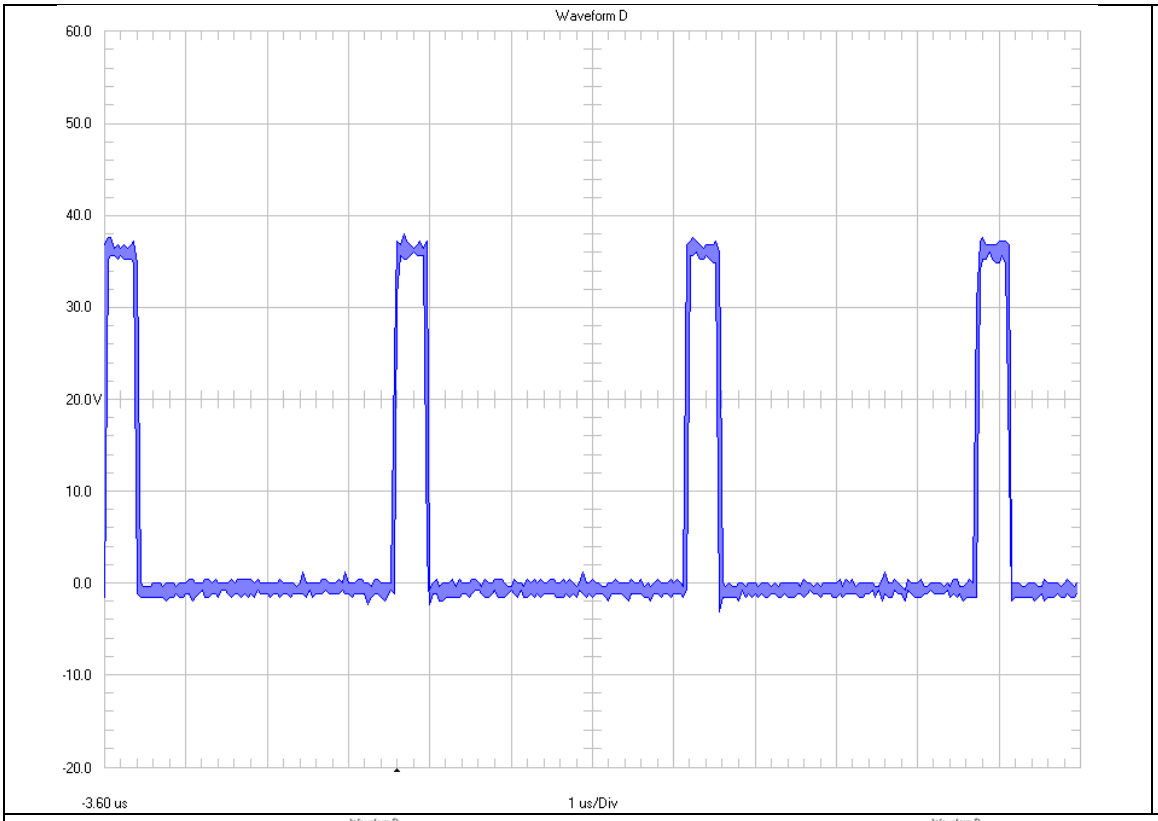


Figure 28

The waveform of the voltage on switch node is shown in Figure 29.
Input voltage was set to 48V.

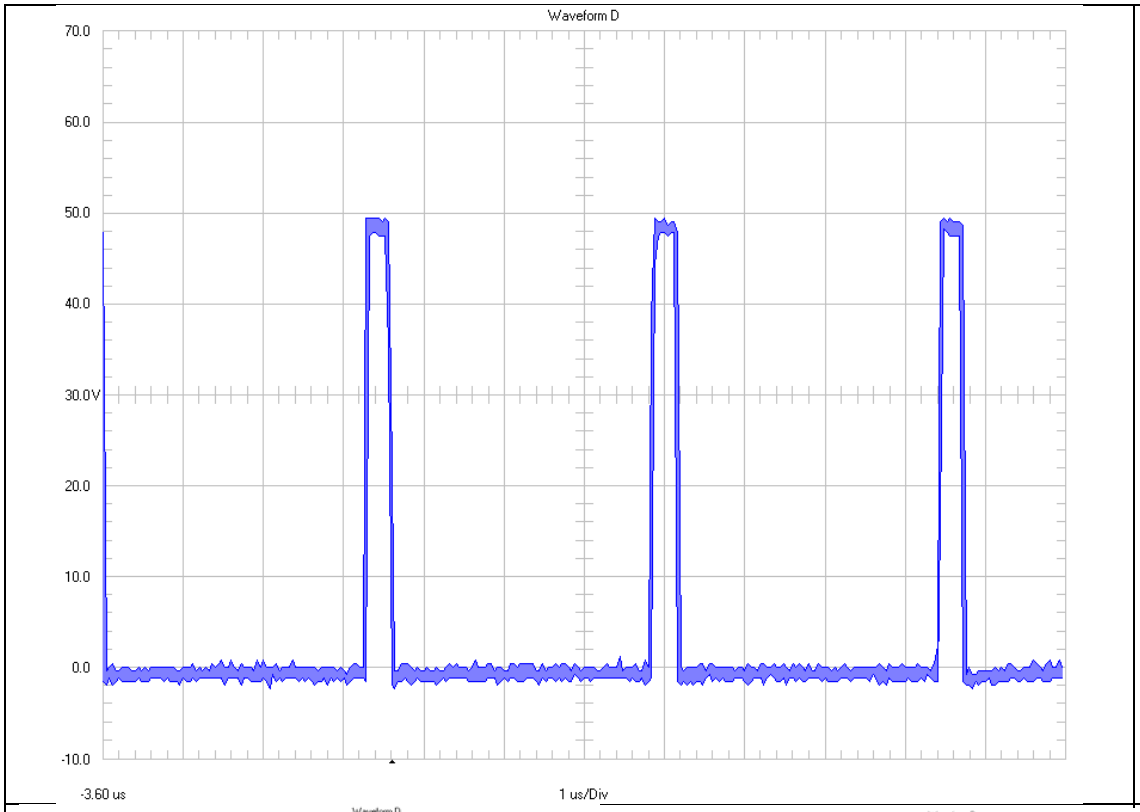
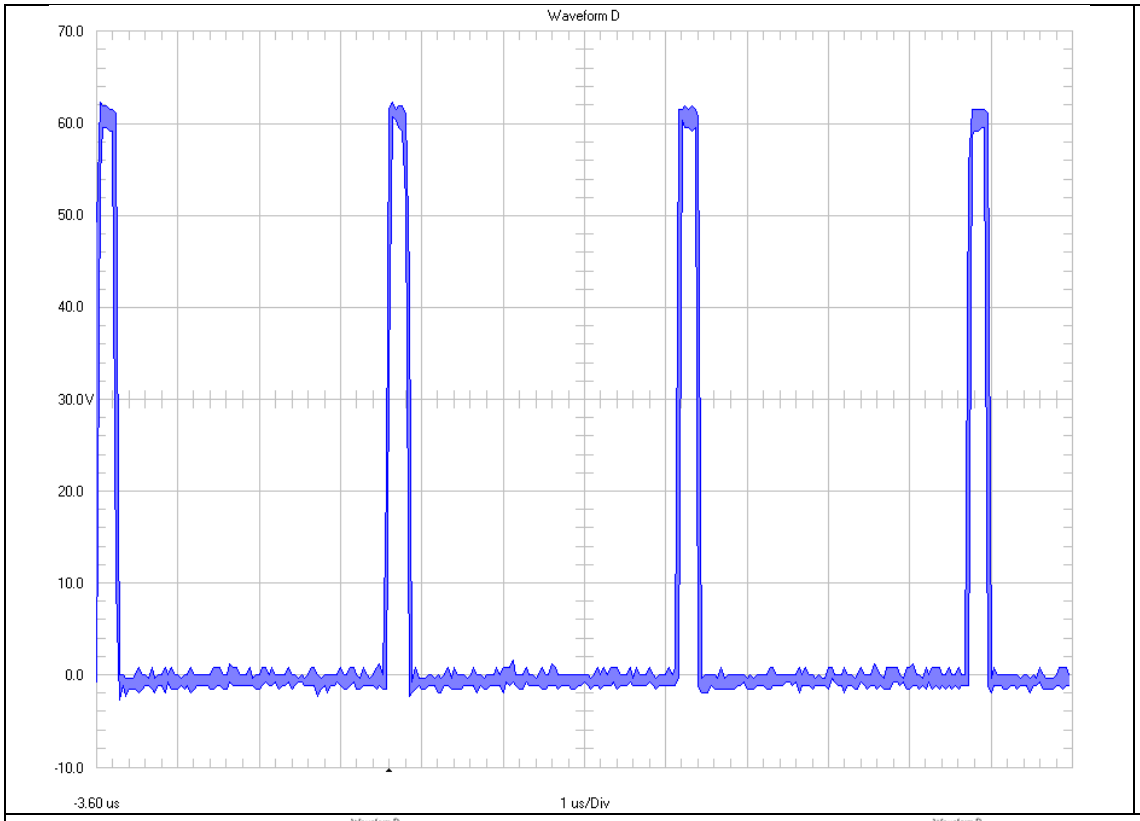


Figure 29

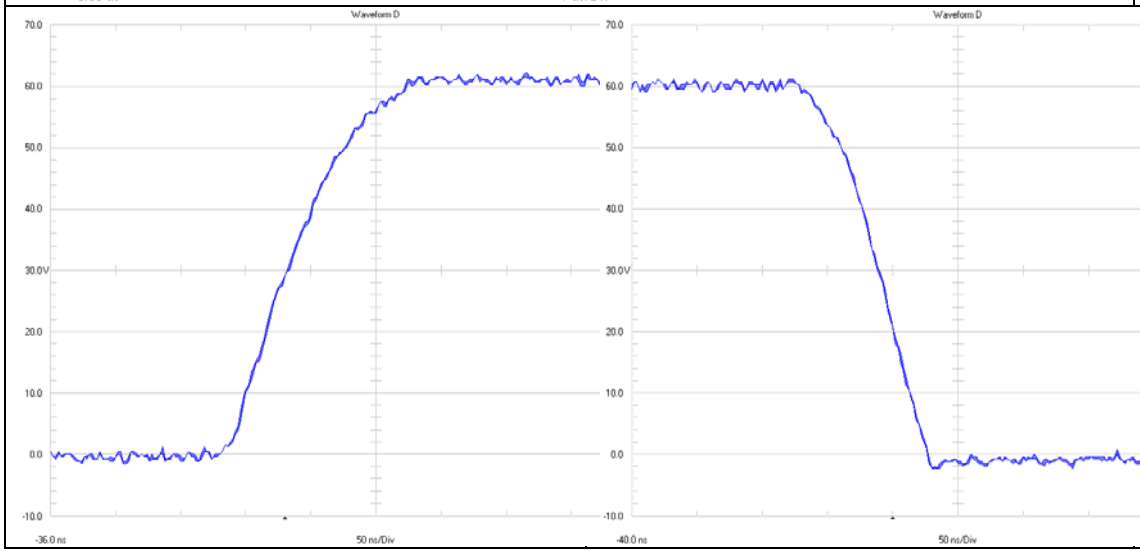
The waveform of the voltage on switch node is shown in Figure 30.
Input voltage was set to **60V.**



Ch1 =>
10V/div

1µs/div

full bandwidth



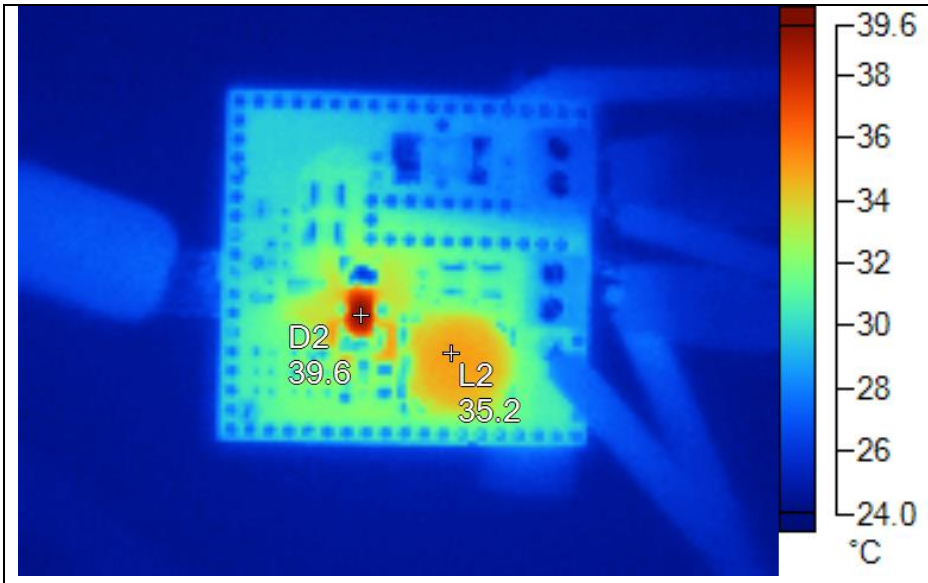
Ch1 =>
10V/div
50ns/ major div

Figure 30

even at max. input voltage 60V no ringing, no overshoot at switch node, so low RF distortion !

11 Thermal Image

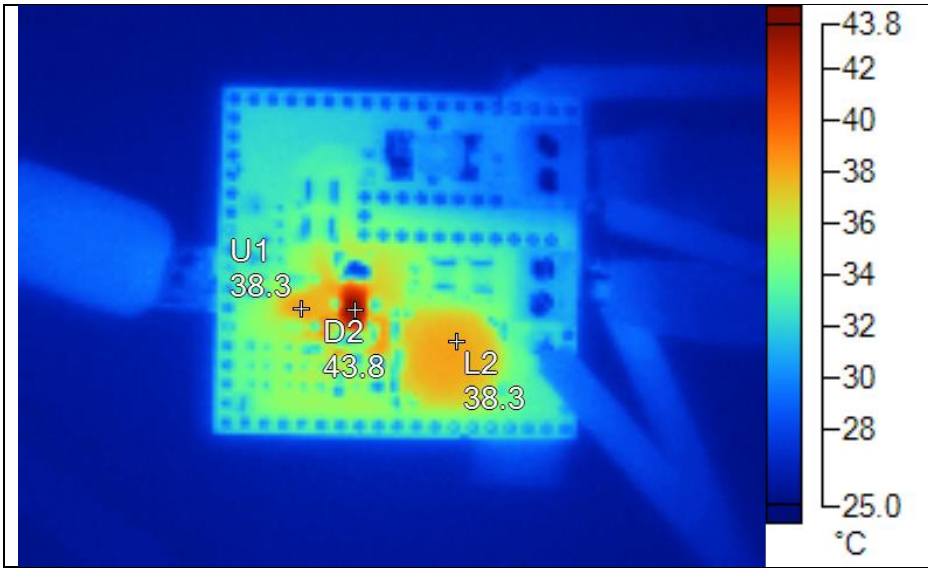
Figure 31 shows the thermal image at 18V input voltage.



Name	Temperature
D2	39.6°C
L2	35.2°C

Figure 31

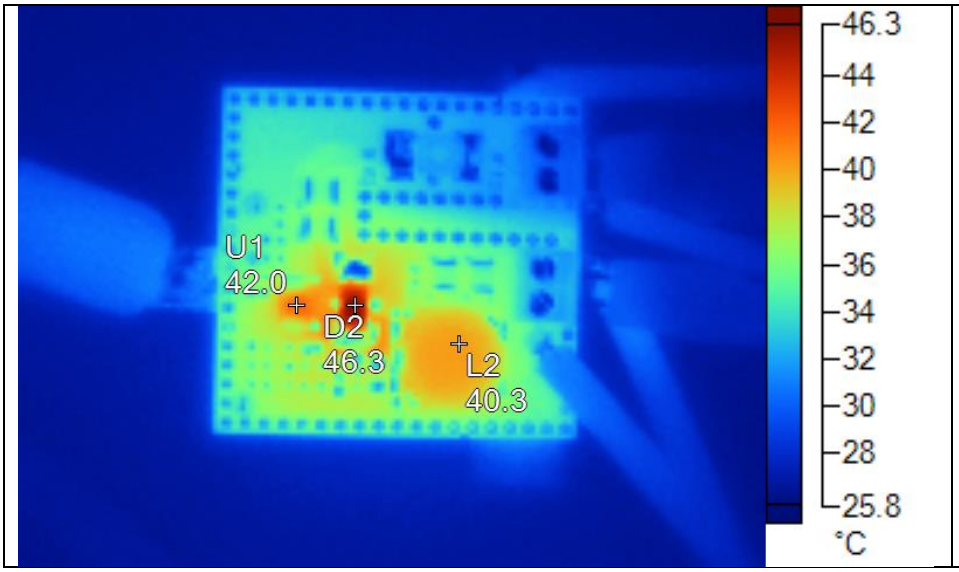
Figure 32 shows the thermal image at 36V input voltage.



Name	Temperature
D2	43.8°C
U1	38.3°C
L2	38.3°C

Figure 32

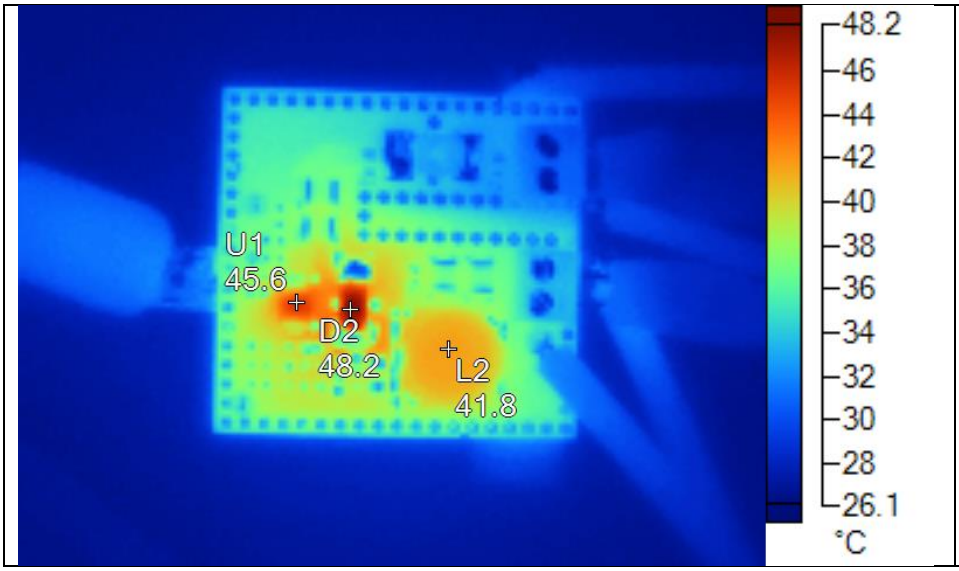
Figure 33 shows the thermal image at 48V input voltage.



Name	Temperature
D2	46.3°C
U1	42.0°C
L2	40.3°C

Figure 33

Figure 34 shows the thermal image at 60V input voltage.



Name	Temperature
D2	48.2°C
U1	45.6°C
L2	41.8°C

Figure 34

At worst case condition 60V input, means losses at internal linear regulator and switching losses at internal FET, the thermal stress is well distributed and overall temperature rise around +25K only.

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