Design Guide: TIDA-020002

Automotive 2-MP camera module reference design with MIPI CSI-2 video interface, FPD-Link III and POC

Description

This camera module reference design addresses the need for small cameras in automotive systems by combining a 2-megapixel imager with a 4-Gbps serializer. Additionally, it provides power supplies and voltage supervision for both devices in an ultra-small form factor. This design includes a high-speed serial interface to connect a remote automotive camera module to a display or machine vision processing system with a coaxial cable transmitting both data and power. The 4-Gbps FPD-Link III SerDes technology used in this reference design enables the transmission of uncompressed 2MP video data, bidirectional control signals, and power over coax (POC) using a single cable.

Resources

TIDA-020002	Design Folder
DS90UB953-Q1	Product Folder
TPS62162-Q1	Product Folder
TPS62423-Q1	Product Folder
LP5907-Q1	Product Folder
TPS3700-Q1	Product Folder
TPS3702-Q1	Product Folder

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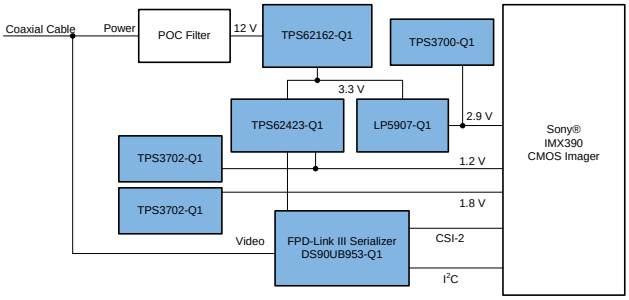
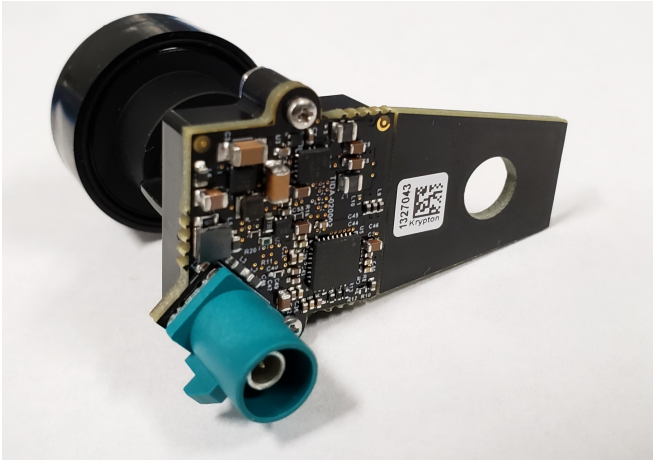
Features

- Space-optimized design with discrete power supply that fits on a single PCB 20 × 20 mm
- Power-supply optimized for high efficiency and low noise
- Enables high-resolution camera applications using 4-Gbps DS90UB953
- 2.1-MP IMX390 image sensor from Sony providing full-HD, AD 10-bit, MIPI 4-lane, RAW24, RAW20, RAW12
- Single Rosenberger Fakra coaxial connector for digital video, power, control, and diagnostics
- Additional diagnostic capabilities to enable ASIL applications
- Includes design considerations and characterization test data

Applications

- Camera module without processing
- Front camera
- Mirror replacement, CMS
- Surround view system ECU



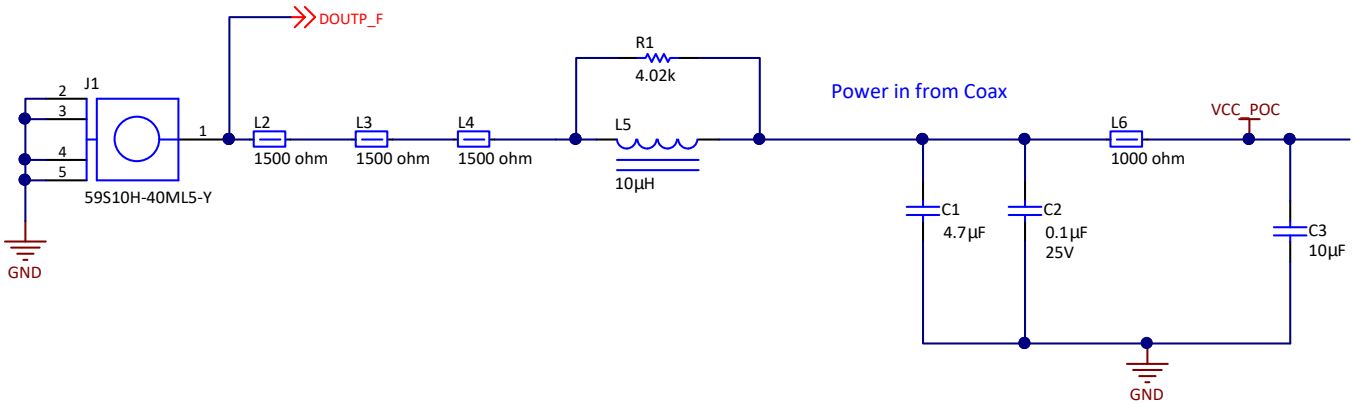


1 System Description

Many automotive applications require small form factors with reduced circuit area that enable compact and modular systems. As a result, most cameras along with electronic components must meet this minimal area constraint when designing ADAS camera applications. This reference design addresses these needs by including a 2-megapixel imager, 4 Gbps serializer, and the necessary power supply for both, and all components contained within a single 20 × 20-mm circuit board. The only connection required by the system is a single 50-Ω coaxial cable.

A combined signal containing the DC power, the FPD-Link front and backchannels enter the board through the FAKRA coax connector. The filter shown in Figure 1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

Figure 1. FPD-Link III Signal Path



The DC portion is connected to the input of the TPS62162 buck converter to output 3.3 V. This voltage powers the TPS62423 and LP5907 devices, which are responsible for creating the supply rails to the imager and serializer. The LP5907 creates a low-noise, 2.9-V analog supply to the imager, while the TPS62423 device creates the imager dedicated 1.2 V and also generates a universal 1.8-V digital supply that is shared by both the imager and serializer. The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control backchannel takes between the serializer and deserializer.

The output of the imager is connected through a four-lane MIPI CSI-2 interface to the serializer. The serializer transmits this video data over a single LVDS pair to the deserializer located on the other end of the coax cable.

Additionally, on the same coax cable, there is a separate low-latency, bidirectional control channel that provides the additional function of transmitting control information from an I^2C port. This control channel is independent of the video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

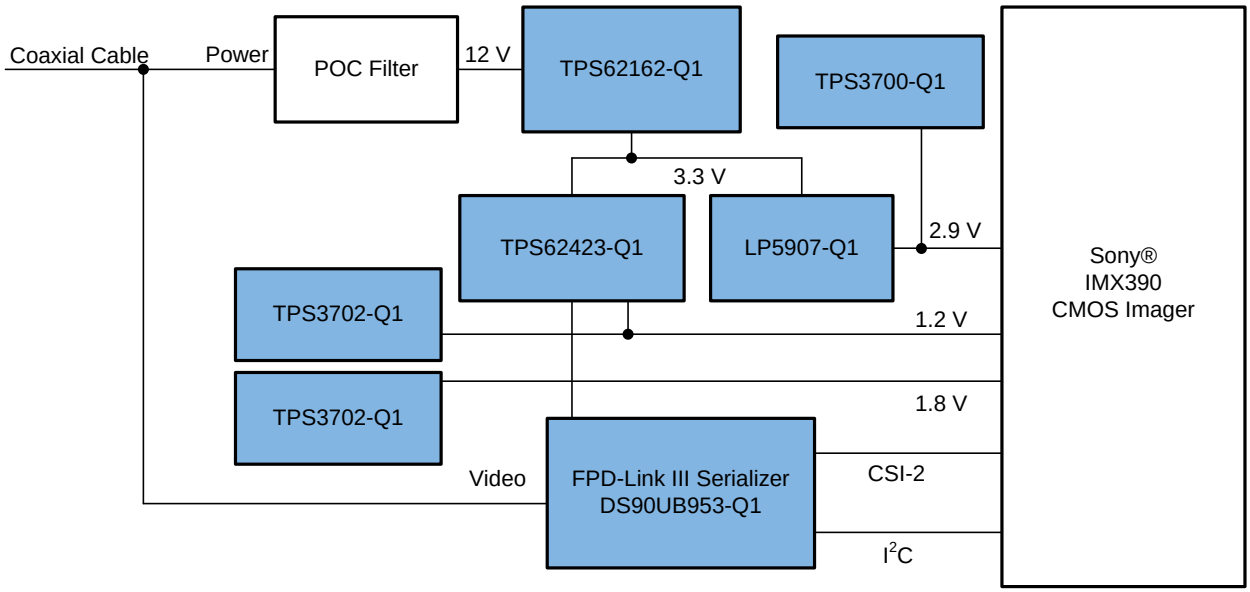
Table 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (POC)	4	12	17	V
P_{TOTAL}	Total power consumption	V_{POC} = 12 V	—	0.6	1	W

2 System Overview

2.1 Block Diagram

Figure 2. Camera Block Diagram



2.2 Highlighted Products

This reference design uses the following TI products:

- DS90UB953-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).
- TPS62162-Q1: an automotive qualified step-down DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response.
- TPS62423-Q1: an automotive qualified step-down DC converter with high efficiency. The device includes a 2.25 MHz fixed switching frequency, along with a power-save mode feature that enables high efficiency over the entire load-current range.
- LP5907-Q1: a low-noise 250-mA LDO qualified for automotive applications. The device provides low noise, high PSRR, low quiescent current, and low line or load transient response.
- TPS3700-Q1: an automotive qualified voltage window comparator supervisor. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to FPD-Link III 18 V for overvoltage and undervoltage detection. The device can be used as a window comparator or as two independent voltage monitors; the monitored voltage is set with the use of external resistors.
- TPS3702-Q1: an automotive-qualified integrated overvoltage and undervoltage window comparator supervisor with fixed voltage options. This highly accurate voltage detector is ideal for systems that operate on low-voltage supply rails and have narrow margin supply tolerances. Low threshold hysteresis options of 0.55% and 1.0% prevent false reset signals when the monitored voltage supply is in its normal range of operation.

2.2.1 IMX390 Imager

The Sony® IMX390 is a diagonal 6.67-mm (Type 1/2.7) CMOS active pixel type solid-state image sensor with a square pixel array and 2.12 effective pixels. The sensor supports Full-HD, AD 12-bit, MIPI 4-lane, RAW24, RAW20, RAW12 output. Other included features follow:

- Supports image sizes: (2.07MB pixels) 1920 × 1080 Full-HD, (2.30M pixels) 1920 × 1200 WUXGA
- Requires three voltage rails (2.9 V, 1.8 V, and 1.2 V)
- Can be configured using an I^2C-compatible two-wire serial interface

2.2.2 DS90UB953-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The CSI-2 input of the DS90UB953-Q1 mates well with the MIPI CSI-2 video output of the IMX390 imager. Once combined with the filters for the POC, video, I^2C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coax cable. For more information on the cable itself, see the *Cable requirements for the DS90UB913A and DS90UB914A application report*.

2.2.3 TPS62162-Q1 and TPS62423-Q1

To minimize form factor without trading performance, smaller components with specific features are selected for the power supply section of the design. One important design goal is to increase power efficiency without adding any significant noise that may couple to the imager output. This is often a challenge, as these two requirements typically stand in opposition. A switching power supply is generally more efficient than a linear regulator, but can add noise to the system. To navigate around this disadvantage, frequencies below 1 MHz are avoided, as camera sensor circuits are particularly sensitive to this frequency range. Additionally, to avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. The selected TPS62162-Q1 and TPS62423-Q1 switching regulators both meet this requirement as they operate at 2.25 MHz. The importance of switching frequency is twofold, as it also helps to reduce the size of discrete components in the circuit, enabling the design of a smaller form factor.

2.2.4 LP5907-Q1

The LP5907-Q1 series of LDO linear regulators are a low-noise, low quiescent current, line of devices that can supply up to 250 mA of output current. The components are additionally available in a small 1-mm × 1-mm X2SON package, making them ideal for creating supply rails with very minimal area. In addition to the aforementioned, the devices also feature a high power-supply rejection ratio (PSRR) and a tight output voltage tolerance (±2%) making the devices ideal for ADAS camera applications.

2.2.5 TPS3700-Q1 and TPS3702-Q1

Voltage supervision of the design supply rails for both IMX390 and DS90UB953-Q1 serializer -- 2.9 V, 1.8 V, 1.2 V -- is accomplished through the TPS3700-Q1 and TPS3702-Q1 devices. The TPS3700-Q1 includes two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs. The device features adjustment of monitoring thresholds through the selection of external resistors. Low quiescent current, high accuracy, and its small footprint (1.5 mm × 1.5 mm) WSON make the device well suited for automotive applications with small form factors. The TPS3702-Q1 is an integrated overvoltage and undervoltage window comparator with a large input voltage range, and high threshold accuracy. The TPS3702-Q1 fixed voltage devices come in various thresholds from ±1% to ±10% of the nominal monitored voltage. The flexibility of threshold options, small footprint and low quiescent current make it an excellent choice for voltage monitoring in automotive applications.

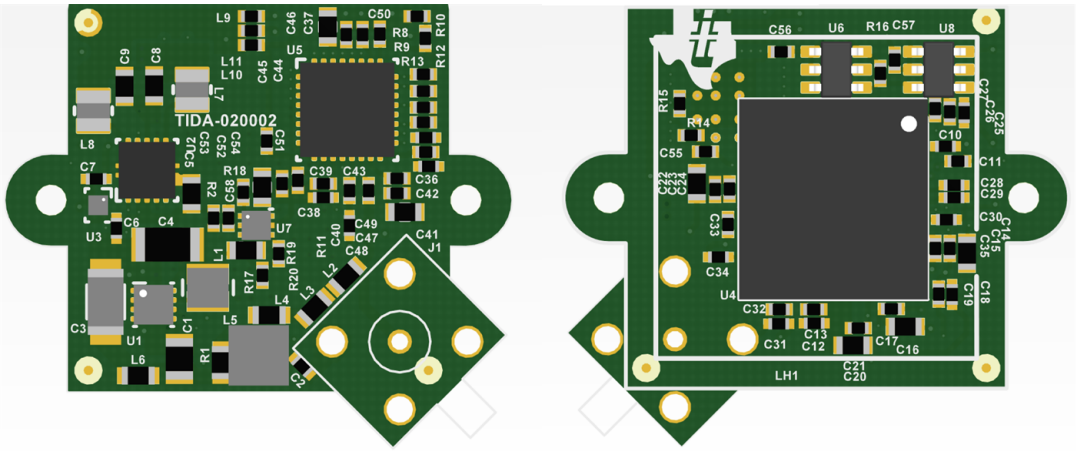
2.3 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.3.1 PCB and Form Factor

This reference design is not intended to fit any particular form factor; however, the goal of the design is to showcase a solution with minimal PCB area and compact design. The square portion of the board is 20 mm × 20 mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.

Figure 3. PCB Top and Bottom Views



2.3.2 Power Supply Design

2.3.2.1 POC Filter

One of the most critical portions of a design that uses POC is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise-coupled backwards from the rest of the system.

The DS90UB953-Q1 and DS90UB960-Q1 SerDes devices used in this system communicate over two carrier frequencies, 2 GHz at full speed ("forward channel") and a lower frequency of 25 MHz ("backchannel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC.

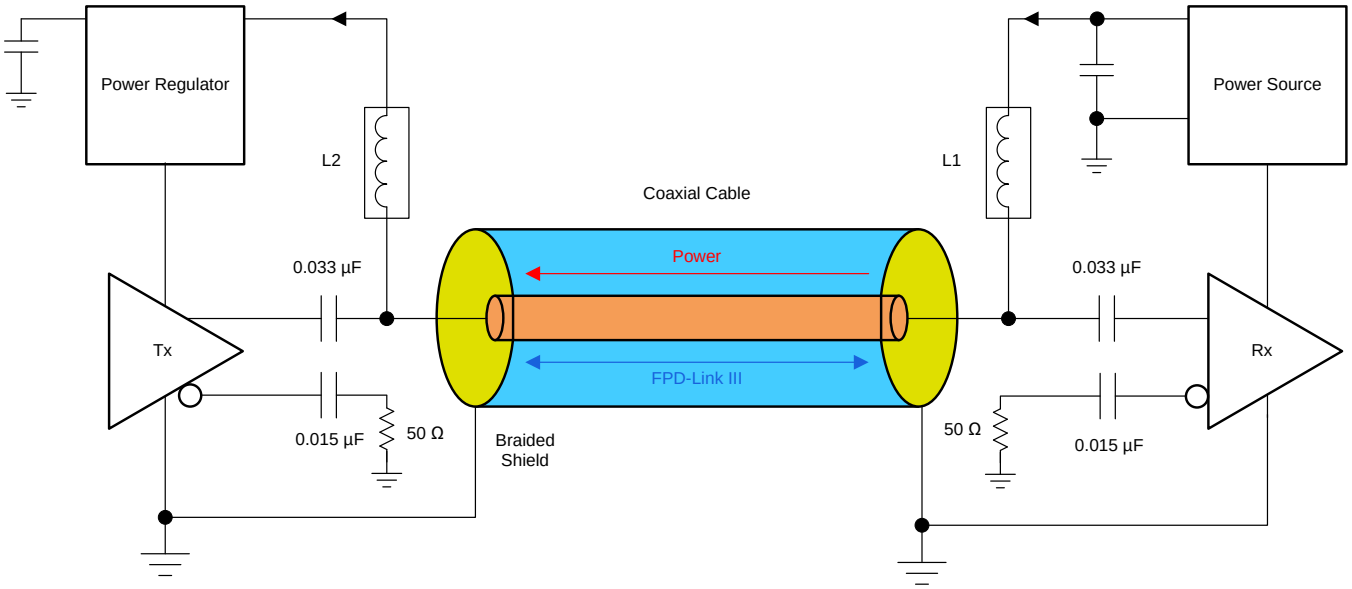
For the POC design, to enable the forward channel and backchannel to pass uninterrupted over the coax, an impedance of > 2 kΩ across the 10-MHz to 2.2-GHz bandwidth is required. To accomplish this, an inductor is typically chosen for filtering the 10-MHz to 1-GHz range, while a ferrite bead is chosen for filtering the 1- to 2.2-GHz frequency band. This complete filter is shown by L2 in Figure 4. L1 would be the same but its POC filter for the deserializer side of the FPD-Link III transmission.

In this camera design, it is imperative that this filter has the smallest footprint allowable. To accomplish this, the LQH3NPZ100MJRL 10-µH inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. This eliminates the need for a solution that would typically require two inductors, one for the lower frequency and another for the higher frequency.

For the high-frequency forward-channel filtering, inductors usually are not sufficient to filter above 1 GHz. This reference design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2.2-GHz range. This design uses three 1.5-kΩ ferrite beads because when in operation, the current through these devices reduces the effective impedance. Therefore three ferrite beads instead of two allows for more headroom across the whole frequency band. For good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the solution size can be minimized onboard for the POC inductor filtering. For more details, see the *Sending power over coax in DS90UB913A designs application report*.

Lastly, in regards to filtering, ensuring that the FPD-Link signal is uninterrupted is just as important as providing a clean, noise-free DC supply to the system. To achieve this, AC coupling capacitors shown by the 0.033 µF and 0.015 µF are chosen to ensure the high-speed AC data signals are passed through but that the DC is blocked from getting on the data lines. A smaller capacitance is required for the DS90UB953-Q1 and DS90UB954-Q1 devices than previous generations, because they need to pass 4 Gbps of data while the previous generation only needed to pass the 2 Gbps of data seen on 1-MP cameras.

Figure 4. Power Over Coax



2.3.2.2 Power Supply Considerations

As this reference design is targeted at automotive applications, there are several considerations that limit design choices. Additionally, the following list of system-level specifications helped shape the final overall design:

- The total solution size needs to be minimized to meet the size requirement of this design, which is less than 20 mm × 20 mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate the need for external circuitry.
- To avoid interference with the AM radio band, all switching frequencies need to be greater than 1700 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this reference design looks at higher frequency switchers
- All devices need to be AEC Q100-Q1 rated.

Before parts can be chosen, the input voltage range, required voltage rails, and required current per rail must be known. In this case, the input voltage is a pre-regulated 12-V supply coming in over the coaxial cable. This system has only two main devices, the imager and serializer, which consume the majority of the power; the current draw of the supervisors is insignificant and can be left out of these calculations. The requirements for these devices are shown in Table 2:

Table 2. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (MAX) (A)	POWER (MAX) (W)
DS90UB953			
VDD-1.8	1.8	0.225	0.405
IMX390			
VDD-1.2	1.2	0.388	0.4656
VDD-1.8	1.8	negligible	0
VDD-2.9	2.9	0.063	0.1827
Supply Rails Total Current Requirement and Maximum Power			
1.2-V rail	1.2	0.388	0.4656
1.8-V rail	1.8	0.225	0.2810
2.9-V rail	2.9	0.063	0.1827
3.3-V rail	3.3	0.327	1.0785

The 12-V supply over the coaxial is first stepped down to 3.3 V, which then supplies the rest of the system on the camera module. In this design, the 1.8-V rail supplies both the DS90UB953 supply, and the interface supply of the IMX390 imager. Since the current consumed by the DS90UB953 serializer is predominantly greater than the IMX390 interface supply, the 1.8-V current provided to the IMX390 imager can be considered as negligible. The IMX390 2.9-V analog rail requires 63 mA, the DS90UB953 serializer 1.8-V rail requires 225 mA, and the IMX390 digital 1.2-V rail requires 388 mA. Assuming 100% efficiency to simplify calculations with the previous values, it is calculated that the 3.3-V supply will require 327 mA to successfully power the 1.2-V, 1.8-V, and 2.9-V rails. Because the input and output voltages, output current requirements, and total wattage consumption are known, the input current can be calculated with the following equation:

$$P = V \times I = 12V \times I_{IN} = 1.0785\ W$$
$$\therefore\ I_{IN} = (1.0785\ W \times 12V) = 89.9\ mA \quad (1)$$

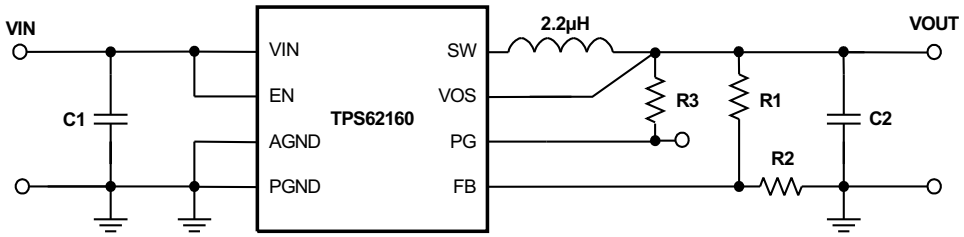
This information provides a strong foundation in the selection of power topologies and inductive passives that will be explained in later sections. This approximation does ease calculations with the assumption of 100% efficiency; however, for more understanding of true efficiency values reference the device data sheets.

Due to the requirement of Q100, it is mandatory that the switching frequency is rated outside of the AM band and must satisfy the voltage and current requirements derived previously. As the input voltage is a regulated voltage that will always be greater than any of the power rails produced, it is easily understood that the devices to select should either be step-down converters (bucks) or LDOs. Bucks are generally included in supplies where switching noise is not a significant concern, and power savings is the largest care about. On the other hand, LDOs can be incorporated in establishing low-noise analog supplies that reduce inherent noise and are more robust against EMI interactions; however, this is at the expense of larger current consumption.

The required current consumption and efficiency demands of the design make the TPS62162, TPS62423, and LP5907 excellent candidates in establishing the supply rails of the design. In this reference design, the TPS62162-Q1 is primarily responsible for providing a pre-regulator voltage of 3.3 V. Essentially the TPS62162-Q1 switching supply steps down the 12-V POC input to 3.3 V. This 3.3-V rail then supplies power to the TPS62423 step-down buck and the LP5907 linear regulator (LDO). The TPS62423 provides the interface and digital supply for both the IMX390 imager and DS90UB953 serializer, while the LP5907 device creates a clean, low-noise supply for the 2.9-V analog supply for the IMX390.

This cascaded topology allows for a more efficient design as it prevents the TPS62162 device from operating in discontinuous mode. This allows better prediction and control of switching noise produced by the devices, which results in operation with increased efficiency.

Figure 5. Typical Application Circuit



Component selection and design theory are found in the *Application Information* section of the *TPS62162-Q1 3-V to 17-V 1-A step-down Ccnverter with DCS-Control™ data sheet*.

2.3.2.2.1 Choosing the TPS62162-Q1 Output Inductor and Capacitor

To remain above the 1700-kHz frequency value mentioned in Section 2.3.2.2, the buck converter must always operate in continuous mode. To ensure that it does operate in this mode, the inductance is calculated with the previously-calculated output current, along with input and output voltage:

$$L_{MIN} = \frac{[V_{OUT} \times (V_{IN(MAX)} - V_{OUT})]}{\left(2 \times V_{IN(MAX)} \times I_{OUT} \times f\right)} = \frac{[3.3\ V \times (17\ V - 3.3\ V)]}{\left(2 \times 17\ V \times 0.327\ A \times 2.25\ MHz\right)} = 1.81\ \mu H \quad (2)$$

Since 1.81 µH is not a standard value for inductive passives, a 3.3 µH was chosen to ensure additional margin, and to effectively minimize voltage and current ripple on the supply line.

Due to the fact that this device is internally compensated, it is only stable for certain component values in the LC output filter. The application note on optimizing the output filter[6] has the chart of stable values shown in Table 3. The value 3.3 µH is on this chart and with these recommended values, this reference design uses a 22-µF output capacitor and remains in the stable region of effective corner frequencies.

Table 3. Stability Versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
	EFFECTIVE CORNER FREQUENCIES (kHz)								
0.47 µH	151.4	103.8	70.0	47.9	32.8	23.2	16.4	11.6	8.2
1.00 µH	103.8	71.2	48.0	32.8	22.5	15.9	11.3	8.0	5.6
2.2 µH	70.0	48.0	32.4	22.1	15.2	10.7	7.6	5.4	3.8
3.3 µH	57.2	39.2	26.4	18.1	12.4	8.8	6.2	4.4	3.1
4.7 µH	47.9	32.8	22.1	15.1	10.4	7.3	5.2	3.7	2.6
10.0 µH	32.8	22.5	15.2	10.4	7.1	5.0	3.6	2.5	1.8

	Recommended for TPS6213x, TPS6214x, TPS6215x, TPS6216x, and TPS6217x
	Recommended for TPS6213x, TPS6214x, and TPS6215x only
	Stable without Cff (within recommended LC corner frequency range)
	Stable without Cff (outside recommended LC corner frequency range)
	Unstable

With the inductance value chosen, the design now needs an inductor with a proper saturation current. This is the combination of the steady-state supply current as well as the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current from *TPS6216x-Q1 3-V to 17-V 1-A step-down converter with DCS-Control™ data sheet* using:

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L(min) \times f_{SW}} \right) \quad (3)$$

where

- I_L(max) is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- $L_{(min)}$ is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency

The parameters for this reference design using the TPS62162-Q1 are:

- V_{OUT} = 3.3 V
- $V_{IN(max)}$ = 17 V
- $L_{(min)}$ = 3.3 µH

- f_{SW} = 2.25 MHz

These parameters yield an inductor current of ΔI_L = 360 mA. The maximum current draw of the system through this regulator is 270 mA. The minimum saturation current is calculated as:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} = 327\ mA + \frac{360\ mA}{2} = 507\ mA \quad (4)$$

The TPS62162-Q1 on this design uses a Coilcraft® XPL2010-332MLB, which has a saturation current of 700 mA with a 10% drop-in inductance. This part comes in a very small 1.9-mm × 2.0-mm package.

2.3.2.2.2 Choosing the TPS62423-Q1 Output Inductor and Capacitor

Similar to the TPS62162-Q1, this device is internally compensated, and is only stable for certain component values in the LC output filter. The TPS62423-Q1 has internal loop compensation to work with a specific output filter corner frequency, with L = 2.2 µH and Cout = 10 µF as the recommended value. This design uses these recommended inductor and capacitor values. If selecting different values, the product of L × Cout must be constant while selecting a smaller inductor or increasing capacitor value.

Once the inductance value is chosen, the saturation requirement of the inductor must be determined again by combining the steady-state supply current and the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current using:

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (5)$$

where

- f = Switching frequency (2.25-MHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current

The parameters for this design using the TPS62423-Q1 1.8-V output rail are:

- V_{OUT} = 1.8 V
- V_{IN} = 3.3 V
- L = 2.2 µH
- f_{SW} = 2.25 MHz

These parameters yield an inductor current of ΔI_L = 166 mA. The maximum current draw through this regulator is 156 mA, which results in the following minimum saturation current calculation:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} = 156\ mA + \frac{166\ mA}{2} = 239\ mA \quad (6)$$

While the parameters for the TPS62423-Q1 1.2-V rail are:

- V_{OUT} = 1.2 V
- V_{IN} = 3.3 V
- L = 2.2 µH
- f_{SW} = 2.25 MHz

These parameters yield an inductor current of ΔI_L = 154 mA. The maximum current draw through this regulator is 388 mA, resulting in the following minimum saturation current calculation:

$$L_{SAT} \geq I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} = 388\ mA + \frac{154\ mA}{2} = 465\ mA \quad (7)$$

Both outputs on the TPS62423-Q1 device of this design use a Murata® LQM2MPN2R2NG0, which has a rated current of 900 mA at an ambient temperature of 125°C. This part comes in a very small 1.6-mm × 2.0-mm package.

2.3.2.2.3 LP5907-Q1 LDO

The design considerations for the LP5907-Q1 device are more relaxed than the previous buck converters as they do not require an output inductor. The only considerations for this LDO are sizing the input and output capacitance. For the input capacitance, a capacitor is not required for stability but for improved transient response performance, a 0.1-µF effective capacitance is recommended. The output capacitor requires a minimum effective capacitance of 0.1 µF for stability. In both cases, the input and output capacitor can benefit from using a 1-µF X5R/X7R capacitor so that when experiencing derating, they will be above 0.1 µF.

2.3.2.2.4 Voltage Supervision Using TPS3700-Q1 and TPS3702-Q1

This design uses supervisors to monitor the regulation of all three power rails (1.2 V, 1.8 V, and 2.9 V). If needed, the output of these supervisors can be utilized as part of a functional safety implementation. The supervisor outputs are routed to GPIO pins on the DS90UB953-Q1 serializer. This allows them to be transmitted over the backchannel on the coaxial cable to the deserializer. These signals can then be output to GPIO pins on the deserializer side, and read by an MCU or processor.

Both the TPS3700-Q1 and TPS3702-Q1 devices have open-drain, active-low outputs. This means that the output requires a pullup resistor, and the signal is high when the voltage is within the specified window. When the monitored voltage falls out of regulation, the output is then pulled low. The use of open-drain outputs allows the outputs of multiple supervisors to be tied together directly and create an OR logic, where the signal will be pulled low if either supervisor detects voltage out of regulation. This design takes advantage of this fact to reduce the number of GPIOs used on the DS90UB953-Q1 serializer. The two TPS3702-Q1 supervisors, monitoring the 1.2-V and 1.8-V digital rails, are tied together. This allows for the TPS3700-Q1 device, monitoring the sensitive 2.9-V analog rail, to have its own GPIO pin. This results in one GPIO dedicated to monitoring both digital rails, and a second GPIO dedicated to monitoring the analog rail for the imager.

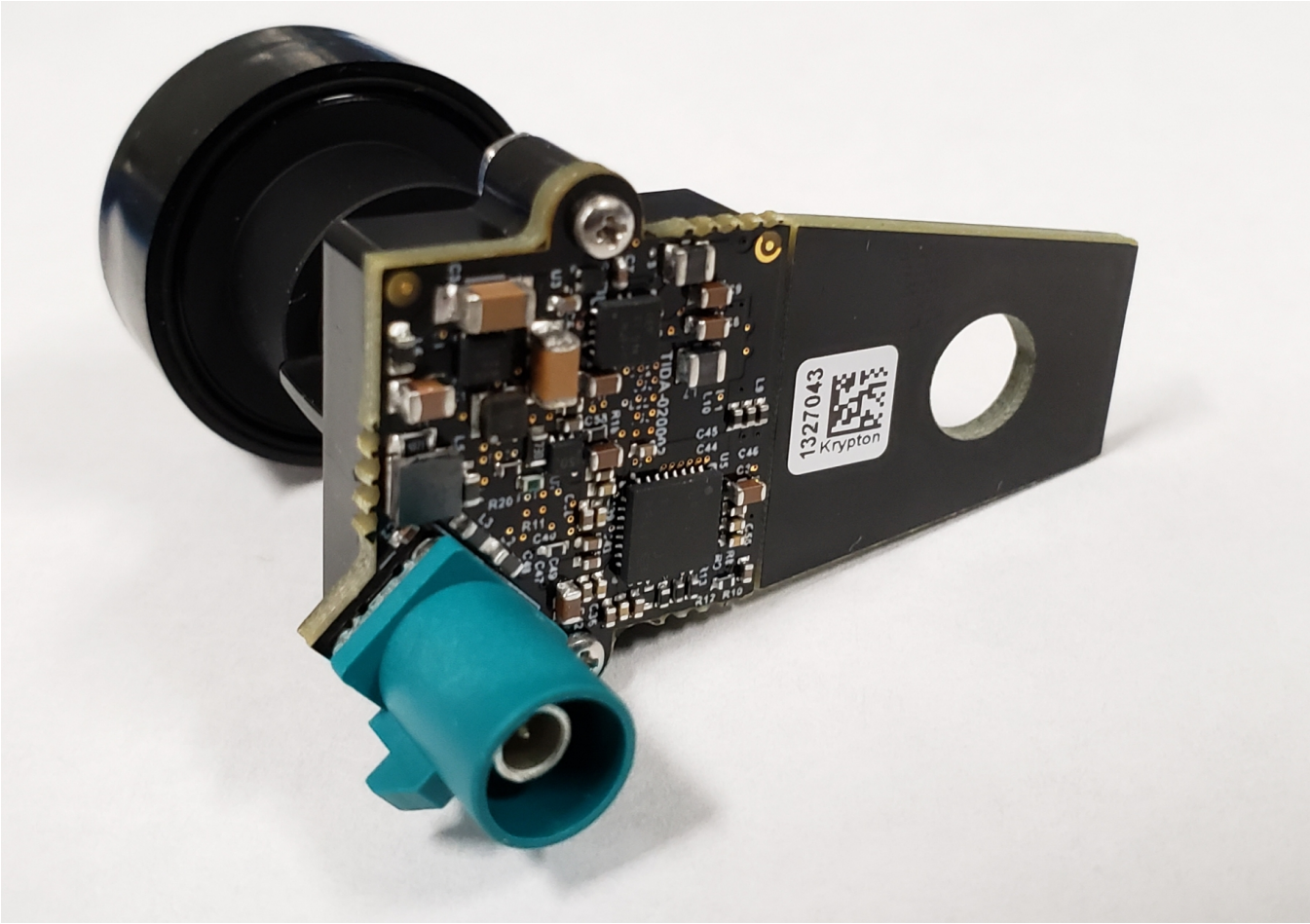
Once these signals are received on the deserializer side, an MCU or processor can then send commands over the coaxial cable back to the camera module. For example, one of the GPIO pins on the DS90UB953 serializer is tied to the reset pin of the IMX390 imager, and could be used to reset the imager device. The serializer is also capable of being reset through the 'RESET_CTL' register (Address 0x01), which can be accessed over I2C communications from the deserializer side. If the MCU is controlling the power supply providing the power over coax voltage, this signal could also be used to cycle the power to the entire camera module.

3 Hardware, Testing Requirements, Test Results

3.1 Required Hardware

This reference design needs only one connection to a system with a compatible deserializer over the FAKRA connector as shown in Figure 6.

Figure 6. Getting Started With Board

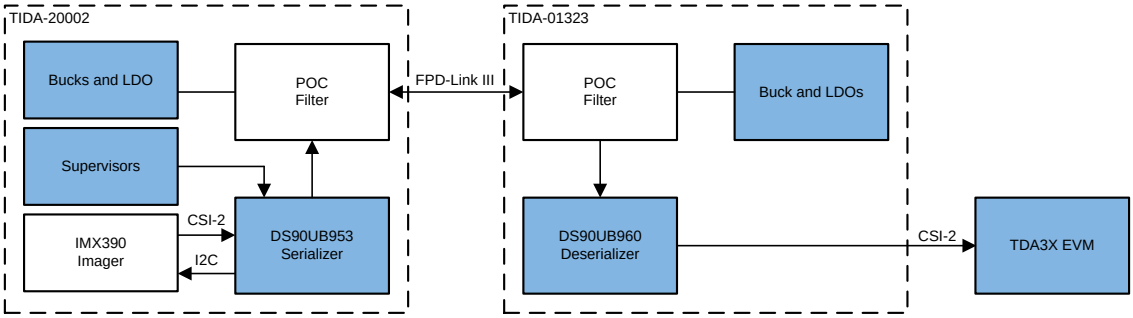


3.1.1 Video Output Hardware Setup

Figure 7 shows the setup to test the video output of the camera module on this reference design. This reference design includes an IMX390 image sensor, which connects to the DS90UB953-Q1 serializer over CSI-2 and I^2C interfaces. The DS90UB953-Q1 serializer then connects through POC to a DS90UB960-Q1 quad deserializer. Note that for test setup, only one channel is used from the DS90UB960-Q1 device.

To enable video output from the DS90UB960-Q1 device, the EVM is connected to the CSI-2 Samtec connector on the TDA3x EVM. The TDA3x EVM enables video output by writing all the backchannel I^2C setting configurations for the IMX390, DS90UB953-Q1, and DS90UB960-Q1 devices. When these writes are completed, Vision SDK software enables video output to an HDMI-connected monitor.

Figure 7. Block Diagram of Video Output Setup



3.1.2 FPD-Link III I^2C Initialization

With the setup in Figure 7 connected, the TIDA-01323 design is supplied input power and this is delivered to the POC supply for the camera power of this reference design and also is used to step down to 1.8 V and 1.1 V for the DS90UB960-Q1 supplies. Now the IMX390, DS90UB953-Q1, and DS90UB960-Q1 devices have power. Lastly, by connecting the TDA3x EVM to the TIDA-01323 design, the I^2C writes for initialization can begin. Note that the following writes are only showing one channel camera and may not be the mode wanted for specific multi-camera mode. For example, each camera requires its own port initialization using address 0x3A for that specific port. The writes to initialize the DS90UB960-Q1 deserializer and DS90UB953-Q1 serializer are as follows:

- Deserializer slave I^2C address 0x7A (8-bit) or 0x3D (7-bit):
  - Register 0x4C with 0x01: Enables write enable for Port 0
  - Register 0x58 with 0x5D: I^2C passthrough enabled and backchannel frequency select
  - Register 0x5C with 0x30: Sets serializer alias to 0x30 (8-bit) or 0x18 (7-bit)
  - Register 0x5D with 0x34: Sets slave ID for imager to 0x34 (8-bit) or 0x1A (7-bit)
  - Register 0x65 with 0x34: Sets slave alias for imager to 0x34 (8-bit) or 0x1A (7-bit)
  - Register 0x6D with 0x7C: Configures port to coaxial mode and FPD III to CSI mode
  - Register 0x32 with 0x01: Enables TX write enable for port 0 and port 1
  - Register 0x33 with 0x03: Enables DS90UB960-Q1 CSI output and sets to 2 lane mode
  - Register 0x21 with 0x03: Sets round robin forwarding for CSI0 and CSI1
  - Register 0x20 with 0x00: Forwarding enabled for all ports and ports forwarded to CSI-2 Port 0
- Serializer slave I^2C address 0x30 (8-bit) or 0x18 (7-bit):
  - Register 0x06 with 0x21: Sets HS_CLK_DIV and DIV_M_VAL for CLKOUT from DS90UB953-Q1 to IMX390
  - Register 0x07 with 0x28: Sets DIV_N_VAL for CLKOUT from DS90UB953-Q1 to IMX390
  - Register 0x0E with 0xF0: Sets GPIO0 and GPIO1 as outputs, and GPIO2 and GPIO3 as outputs on DS90UB953-Q1
  - Register 0x0D with 0x01: Pulls RESET pin on IMX390 high to bring imager out of reset

3.1.3 IMX390 Initialization

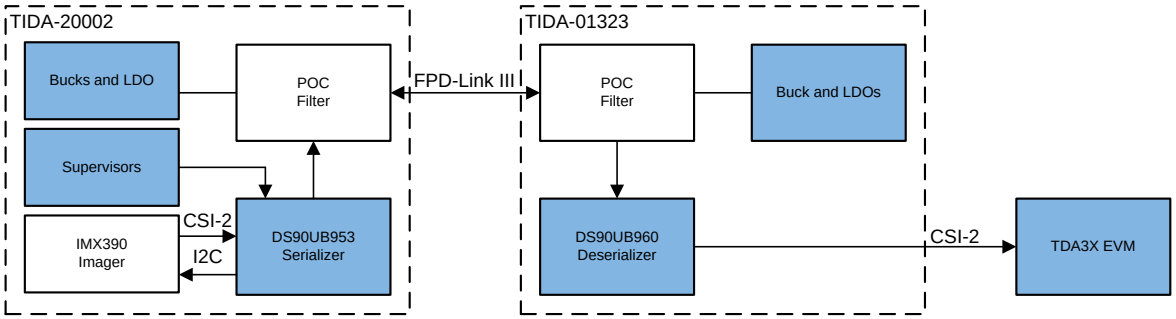
Once the FPD-Link III setup is done for the DS90UB953-Q1 and DS90UB960-Q1 devices, the I^2C initialization can now be done on the IMX390. For these writes, see the IMX390 data sheet for register settings. There are many register settings listed, but as long as the DS90UB953-Q1 and DS90UB960-Q1 FPD-Link III parts are configured, the I^2C backchannel allows for the IMX390 to be accessed at address 0x34 in 8-bit addressing or 0x1A in 7-bit addressing.

3.2 Testing and Results

3.2.1 Characterization Test Setup

For the following tests to verify power supply and I^2C communication, the camera is connected to TIDA-01323, a quad 2MP FPD-Link III hub which utilizes the DS90UB960-Q1 deserializer. The TIDA-01323 then connects to the TDA3XEVM.

Figure 8. Block Diagram of Characterization Test Setup



3.2.1.1 Power Supplies Start Up

Figure 9 shows the probe setup to measure the power sequence turnon for the system power, measuring 12-V input from POC and the 3.3-V supply to the system.

Figure 9. Measuring System Power Supply

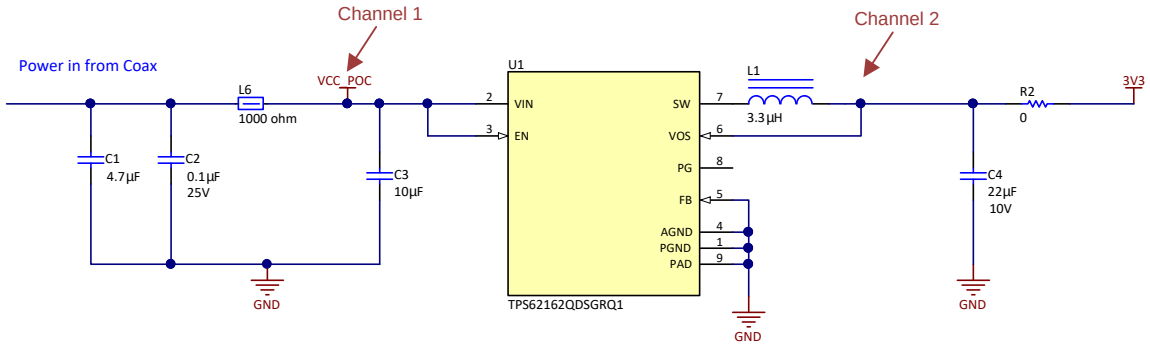
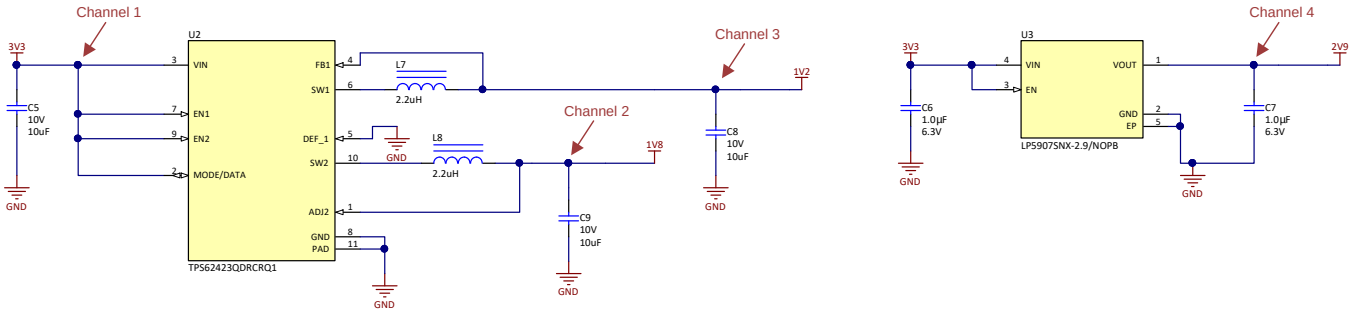


Figure 10 shows the probe setup to measure the power sequence turnon for the point-of-load power, measuring the 3.3-V system supply, 2.9-V supply to imager, 1.8 V to the imager and serializer, and 1.2 V to the imager.

Figure 10. Measuring Point-of-Load Power Supplies



3.2.1.2 Power Supply Start Up—1.8-V Rail and Serializer PDB Setup

For the serializer to be initialized after the 1.8-V power supply comes up, an RC time constant delay is added to the 1.8-V power supply of the DS90UB953-Q1 serializer. This ensures that the PDB reset line goes high only after the supply is high.

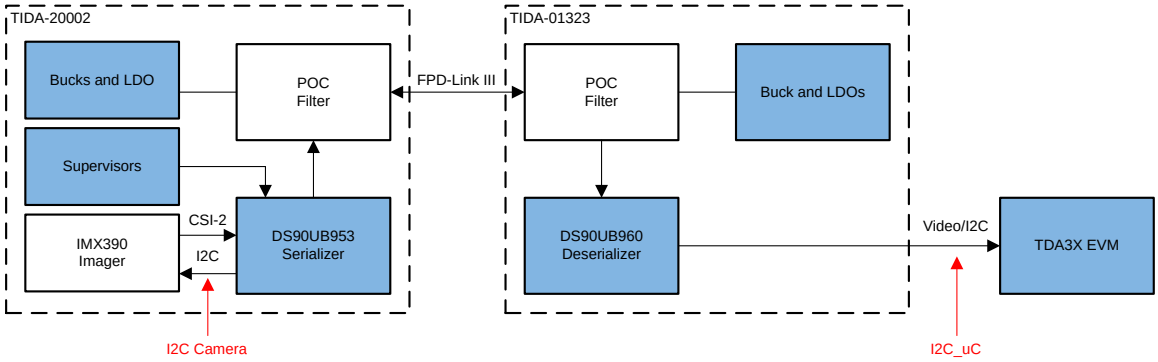
3.2.1.3 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two buses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)
2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

Connections are made to both the clock and data lines of each bus as Figure 11 shows.

Figure 11. Setup for Monitoring I²C Transactions



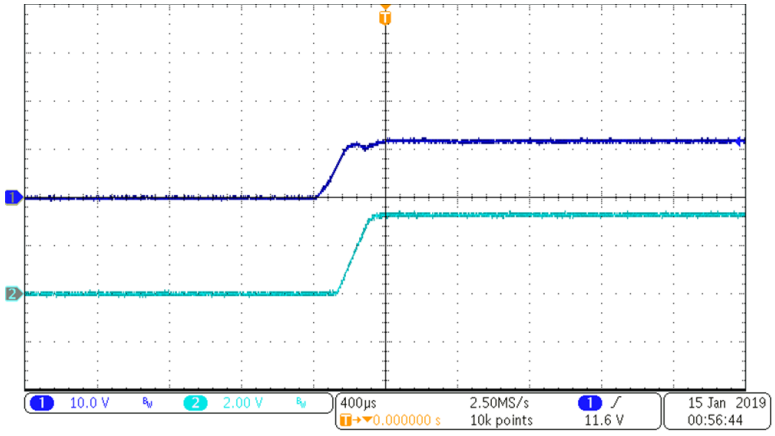
3.2.2 Characterization Test Data

The following sections show the test data from verifying the functionality of the camera design.

3.2.2.1 Power Supplies Start Up

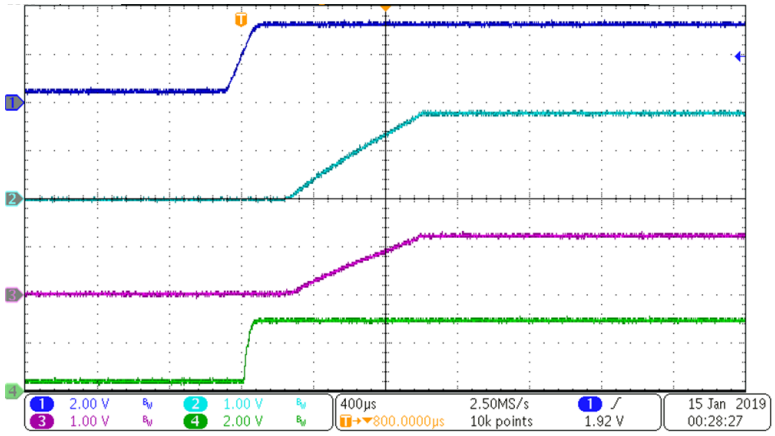
Power start-up behavior for the input power supply, and a 3.3-V system supply is shown in Figure 12. The start-up sequence shows that when the 12-V input reaches turnon voltage for the TPS62162-Q1 device, the 3.3-V supply starts turning on.

Figure 12. System Power Supply Start Up



The same behavior is exhibited for the 2.9-V, 1.8-V, and 1.2-V supplies, which start turning on when the 3.3-V output has reached the minimum input needed for the switching supplies and the LP5907-Q1 device. Figure 13 shows the 3.3-V system supply followed by the 2.9-V supply, which is generated from the LDO. While the 1.8-V and 1.2-V analog rails trail behind and are generated from the switching supply.

Figure 13. Point-of-Load Power Supply Start Up

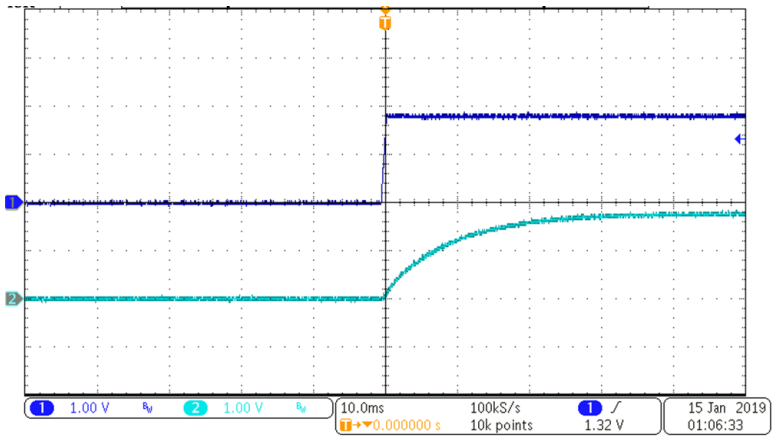


NOTE: (Channel 1): 3.3-V supply; (Channel 2): 1.8-V supply; (Channel 3): 1.2-V supply; (Channel 4): 2.9-V supply

3.2.2.2 Power Supply Start Up—1.8-V Rail and PDB

The only start-up requirement is that the PDB pin of the serializer remains low until all power supplies stabilize to their final voltages. Figure 14 shows the power supply start up.

Figure 14. Serializer Power-Up Sequence



NOTE: Channel 1 (blue) 1.8 V; channel 2 (turquoise) PDB

Figure 14 shows that PDB comes to V_{DD} × 0.65 in approximately 10 ms because of the 1-µF delay capacitor on the PDB pin. This delay is more than sufficient for the PDB pin, which is required to come up only after the 1.8-V supply is stable.

3.2.2.3 Power Supply Voltage Ripple

To achieve a quality output video stream, the output voltage ripple on the IMX390 and DS90UB953-Q1 supplies must be low so that it does not affect the integrity of the high-speed CSI-2 data and internal PLL clocks. Measurements for 3.3-V, 2.9-V, 1.8-V, and 1.2-V rails are shown in Figure 15, Figure 16, and Figure 17, respectively. The key rails that are significant to impact on the imager are the 2.9-V and 1.2-V rails because 2.9 V is the analog rail and 1.2 V is the VDD rail for the imager. As measured, the 2.9-V and 1.2-V rails have a ripple performance of 3.4% and 1% respectively . The 1.8-V rail is significant to the serializer, as it supplies the VDD and VDD_PLL rails. The 1.8-V rail has great voltage ripple performance at 0.4%. The 3.3-V rail powers the entire system and also has excellent ripple performance of 0.3%. The voltage ripple on all rails is low enough for video output to be successfully transmitted.

Figure 15. 3.3-V Output Voltage Ripple

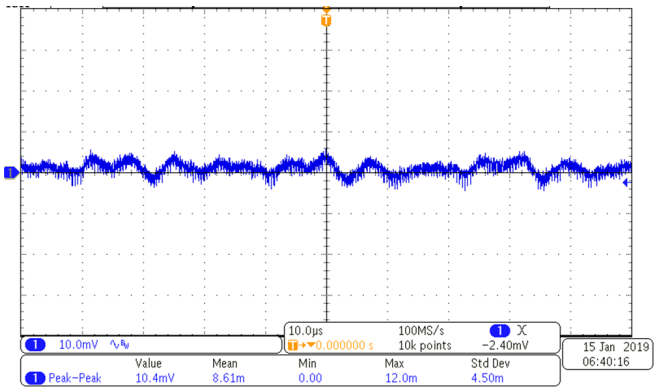


Figure 16. 2.9-V Output Voltage Ripple

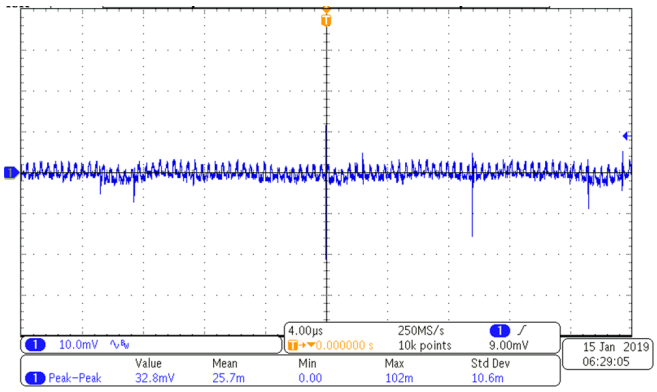


Figure 17. 1.8-V Output Voltage Ripple

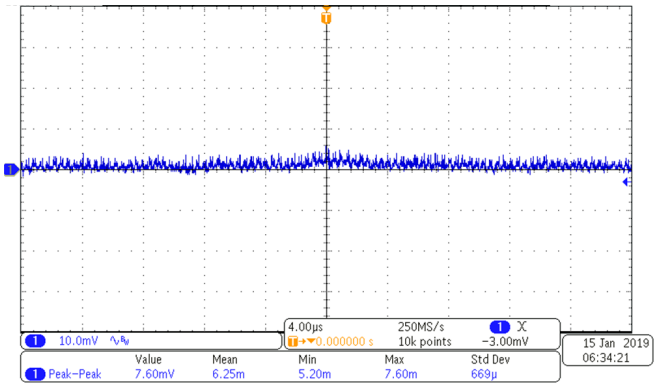
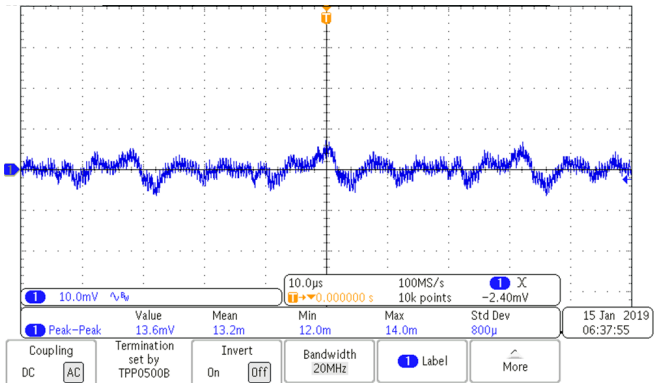


Figure 18. 1.2-V Output Voltage Ripple



3.2.2.4 Power Supply Load Currents

The last measurements to take in regard to the power supplies on the camera module are the load currents for the system supply, and the load currents on the IMX390 imager. These measurements verify total power consumption of the camera module as well as the load current for each individual rail on the IMX390 imager. For the following test data, each rail is drawing the specific load current outlined for the serializer and imager. All load current measurements are taken while a video output stream is present.

Table 4 displays the currents measured through each supply voltage in this reference design. The 12-V load current is the total input load for the camera module and measures at 80 mA. With this amount of current, the total input power consumption of the camera module is 960 mW. The 3.3-V system voltage from the TPS6216-Q1 is measured to be drawing 254 mA.

Table 4. Measured Supply Currents

VOLTAGE RAIL	MEASURED CURRENT
3.3 V	254 mA
1.2 V	245 mA
1.8 V	119 mA
2.9 V	57 mA
12 V	80mA

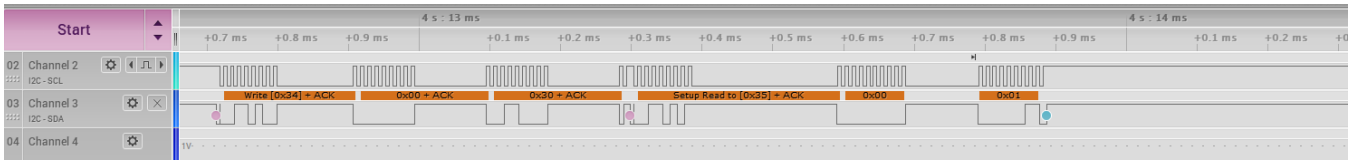
These values give both the input and output currents and voltages for the TPS62162-Q1 device, providing an estimate of the efficiency for this switching supply. The input power already mentioned is 960 mW from the 12-V power over coax. For the output power, using measured voltages of 3.29 V on the board and 254 mA, the total output power is 836 mW. To calculate system efficiency, the output power is divided by the input power to get 87%. With the larger step-down from 12 V to 3.3 V and a fairly low load current, 87% efficiency is reasonable.

As mentioned previously, the TPS62423-Q1 provides the design with the 1.2-V and 1.8-V supplies, and these rails source 245 mA and 119 mA, respectively. Using the previously-specified principal, the efficiency for the bucked supplies is the total output power of the TPS62423-Q1 divided by its input power, which results in an efficiency of 78%. The low-noise LDO sinks an additional 57 mA from the 3.3-V supply to provide a 2.9-V (VDDH) supply to the IMX390.

3.2.2.5 I²C Communications

Now that the power supplies are up and running, the I²C communication between the processor and the IMX390 imager over the FPD-Link III backchannel can be confirmed. Figure 19 shows a read I²C communication from the TDA3x EVM to the IMX390 imager on this reference design.

Figure 19. I²C Transactions



The I²C transactions are measured at the deserializer side between the host microprocessor and the DS90UB960-Q1 device. The read is to the imager, which is at slave alias address 0x1A (7-bit) or 0x34 (8-bit). The read to the imager is for its register 0x0030 with data 0x0100, which is a default value for the imagers *White Balance Gain Register*.

The image illustrates successful communication over the FPD-Link III backchannel as the imager is able to relay register contents to the deserializer. By acknowledging the I²C read, the imager has confirmed that it is present and at the correct slave address.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-020002.

4.2 Bill of Materials

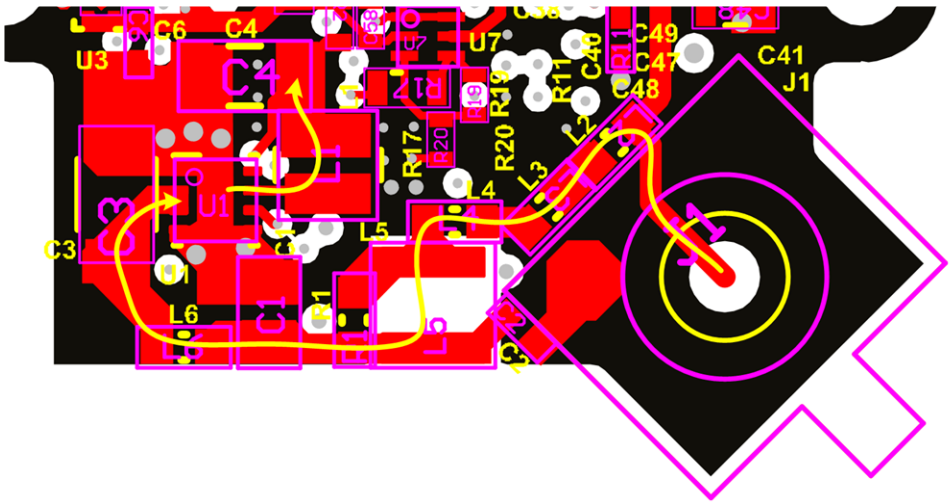
To download the bill of materials (BOM), see the design files at TIDA-020002.

4.3 PCB Layout Recommendations

4.3.1 Switching DC/DC Converters

During part placement and routing, it is helpful to always consider the path the current will be taking through the circuit. The yellow line in Figure 20 shows the current path from the coax in through the POC filter -- L2, L3, L4, L5, R1, C1, C2 -- and then out to the ferrite bead, L6, input capacitor, C3, to U1, or the TPS62162-Q1. The path then continues to the 3.3-V output of the switcher to the output inductor L1 and output capacitor C4. Any return currents from the input capacitor C3 or the output capacitor C4 are joined together at the top left of U1 before they are connected to the ground plane. This reduces the amount of return currents, and thereby, voltage gradients in the ground plane. This may not be noticeable in the performance of the converter, but it will reduce its coupled noise into other devices.

Figure 20. Routing FB Traces Around SW Nodes

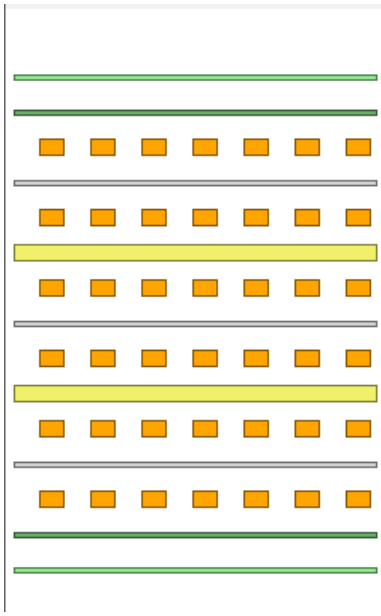


4.3.2 PCB Layer Stackup Recommendations

The following are PCB layer stackup recommendations. Because automotive is the target space, there are a few extra measures and considerations to take, especially when dealing with high-speed signals and small PCBs:

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines
- If using a four-layer board, layer 2 must be a ground plane. Because most of the components and switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers are used in this board to simplify BGA fan out and routing. Figure 21 shows the stackup used in this board:

Figure 21. Layer Stackup



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Layer	Signal	Copper	1.4		
Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Core	8	370HR	4.2
Layer 3 - PWR	Signal	Copper	1.4		
Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.4		
Dielectric 4	Dielectric	Core	8	370HR	4.2
Layer 5 - Signal/...	Signal	Copper	1.4		
Dielectric 3	Dielectric	Prepreg	12.6	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

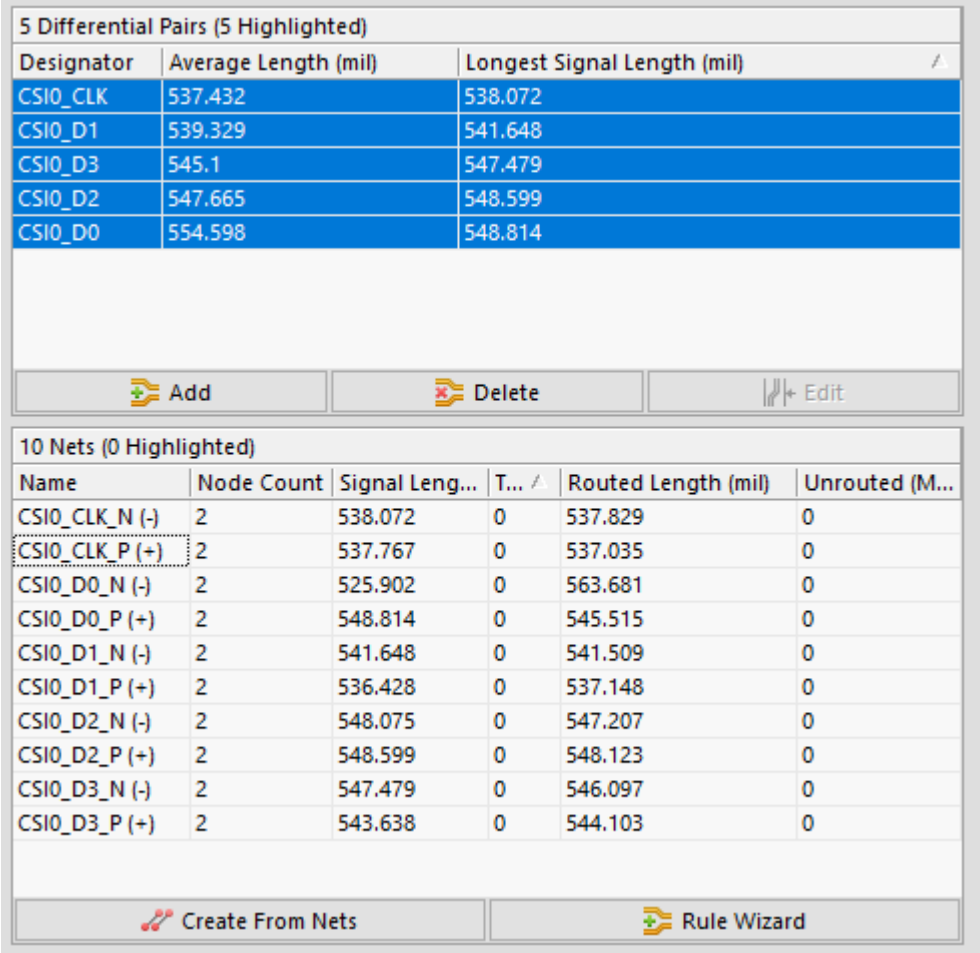
4.3.3 Serializer Layout Recommendations

High-speed CSI-2 routing is an important design aspect for the DS90UB953 on this reference design. Layout considerations for trace impedance and length matching must be a high priority for good signal quality of the high-speed video data. For location of the CSI-2 traces, crosstalk can easily happen with high-speed signals, so it is important on this camera module design that the traces are away from the FPD-Link III RX traces to reduce coupling.

Trace impedance is one critical aspect to the CSI-2 lane routing. Route the differential pairs for CLK and DATA with a controlled 100-Ω differential impedance (±20%). For trace impedance to be within specifications and within range of each other, the length and width of the trace plays a factor in this. To achieve tight impedance specs, length specifications also need to be strict within the positive-to-negative differential pair length and pair-to-pair length. If the length is not matched, at these high data switching speeds, the data can arrive at the 953 at different times and cause issues of synchronization between data and clock. The length difference between the positive and negative differential pair trace should be within 5 mils of each other. For length matching between each CSI-2 lane pair, the difference must be kept within 25 mils.

The last key points to address with CSI-2 routing is crosstalk and reflections. To reduce the effects of crosstalk between lanes, spacing between each differential lane must be at least three times the signal trace width. In addition, keep vias and bends on the traces to a minimum. The vias must ideally be two or fewer to minimize stubs that cause reflections. Bends must be as equal as possible in the number of left and right bends, and the angle of the bend must be greater than or equal to 135 degrees. When these layout considerations are followed, the video data integrity can be maintained. If for any reason there are high-speed concerns on the CSI-2 lane design, debug tools are available to run video data over the 1, 2, or 4 lanes. The imager must be set to output over the specified number of data lanes, and the DS90UB953 can then be set to correct number of lanes in register 0x02.

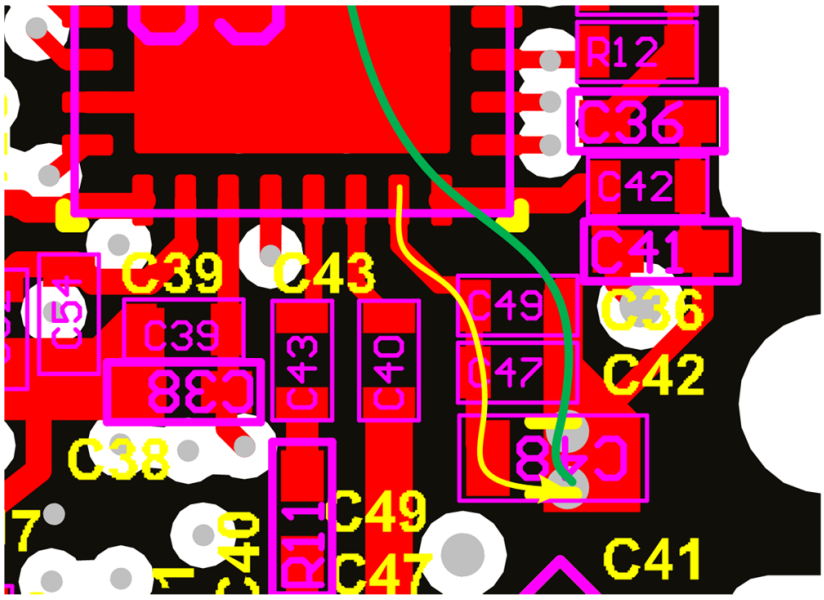
Figure 22. CSI-2 Differential Trace Routing



Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

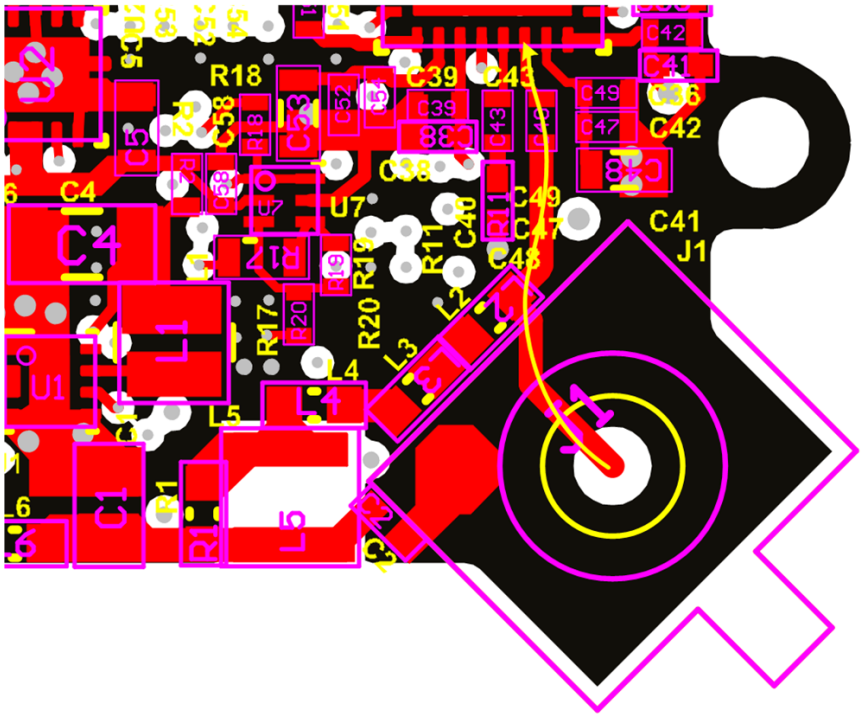
Figure 23 shows the supply current from C49 in yellow. The green line is the return path. The cross sectional area of this loop is very small.

Figure 23. Decoupling Current Loop



For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. Figure 24 shows the routing of the high-speed serial line, highlighted by the yellow line. The total length of the yellow line is about ½ inch.

Figure 24. High-Speed Serial Trace



4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-020002.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-020002.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-020002.

5 Related Documentation

1. Texas Instruments, *DS90UB953-Q1 MIPI CSI-2 FPD-Link III serializer for 2-MP/60-fps cameras and RADAR data sheet*
2. Texas Instruments, *TPS6216x-Q1 3-V to 17-V 1-A step-down converter with DCS-Control™ data sheet*
3. Texas Instruments, *TPS624xx-Q1 automotive 2.25-MHz fixed VOUT dual step-down converter data sheet*
4. Texas Instruments, *LP5907-Q1 automotive 250-mA, ultra-low-noise, low-I_Q LDO data sheet*
5. Texas Instruments, *Sending power over coax in DS90UB913A designs application report*
6. Texas Instruments, *Cable requirements for the DS90UB913A and DS90UB914A application report*
7. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 output filter application report*

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265