Design Guide: TIDA-050038
Integrated Power Supply Reference Design for NXP i.MX 8M Mini Processor

Description

TIDA-050038 is a system-on-module (SoM) development board integrating two TI PMICs, TPS6521825 and LP873347, with the NXP™ i.MX 8M Mini Application Processor. The hardware design also includes LPDDR4 SDRAM (2GB, x32-bit), QSPI NOR-Flash (32MB), 16GB eMMC 5.1, 32-kHz RTC oscillator, WiFi + Bluetooth module, and 9-channel current monitoring. The SoM board is compatible with the 8MMiniLPD4-EVK base board for full system evaluation. This design is intended for any project that is using the i.MX 8M Mini or i.MX 8M Nano processor and requires evaluation of alternate power solutions.

Resources

TIDA-050038	Design Folder
TPS6521825	Product Folder
LP873347	Product Folder
INA3221	Product Folder

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Features

- SoM for rapid development of NXP i.MX8M Mini systems
- Low-power modes and DVFS supported
- 9-channel current monitoring for DC-DCs and LDOs
- Wi-Fi® + Bluetooth® wireless connectivity
- Display connector (DSI), Camera connector (CSI), additional peripherals on compatible base-board
- Selectable boot options (SD, eMMC, QSPI)

Applications

- ARM-based SoM/CoM
- Intrusion control panel
- Barcode scanner
- HVAC gateway
- Thermostat
- Building security gateway
- Panel PLC (HMI)

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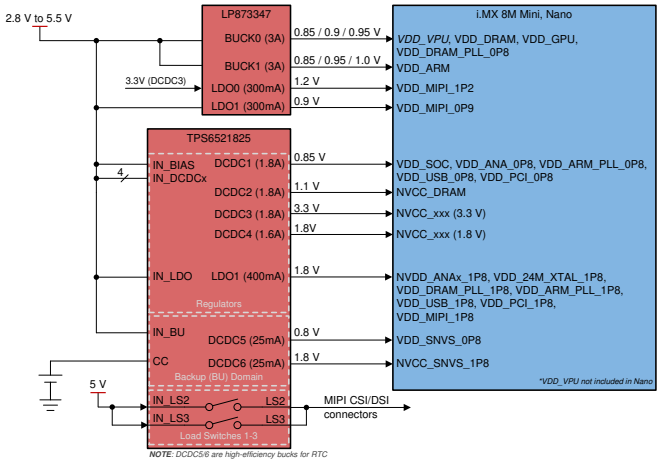

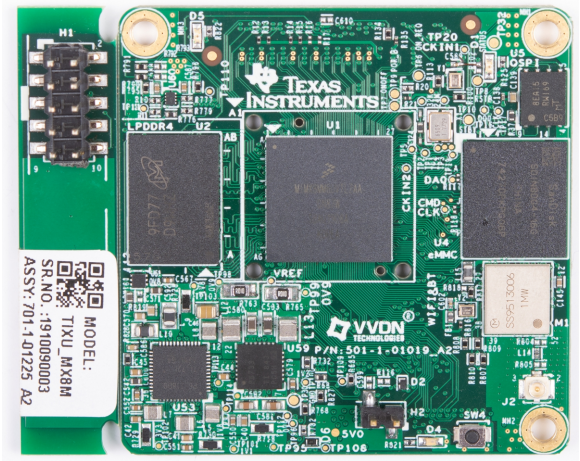

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1 System Description

TIDA-050038 is first-and-foremost a reference design for powering the NXP i.MX 8M Mini processor from the TPS6521825 and LP873347 PMICs. In order to show that the PMICs can power the processor, it made the most sense to build a SoM board that is compatible with the existing base-board (8MMiniLPD4-EVK), which includes a variety of peripheral connections to assist with development of various end equipments. As a result, the base board contains all the large connectors for wired communication, a slot for an SD Card containing the software image, as well as DIP switches for multiple BOOT options. The SoM board, on the other hand, contains all the on-board memory and module for wireless communication. Finally, to ensure the entire board is operational, we developed and tested software using the open-source embedded Linux Yocto SDK to get started testing this design.

1.1 Key System Specifications

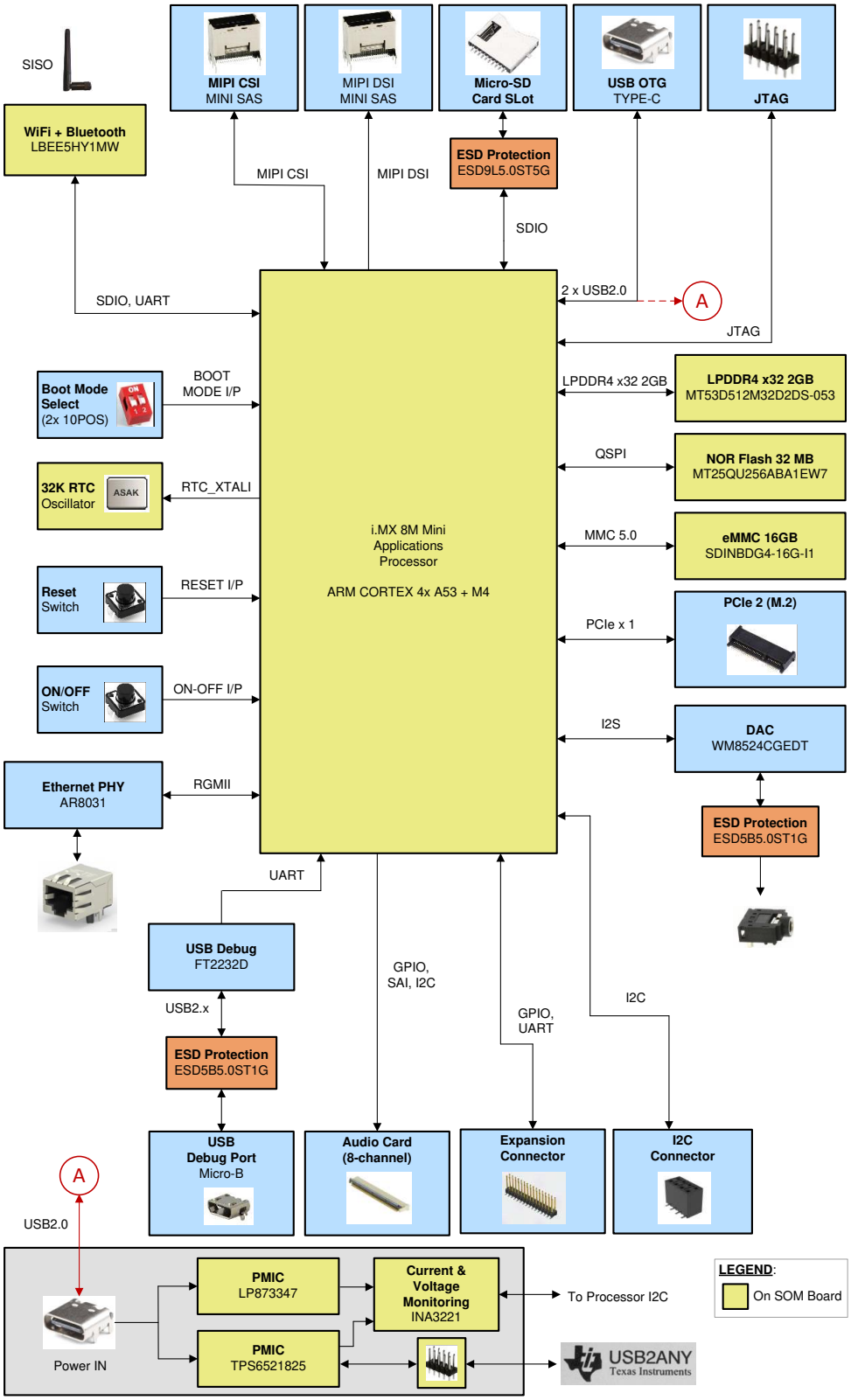
Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Processor	i.MX 8M Mini Dual-Core Applications Processor, MIMX8MM6DVTLZAA	Section 2.2.1
PMICs	TPS6521825 PMIC for powering RTC (SNVS) domain with GPIOs to enable external ICs, EEPROM pre-programmed with correct automatic sequencing for i.MX 8M Mini & DVFS controlled by I^2C	Section 2.3.1
	LP873347PMIC for delivering up to 3 A for core rails of i.MX 8M Mini processor, OTP pre-programmed with correct sequencing for i.MX 8M Mini & DVFS controlled by I^2C	Section 2.3.2
Memory	2GB x32-bit LPDDR4, 512Mb QSPI NOR-Flash (64MB), 8GB eMMC 5.0, SD v3.0 interface	Section 2.2.2
Wifi + Bluetooth	Support WiFi + Bluetooth with Murata device. WiFi must support 802.11ac standard and package size must fit in allotted board area.	Section 2.2.3
Current Monitoring	3x TI INA3221 devices are used to monitor current through 9 rails in the system (all DC-DCs and LDOs providing >100-mA of current)	Section 2.3.3
USB2ANY header	Debug method for PMIC separate from processor provided by USB2ANY (standard 100-mil pitch, 10-pin header). Must be outside of 2" x 2" square and capable of being detached from PCB.	Section 2.2.5
Manufacturability	The PCB must be completed without HDI (high-density interconnect) manufacturing technologies. For example, via hole size ≥ 8 mil and no via-in-pad allowed.	Section 2.4
Compatibility	Must be compatible with 8MMiniLPD4-EVK, using same high-density connectors from SoM board to base-board	Section 2.2.4
Size	Main PCB (excluding USB2ANY header) must be same size as original 8MMiniLPD4-EVK SoM board, 2" x 2"	Section 2.4.1

2 System Overview

2.1 Block Diagram

Figure 1. TIDA-050038 Block Diagram



2.2 Design Considerations

This design is intended to show the ability of the TI power devices to provide power to the i.MX 8M Mini processor and all of the peripheral ICs in a variety of designs. In order to verify this, we had to populate all of these other ICs on the design, starting with the processor. All other devices necessary to build an operational evaluation kit are included in this section. The power devices and other TI devices used in this design are described in Section 2.3.

2.2.1 Processor - i.MX 8M Mini Applications Processor

The i.MX 8M Mini applications processor is a processor from NXP and is their first embedded multi-core applications processor built using advanced 14LPC FinFET process technology providing more speed and improved power efficiency. This processor specializes in optimized low power consuming state-of-the-art media-specific features like high performance audio and video processing. The i.MX 8M Mini family of processor features of five cores (Quad Arm® Cortex®-A53 core operating up to 1.8GHz and one Cortex®-M4 core operating at 400MHz). It supports 32-bit/16bit LPDDR4 and DDR3L memory. This processor has number of other interfaces like Ethernet, MIPI CSI, MIPI DSI, PCIe and also supports audio interfaces such as I2S, AC97, TDM and S/PDIF. A detailed table listing the mapping for each pin on the iMX8MM processor can be found in Appendix A.

DESCRIPTION	MFG.	PART NUMBER
IC, i.MX 8M Mini series , Quad ARM Cortex-A53 core	NXP	MIMX8MM6DVTLZAA

2.2.2 i.MX 8M Mini Memory Interfaces

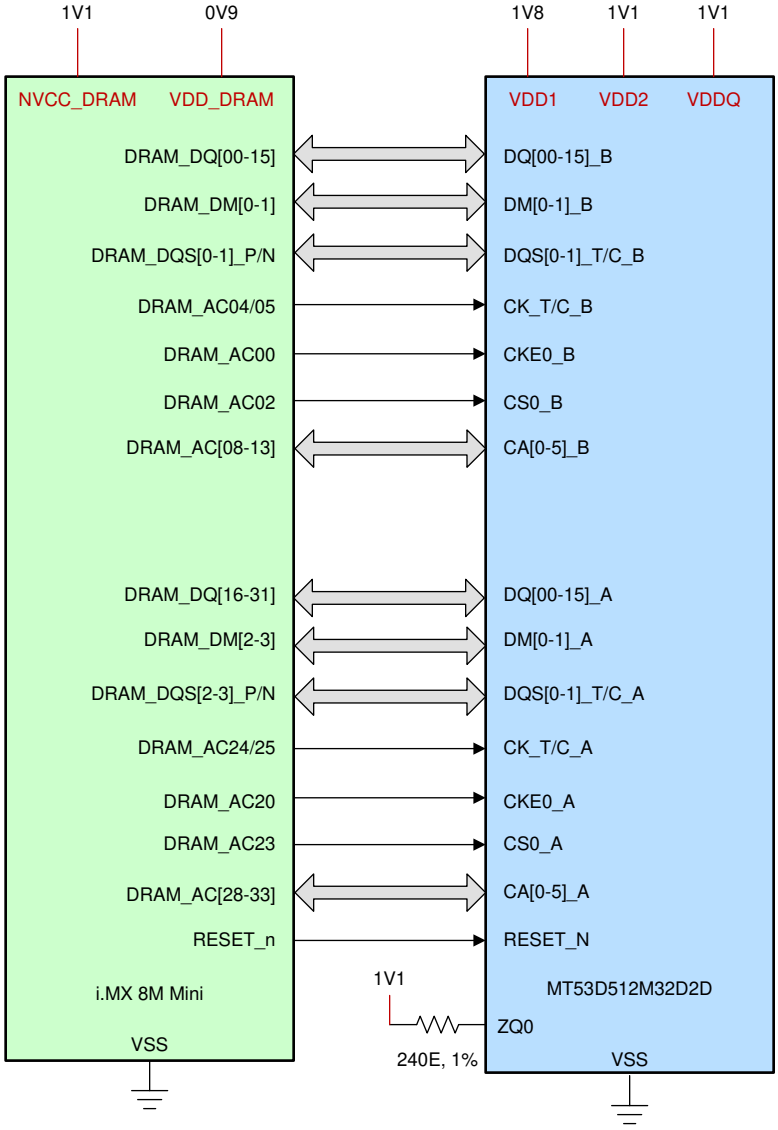
This project makes use of i.MX 8MM processor's four different external memory interfaces using LPDDR4 SDRAM (2GB), 256Mb QSPI NOR-Flash (32MB), 16GB eMMC 5.1, and SD v3.0 (connector on base-board).

2.2.2.1 LPDDR4

i.MX 8M Mini has a dedicated DDR memory controller which supports DDR3L, DDR4, and LPDDR4. Memory speeds supported are LPDDR4 up to 1.5GHz, DDR4-2400 and DDR3L-1600. This design is provided with two 2GB x32 LPDDR4 memory. Micron's, MT53D512M32D2DS-053 WT:D is a 16Gb LPDDR4 SDRAM (two die per package), currently used in this design. The memory interface comprises of two channel of 16-bit data signals, along with separate command and address for each die.

DESCRIPTION	MFG.	PART NUMBER
IC, LPDDR4 SDRAM, 2GB, x32bit, 1866MHz, WFBGA-200	Micron	MT53D512M32D2DS-053 WT:D

Figure 2. LPDDR4 Interface



2.2.2.2 Quad SPI NOR Flash

i.MX 8M Mini processor supports Serial NOR Flash interface (QSPI). This project will support one Serial NOR Flash. Micron's, MT25QU256ABA1EW7-0SIT is a Serial NOR Flash Memory with a density 256Mb (32MB) at clock frequency 133MHz and data through-put up to 90MB/s.

DESCRIPTION	MFG.	PART NUMBER
IC, NOR Flash, 32MB, 133MHz, SPI, 1.7-2V, W-PDFN-8	Micron	MT25QU256ABA1EW7-0SIT

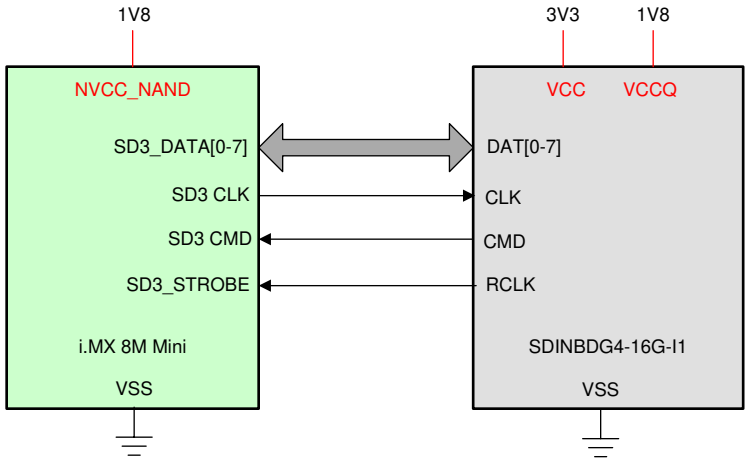
2.2.2.3 eMMC iNAND

For this design an 8GB eMMC 5.1 compliant Memory is included. The interface diagram of eMMC with processor is shown in . The part used here is a from Micron, P/N: MTFC8GAKAJCN- 4M IT. It supports HS400 which is High Speed Mode supporting 400MBps @ 200MHz Dual Data Rate Bus.

For this design an 16GB eMMC 5.1 compliant Memory is included. The interface diagram of eMMC with processor is shown in Figure 3. The part used here is from Western Digital, SDINBDG4-16G-I1. It supports HS400 which is High Speed Mode supporting 400MBps at 200-MHz Dual Data Rate Bus with 8-bit bus width.

DESCRIPTION	MFG.	PART NUMBER
IC, eMMC 16GB iNAND 7250 eMMC 5.1	Western Digital	SDINBDG4-16G-I1

Figure 3. eMMC interface

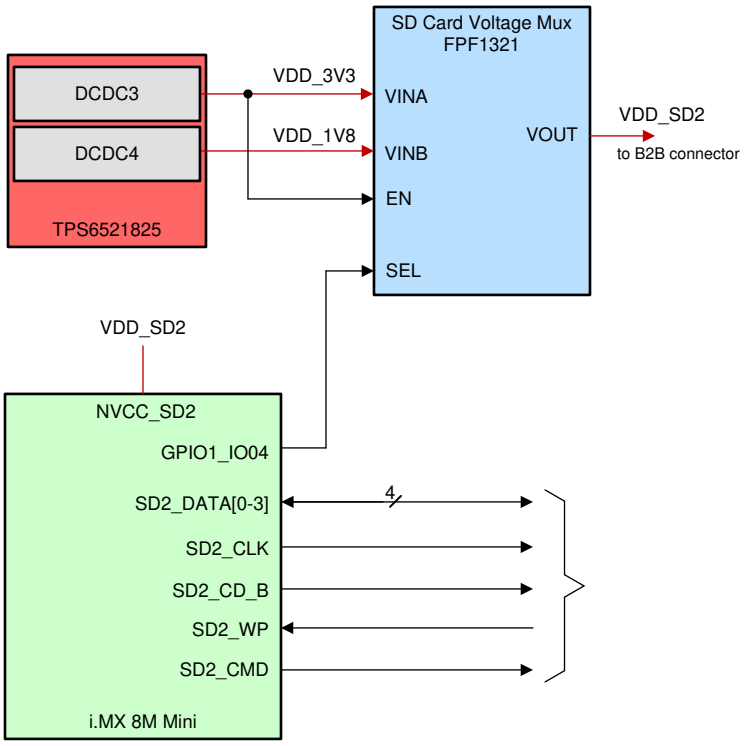


2.2.2.4 Power for SD Card (connector on base-board)

In this design, there is an SD card connector on the base-board but the power supply for the SD card is on the TIDA-050038 SoM board. The power supply to the SD Card is selectable between 1.8 V and 3.3 V using a power multiplexer (mux), and both input voltages to the mux are provided by the TPS6521825 PMIC. The initial voltage applied to the VDD pin of the SD Card connector must always be 3.3 V and may be lowered to 1.8 V after the SD Card confirms the allowed operating voltages. The power circuit for the SD Card connector are shown in Figure 4.

DESCRIPTION	MFG.	PART NUMBER
IC, Power Switch P-Channel 2:1, 6WLCSP	ON Semiconductor	FPF1321UCX

Figure 4. SD Card Power



2.2.3 WiFi + Bluetooth Module

This design makes use of Murata's WiFi + Bluetooth Module, the LBEE5HY1MW device. The interface with the processor is through UART for Bluetooth and SDIO for WLAN (WiFi). The design provides a coaxial connection for connection to the antenna, which is on the 8MMiniLPD4-EVK base-board.

DESCRIPTION	MFG.	PART NUMBER
Module, WiFi-Bluetooth, 802.11a/b/g/n/ac 2.4GHz/5GHz, BLE 5.0, Shielded, Type 1MW	Murata	LBEE5HY1MW-230

2.2.4 High-Density Connectors

The connections between the TIDA-050034 SoM board and 8MMiniLPD4-EVK base-board are pre-defined and there are no deviations possible from the electrical and mechanical specifications.

The interfaces contained on the base-board are as follows:

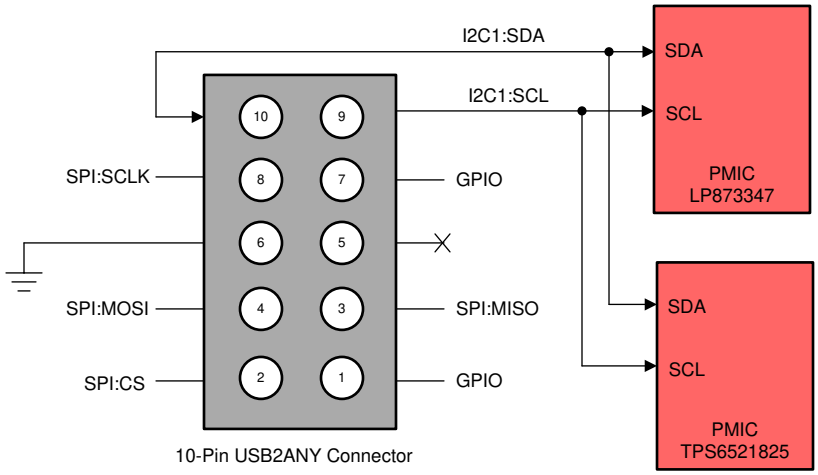
- SD Card connector
- Audio CODEC IC and connectors
- Ethernet PHY and connector
- USB-to-UART IC and connector
- USB Type-C connectors for main power supply and data transmission
- MIPI DSI connector
- MIPI CSI connector
- mini-PCI Express connector
- JTAG header

2.2.5 USB2ANY Header

USB2ANY is TI MCU-based adaptor intended to allow a computer to control an electronic evaluation module (EVM) via a USB connection. In this design, the I^2C interface of USB2ANY is used to externally monitor, control, and/or re-program the internal registers of PMIC. The wiring of the USB2ANY header is shown in Figure 5.

DESCRIPTION	MFG.	PART NUMBER
Connector, Berg strip, 2x5, 2.54mm, 3A, RA, TH	FCI	68021-210HLF

Figure 5. USB2ANY Header Connections to PMIC I^2C pins



2.3 Highlighted Products

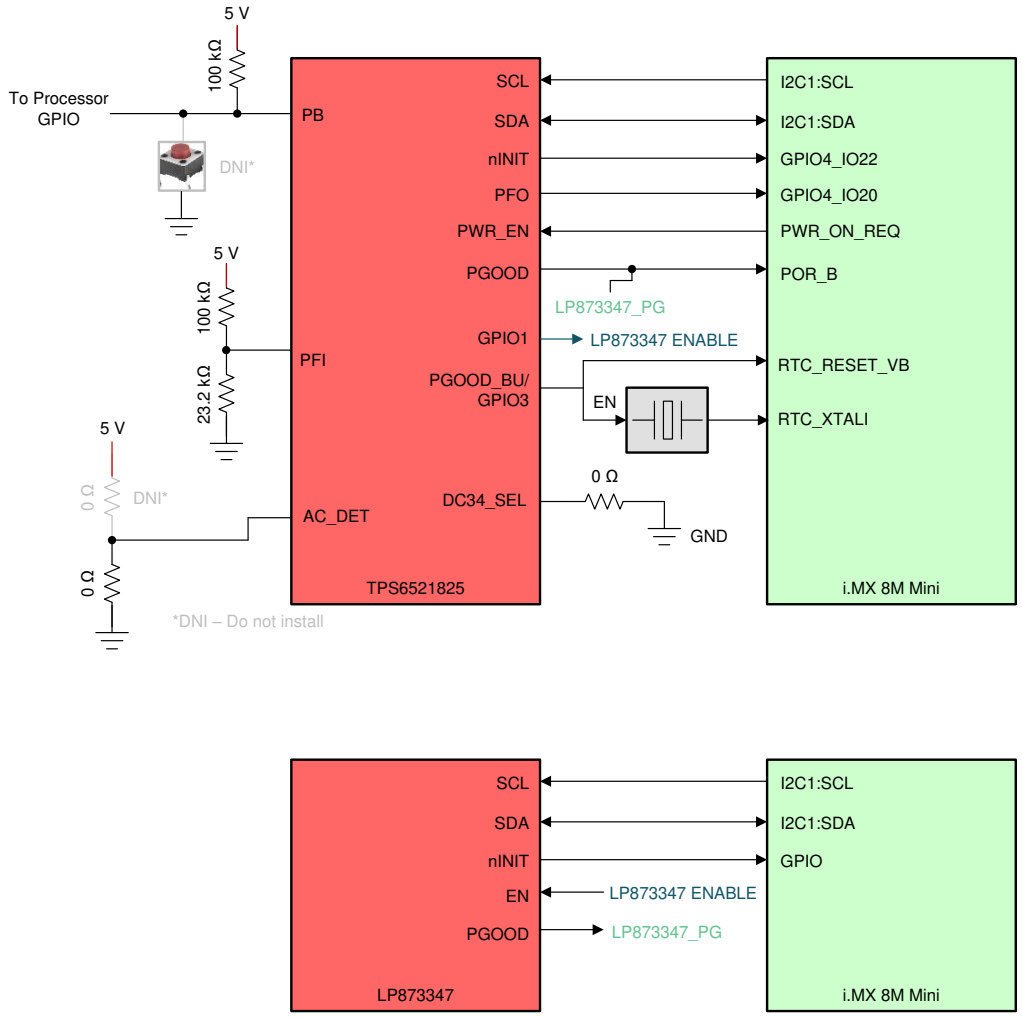
2.3.1 TPS6521825 - Power Management IC

The TPS6521825 device is a Power Management IC (PMIC) specifically designed to support Arm Cortex processors like the i.MX 8M Mini from NXP. The PMIC is a good fit for applications powered from a 5-V supply or a Li-Ion battery. The IC consists of three adjustable step-down (buck) converters, one buck-boost converter, one adjustable LDO and three load switches with two selectable current limit. The PMIC supports undervoltage lockout (UVLO), over-temperature warning and shutdown, separate power-good output for all regulators, programmable power sequencing for all regulators, and an I^2C interface for register reading and writing to the device.

For this project, PMIC powers NXP's i.MX 8M Mini Processor, providing VDD_SNVS (0V8) and NVCC_SNVS (1V8) from DCDC5 and DCDC6 respectively. It also provides VDD_SOC (0V85/0V9) through DCDC1, NVCC_DRAM (1V1) through DCDC2 and voltages such as 3.3V, 1.8V digital, 1V8 Analog and 2V5 are also generated from this PMIC. The voltage 5V0 is send through load switches LS2 and LS3 to peripherals. However, 3V3 for PCIe, MIPI CSI, and MIPI DSI is powered through an external buck converter located on the base-board. The power architecture and estimation can be viewed in Section.5.3 and Section.5.1. The full power architecture of this design is shown in Figure 7.

The control pins of the TPS6521825 PMIC are shown connected to the processor in Figure 6, as well as analog and digital input pins on the PMIC.

Figure 6. TPS6521825 PMIC I/O Wiring to i.MX 8M Mini Processor



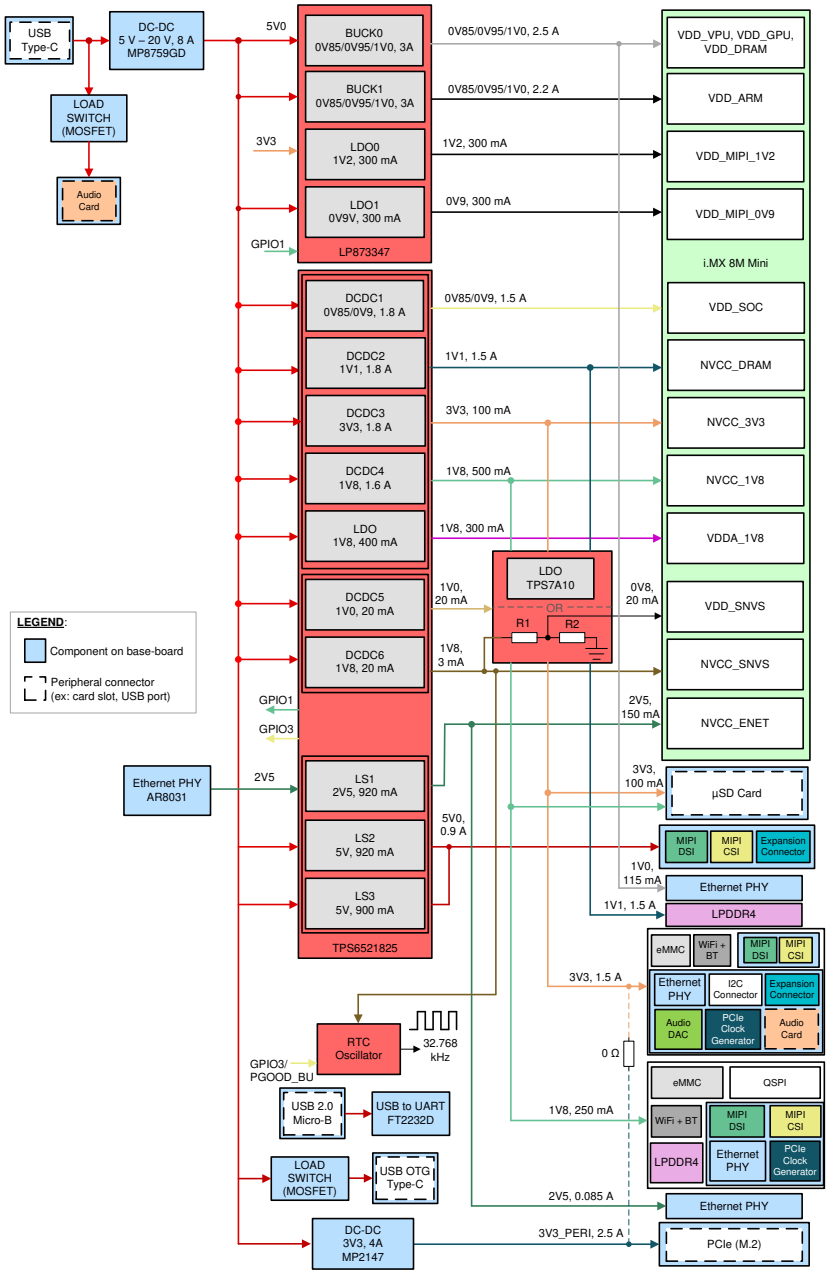
NOTE: PGOOD of both PMICs will be shorted together which creates a “wire-AND” connection due to open drain topology (as in Fig.5) to drive the Power on Reset (POR_B) input pin on the processor. The voltage for I2C operation is 1V8, so all the open drain input-outputs (SDA & SCL) are connected to a 4.7-kΩ pull-up resistor.

2.3.2 LP873347 - Core rail power up to 3 A

Figure 7 shows the full power architecture. For this design, two of the core rails will require up to 3 A of current and two additional LDOs are required for MIPI to meet the power needs of the i.MX 8M Mini processor. LP873347, an OTP variant of LP8733 base part number, is a PMIC that has been programmed specifically to meet the power requirements of this application when paired with the TPS6521825 device. The IC has two step-down converters with both single and dual phase regulators for improved efficiency with higher power output. It also has two linear regulators (LDOs), general purpose digital output signals and I2C interface.

For this project LP873347 will be used to generate 0V85/0V95/1V0 (dynamic voltage/frequency scaling, or DVFS) for VDD_VPU, VDD_GPU and VDD_DRAM with an estimated approximate current output of 2.5 A from BUCK0. The same DVFS voltages are required for VDD_ARM with an estimated current output of 2.2 A from BUCK1. The LDOs will provide 1V2 and 0V9 for VDD_MIPI_1V2 and VDD_MIPI_0V9 respectively. The input voltage to both PMICs is 5 V in this design. The LP873347 (slave PMIC) is enabled by a GPIO of the TPS6521825 (master PMIC), and is disabled through a combination of signals to ensure proper power-up and power-down sequencing for the processor.

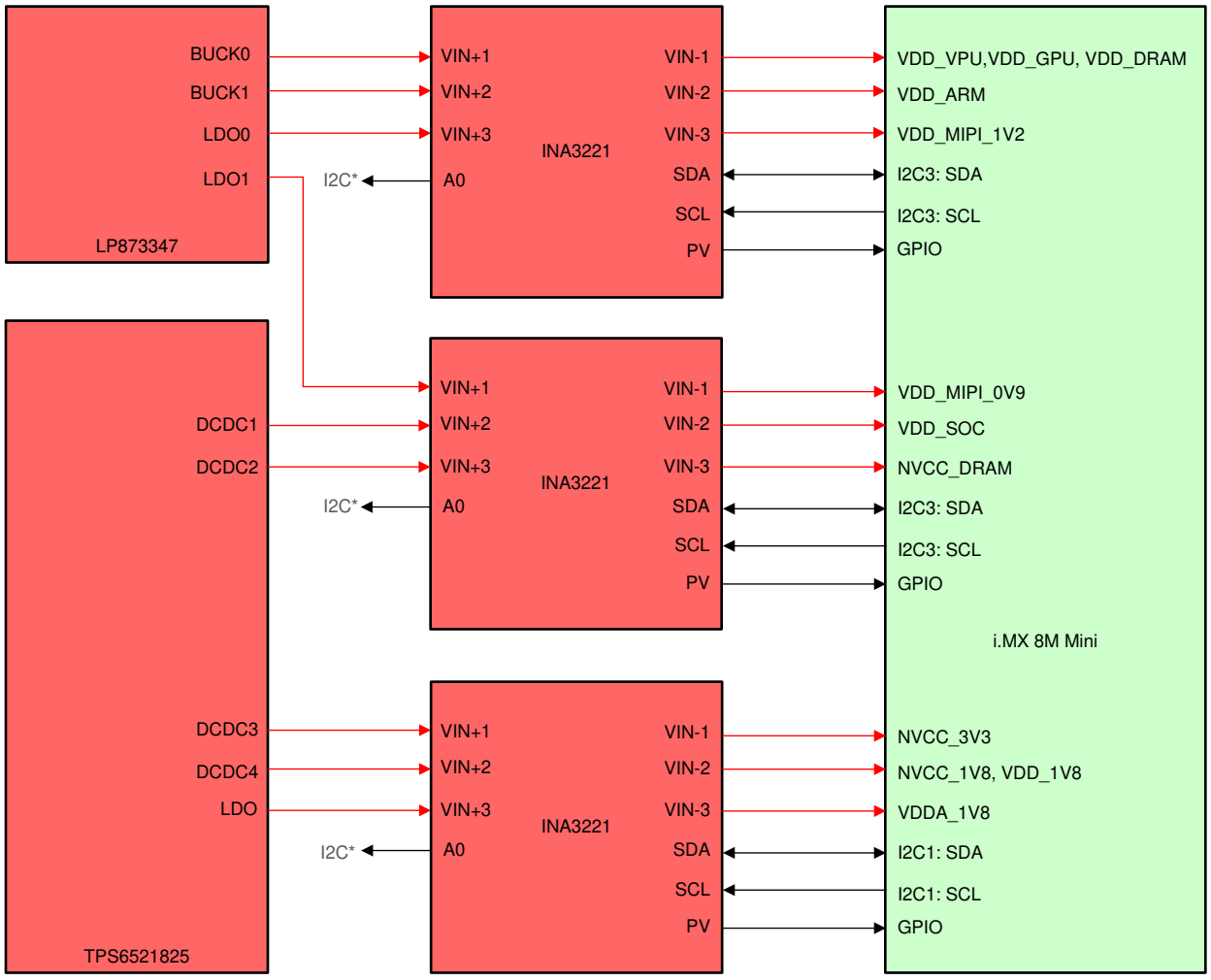
Figure 7. TIDA-050038 Full Power Architecture



2.3.3 INA3221 - Current Monitor

To measure the live current information, a current sense circuit is integrated to the power section of this design. The current sensing is done with the INA3221 device. There are three devices used to monitor all the TPS6521825 and LP873347 PMIC power rails that are sourcing greater than 100-mA of current to the system. The wiring is shown in Figure 8. The address pin A0 of the INA3221 device needs to be terminated according to Table 2.

Figure 8. INA3221 Current Sensor Wiring from PMIC to Processor



*I2C = I2C Slave address is determined by the termination of *A0* pin

Table 2. INA3221 I²C Slave Address Options

7-BIT BINARY ADDRESS	7-BIT HEX ADDRESS	ADDR PIN TERMINATION
1000000b	0x40	GND
1000001b	0x41	V_S
1000010b	0x42	SDA
1000011b	0x43	SCL

2.4 System Design Theory

The full power architecture is the result of carefully estimating the power consumed by ICs on the board and peripherals that can be connected to the board. The ideal power sequencing of the i.MX 8M Mini processor must be known to ensure the power sequencing of the TPS6521825 and LP873347 PMICs is correct, and the mechanisms for resetting the system must be determined. The I²C chain must be drawn in its entirety to ensure there are no I²C address conflicts. The BOOT Mode settings must be mapped to boot the processor using the intended memory storage IC. And finally, designing a SoM board to be compatible with the 8MMiniLPD4-EVK comes with additional size constraints that must be considered. PCB floor planning must be completed to make sure the layout of the board is reasonable. All of this system design theory is taken into consideration in this section.

2.4.1 Size constraints

The original SoM board that is placed on top of the 8MMiniLPD4-EVK is a 2-inch by 2-inch square PCB. The only connection that is added to the PCB is the 10-pin USB2ANY header, which is considered to be outside the 2" by 2" square requirement. All other devices on the PCB (PMIC, WiFi + Bluetooth module) are functionally equivalent to the pre-existing SoM board design and therefore must fit in the same area on the PCB. This includes the INA3221 current monitoring ICs, which are not a feature of the original EVK. For more details on the floor planning, refer to Section 2.4.8.

2.4.2 Power Estimation

The TIDA-050038 SoM board is indirectly powered from the USB Type-C input (5V to 20V) to the base board of the 8MMiniLPD4-EVK. This input is given to a DCDC converter (MP8759GD on base-board) for a constant 5V output, which is the given as the input to the SoM board. This 5-V supply is provided directly to the PMICs. The PMICs will generate voltages for 11 different rails. The load switches 2 and 3 are used to power ICs and USBs with 5.0 V. The estimated current consumption for each rail is listed in Table 3.

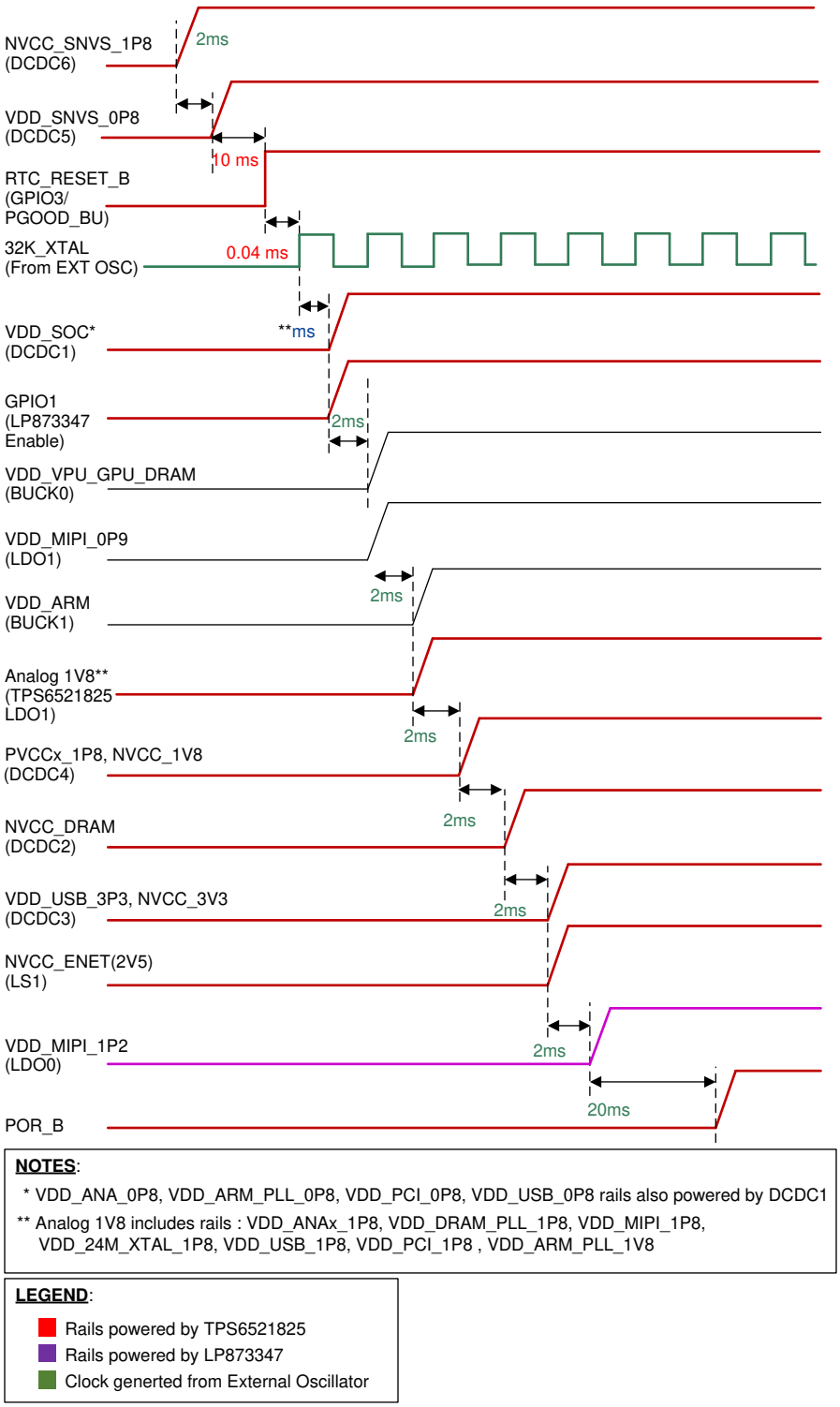
Table 3. System Power Estimation

VOLTAGE (V)	SUPPLY IC, RAIL NAME	SUPPLY CURRENT (mA)	LOAD IC, RAIL NAME	CURRENT (mA)	POWER (mW)
0.85/0.95/1.0	LP873347, BUCK0	3000	iMX8MM VDD_VPU, VDD_GPU, VDD_DRAM	2500	2500
0.85/0.95/1.0	LP873347, BUCK0	3000	iMX8MM VDD_ARM	2200	2200
1.2	LP873347, LDO0	300	iMX8MM VDD_MIPI_1P2	10	12
0.9	LP873347, LDO1	300	iMX8MM VDD_MIPI_0P9	10	9
0.85	TPS6521825, DCDC1	1800	iMX8MM VDD_SOC	1050	893
1.1	TPS6521825, DCDC2	1800	iMX8MM NVCC_DRAM	500	550
			LPDDR4 VDD2/VDDQ	365	402
3.3	TPS6521825, DCDC3	1800	iMX8MM NVCC_3V3	100	330
			eMMC VCC	60	198
			WiFi/BT VIO	200	660
			Eth PHY VDD	65	215
1.8	TPS6521825, DCDC4	1600	i.MX8MM NVCC_1V8	500	900
			LPDDR4 VDD1	3.6	6.5
			QSPI VCC	35	63
			eMMC VCCQ	245	441
			WiFi/BT VBAT_x	800	1440
1.8(Analog)	TPS6521825, LDO1	400	iMX8MM VDD_ANA_1V8	300	540
5	TPS6521825, LS2/3	1820	FTD2232D	30	150
			2x USB2 Ports	1000	5000
0.8	TPS6521825, DCDC5	30	VDD_SNVS_0V8	10	8
1.8	TPS6521825, DCDC6	30	NVCC_SNVS_1V8	10	18
				Total Estimated Power	**17 W**

2.4.3 Power Sequencing

The i.MX 8M Mini processor power sequencing is shown in Figure 9. Before the majority of high current rails are turned on, SNVS power must be available. NVCC_SNVS_1P8 and VDD_SNVS_0P8 are the first rails to be enabled, then the RTC reset (RTC_RESET_B signal) should be asserted high, followed by enabling the RTC clock. The LP873347 is enabled by GPIO1 of the TPS6521825 after VDD_SOC turns on. The LP873347 timing for VDD_VPU_GPU_DRAM, VDD_MIPI_0P9, and VDD_ARM is pre-programmed in the LP873347 device to match this timing requirement and delay VDD_MIPI_1P2 for the appropriate amount of time. The TPS6521825 internally sequences the remaining rails, which are pre-programmed into the EEPROM of the device. After all the rails are enabled and within the acceptable voltage range, POR_B is asserted.

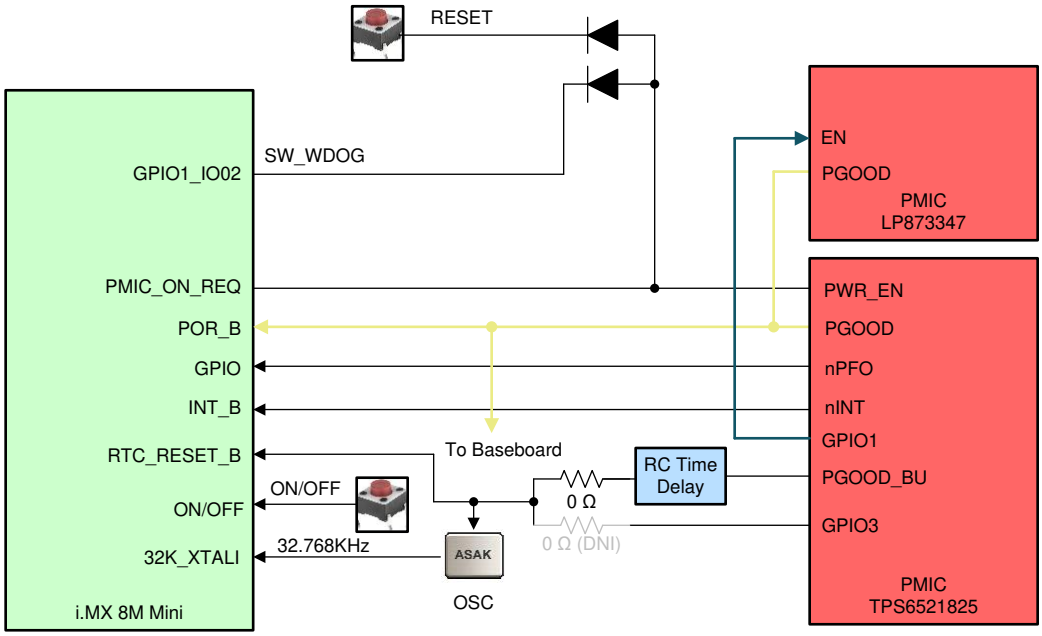
Figure 9. Required Power Sequence for i.MX 8M Mini Processor



2.4.4 Reset Scheme

The reset scheme for this project is shown in Figure 10. There are three RESET inputs to the PMICs. The first is through a RESET switch, which is used as hardware reset, then a Watchdog reset is used and finally a PMIC_ON_REQ from Processor. The PGOOD output of the PMICs are shorted (AND) together to act as the POR_B for the processor. This signal is shared to the base-board.

Figure 10. Reset Scheme

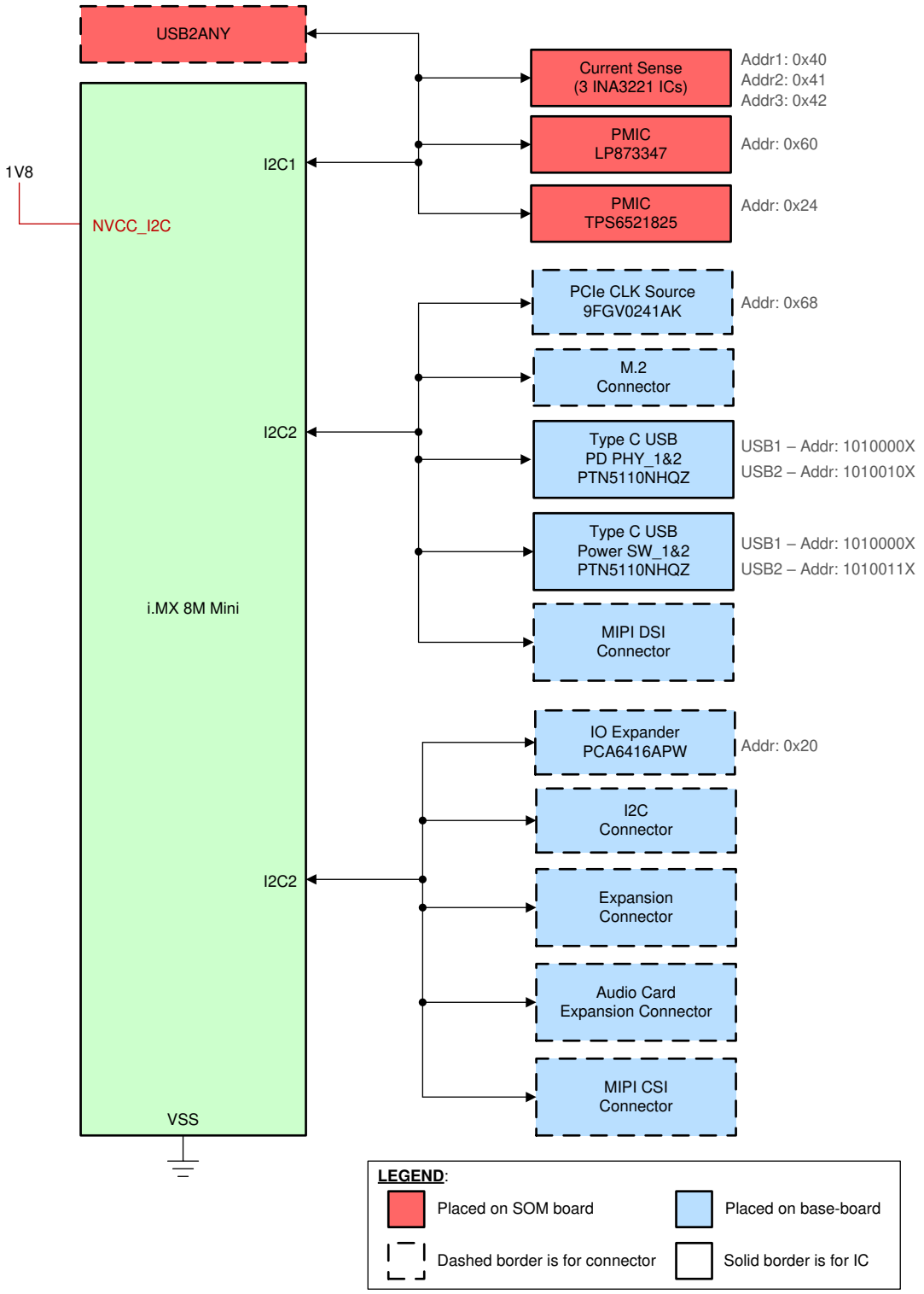


Provide pull-up through 100-kΩ resistor to VSNVS for PGOOD output. Both nPFO and nINT are pulled up to 1V8 using a 2.2-kΩ resistor. The I²C lines are pulled up using a 4.7kΩ resistor to 1V8.

2.4.5 I²C Device Chain

Figure 11 shows the I²C channel mapping from the processor to each slave device.

Figure 11. I²C Device Chain



2.4.6 Clock Scheme

Below is a list matching the required clock frequency to each IC that needs clocking on the SoM board.

- i.MX 8M Mini – 24MHz and 32.768 kHz
- LBEE5HY1MW (Wi-Fi/BT) – 32.768KHz

All other clock sources are generated on the 8MMiniLPD4-EVK base-board.

2.4.7 BOOT Configuration

This design uses two BOOT configuration. BOOT Mode pins controlled by DIP switches 1-2 on SW1101 of the base-board are connected to dedicated BOOT_MODE0 and BOOT_MODE1 input pins of i.MX 8M Mini processor. Along with these, there are 16 additional pins for setting the BOOT configuration (BOOT_CFG0-15) which are dual-purpose pins (also SAI1_RXD0-7, SAI1_TXD0-7). These 16 pins are controlled by DIP switches 5-10 of SW1101 and all 10 DIP switches of SW1102. All of the required BOOT settings for TIDA-050038 are given in Table 4 (SW1101, switches 1-2) and Table 5 (SW1101, switches 5-10; SW1102).

Table 4. SW1101[1-2] BOOT Mode Settings

BOOT_MODE[1..0]	BIT 1 (SW1101[2])	BIT 0 (SW1101[1])
Fuses	0	0
Serial Download	0	1
Internal BOOT	1	0
Reserved	1	1

Table 5. SW1101, SW1102 BOOT Mode Settings for TIDA-050038

BOOT Device	SW1101[1-10], SW1102[1-10] Settings
eMMC/SDHC3	01 10 11 00 01, 00 01 01 01 00
MicroSD/SDHC2	01 10 11 00 10, 00 01 10 10 00
NAND	01 10 00 00 00, 10 00 11 11 00
Download Mode	10 10 xx xx xx, xx xx xx xx x0

2.4.8 PCB Floor Planning

Figure 12 shows the floor planning for the top side of the PCB and Figure 13 shows the floor planning for the bottom side of the PCB.

Figure 12. PCB Floor Planning (top)

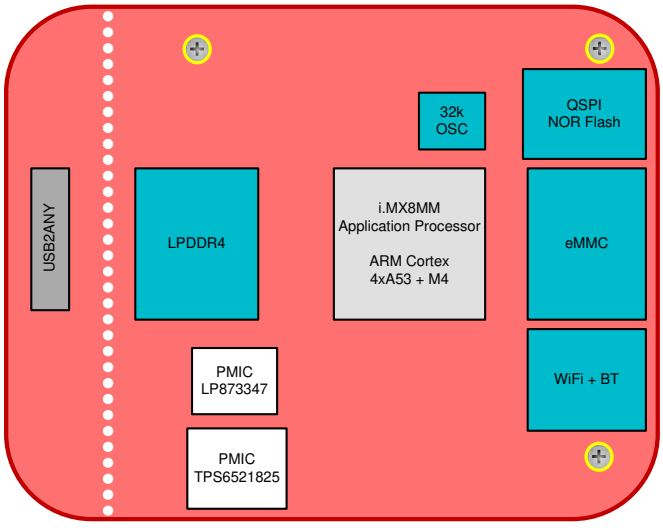
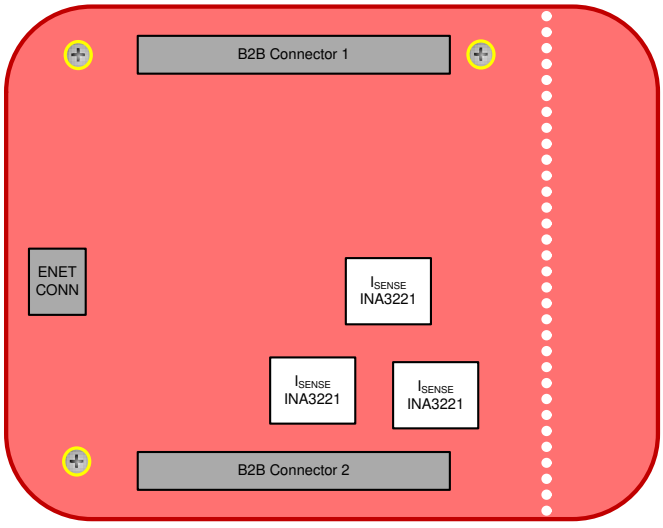


Figure 13. PCB Floor Planning (bottom)



3 Getting Started, Testing Setup, and Test Results

3.1 Getting Started with Hardware and Software

3.1.1 Hardware

This section contains information about the initial set-up of the TIDA-050038 board, power-up options and user interfaces. Figure 14 shows the top side of the fully assembled PCB with labels to help locate connectors or switches on the boards.

Figure 14. Top of TIDA-050038 PCB with Labels

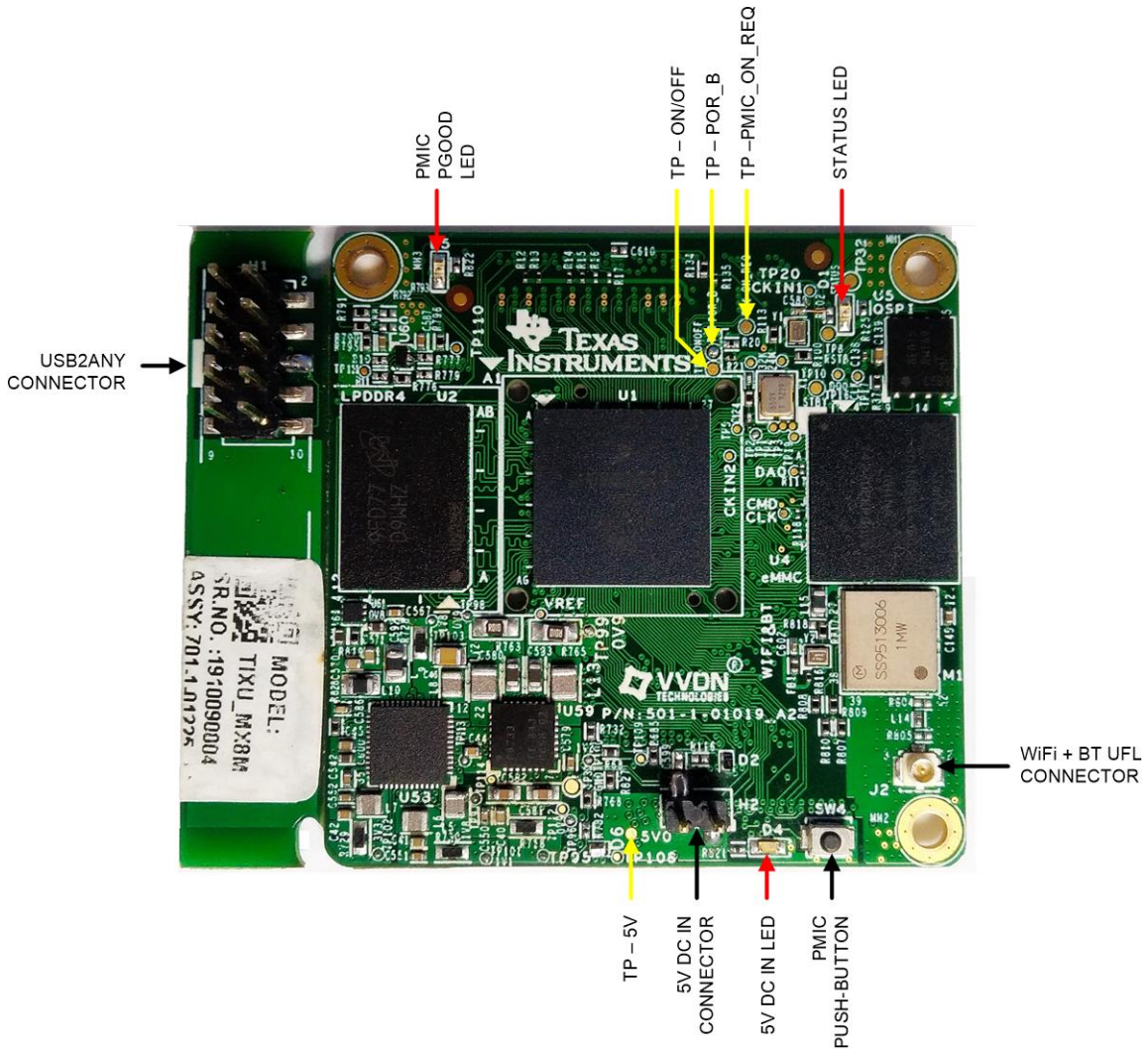
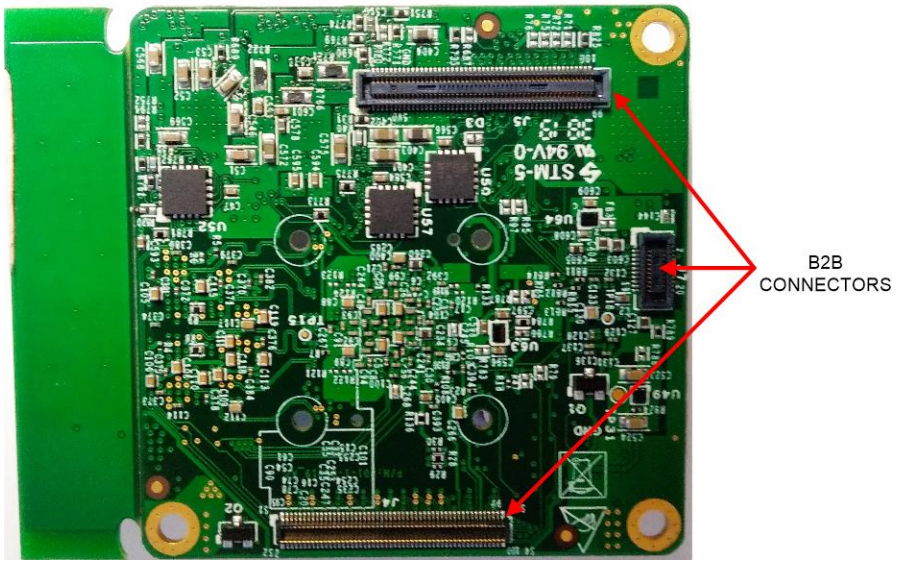


Figure 15 shows the bottom side of the fully assembled PCB with labels.

Figure 15. Bottom of TIDA-050038 PCB with Labels



Below is a list of steps that must be followed to set up the hardware of the system:

1. Place and attach TIDA-050034 SoM board to the 8MMiniLPD4-EVK base-board with screws inserted in the three holes at the corners of the PCB (Figure 16 and Figure 17).
2. Set the BOOT option using SW1101/SW1102 DIP switches (Figure 18).
3. Insert and push-in the µSD card into slot J701 on base-board, if µSD Card is used for BOOT (Figure 19). Push-out to remove µSD card, when necessary.
4. Insert the USB micro-B cable into port J901 on base-board for UART debug in Terminal window (Figure 20). Type-A plug connects to computer USB port.
5. Insert the DC adaptor with USB Type-C plug into J302 connector to supply power (Figure 21). The recommended power supply is included in the 8MMiniLPD4-EVK.
6. Set SW101 in the *ON* position.
7. After BOOT is complete, connect the desired peripherals to the base-board. For example: RJ-45 Ethernet, mini-PCIe (Figure 22), 3.5-mm headphone jack, MIPI camera (CSI), MIPI display (DSI), USB device.

Figure 16. Placing SoM Board on Base-board, Aligning B2B Connectors

Figure 17. Screwing SoM Board to Base-board

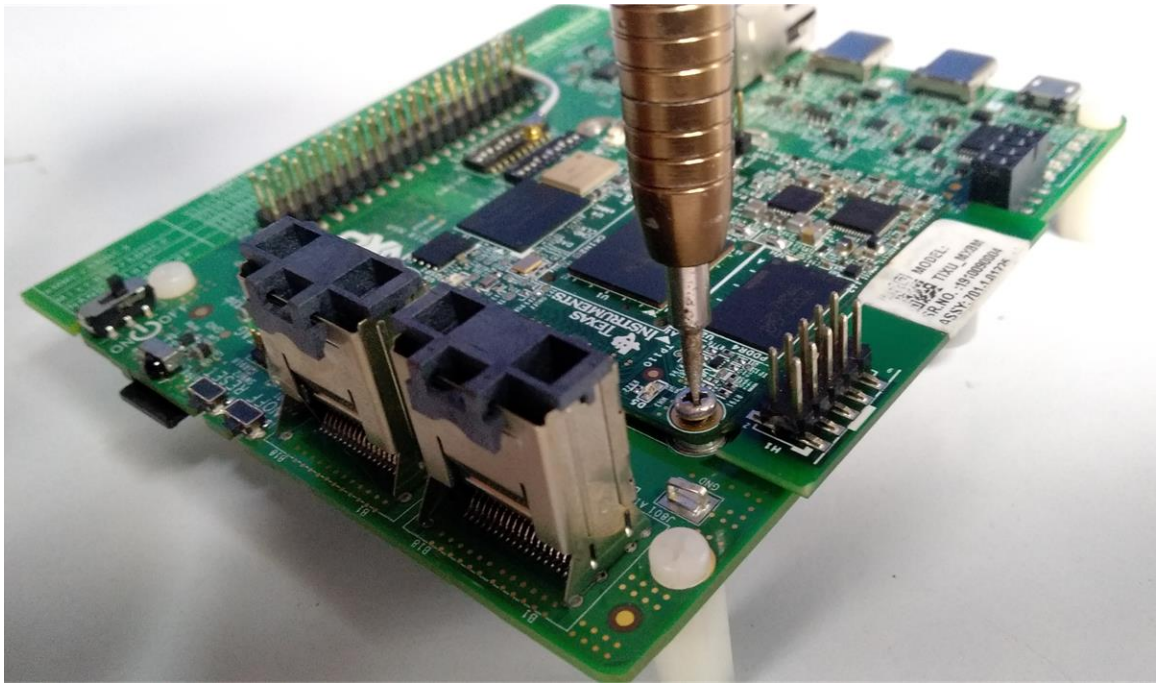


Figure 18. Setting DIP Switches (SW1101, SW1102) for BOOT from SD Card

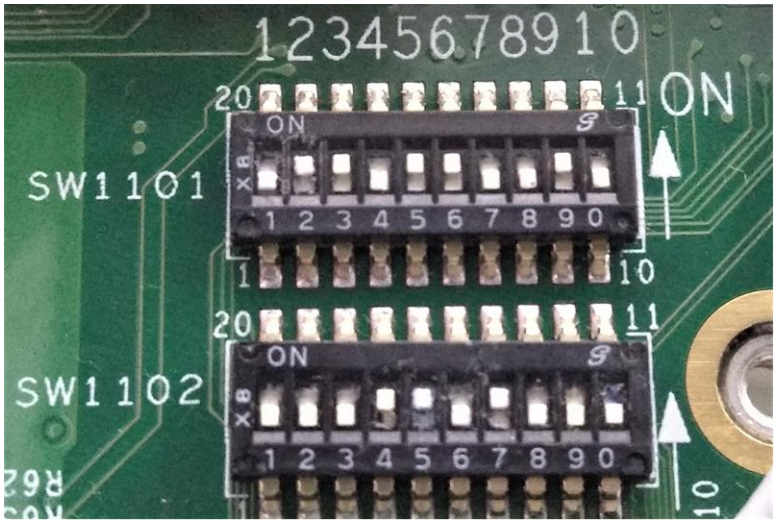


Figure 19. Inserting SD Card into J701 on Base-Board

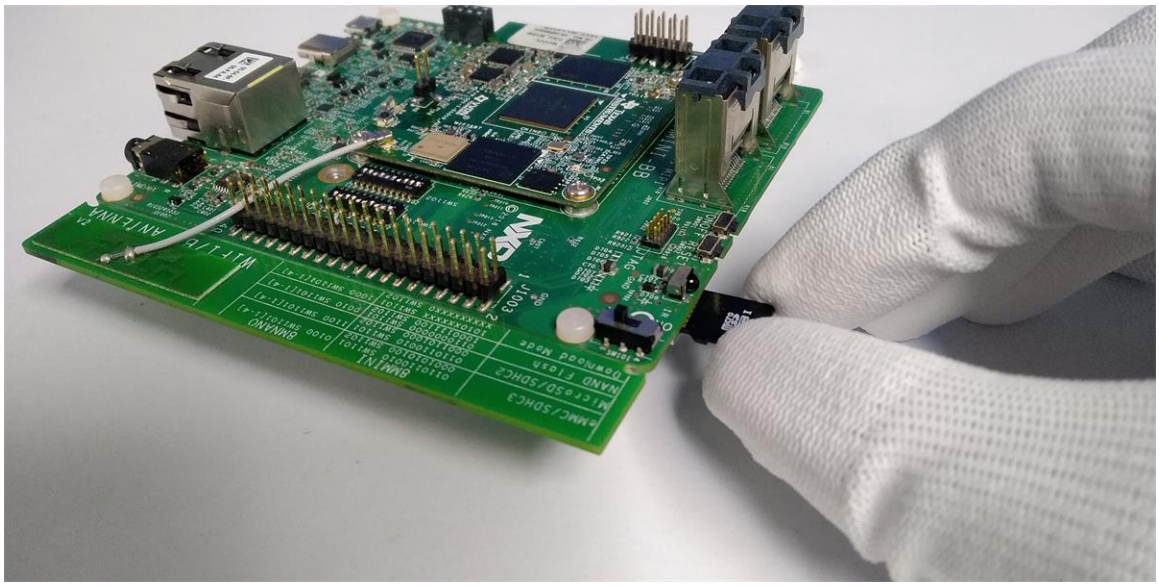
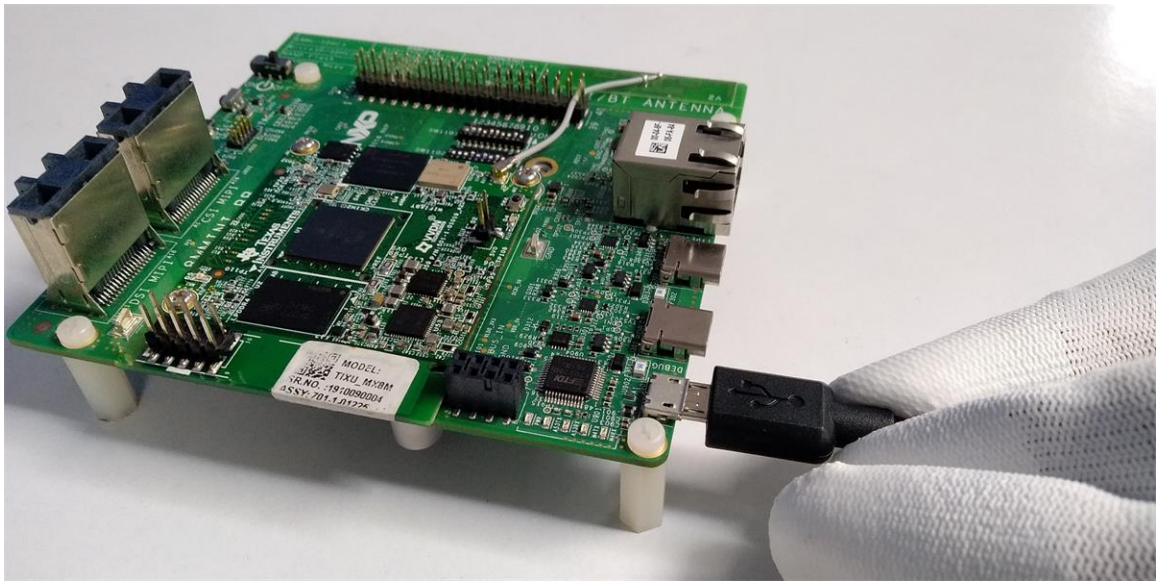


Figure 20. Inserting Micro-B Cable into J901



NOTE: Refer to Section 3.1.2 for the procedure to debug TIDA-050038 through Terminal window.

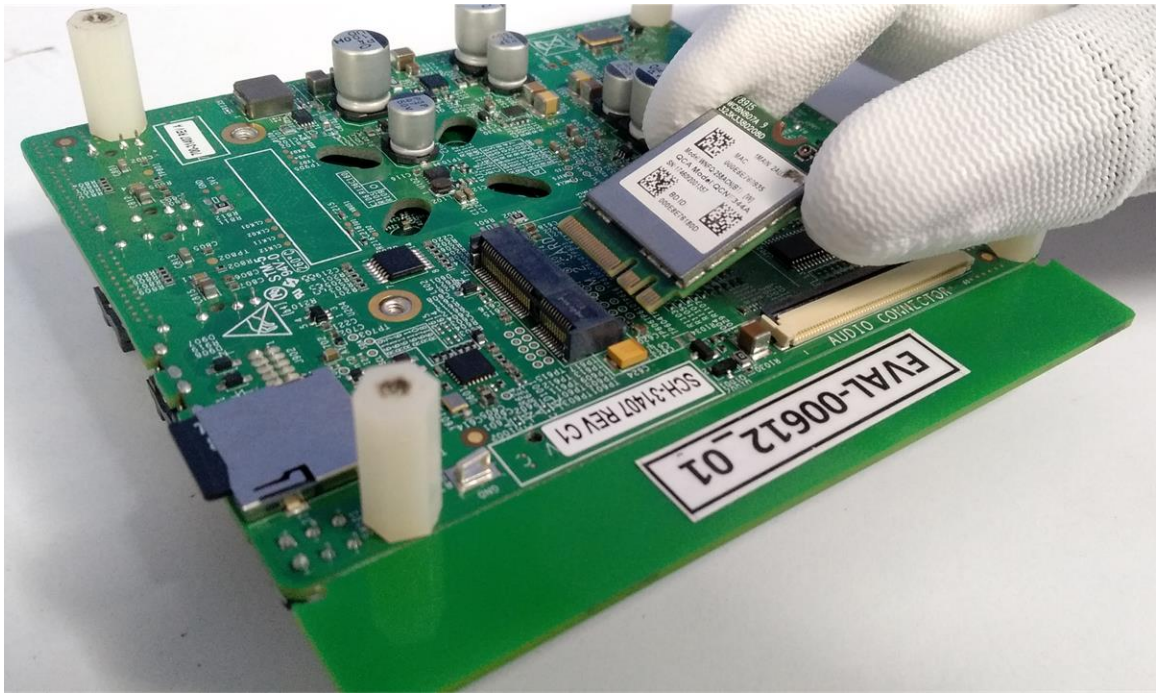
Figure 21. Inserting 5-V DC Adaptor into J302

NOTE: It is always recommended to power-down the system by switching SW101 to the *OFF* position before unplugging the DC adaptor power supply.

CAUTION

Do not connect the power cable to J301.

Figure 22. Inserting mPCIe Card into Bottom of Base-Board



3.1.1.1 On-board LED Information

Table 6 lists the indicator LEDs installed on the TIDA-050038 SoM PCB and provides a short description of their meaning to improve the user experience getting started with the TIDA-050038 reference design.

Table 6. Indicator LEDs

DESIGNATOR	DESCRIPTION (IN Figure 14)	MEANING
D1	PMIC PGOOD LED	ON: Both PMICs set PGOOD high (all power rails are in regulation)
		OFF: PMICs powered-down or fault occurred on one or more power rails
D4	5V DC Input LED	ON: 5 V applied to SoM board from base board
		OFF: SoM board is not receiving power
D5	Status LED	ON: Boot completed
		OFF: Boot not completed

3.1.2 Software

The primary boot source used for testing TIDA-050038 was the SD card. The primary method for testing was using a pre-built binary image to prepare SD card. The purpose of this section is getting started using the software and assumes the software used is already written onto an SD Card that is inserted into the correct slot on the PCB and the BOOT switches are set properly.

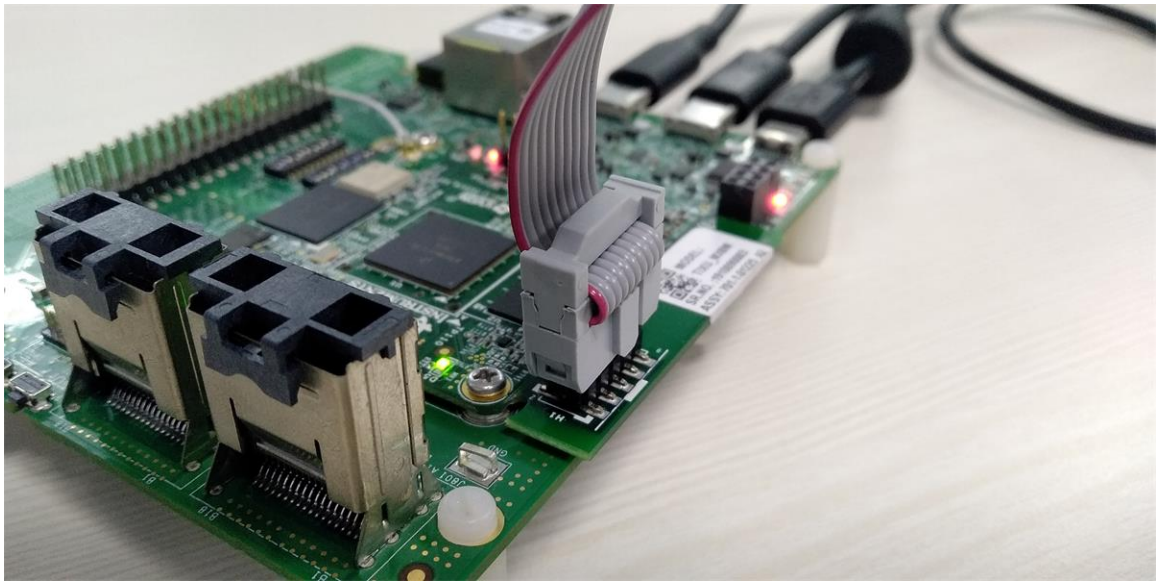
The software used for testing is an embedded Linux Yocto build with drivers written for all of the TI ICs and patches to modify the original SDK written for the NXP i.MX 8MM processor. Building and installing the image requires a laptop running Ubuntu 16.04 (or later), 120 GB HDD, a fully-assembled TIDA-050038 board, a µSD card, a micro-USB cable, and a USB Type-C DC power supply. The procedure for building and installing the software image is outside the scope of this document.

3.1.2.1 Booting of TIDA-050038

Insert the SD card into the SD card slot provided on the base-board and set the boot switches to boot from SD card. If executables are not found in the configured boot source, then the software is automatically fetched from the SD card.

Connect micro-B side of a USB cable to debug port of the board and Type-A side to a host PC. The connections on the board at this step will look like Figure 23 with all USB ports connected, including USB2ANY 10-pin header.

Figure 23. Board Connections for BOOT with All USB Ports Connected



Use TeraTerm or Putty to open a Terminal and get the debug log from the device node if the host PC is running Windows. Change port number according to the COMxx port found in Device Manager for the FTDI chip. Note that two (2) COMxx ports will be available even though only one USB cable is connected between the PC and the TIDA-050038 board.

For example, when I am testing this board I can select either **COM7** or **COM8** port with a baud rate of **115200** and leave the other **Putty** settings as the default option.

If the debug prints are coming when the board is powered on, then that interface is working. When prompted to logon, enter *root'* and press the **Enter** key.

```
timx8m login: root
root@timx8m:~#
```

At the time of writing, the latest software/firmware version for TIDA-050038 is 2.0.1_1, which can be verified using a simple Linux command.

```
root@timx8m:~# fw-version
firmware version : 2.0.1_1
```

There are many other Linux commands that are useful for testing the power supplies and consumption of TIDA-050038, and the next section will provide some examples.

3.1.2.2 Example Linux Commands for Testing TIDA-050038

To figure out which I^2C devices are on the bus, where "0" means I am looking for I^2C devices on channel 0 (because the TPS6521825 should be here at 0x24 and the LP873347 should be at 0x60):

```
root@timx8m:~# i2cdetect -y -r 0
     0   1   2  3   4   5   6   7   8   9   a   b   c   d  e   f
00:             --  --  --  UU  --  --  --  --  --  --  --  --  --
10: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
20: --  --  --  --  UU  --  --  --  --  --  --  --  --  --  --  --
30: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

```
40: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
50: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
60: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
70: --  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

To test changing the output state of a GPIO, I will change the state of the system status LED (D5) using GPIO number (*-n*) *80* where *"1"* sets (-*s*) the GPIO high and *"0"* sets the GPIO low (which will override the value system status LED until the next time the processor boots):

```
root@timx8m:~# test_gpio -n 80 -s 0
set value at 80
root@timx8m:~# test_gpio -n 80 -s 1
set value at 80
```

To verify dynamic voltage scaling is working for the PMIC with respect to the CPU frequency of the processor, where 1.2 GHz corresponds to LP873347 BUCK1 = 0.85 V while 1.6 GHz corresponds to BUCK1 = 0.95 V:

```
root@timx8m:~# echo userspace > /sys/devices/system/cpu/cpu0/cpufreq/scaling_governor
root@timx8m:~# echo 1200000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
root@timx8m:~# echo 1600000 > /sys/devices/system/cpu/cpu0/cpufreq/scaling_setspeed
```

To run a current sensor application and measure the current on any rail coming out of the LP873347 or TPS6521825 PMIC, where "*3*" in the first prompt is current sensor IC #3 (address 0x42), "*2*" in the second prompt is channel 2, and "*curr1_input*" returns a value 0f 1000 mA that is being used by the VDD_ARM rail:

```
root@timx8m:~# test_currentsensor
Enter current sensor no[1-3]: 3
Enter voltage Level[1-3]: 2
/*****************************************************************************/
/*                              CURRENT SENSOR1                              */
/*           Location of node:/sys/bus/i2c/devices/2-0040/hwmon/h1mon1/      */
/*****************************************************************************/
/* ========================================================================= */
/*                             VDD_ARM                                       */
/* ========================================================================= */
      curr1_crit :  16380 mA
curr1_crit_alarm :  0
     curr1_input :  1000 mA
       curr1_max :  16380 mA
 curr1_max_alarm :  0
       in1_input :  950 mV
/*****************************************************************************/
```

There are many other useful functions that are written specifically for testing TIDA-050038 in addition to the thousands of pre-defined Linux commands that can be included as part of the Yocto build for iMX. The most useful one for stress testing the processor and increase load current to test the PMIC is stress-ng. More information on Linux commands can be found in the Ubuntu manual.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-050038.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050038.

4.3 CAD Files

To download the CAD files, see the design files at TIDA-050038.

4.4 Gerber Files

To download the Gerber files, see the design files at TIDA-050038.

4.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050038.

5 Software Files

To download the software files, see the design files at TIDA-050038.

6 Related Documentation

1. *TPS6521825 Power Management IC (PMIC) for NXP i.MX 8M Mini* data sheet
2. *LP873347 Technical Reference Manual*
3. *LP8733xx Dual High-Current Buck Converter and Dual Linear Regulator* data sheet
4. *Powering the NXP i.MX 8M Mini with the with the TPS6521825 and LP873347 PMICs*
5. *8MMINILPD4-EVK: Quick Start Guide for i.MX 8M Mini EVK*
6. *Ubuntu Manpage Repository*
7. *Yocto Project* home page

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2019) to A Revision	Page
• Added link to download software files	26

Appendix A Processor Pin Mapping

A.1 i.MX 8M Mini Pin Mapping

The following table is a detailed list of the mapping for each pin on the i.MX 8M Mini processor.

Table 7. i.MX 8M Mini Pin Mapping

Pin	Peripheral	Signal	Route to	Power group	Direction
F4	DRAM	dram_ac, 00	DRAM_AC00	NVCC_DRAM (0V)	Output
F5	DRAM	dram_ac, 01	DRAM_AC01	NVCC_DRAM (0V)	Output
K4	DRAM	dram_ac, 02	DRAM_AC02	NVCC_DRAM (0V)	Output
J4	DRAM	dram_ac, 03	DRAM_AC03	NVCC_DRAM (0V)	Output
L2	DRAM	dram_ac, 04	DRAM_AC04	NVCC_DRAM (0V)	Output
L1	DRAM	dram_ac, 05	DRAM_AC05	NVCC_DRAM (0V)	Output
J6	DRAM	dram_ac, 08	DRAM_AC08	NVCC_DRAM (0V)	Output
K6	DRAM	dram_ac, 09	DRAM_AC09	NVCC_DRAM (0V)	Output
E4	DRAM	dram_ac, 10	DRAM_AC10	NVCC_DRAM (0V)	Output
D5	DRAM	dram_ac, 11	DRAM_AC11	NVCC_DRAM (0V)	Output
N4	DRAM	dram_ac, 12	DRAM_AC12	NVCC_DRAM (0V)	Output
N5	DRAM	dram_ac, 13	DRAM_AC13	NVCC_DRAM (0V)	Output
N2	DRAM	dram_ac, 19	DRAM_AC19	NVCC_DRAM (0V)	Output
AB4	DRAM	dram_ac, 20	DRAM_AC20	NVCC_DRAM (0V)	Output
AB5	DRAM	dram_ac, 21	DRAM_AC21	NVCC_DRAM (0V)	Output
W4	DRAM	dram_ac, 22	DRAM_AC22	NVCC_DRAM (0V)	Output
V4	DRAM	dram_ac, 23	DRAM_AC23	NVCC_DRAM (0V)	Output
U2	DRAM	dram_ac, 24	DRAM_AC24	NVCC_DRAM (0V)	Output
U1	DRAM	dram_ac, 25	DRAM_AC25	NVCC_DRAM (0V)	Output
W6	DRAM	dram_ac, 28	DRAM_AC28	NVCC_DRAM (0V)	Output
V6	DRAM	dram_ac, 29	DRAM_AC29	NVCC_DRAM (0V)	Output
AC4	DRAM	dram_ac, 30	DRAM_AC30	NVCC_DRAM (0V)	Output
AD5	DRAM	dram_ac, 31	DRAM_AC31	NVCC_DRAM (0V)	Output
R4	DRAM	dram_ac, 32	DRAM_AC32	NVCC_DRAM (0V)	Output
R5	DRAM	dram_ac, 33	DRAM_AC33	NVCC_DRAM (0V)	Output
A4	DRAM	dram_dm, 0	DRAM_DM0	NVCC_DRAM (0V)	Output
F1	DRAM	dram_dm, 1	DRAM_DM1	NVCC_DRAM (0V)	Output
AB1	DRAM	dram_dm, 2	DRAM_DM2	NVCC_DRAM (0V)	Output
AG4	DRAM	dram_dm, 3	DRAM_DM3	NVCC_DRAM (0V)	Output
A5	DRAM	dram_dq, 00	DRAM_DQ00	NVCC_DRAM (0V)	Input/Output
B5	DRAM	dram_dq, 01	DRAM_DQ01	NVCC_DRAM (0V)	Input/Output
D2	DRAM	dram_dq, 02	DRAM_DQ02	NVCC_DRAM (0V)	Input/Output
D1	DRAM	dram_dq, 03	DRAM_DQ03	NVCC_DRAM (0V)	Input/Output
C1	DRAM	dram_dq, 04	DRAM_DQ04	NVCC_DRAM (0V)	Input/Output
B1	DRAM	dram_dq, 05	DRAM_DQ05	NVCC_DRAM (0V)	Input/Output
A3	DRAM	dram_dq, 06	DRAM_DQ06	NVCC_DRAM (0V)	Input/Output
B4	DRAM	dram_dq, 07	DRAM_DQ07	NVCC_DRAM (0V)	Input/Output
F2	DRAM	dram_dq, 08	DRAM_DQ08	NVCC_DRAM (0V)	Input/Output
G2	DRAM	dram_dq, 09	DRAM_DQ09	NVCC_DRAM (0V)	Input/Output
J1	DRAM	dram_dq, 10	DRAM_DQ10	NVCC_DRAM (0V)	Input/Output
J2	DRAM	dram_dq, 11	DRAM_DQ11	NVCC_DRAM (0V)	Input/Output

Table 7. i.MX 8M Mini Pin Mapping (continued)

Pin	Peripheral	Signal	Route to	Power group	Direction
K2	DRAM	dram_dq, 12	DRAM_DQ12	NVCC_DRAM (0V)	Input/Output
K1	DRAM	dram_dq, 13	DRAM_DQ13	NVCC_DRAM (0V)	Input/Output
E1	DRAM	dram_dq, 14	DRAM_DQ14	NVCC_DRAM (0V)	Input/Output
E2	DRAM	dram_dq, 15	DRAM_DQ15	NVCC_DRAM (0V)	Input/Output
AB2	DRAM	dram_dq, 16	DRAM_DQ16	NVCC_DRAM (0V)	Input/Output
AA2	DRAM	dram_dq, 17	DRAM_DQ17	NVCC_DRAM (0V)	Input/Output
W1	DRAM	dram_dq, 18	DRAM_DQ18	NVCC_DRAM (0V)	Input/Output
W2	DRAM	dram_dq, 19	DRAM_DQ19	NVCC_DRAM (0V)	Input/Output
V2	DRAM	dram_dq, 20	DRAM_DQ20	NVCC_DRAM (0V)	Input/Output
V1	DRAM	dram_dq, 21	DRAM_DQ21	NVCC_DRAM (0V)	Input/Output
AC1	DRAM	dram_dq, 22	DRAM_DQ22	NVCC_DRAM (0V)	Input/Output
AC2	DRAM	dram_dq, 23	DRAM_DQ23	NVCC_DRAM (0V)	Input/Output
AG5	DRAM	dram_dq, 24	DRAM_DQ24	NVCC_DRAM (0V)	Input/Output
AF5	DRAM	dram_dq, 25	DRAM_DQ25	NVCC_DRAM (0V)	Input/Output
AD2	DRAM	dram_dq, 26	DRAM_DQ26	NVCC_DRAM (0V)	Input/Output
AD1	DRAM	dram_dq, 27	DRAM_DQ27	NVCC_DRAM (0V)	Input/Output
AE1	DRAM	dram_dq, 28	DRAM_DQ28	NVCC_DRAM (0V)	Input/Output
AF1	DRAM	dram_dq, 29	DRAM_DQ29	NVCC_DRAM (0V)	Input/Output
AG3	DRAM	dram_dq, 30	DRAM_DQ30	NVCC_DRAM (0V)	Input/Output
AF4	DRAM	dram_dq, 31	DRAM_DQ31	NVCC_DRAM (0V)	Input/Output
B2	DRAM	dram_dqs0_n	DRAM_DQS0_N	NVCC_DRAM (0V)	Input/Output
A2	DRAM	dram_dqs0_p	DRAM_DQS0_P	NVCC_DRAM (0V)	Input/Output
H1	DRAM	dram_dqs1_n	DRAM_DQS1_N	NVCC_DRAM (0V)	Input/Output
G1	DRAM	dram_dqs1_p	DRAM_DQS1_P	NVCC_DRAM (0V)	Input/Output
Y1	DRAM	dram_dqs2_n	DRAM_DQS2_N	NVCC_DRAM (0V)	Input/Output
AA1	DRAM	dram_dqs2_p	DRAM_DQS2_P	NVCC_DRAM (0V)	Input/Output
AF2	DRAM	dram_dqs3_n	DRAM_DQS3_N	NVCC_DRAM (0V)	Input/Output
AG2	DRAM	dram_dqs3_p	DRAM_DQS3_P	NVCC_DRAM (0V)	Input/Output
R1	DRAM	dram_reset_n	DRAM_RESET_N	NVCC_DRAM (0V)	Output
P1	DRAM	dram_vref	DRAM_VREF	NVCC_DRAM (0V)	Input
P2	DRAM	dram_zn	DRAM_ZN	NVCC_DRAM (0V)	Input
N22	RAWNAND	rawnand_ale	NAND_ALE	NVCC_NAND (0V)	Output
N24	RAWNAND	rawnand_ce0_b	NAND_CE0_B	NVCC_NAND (0V)	Output
P27	RAWNAND	rawnand_ce1_b	NAND_CE1_B	NVCC_NAND (0V)	Output
M27	RAWNAND	rawnand_ce2_b	NAND_CE2_B	NVCC_NAND (0V)	Output
L27	RAWNAND	rawnand_ce3_b	NAND_CE3_B	NVCC_NAND (0V)	Output
K27	RAWNAND	rawnand_cle	NAND_CLE	NVCC_NAND (0V)	Output
P23	RAWNAND	rawnand_data, 00	NAND_DATA00	NVCC_NAND (0V)	Output
K24	RAWNAND	rawnand_data, 01	NAND_DATA01	NVCC_NAND (0V)	Output
K23	RAWNAND	rawnand_data, 02	NAND_DATA02	NVCC_NAND (0V)	Output
N23	RAWNAND	rawnand_data, 03	NAND_DATA03	NVCC_NAND (0V)	Output
M26	RAWNAND	rawnand_data, 04	NAND_DATA04	NVCC_NAND (0V)	Output
L26	RAWNAND	rawnand_data, 05	NAND_DATA05	NVCC_NAND (0V)	Output
K26	RAWNAND	rawnand_data, 06	NAND_DATA06	NVCC_NAND (0V)	Output
N26	RAWNAND	rawnand_data, 07	NAND_DATA07	NVCC_NAND (0V)	Output
R22	RAWNAND	rawnand_dqs	NAND_DQS	NVCC_NAND (0V)	Input/Output
N27	RAWNAND	rawnand_re_b	NAND_RE_B	NVCC_NAND (0V)	Output

Table 7. i.MX 8M Mini Pin Mapping (continued)

Pin	Peripheral	Signal	Route to	Power group	Direction
P26	RAWNAND	rawnand_ready_b	NAND_READY_B	NVCC_NAND (0V)	Input/Output
R26	RAWNAND	rawnand_we_b	NAND_WE_B	NVCC_NAND (0V)	Output
R27	RAWNAND	rawnand_wp_b	NAND_WP_B	NVCC_NAND (0V)	Output
AC27	ENET1	enet_mdc	ENET_MDC	NVCC_ENET (0V)	Output
AB27	ENET1	enet_mdio	ENET_MDIO	NVCC_ENET (0V)	Input/Output
AF24	ENET1	enet_rgmii_tx_ctl	ENET_TX_CTL	NVCC_ENET (0V)	Output
AG24	ENET1	enet_rgmii_txc	ENET_TXC	NVCC_ENET (0V)	Output
AG26	ENET1	enet_rgmii_td, 0	ENET_TD0	NVCC_ENET (0V)	Output
AF26	ENET1	enet_rgmii_td, 1	ENET_TD1	NVCC_ENET (0V)	Output
AG25	ENET1	enet_rgmii_td, 2	ENET_TD2	NVCC_ENET (0V)	Output
AF25	ENET1	enet_rgmii_td, 3	ENET_TD3	NVCC_ENET (0V)	Output
AE27	ENET1	enet_rgmii_rd, 0	ENET_RD0	NVCC_ENET (0V)	Input
AD27	ENET1	enet_rgmii_rd, 1	ENET_RD1	NVCC_ENET (0V)	Input
AD26	ENET1	enet_rgmii_rd, 2	ENET_RD2	NVCC_ENET (0V)	Input
AC26	ENET1	enet_rgmii_rd, 3	ENET_RD3	NVCC_ENET (0V)	Input
AF27	ENET1	enet_rgmii_rx_ctl	ENET_RX_CTL	NVCC_ENET (0V)	Input
V26	uSDHC1	usdhc_clk	SD1_CLK	NVCC_SD1 (0V)	Output
V27	uSDHC1	usdhc_cmd	SD1_CMD	NVCC_SD1 (0V)	Input/Output
Y27	uSDHC1	usdhc_data, 0	SD1_DATA0	NVCC_SD1 (0V)	Input/Output
Y26	uSDHC1	usdhc_data, 1	SD1_DATA1	NVCC_SD1 (0V)	Input/Output
T27	uSDHC1	usdhc_data, 2	SD1_DATA2	NVCC_SD1 (0V)	Input/Output
T26	uSDHC1	usdhc_data, 3	SD1_DATA3	NVCC_SD1 (0V)	Input/Output
U27	uSDHC1	usdhc_data, 4	SD1_DATA4	NVCC_SD1 (0V)	Input/Output
U26	uSDHC1	usdhc_data, 5	SD1_DATA5	NVCC_SD1 (0V)	Input/Output
W27	uSDHC1	usdhc_data, 6	SD1_DATA6	NVCC_SD1 (0V)	Input/Output
W26	uSDHC1	usdhc_data, 7	SD1_DATA7	NVCC_SD1 (0V)	Input/Output
R23	uSDHC1	usdhc_reset_b	SD1_RESET_B	NVCC_SD1 (0V)	Output
R24	uSDHC1	usdhc_strobe	SD1_STROBE	NVCC_SD1 (0V)	Output
AA26	uSDHC2	usdhc_cd_b	SD2_CD_B	NVCC_SD2 (0V)	Input
W23	uSDHC2	usdhc_clk	SD2_CLK	NVCC_SD2 (0V)	Output
W24	uSDHC2	usdhc_cmd	SD2_CMD	NVCC_SD2 (0V)	Input/Output
AB23	uSDHC2	usdhc_data, 0	SD2_DATA0	NVCC_SD2 (0V)	Input/Output
AB24	uSDHC2	usdhc_data, 1	SD2_DATA1	NVCC_SD2 (0V)	Input/Output
V24	uSDHC2	usdhc_data, 2	SD2_DATA2	NVCC_SD2 (0V)	Input/Output
V23	uSDHC2	usdhc_data, 3	SD2_DATA3	NVCC_SD2 (0V)	Input/Output
AA27	uSDHC2	usdhc_wp	SD2_WP	NVCC_SD2 (0V)	Input
E14	UART1	uart_rx	UART1_RXD	NVCC_UART (0V)	Input
F13	UART1	uart_tx	UART1_TXD	NVCC_UART (0V)	Output
F15	UART2	uart_rx	UART2_RXD	NVCC_UART (0V)	Input
E15	UART2	uart_tx	UART2_TXD	NVCC_UART (0V)	Output
E18	UART3	uart_rx	UART3_RXD	NVCC_UART (0V)	Input
D18	UART3	uart_tx	UART3_TXD	NVCC_UART (0V)	Output
F19	UART4	uart_rx	UART4_RXD	NVCC_UART (0V)	Input
F18	UART4	uart_tx	UART4_TXD	NVCC_UART (0V)	Output
E9	I2C1	i2c_scl	I2C1_SCL	NVCC_I2C (0V)	Input/Output
F9	I2C1	i2c_sda	I2C1_SDA	NVCC_I2C (0V)	Input/Output
D10	I2C2	i2c_scl	I2C2_SCL	NVCC_I2C (0V)	Input/Output

Table 7. i.MX 8M Mini Pin Mapping (continued)

Pin	Peripheral	Signal	Route to	Power group	Direction
D9	I2C2	i2c_sda	I2C2_SDA	NVCC_I2C (0V)	Input/Output
E10	I2C3	i2c_scl	I2C3_SCL	NVCC_I2C (0V)	Input/Output
F10	I2C3	i2c_sda	I2C3_SDA	NVCC_I2C (0V)	Input/Output
AD15	SAI5	sai_mclk	SAI5_MCLK	NVCC_SAI5 (0V)	Output
AB15	SAI5	sai_rx_sync	SAI5_RXFS	NVCC_SAI5 (0V)	Input/Output
AC15	SAI5	sai_rx_bclk	SAI5_RXC	NVCC_SAI5 (0V)	Output
AD18	SAI5	sai_rx_data, 0	SAI5_RXD0	NVCC_SAI5 (0V)	Input
AC14	SAI5	sai_rx_data, 1	SAI5_RXD1	NVCC_SAI5 (0V)	Input
AD13	SAI5	sai_rx_data, 2	SAI5_RXD2	NVCC_SAI5 (0V)	Input
AC13	SAI5	sai_rx_data, 3	SAI5_RXD3	NVCC_SAI5 (0V)	Input
AD6	SAI3	sai_mclk	SAI3_MCLK	NVCC_SAI3 (0V)	Output
AC6	SAI3	sai_tx_data, 1	SAI3_TXFS	NVCC_SAI3 (0V)	Output
AG6	SAI3	sai_tx_bclk	SAI3_TXC	NVCC_SAI3 (0V)	Output
AF6	SAI3	sai_tx_data, 0	SAI3_TXD	NVCC_SAI3 (0V)	Output
AG8	SAI3	sai_rx_data, 1	SAI3_RXFS	NVCC_SAI3 (0V)	Input
AG7	SAI3	sai_rx_bclk	SAI3_RXC	NVCC_SAI3 (0V)	Output
AF7	SAI3	sai_rx_data, 0	SAI3_RXD	NVCC_SAI3 (0V)	Input
AF8	SPDIF1	spdif_ext_clk	SPDIF_EXT_CLK	NVCC_SAI3 (0V)	Input
AG9	SPDIF1	spdif_in	SPDIF_RX	NVCC_SAI3 (0V)	Input
AF9	SPDIF1	spdif_out	SPDIF_TX	NVCC_SAI3 (0V)	Output
AF19	SAI1	sai_rx_data, 7	SAI1_RXD7	NVCC_SAI1 (0V)	Input
AG19	SAI1	sai_rx_data, 6	SAI1_RXD6	NVCC_SAI1 (0V)	Input
AF18	SAI1	sai_rx_data, 5	SAI1_RXD5	NVCC_SAI1 (0V)	Input
AG18	SAI1	sai_rx_data, 4	SAI1_RXD4	NVCC_SAI1 (0V)	Input
AB18	SAI1	sai_mclk	SAI1_MCLK	NVCC_SAI1 (0V)	Output
AF16	SAI1	sai_rx_bclk	SAI1_RXC	NVCC_SAI1 (0V)	Output
AG15	SAI1	sai_rx_data, 0	SAI1_RXD0	NVCC_SAI1 (0V)	Input
AF15	SAI1	sai_rx_data, 1	SAI1_RXD1	NVCC_SAI1 (0V)	Input
AG17	SAI1	sai_rx_data, 2	SAI1_RXD2	NVCC_SAI1 (0V)	Input
AF17	SAI1	sai_rx_data, 3	SAI1_RXD3	NVCC_SAI1 (0V)	Input
AG16	SAI1	sai_rx_sync	SAI1_RXFS	NVCC_SAI1 (0V)	Input/Output
AG20	SAI1	sai_tx_data, 0	SAI1_TXD0	NVCC_SAI1 (0V)	Output
AF20	SAI1	sai_tx_data, 1	SAI1_TXD1	NVCC_SAI1 (0V)	Output
AG21	SAI1	sai_tx_data, 2	SAI1_TXD2	NVCC_SAI1 (0V)	Output
AF21	SAI1	sai_tx_data, 3	SAI1_TXD3	NVCC_SAI1 (0V)	Output
AG22	SAI1	sai_tx_data, 4	SAI1_TXD4	NVCC_SAI1 (0V)	Output
AF22	SAI1	sai_tx_data, 5	SAI1_TXD5	NVCC_SAI1 (0V)	Output
AG23	SAI1	sai_tx_data, 6	SAI1_TXD6	NVCC_SAI1 (0V)	Output
AB19	SAI1	sai_tx_sync	SAI1_TXFS	NVCC_SAI1 (0V)	Input/Output
AC18	SAI1	sai_tx_bclk	SAI1_TXC	NVCC_SAI1 (0V)	Output
AD19	SAI2	sai_mclk	SAI2_MCLK	NVCC_SAI2 (0V)	Output
AD23	SAI2	sai_tx_data, 1	SAI2_TXFS	NVCC_SAI2 (0V)	Output
AD22	SAI2	sai_tx_bclk	SAI2_TXC	NVCC_SAI2 (0V)	Output
AC22	SAI2	sai_tx_data, 0	SAI2_TXD0	NVCC_SAI2 (0V)	Output
AC24	SAI2	sai_rx_data, 0	SAI2_RXD0	NVCC_SAI2 (0V)	Input
AB22	SAI2	sai_rx_bclk	SAI2_RXC	NVCC_SAI2 (0V)	Output
AC19	SAI2	sai_rx_data, 1	SAI2_RXFS	NVCC_SAI2 (0V)	Input

Table 7. i.MX 8M Mini Pin Mapping (continued)

Pin	Peripheral	Signal	Route to	Power group	Direction
A7	ECSPI1	ecspi_miso	ECSPI1_MISO	NVCC_ECSPI (0V)	Input/Output
B7	ECSPI1	ecspi_mosi	ECSPI1_MOSI	NVCC_ECSPI (0V)	Input/Output
D6	ECSPI1	ecspi_sclk	ECSPI1_SCLK	NVCC_ECSPI (0V)	Input/Output
B6	ECSPI1	ecspi_ss, 0	ECSPI1_SS0	NVCC_ECSPI (0V)	Input/Output
A8	ECSPI2	ecspi_miso	ECSPI2_MISO	NVCC_ECSPI (0V)	Input/Output
B8	ECSPI2	ecspi_mosi	ECSPI2_MOSI	NVCC_ECSPI (0V)	Input/Output
E6	ECSPI2	ecspi_sclk	ECSPI2_SCLK	NVCC_ECSPI (0V)	Input/Output
A6	ECSPI2	ecspi_ss, 0	ECSPI2_SS0	NVCC_ECSPI (0V)	Input/Output
AG14	GPIO1	gpio_io, 00	GPIO1_IO00	NVCC_GPIO1 (0V)	Not Specified
AF14	GPIO1	gpio_io, 01	GPIO1_IO01	NVCC_GPIO1 (0V)	Not Specified
AG13	GPIO1	gpio_io, 02	GPIO1_IO02	NVCC_GPIO1 (0V)	Not Specified
AF13	GPIO1	gpio_io, 03	GPIO1_IO03	NVCC_GPIO1 (0V)	Not Specified
AG12	GPIO1	gpio_io, 04	GPIO1_IO04	NVCC_GPIO1 (0V)	Not Specified
AF12	GPIO1	gpio_io, 05	GPIO1_IO05	NVCC_GPIO1 (0V)	Not Specified
AG11	GPIO1	gpio_io, 06	GPIO1_IO06	NVCC_GPIO1 (0V)	Not Specified
AF11	GPIO1	gpio_io, 07	GPIO1_IO07	NVCC_GPIO1 (0V)	Not Specified
AG10	GPIO1	gpio_io, 08	GPIO1_IO08	NVCC_GPIO1 (0V)	Not Specified
AF10	GPIO1	gpio_io, 09	GPIO1_IO09	NVCC_GPIO1 (0V)	Not Specified
AD10	GPIO1	gpio_io, 10	GPIO1_IO10	NVCC_GPIO1 (0V)	Not Specified
AC10	GPIO1	gpio_io, 11	GPIO1_IO11	NVCC_GPIO1 (0V)	Not Specified
AB10	GPIO1	gpio_io, 12	GPIO1_IO12	NVCC_GPIO1 (0V)	Not Specified
AD9	GPIO1	gpio_io, 13	GPIO1_IO13	NVCC_GPIO1 (0V)	Not Specified
AC9	GPIO1	gpio_io, 14	GPIO1_IO14	NVCC_GPIO1 (0V)	Not Specified
AB9	GPIO1	gpio_io, 15	GPIO1_IO15	NVCC_GPIO1 (0V)	Not Specified
A22	USB1	usb_dn	USB1_DN	USB1_VDD33 (0V)	Input
B22	USB1	usb_dp	USB1_DP	USB1_VDD33 (0V)	Input
D22	USB1	usb_id	USB1_ID	USB1_VDD33 (0V)	Input
F22	USB1	usb_vbus	USB1_VBUS	USB1_VDD33 (0V)	Input
A23	USB2	usb_dn	USB2_DN	USB2_VDD33 (0V)	Input
B23	USB2	usb_dp	USB2_DP	USB2_VDD33 (0V)	Input
D23	USB2	usb_id	USB2_ID	USB2_VDD33 (0V)	Input
F23	USB2	usb_vbus	USB2_VBUS	USB2_VDD33 (0V)	Input
A11	MIPI_DSI	mipi_dsi_clk_n	MIPI_DSI_CLK_N	MIPI_DSI_VDDH (0V)	Input/Output
B11	MIPI_DSI	mipi_dsi_clk_p	MIPI_DSI_CLK_P	MIPI_DSI_VDDH (0V)	Input/Output
A9	MIPI_DSI	mipi_dsi_d0_n	MIPI_DSI_D0_N	MIPI_DSI_VDDH (0V)	Input/Output
B9	MIPI_DSI	mipi_dsi_d0_p	MIPI_DSI_D0_P	MIPI_DSI_VDDH (0V)	Input/Output
A10	MIPI_DSI	mipi_dsi_d1_n	MIPI_DSI_D1_N	MIPI_DSI_VDDH (0V)	Input/Output
B10	MIPI_DSI	mipi_dsi_d1_p	MIPI_DSI_D1_P	MIPI_DSI_VDDH (0V)	Input/Output
A12	MIPI_DSI	mipi_dsi_d2_n	MIPI_DSI_D2_N	MIPI_DSI_VDDH (0V)	Input/Output
B12	MIPI_DSI	mipi_dsi_d2_p	MIPI_DSI_D2_P	MIPI_DSI_VDDH (0V)	Input/Output
A13	MIPI_DSI	mipi_dsi_d3_n	MIPI_DSI_D3_N	MIPI_DSI_VDDH (0V)	Input/Output
B13	MIPI_DSI	mipi_dsi_d3_p	MIPI_DSI_D3_P	MIPI_DSI_VDDH (0V)	Input/Output
D15	MIPI_DSI	mipi_dsi_rext	MIPI_DSI_REXT	MIPI_DSI_VDDH (0V)	Output
A21	PCIE1	pcie_ref_pad_clk_n	PCIE_REF_PAD_CLK_N	PCIE_VDDH_CMN (0V)	Input
B21	PCIE1	pcie_ref_pad_clk_p	PCIE_REF_PAD_CLK_P	PCIE_VDDH_CMN (0V)	Input
A19	PCIE1	pcie_rxn_n	PCIE_RXN_N	PCIE_VDDH_CH0 (0V)	Input
B19	PCIE1	pcie_rxn_p	PCIE_RXN_P	PCIE_VDDH_CH0 (0V)	Input

Table 7. i.MX 8M Mini Pin Mapping (continued)

Pin	Peripheral	Signal	Route to	Power group	Direction
A20	PCIE1	pcie_txn_n	PCIE_TXN_N	PCIE_VDDH_CH0 (0V)	Output
B20	PCIE1	pcie_txn_p	PCIE_TXN_P	PCIE_VDDH_CH0 (0V)	Output
D19	PCIE1	pcie_resref	PCIE_RESREF	PCIE_VDDH_CMN (0V)	Input/Output
A16	MIPI_CSI	mipi_csi_clk_n	MIPI_CSI_CLK_N	MIPI_CSI_VDDH (0V)	Input/Output
B16	MIPI_CSI	mipi_csi_clk_p	MIPI_CSI_CLK_P	MIPI_CSI_VDDH (0V)	Input/Output
A14	MIPI_CSI	mipi_csi_d0_n	MIPI_CSI_D0_N	MIPI_CSI_VDDH (0V)	Input/Output
B14	MIPI_CSI	mipi_csi_d0_p	MIPI_CSI_D0_P	MIPI_CSI_VDDH (0V)	Input/Output
A15	MIPI_CSI	mipi_csi_d1_n	MIPI_CSI_D1_N	MIPI_CSI_VDDH (0V)	Input/Output
B15	MIPI_CSI	mipi_csi_d1_p	MIPI_CSI_D1_P	MIPI_CSI_VDDH (0V)	Input/Output
A17	MIPI_CSI	mipi_csi_d2_n	MIPI_CSI_D2_N	MIPI_CSI_VDDH (0V)	Input/Output
B17	MIPI_CSI	mipi_csi_d2_p	MIPI_CSI_D2_P	MIPI_CSI_VDDH (0V)	Input/Output
A18	MIPI_CSI	mipi_csi_d3_n	MIPI_CSI_D3_N	MIPI_CSI_VDDH (0V)	Input/Output
B18	MIPI_CSI	mipi_csi_d3_p	MIPI_CSI_D3_P	MIPI_CSI_VDDH (0V)	Input/Output
A25	SNVS	snvs_onoff	ONOFF	NVCC_SNVS (0V)	Input
A24	SNVS	snvs_pmic_on_req	PMIC_ON_REQ	NVCC_SNVS (0V)	Input
B24	SNVS	snvs_por_b	POR_B	NVCC_SNVS (0V)	Input
A26	SNVS	snvs_rtc	RTC_XTALI	NVCC_SNVS (0V)	Output
F24	SNVS	snvs_rtc_reset_b	RTC_RESET_B	NVCC_SNVS (0V)	Output
E24	CCM	ccm_pmic_stby_req	PMIC_STBY_REQ	NVCC_SNVS (0V)	Output
B27	XTALOSC	xtalosc_xtal_in_24m	XTALI_24M	NVCC_CLK (0V)	Input
D27	CJTAG	jtag_mode	JTAG_MOD	NVCC_JTAG (0V)	Input
F26	CJTAG	jtag_tck	JTAG_TCK	NVCC_JTAG (0V)	Input
E27	CJTAG	jtag_tdi	JTAG_TDI	NVCC_JTAG (0V)	Input
E26	CJTAG	jtag_tdo	JTAG_TDO	NVCC_JTAG (0V)	Output
F27	CJTAG	jtag_tms	JTAG_TMS	NVCC_JTAG (0V)	Input
C27	CJTAG	jtag_trst_b	JTAG_TRST_B	NVCC_JTAG (0V)	Input
D26	TCU	tcu_test_mode	TEST_MODE	NVCC_JTAG (0V)	Input
D13	GPIO5	gpio_io, 20	I2C4_SCL	NVCC_I2C (0V)	Not Specified
E13	GPIO5	gpio_io, 21	I2C4_SDA	NVCC_I2C (0V)	Not Specified
G27	SRC	src_boot_mode, 1	BOOT_MODE1	NVCC_JTAG (0V)	Input
H27	XTALOSC	xtalosc_clkin, 1	CLKIN1	NVCC_CLK (0V)	Input
J27	XTALOSC	xtalosc_clkin, 2	CLKIN2	NVCC_CLK (0V)	Input
G26	SRC	src_boot_mode, 0	BOOT_MODE0	NVCC_JTAG (0V)	Input
AB26	GPIO2	gpio_io, 19	SD2_RESET_B	NVCC_SD2 (0V)	Not Specified
AE26	ENET1	enet_rgmii_rxc	ENET_RXC	NVCC_ENET (0V)	Input
AF23	SAI1	sai_tx_data, 7	SAI1_TXD7	NVCC_SAI1 (0V)	Output
H26	XTALOSC	xtalosc_clkout, 1	CLKOUT1	NVCC_CLK (0V)	Output
J26	XTALOSC	xtalosc_clkout, 2	CLKOUT2	NVCC_CLK (0V)	Output

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