Design Guide: TIDA-050051

Automotive 8.3-MP POC Camera Module Reference Design with PMIC and FPD-Link III

Description

This camera module reference design addresses the need for small low-cost cameras in automotive driver assistance systems (ADAS) by combining a 8.3-megapixel imager with a 4.16-Gbps TI FPD-Link III serializer. Additionally, it provides a power-management integrated circuit (PMIC) power supply for both devices in an ultra-small form factor. This design includes a high-speed serial interface to connect a remote automotive camera module to a display or machine vision processing system with a single coaxial cable transmitting both 8.3-MP RAW12 HDR video data and power.

Resources

TIDA-050051	Design Folder
TPS650330-Q1	Product Folder
DS90UB953-Q1	Product Folder

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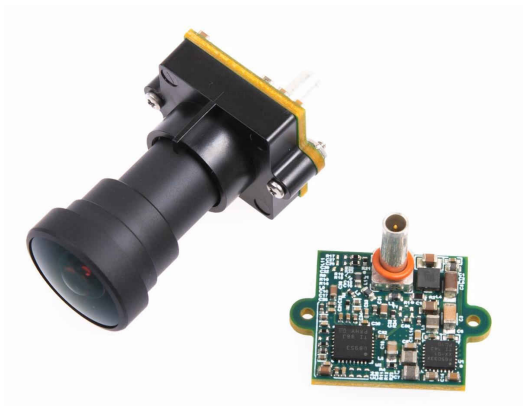
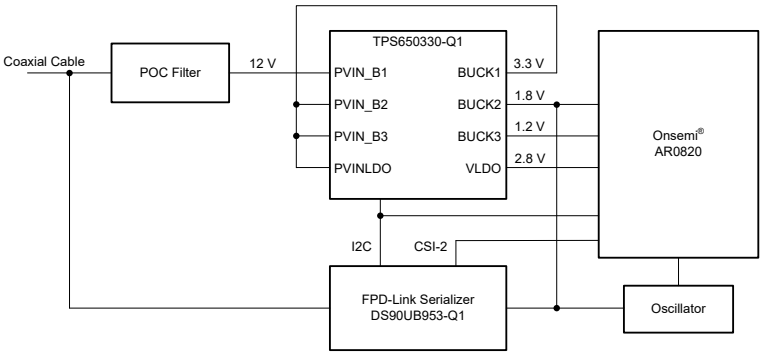
Features

- Space-optimized design with integrated power supply that fits on a single 20 mm × 20 mm PCB
- Integrated TPS650330-Q1 power supply includes three step-down converters and LDO to enable high efficiency and low noise supply generation
- P2P compatible power supplies to enable functional safety applications
- Enables camera applications up to 8-MP/27-fps using DS90UB953-Q1
- 8.3-MP AR0820 image sensor from Onsemi providing AD 12-bit, MIPI 4-lane, HDR RAW12, RAW14, RAW16, RAW20, RAW24
- Single Rosenberger Fakra coaxial connector for digital video, power, control, and diagnostics

Applications

- Camera Module without Processing
- Front Camera
- Rear Camera
- Surround View System





1 System Description

Many automotive applications require small form factors with reduced circuit area that enable compact and modular systems. As a result, most cameras along with electronic components must meet strict area constraints when designing ADAS camera applications. This reference design addresses this challenge by including a 8.3-megapixel imager, 4.16 Gbps serializer, and a single Power Management IC, and all components contained within an area of an 20-mm × 20-mm circuit board. The only connection required by the system is a single 50-Ω coaxial cable.

DC Power, the FPD-Link front-channel, and the FPD-Link back-channel enter the board through the FAKRA coax connector. The filter in Figure 1-1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

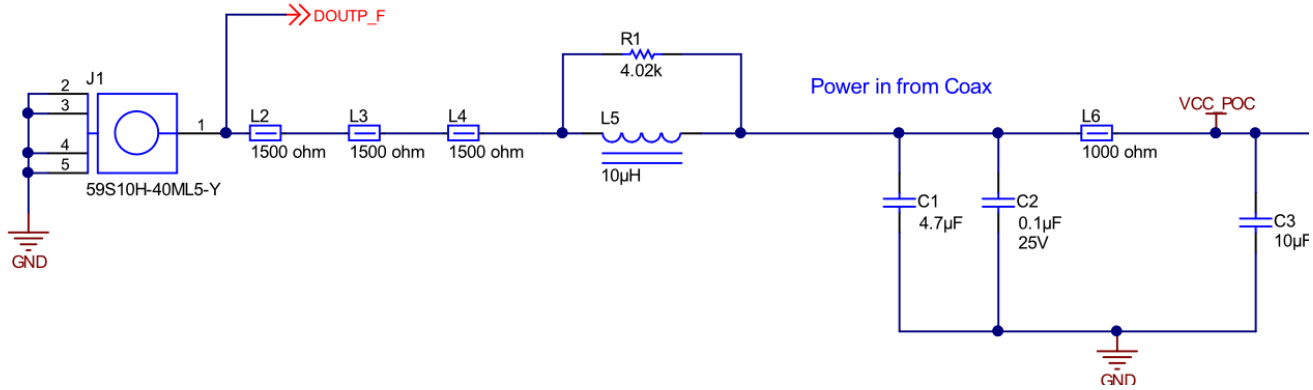


Figure 1-1. FPD-Link III Signal Path

The DC portion is connected to the buck 1 input of the TPS650330-Q1 Power Management IC. This voltage powers buck 2 and buck 3 of the device, which are responsible for creating the supply rails to the imager and serializer. The LDO input pin is supplied 3.3 V, which is responsible for providing a low-noise, 2.8-V analog supply to the imager. Buck 3 outputs the imager-dedicated 1.1-V and buck 2 generates a universal 1.8-V digital supply that is shared by both the imager and serializer. The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control back channel takes between the serializer and deserializer.

The output of the imager is connected through a MIPI 4-lane CSI-2 interface to the serializer. The serializer transmits this video data over a single LVDS pair to the deserializer located on the other end of the coax cable.

Additionally, on the same coax cable, there is a separate low-latency, bidirectional control channel that provides the additional function of transmitting control information from an I^2C port. This control channel is independent of the video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (POC)	5	12	18.3	V
P_{TOTAL}	Total power consumption	V_{POC} = 12 V	—	1	1.5	W
A_{PCB}	PCB Area		—	—	20 x 20	mm^2

2 System Overview

2.1 Block Diagram

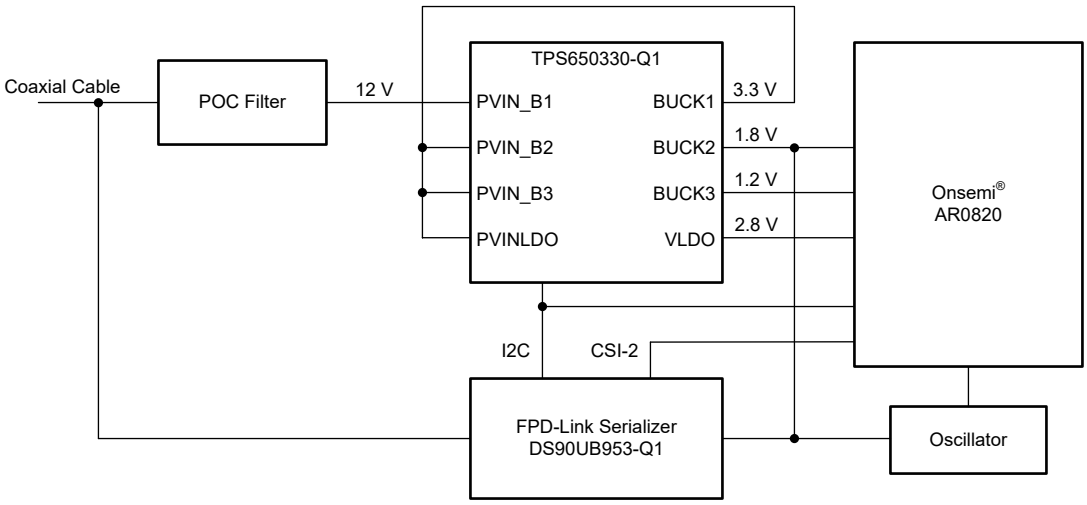


Figure 2-1. Camera Block Diagram

2.2 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.2.1 PCB and Form Factor

This reference design is not intended to fit any particular form factor; however, the goal of the design is to showcase a solution with minimal PCB area and compact design. The area of the board roughly equates to a dimension of 20 mm × 20 mm. The area near the board edge in Figure 2-2 is reserved for attaching the optics housing that holds the lens.

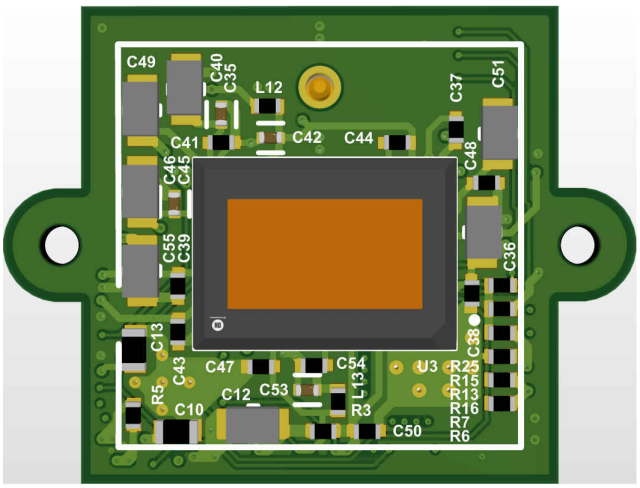


Figure 2-2. 3-D PCB Top Layer

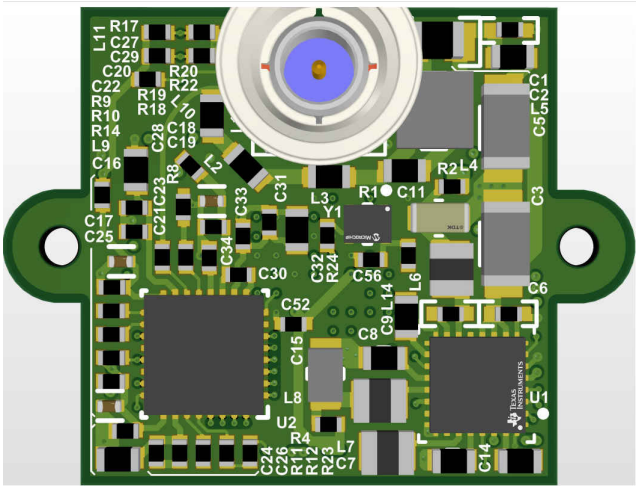


Figure 2-3. 3-D PCB Bottom Layer

2.2.2 Power Supply Design

2.2.2.1 POC Filter

One of the most critical portions of a design that uses POC is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise-coupled backwards from the rest of the system.

The DS90UB953-Q1 and DS90UB960-Q1 SerDes devices used in this system communicate over two carrier frequencies, 2 GHz at full speed (forward channel) and a lower frequency of 50 MHz (backchannel) determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC. An impedance of > 2 kΩ across the 25-MHz to 2-GHz bandwidth is required to allow the forward channel and back channel to pass uninterrupted over coax. To accomplish this, an inductor is typically chosen for filtering the 25-MHz to 1-GHz range, while a ferrite bead is chosen for filtering the 1- to 2-GHz frequency band. This complete filter is shown by L2 in Figure 2-4. L1 would be the same but its POC filter for the deserializer side of the FPD-Link III transmission. In this camera design, it is critical for the POC filter to have the smallest footprint possible. To accomplish this, the LQH3NPZ100MJRL 10-µH inductor is chosen because it has a wide band impedance that filters from 10 MHz to 1 GHz. This eliminates the need for a solution that would typically require two inductors, one for the lower frequency and another for the higher frequency.

For the high-frequency forward-channel filtering, this reference design uses three 1.5-kΩ ferrite beads in series with the 10-µH inductor to bring the impedance above 2 kΩ across the 1- to 2-GHz range. This design uses three 1.5-kΩ ferrite beads because when in operation, the current through these devices reduces the effective impedance. Therefore three ferrite beads instead of two allows for more headroom across the whole frequency band. For good measure, this design uses a 4-kΩ resistor in parallel with the 10-µH inductor to provide a constant impedance across the complete frequency band for impedance smoothing. With this approach, the solution size can be minimized onboard for the PoC inductor filtering. For more details, see the *Power Over Coax Design Guidelines for DS90UB953-Q1* application report.

Lastly, in regards to filtering, ensuring that the FPD-Link signal is uninterrupted is just as important as providing a clean, noise-free DC supply to the system. To achieve this, AC coupling capacitors shown by the 0.033 µF and 0.015 µF are chosen to ensure the high-speed AC data signals are passed through but that the DC is blocked from getting on the data lines. A smaller capacitance is possible for the DS90UB953-Q1 and DS90UB954-Q1 devices compared to previous generations due to the increased back channel speed.

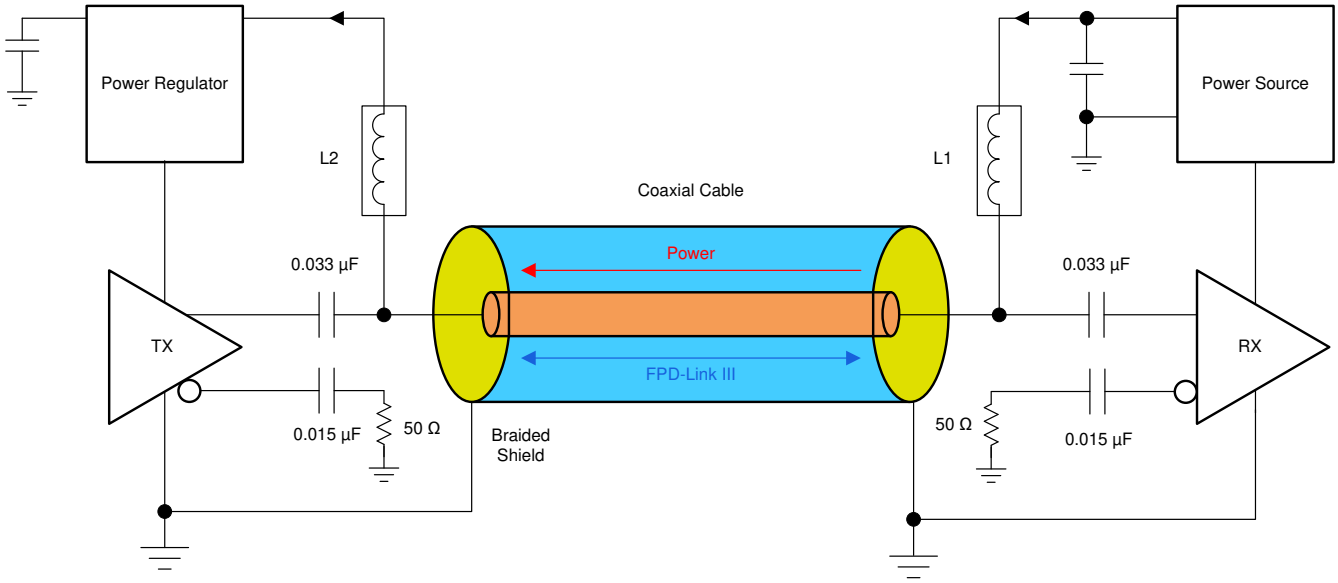


Figure 2-4. Power Over Coax

2.2.2.2 Power Supply Considerations

Because this reference design is targeted at automotive applications, there are several considerations that limit design choices. Additionally, the following list of system-level specifications helped shape the final overall design:

- The total solution size must be minimized to meet the size requirement of this design, which is equivalent to 20 mm × 20 mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate the need for external circuitry.
- To avoid interference with the AM radio band, all switching frequencies must be greater than 1700 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this reference design looks at higher frequency switchers.
- All devices must be AEC Q100 (-Q1) rated.

Before parts are chosen, the input voltage range, required voltage rails, and required current per rail must be known. In this case, the input voltage is a pre-regulated 12-V supply coming in over the coaxial cable. This system has only two main devices, the imager and serializer, which are responsible for power consumption during operation. Table 2-1 shows the requirements of the supplies:

Table 2-1. System Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (mA)	POWER (mW)
DS90UB953			
VDD	1.8	225	405
AR0820			
VDD-D	1.2	217	260
VDD-IO	1.8	4	7
VDD-A	2.8	141	395
Oscillator			
VDD	1.8	3	5
Total			
VDD-D	1.2	217	260
VDD-IO	1.8	232	418
VDD-A	2.8	141	395

The 12-V supply over the coaxial cable is first stepped down to 3.3 V, which then supplies the rest of the system on the camera module. In this design, the 1.8-V rail supplies both the DS90UB953 supply, and the interface supply of the AR0820 imager. The AR0820 2.8-V analog rail requires 141 mA, the DS90UB953 serializer 1.8-V rail requires 225 mA, and the AR0820 digital 1.2-V rail requires 217 mA.

Assuming 85% efficiency to simplify calculations with the previous values, it is calculated that the 3.3-V supply will require 124 mA to successfully power the 1.2-V, 1.8-V, and 2.8-V rails. Because the input and output voltages, output current requirements, and total wattage consumption are known, calculate the input current using Equation 1.

$$P_{IN} = V_{IN} \times I_{IN} = \frac{P_{OUT}}{\eta_{SYSTEM}} = \frac{\frac{P_{OUT2}}{\eta_2} + \frac{P_{OUT3}}{\eta_3} + \frac{P_{LDO}}{\eta_{LDO}}}{\eta_1} \quad (1)$$

$$\therefore I_{IN} = \frac{\frac{260\ mW}{85\,\%} + \frac{418\ mW}{85\,\%} + \frac{395\ mW}{85\,\%}}{12\ V \times 85\,\%} = 124\ mA$$

This information provides a strong foundation in the selection of power topologies and inductive passives that are explained in later sections.

Due to the requirement of Q100, it is mandatory that the switching frequency is rated outside of the AM band and must satisfy the voltage and current requirements derived previously. As the input voltage is a regulated voltage that will always be greater than any of the power rails produced, the power topologies selected should either be step-down converters (bucks) or LDOs. Bucks are generally included in supplies where switching noise is not a significant concern, and power savings is the largest care about. Conversely, LDOs can be incorporated in establishing low-noise analog supplies that reduce inherent noise and are more robust against EMI interactions; however, this is at the expense of larger current consumption.

In this design, a single Power Management IC is responsible for powering the supply rails. This device, the TPS650330-Q1, was chosen as it incorporates three step-down converters (BUCKS) and an LDO in a single 4.0-mm x 4.0-mm VQFN package. The current requirements of the design also played an important role in the selection of the device, as the secondary BUCKS are capable of providing 1200 mA, while the LDO is capable of supplying a maximum current output of 300 mA. BUCK1 steps down the 12-V POC input to 3.3 V. The 3.3-V rail then supplies power to BUCK2, BUCK3, and the LDO input. BUCK 2 provides the interface and digital supply for both the AR0820 imager and DS90UB953 serializer, while the LDO output creates a clean, low-noise supply for the 2.8-V analog supply for the AR0820.

2.2.2.2.1 Choosing External Components

For simplicity, the efficiency of the buck regulators is assumed to be 85% for these operating conditions, and the efficiency of the LDO is given by Equation 2.

$$\eta_{LDO} = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

System and Buck 1 currents calculated assuming 85% switching regulator efficiency are given in Equation 1.

Table 2-2 shows the load capability of each regulator compared to the requirements of the camera module. The TPS650330-Q1 device is capable of supplying the system power with plenty of margin to account for variations between typical and maximum current variation.

Table 2-2. Regulator Load Capability

REGULATOR	OUTPUT VOLTAGE (V)	MAX CURRENT (mA)	REQUIRED CURRENT (mA)
Buck 1	3.3	1500	383
Buck 2	1.8	1200	232
Buck 3	1.2	1200	217
LDO	2.8	300	141

After determining that the TPS650330-Q1 device is suitable based on the power requirements, the external components can be chosen quickly based on the data sheet recommendations, simplifying the design process. These recommendations are shown in Figure 2-5 and Table 2-3.

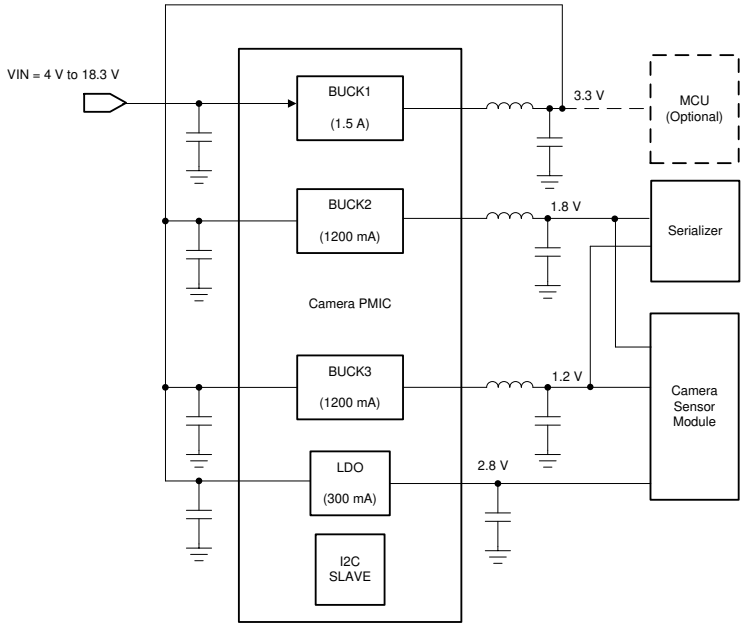


Figure 2-5. TPS650330-Q1 Typical Application Circuit

Table 2-3. TPS650330-Q1 Recommended Components

COMPONENT	DESCRIPTION	VALUE	UNIT
$C_{VSYS,VSYS\_S}$	VSYS and VSYS_S decoupling	10	µF
C_{PVIN_B1}	Buck 1 input capacitor	10	µF
L_{SW_B1}	Buck 1 inductor	1.5	µH
C_{OUT_B1}	Buck 1 output capacitor	10	µF
C_{PVIN_B2}	Buck 2 input capacitor	10	µF
L_{SW_B2}	Buck 2 inductor	1.0	µH
C_{OUT_B2}	Buck 2 output capacitor	10	µF
C_{PVIN_B3}	Buck 3 input capacitor	10	µF
L_{SW_B3}	Buck 3 inductor	1.0	µH
C_{OUT_B3}	Buck 3 output capacitor	10	µF
C_{PVIN_LDO}	LDO input capacitor	1.0	µF
C_{OUT_LDO}	LDO output capacitor	2.2	µF

2.2.2.2.2 Choosing the Buck 1 Inductor

With an inductance value of 1.5 µH selected, the minimum inductor saturation current must be derived to choose an appropriate inductor for the design. This is the combination of the steady-state supply current as well as the inductor ripple current. To ensure flexibility of the power and serializer base board to higher power image sensors, the inductor is chosen based on each maximum rated output current of the regulator. Equation 3 calculates inductor ripple current:

$$\Delta I_{L(max)} = V_{OUT} \times \left(\frac{1 - \frac{V_{OUT}}{V_{IN(max)}}}{L_{(min)} \times f_{sw}} \right) \quad (3)$$

where

- $\Delta I_{L(max)}$ is the maximum peak-to-peak inductor ripple current
- $L_{(min)}$ is the minimum effective inductor value
- f_{sw} is the actual PWM switching frequency

The parameters for Buck 1 of this reference design are:

- V_{OUT} = 3.3 V
- $V_{IN(max)}$ = 18.3 V
- $L_{(min)}$ = 1.5 µH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 784 mA. Assuming a maximum load current of 1500 mA, use Equation 4 to calculate a minimum saturation current of 1900 mA.

$$L_{SAT} \geq I_{OUT,(MAX)} + \frac{\Delta I_{L(MAX)}}{2} \quad (4)$$

The TPS650330-Q1 device on this design uses a TDK® TFM201610ALMA1R5MTAA, which has a rated current of 2 A and a DC resistance maximum of 152 mΩ. Additionally, this inductor has an operating temperature from –55°C to 150°C in a very small 2.0-mm × 1.6-mm package.

2.2.2.2.3 Choosing the Buck 2 and Buck 3 Inductors

Buck 2 and Buck 3 have a recommended inductor value of 1.0 µH. When selecting a component, it is important to verify the DC resistance and saturation current. The DC resistance of the inductance influences the efficiency of the converter directly – lower DC resistance is directly proportional to efficiency. The saturation requirement of the inductor is determined by combining the steady-state supply current and the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current using Equation 3.

The parameters for the Buck 2 1.8-V rail include:

- V_{OUT} = 1.8 V
- $V_{IN(max)}$ = 3.3 V
- $L_{(min)}$ = 1.0 µH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 356 mA. Assuming a maximum load current of 1200 mA, Equation 4 can be used to calculate a minimum saturation current of 1400 mA.

The parameters for the Buck 3 1.2-V rail include:

- V_{OUT} = 1.2 V
- $V_{IN(max)}$ = 3.3 V
- $L_{(min)}$ = 1.0 µH
- f_{sw} = 2.3 MHz

These parameters yield an inductor ripple current of ΔI_L = 332 mA. Assuming a maximum load current of 1200 mA, Equation 4 can be used to calculate a minimum saturation current of 1400 mA.

Buck 2 and Buck 3 of this design use the TDK® TFM201610ALMA1R0MTAA, which has a current rating of 3.1 A and a DC resistance of 60 mΩ. Additionally, this inductor has an operating temperature of –55°C to 150°C in a very small 2.0-mm × 1.6-mm package.

2.2.2.3 Functional Safety

The TPS650330-Q1 device has integrated supervisors in addition to temperature and current monitoring. The device is also pin-compatible with the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1. Each of the TPS650331-Q1, TPS650332-Q1, and TPS650333-Q1 devices provides additional safety features as an ASIL-B safety element out of context (SEooC), allowing the scalability of this design to camera applications with functional safety requirements.

2.3 Highlighted Products

This reference design uses the following TI products:

- DS90UB953-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).
- TPS650330-Q1: an automotive qualified, four-channel PMIC optimized for camera applications. The device integrates three buck converters and one LDO, along with overvoltage protection and undervoltage supervisors on each voltage rail. A high, fixed PWM 2.3-MHz switching frequency enables the use of small inductors with a fast transient response. The low-noise, high-PSRR LDO provides an output voltage option for sensitive analog circuits. A wide range of output voltage and sequencing settings, along with other operational settings, are programmable for compatibility with a variety of imagers without the need for any additional components.

2.3.1 AR0820 Imager

The Onsemi® AR0820 is a diagonal 9.25-mm, 1/2" CMOS image sensor with 8.3 effective mega-pixels. The sensor integrates a 12-bit ADC and supports MIPI 4-lane, RAW12 up to RAW24 HDR output. Other features include:

- Supports 3840 x 2160 resolution (8.3-MP) at up to 40-fps
- Fault detection for ASIL-B compliance support
- Multi-camera synchronization support
- Requires three voltage rails (2.8 V, 1.8 V, and 1.2 V)
- Can be configured using an I^2C-compatible two-wire serial interface

2.3.2 DS90UB953-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The CSI-2 input of the DS90UB953-Q1 mates well with the MIPI CSI-2 video output of the AR0820 imager. Once combined with the filters for the PoC, video, I2C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coax cable.

2.3.3 TPS650330-Q1

The TPS650330-Q1 device is a highly-integrated power management IC for automotive camera modules. This device combines three step down converters and one low-dropout (LDO) regulator. The BUCK1 step-down converter has an input voltage range up to 18.3 V for connections to Power over Coax (POC). All converters operate in a forced fixed-frequency PWM mode. The LDO can supply 300 mA and operate with an input voltage range from 3.0 V to 5.5 V. The step-down converters and the LDO have separate voltage inputs that enable maximum design and sequencing flexibility. Additionally, an integrated advanced Spread-Spectrum Clock (SSC) enables robust EMI performance. A small form-factor, added rail supervision features, and programmability make this device a very attractive candidate for designs that need to be expedited or scaled for future applications.

2.4 System Design Theory

The main design challenges to consider for automotive cameras are size, ease of use, and thermal efficiency. Automotive cameras are often placed in remote regions of the vehicle where area is limited, requiring an overall compact solution. Because of this, the system is designed around having the lowest number of components with a fully-integrated PMIC power solution. The ease of use and design flexibility offered by a PMIC solution is also critical to enable a single platform design and reduce development time as ADAS applications continue to grow. The DS90UB953-Q1 and TPS650330-Q1 additionally both provide compatibility with a wide range of imagers. Lastly, the small size and remote placement of these cameras increases their susceptibility to heat. A power-efficient system is crucial to preserve the image quality in these conditions. The TPS650330-Q1 device is optimized for efficiency with a three-buck and one-LDO regulator topology, enabling the support of medium- and high-quality imagers without sacrificing thermal performance. Due to the impact of thermals on the system performance, it is important to calculate total system efficiency as part of the design process. From the Buck 1 output power in Table 2-2, the TPS650330-Q1 efficiency is about 90%. Using this value, Equation 5 calculates a system input power of about 1.4 W. Equation 5 can then be used with the output power of Buck 2, Buck 3, and the LDO to calculate the overall system efficiency.

$$\eta_{SYSTEM} = {P_{OUT}}/{P_{IN}} = \left(P_{OUT,2} + P_{OUT,3} + P_{OUT,LDO}\right)/{P_{IN,1}} = 75\,\% \quad (5)$$

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware Requirements

This reference design needs only one connection to a system with a compatible deserializer over the FAKRA connector as shown in Figure 3-1.

Figure 3-1. Getting Started With the Board

3.1.1 Hardware Setup

Figure 3-2 shows the setup to test the camera module reference design. This design includes an AR0820 image sensor, which connects to the DS90UB953-Q1 serializer over CSI-2 and I^2C interfaces. The DS90UB953-Q1 serializer then connects through POC to a DS90UB960-Q1 deserializer. Note that for test setup, only one channel is used from the DS90UB960-Q1 device.

To enable video output from the DS90UB960-Q1 device, the deserializer Fusion1 Rev C application board is connected to the Jacinto 7 EVM. This EVM enables video output by writing all the backchannel I2C setting configurations for the AR0820, DS90UB953-Q1, and DS90UB960-Q1 devices. When these writes are completed, Vision SDK software enables video output to a DisplayPort connected monitor.

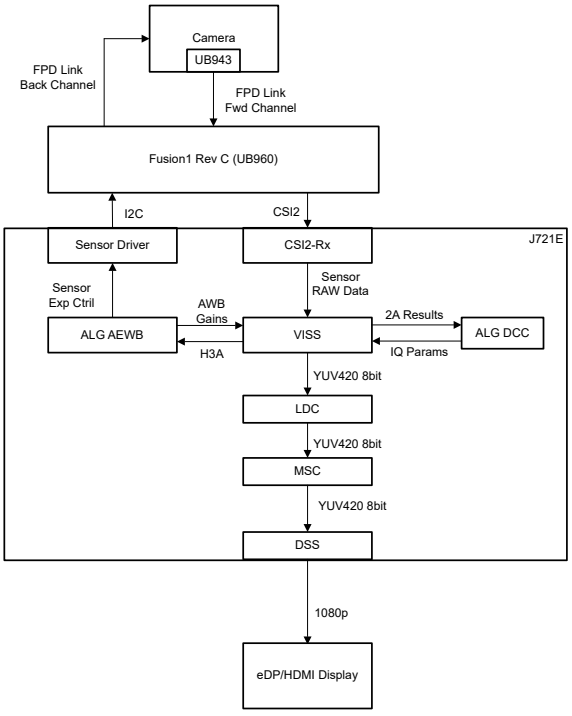


Figure 3-2. Test Setup

3.1.2 FPD-Link III I²C Initialization

With the setup in Figure 3-2 connected, the Fusion1 Board featuring the DS90UB960-Q1 deserializer is supplied 12-V input power, which is delivered through POC to power the TIDA-050051 camera module. Once all rails are established, the I2C writes for initialization can begin. These writes are executed in the single camera application use case available in the Jacinto 7 processor Software Development Kit (SDK). For more information, see the EVM and SDK tool pages.

```
COM3 - PuTTY
. Try again
6 registered sensor drivers
a : IMX390-UB953_D3
b : AR0233-UB953_MARS
c : AR0820-UB953_LI
d : UB9xxx_RAW12_TESTPATTERN
e : UB96x_UYVY_TESTPATTERN
f : GW_AR0233_UYVY
Select a sensor above or press '0' to autodetect the sensor : c
Sensor selected : AR0820-UB953_LI
LDC Selection Yes(1)/No(0) : LDC Selection Yes(1)/No(0) : 0
Querying AR0820-UB953_LI
521562.227617 s: ISS: Querying sensor [AR0820-UB953_LI] ... !!!
521562.227982 s: ISS: Querying sensor [AR0820-UB953_LI] ... Done !!!
521562.227992 s: ISS: Initializing sensor [AR0820-UB953_LI], doing IM_SENSOR_CMD_PWRON ... !!!
521562.228289 s: ISS: Initializing sensor [AR0820-UB953_LI], doing IM_SENSOR_CMD_CONFIG ... !!!
[MCU2_0] 521565.055656 s: AR0820_WriteReg : Error writing to register 0x301a
[MCU2_0] 521565.055721 s:
[MCU2_0] 521565.055747 s:
[MCU2_0] 521565.055785 s:  AR0820: Sensor Reg Write Failed for regAddr 0x301a
[MCU2_0] 521565.055820 s:
521566.131614 s: ISS: Initializing sensor [AR0820-UB953_LI] ... Done !!!
read_test_image_raw : Unable to open file /opt/vision_apps/test_data/img_test.raw
app_create_viss : sensor_dcc_id = 820
Scaler is enabled
521566.162397 s: ISS: Starting sensor [AR0820-UB953_LI] ... !!!


 ==========================
 Demo : Single Camera w/ 2A
 ==========================

 p: Print performance statistics

 s: Save Sensor RAW, VISS Output and H3A output images to File System

 e: Export performance statistics

 u: Update DCC from File System


 x: Exit

 Enter Choice:
```

Figure 3-3. Single Camera Application Initialization

3.1.3 AR0820 Initialization

Once the FPD-Link III setup is done for the DS90UB953-Q1 and DS90UB960-Q1 devices, the I²C initialization can now be done on the AR0820. For these writes, see the AR0820 data sheet for register settings. There are many register settings listed to configure both the imager and ISP, but as long as the DS90UB953-Q1 and DS90UB960-Q1 FPD-Link III parts are configured, the I²C back channel allows for the AR0820 to be accessed at address 0x10. For this testing, the AR0820 is configured for RAW12 HDR output at 3840 × 2160 resolution.

3.2 Test Setup

For the following tests to verify power supply and I²C communication, the camera is connected to the Fusion Application expansion card and the Jacinto 7 EVM as shown in Figure 3-2.

3.2.1 Power Supplies Start Up

To verify the power supply sequencing and start-up behavior, each voltage rail output from the TPS650320-Q1 device is measured after applying power over coax to the system.

In this design, the PDB reset signal of the DS90UB953-Q1 device is connected directly to the nRSTOUT pin of the TPS650330-Q1 device. With the integrated sequencing capabilities of the PMIC, this ensures that the PDB reset line goes high after the 1.8-V supply is stable, eliminating the need for an external RC network.

3.2.2 Camera Functionality

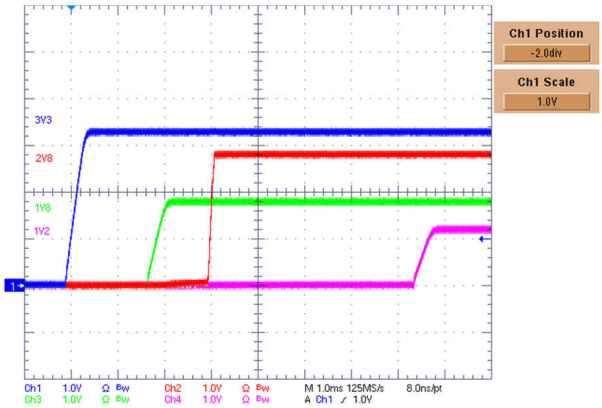
Back-channel I2C communications are verified over serial connection to the Jacinto 7 EVM. A DisplayPort compatible monitor is used to verify the video stream and image quality.

3.3 Test Results

The following sections show the test data from verifying the functionality of the camera design.

3.3.1 Power Supplies Start-Up

Figure 3-4 shows the start-up behavior for the 3.3-V, 1.8-V, 1.2-V, and 2.8-V rails.

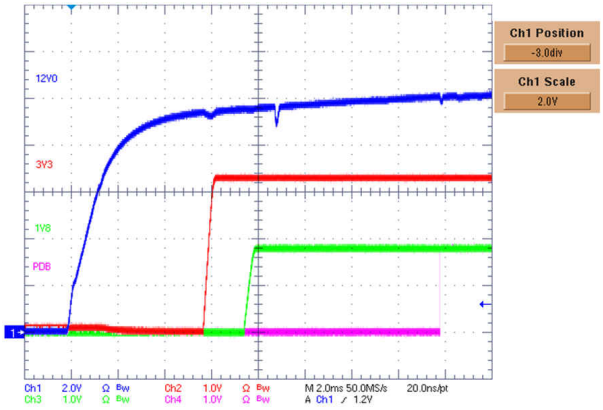


(Channel 1): 3.3-V supply; (Channel 2): 2.8-V supply; (Channel 3): 1.8-V supply; (Channel 4): 1.2-V supply

Figure 3-4. Point-of-Load Power Supply Start-Up

3.3.2 Power Supply Start-Up—1.8-V Rail and PDB

To properly initialize, the PDB pin of the serializer remains low until all power supplies stabilize to their final voltages. Figure 3-5 shows the power supply start up. Note that the PDB pin is directly connected to $\overline{\text{RSTOUT}}$ the of TPS650320-Q1 device and allows proper PDB synchronization after all rails are established.



(Channel 1): 12-V supply; (Channel 2): 2.8-V supply; (Channel 3): 1.8-V supply; (Channel 4): PDB

Figure 3-5. Serializer Power-Up Sequence

3.3.3 Power Supply Voltage Ripple

To achieve a quality output video stream, the output voltage ripple on the AR0820 and DS90UB953-Q1 supplies must be low so that it does not affect the integrity of the high-speed data and internal PLL clocks. Measurements for 3.3-V, 2.8-V, 1.8-V, and 1.2-V rails are shown in Figure 3-6, Figure 3-7, and Figure 3-8, respectively. The rails that impact imager performance are the 2.8-V and 1.2-V rails as they are responsible for providing a clean analog rail and digital supply. The 3.3-V rail powers the entire system and also has excellent ripple performance of 0.5%. As measured, the 2.8-V and 1.2-V rails have a ripple performance of 0.1% and 0.6%, respectively. The 1.8-V rail is significant to the serializer, because it supplies the VDD and VDD_PLL rails. The 1.8-V rail has great voltage ripple performance at 0.7%. The voltage ripple on all rails is low enough for video output to be successfully transmitted.

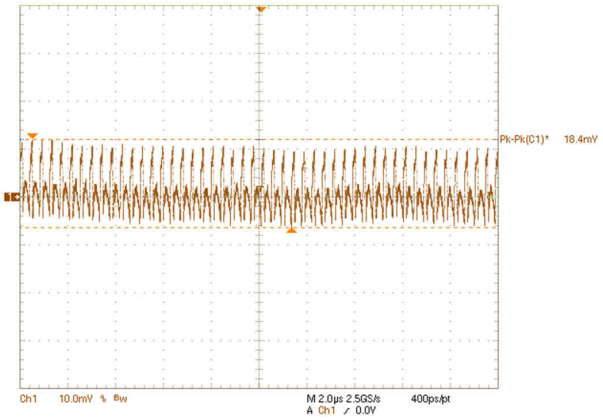


Figure 3-6. Output Voltage Ripple - 3.3 V

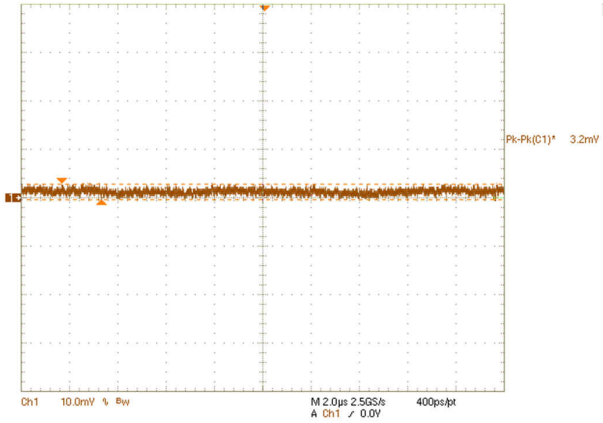


Figure 3-7. Output Voltage Ripple - 2.8 V

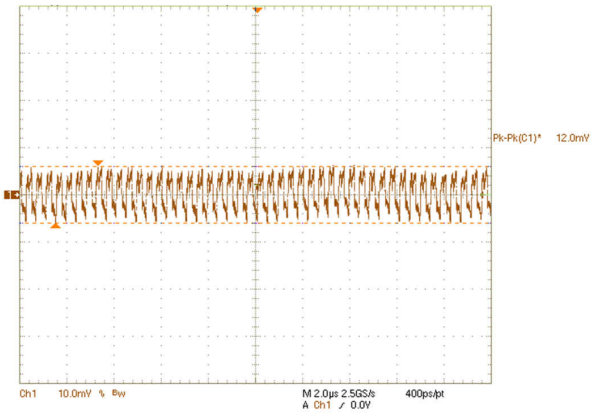


Figure 3-8. Output Voltage Ripple - 1.8 V

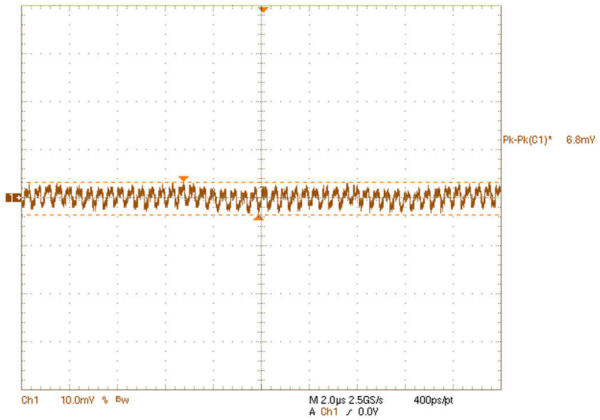


Figure 3-9. Output Voltage Ripple - 1.2 V

3.3.4 Power Supply Load Currents

The last measurements to take in regard to the power supplies on the camera module are the load currents for the system supply, and the load currents on the AR0820 imager. These measurements verify total power consumption of the camera module as well as the load current for each individual rail on the AR0820 imager. For the following test data, each rail is drawing the specific load current outlined for the serializer and imager. All load current measurements are taken while a video output stream is present.

Table 3-1 displays the currents measured through each supply voltage in this reference design. The 12-V load current is the total input load for the camera module and measures at 107 mA. The total power consumption corresponds to an overall system efficiency of 70%, close to the 75% value derived in Section 2.4. The difference can be attributed to lower operating currents than expected, as well as conduction losses in the POC cable and filters.

Table 3-1. Measured Supply Currents

VOLTAGE RAIL	MEASURED CURRENT
12 V	103 mA
3.3 V	320 mA
2.8 V	120 mA
1.8 V	193 mA
1.2 V	155 mA

3.3.5 Video Output

Shows an output frame from the camera modle while operating at 3840 x 2160 resolution and 27-fps. The output format is 8-bit YUV420.

Figure 3-10. TIDA-050051 Video Output

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050050.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050050.

4.1.3 PCB Layout Recommendations

4.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050050.

4.1.3.2 PMIC Layout Recommendations

The PMIC portion of the layout requires careful consideration to minimize both PCB area and noise. As EMI is a critical concern in automotive systems, the TPS650330-Q1 device includes a spread spectrum feature to reduce conducted and radiated emissions, allowing more flexibility with placement and layout for space-constrained applications. However, it is still recommended to follow as many best practices as possible. This includes minimizing the area traveled by switching currents between buck regulator input capacitor, inductor, and output capacitor with tight component placement and minimal return path to the PMIC thermal pad. Figure 4-1 shows an example of this for buck 1 and buck 3.

For the LDO, separation of input and output capacitor ground planes will reduce noise coupling from the switching rails to the sensitive 2.8-V analog rail. To further reduce noise coupling, the dedicated AGND pin of the PMIC is connected to the ground plane on an internal layer with a via, rather than directly to the noisier thermal pad on the top layer.

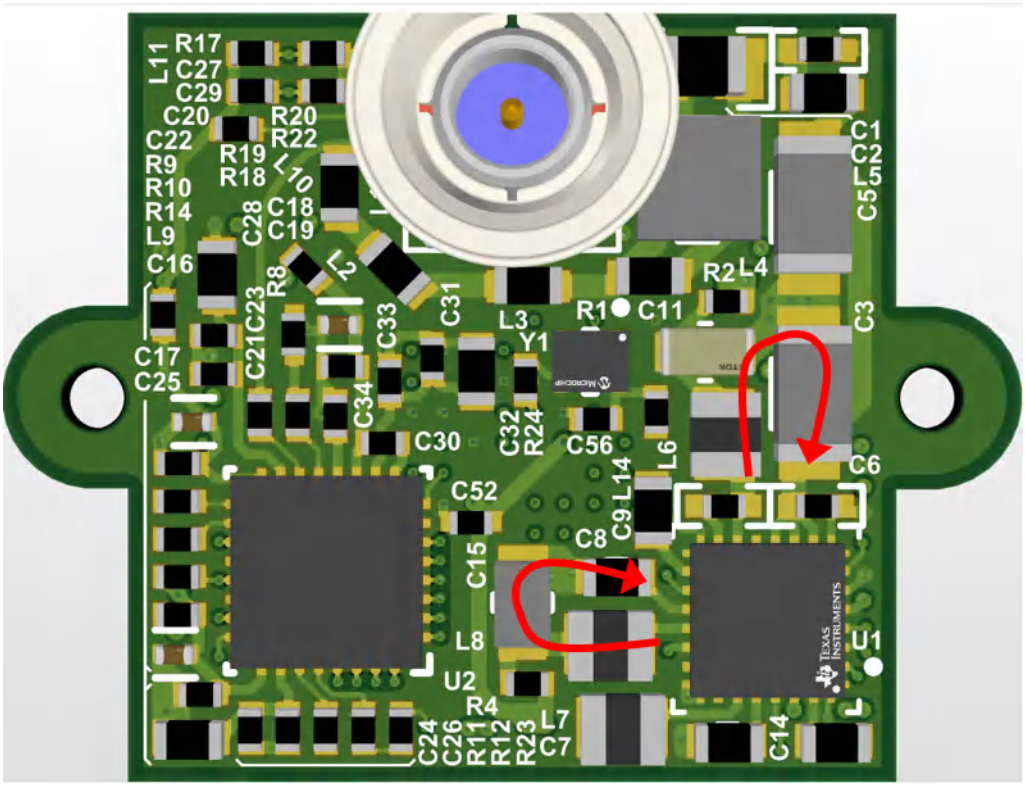


Figure 4-1. PMIC PCB Layout

4.1.3.3 Serializer Layout Recommendations

Decoupling capacitors must be located very close to the supply pin on the serializer. Again, this requires consideration of the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. For decoupling capacitors placed on the opposite layer of the serializer, minimize the return path to the serializer thermal pad. Place smaller value capacitors that provide higher frequency decoupling closest to the device.

For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Anti-pads are implemented in the ground plane under critical components such as the DOUT AC coupling capacitors to minimize impedance mismatch. Keep the coax connection to the serializer short. Figure 4-1 shows the routing of the high-speed serial line, highlighted by the redline. The total length of the red line is about ½ inch.

Lastly, minimize crosstalk between high-speed data lines by ensuring the high-speed data routing on adjacent layers do not overlap. If they must overlap due to space constraints, place a ground layer between the two routing layers as a buffer. Keep high speed trace vias to a minimum. The vias must ideally be two or fewer to reduce stubs that cause reflections.

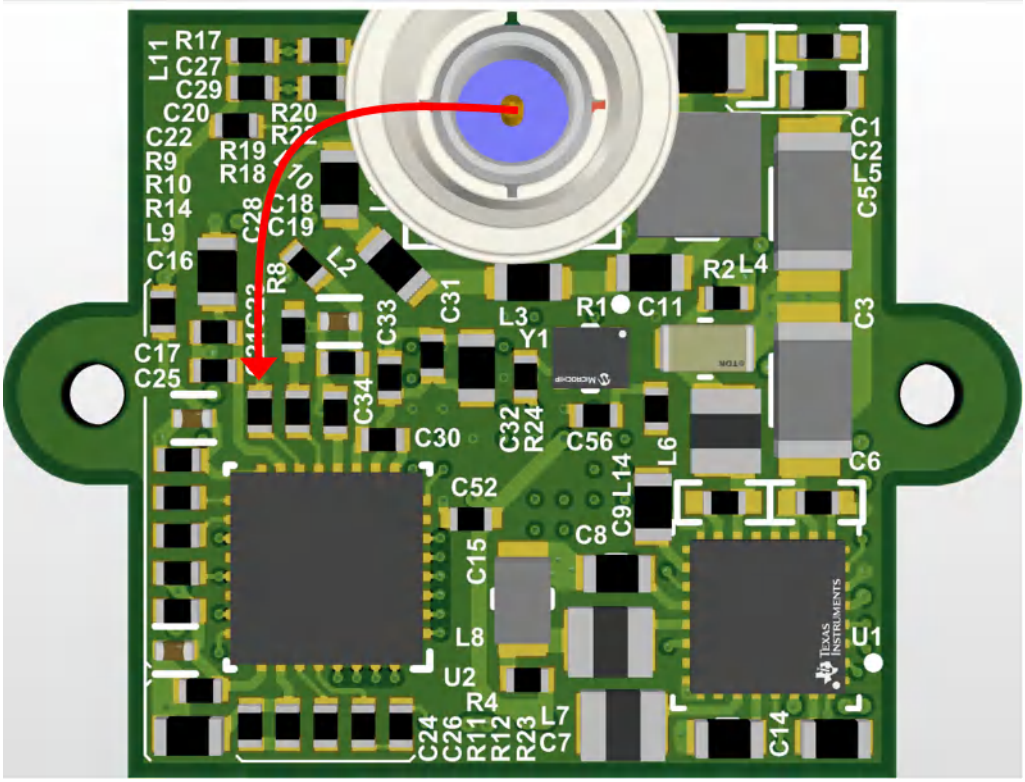


Figure 4-2. High-Speed Trace Routing

4.1.3.4 Imager Layout Recommendations

High-speed data routing must follow the same guidelines previously outlined for the serializer layout. Similarly, place the decoupling capacitors as close as possible to the supply pins, with smaller capacitors taking priority in terms of distance to the pin. Minimize the parasitic resistance and inductance to the ground plane with vias and wide traces. For some imagers, a separate analog ground (AGND) plane is recommended to reduce image noise. Connect imager AGND pins, AVDD decoupling capacitors, and the LDO output capacitor to this AGND plane, and connect the plane back to the main ground at a single point.

4.1.3.5 PCB Layer Stackup Recommendations

Figure 4-3 shows the 8-layer stackup used for the PMIC and serializer board. Two signal layers are required due to the complex routing requirements introduced by the small size requirements of the PCB that must include I2C, logic IOs, clock, and control signals between the PMIC, serializer, and imager. The separation of the outer layers is selected to ensure a single-ended characteristic impedance of 50 Ω, and differential characteristic impedance of 100 Ω.

In this design, high current components are placed on both the top layer and the bottom layer, so Layer 2 and Layer 7 in the stackup are dedicated ground planes to minimize high current return paths.

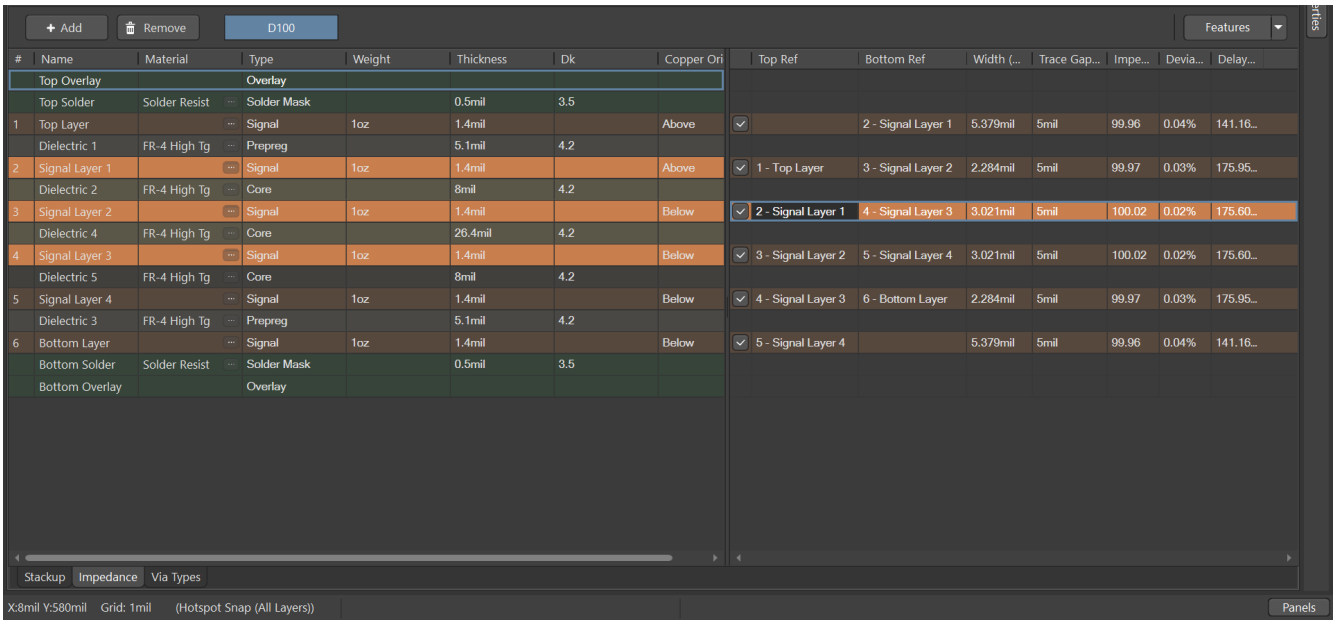


Figure 4-3. Layer Stackup

4.1.4 Altium Project

To download the Altium project files, see the design files at TIDA-050051.

4.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050051.

5 Documentation Support

1. Texas Instruments, *TPS650330-Q1 EVM* user's guide
2. Texas Instruments, *DS90UB95x-Q1EVM Deserializer* user's guide
3. Texas Instruments, *DS90UB953-Q1 FPD-Link III Serializer for 1-MP/60-fps Cameras 10/12 Bits,100 MHz* data sheet
4. Texas Instruments, *Power Over Coax Design Guidelines for DS90UB953-Q1* application note
5. Texas Instruments, *Camera PMIC Spin Selection Guide* application note
6. Texas Instruments, *Jacinto7 J721E/DRA829/TDA4VM Evaluation Module* user's guide
7. Texas Instruments, *Software Development Kit for DRA829 & TDA4VM Jacinto™ processors*

6 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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