*Design Guide: TIDA-050072*

# *65-W, GaN-Based USB PD 3.0 USB Type-C® Adapter Reference Design*

## Description

This reference design is a 65-W, USB power delivery (PD) 3.0 adapter targeted for many charging applications including mobile phones, laptops, and tablets. The design achieves high efficiency and power density with the use of integrated gallium nitride (GaN) technology. High efficiency is enabled with the quasi-resonant flyback, which provides a balance between simplicity and low switching losses. The quasi-resonant scheme varies the switching frequency across line and load, while making sure that the primary field-effect transistor (FET) switches at the lowest possible drain voltage. To further increase the efficiency, the integrated sense emulation of the GaN device provides virtually lossless current sensing. High power density is enabled by the high-frequency capability of the integrated GaN device, which enables a smaller inductance, smaller core size, and reduction in the total number of primary windings.

## Features

- 25.29 W/in$^3$ power density achieved for compact adapter designs
- 92.83% efficiency at full-load, 90 Vac input
- 94.09% efficiency at full-load, 115 Vac input
- 94.32% efficiency at full-load, 230 Vac input
- 70-mW loss reduction provided with integrated lossless current sensing
- 30-mW standby power at 115 Vac
- Low temperatures achieved by GaN device enable simple thermal management
- Universal AC input voltage capability

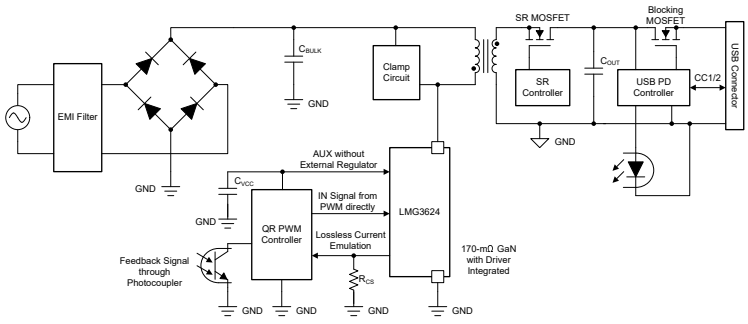
## Applications

- Mobile wall charger design
- USB wall power outlet
- Auxiliary-power supplies

## Resources

| | |
|---|---|
| TIDA-050072 | Design Folder |
| LMG3624 | Product Folder |

Ask our TI E2E™ support experts



# 1 System Description

This reference design focuses on optimizing power density and efficiency in a 65-W, USB PD 3.0 application. The key device that enables this operation is the primary switching device, LMG3624, 170-mΩ integrated GaN FET with current-sense emulation.

The design employs the quasi-resonant flyback topology with synchronous rectification to achieve a balance between performance and simplicity. The flyback transformer is kept to a minimum size by operating at high switching frequencies which enable a low magnetizing inductance requirement.

The design is able to deliver power to a USB PD 3.0 load with outputs of 20 V | 3.25 A, 15 V | 3 A, 9 V | 3 A, 5 V | 3 A.

## 1.1 Key System Specifications

| PARAMETER | VALUE |
|---|---|
| Input voltage | 90 Vac–265 Vac |
| Output | 20 V \| 3.25 A, 15 V \| 3 A, 9 V \| 3 A, 5 V \| 3 A |
| Maximum switching frequency | 163 kHz |
| Minimum switching frequency | 76 kHz |

# 2 System Overview

## 2.1 Block Diagram

The reference design based on a low cost, high efficiency, and high density 65-W USB PD design including a QR flyback power stage, SR control , and USB PD control.

The QR flyback power stage is powered by the LMG3624, 170-mΩ GaN FET with integrated GaN FET and current sensing. The LMG3624 enables high-frequency operation, in which the transformer design is minimized. The integrated current sensing reduces the loss from traditional current shunt resistors, providing higher system efficiency and lower cost.

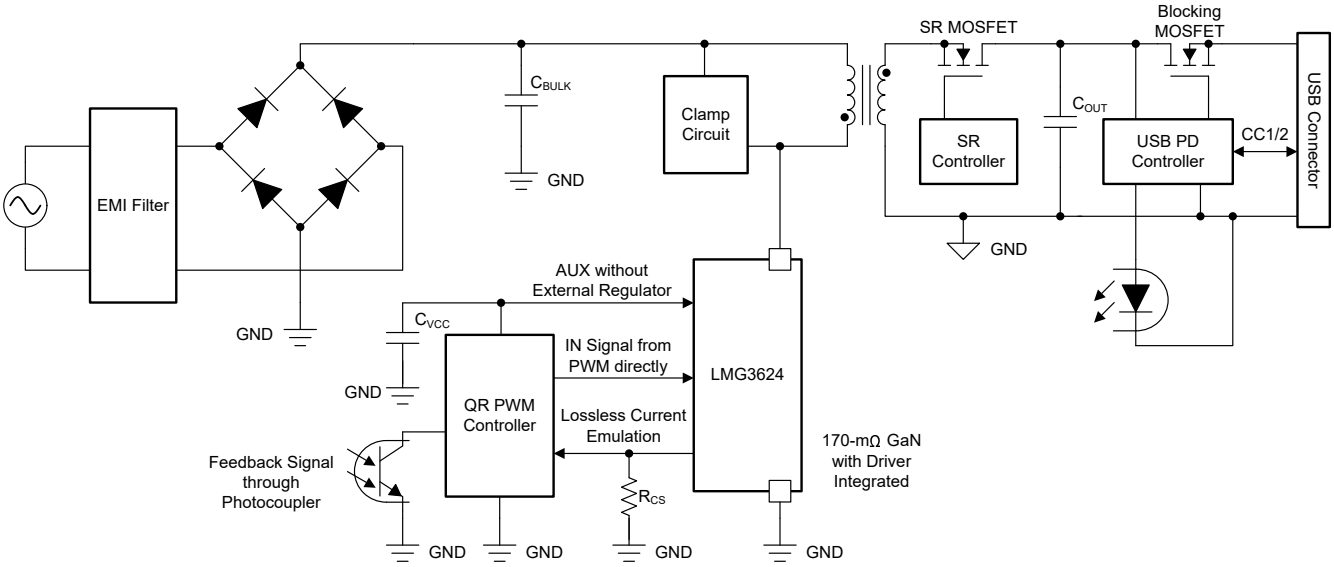



**Figure 2-1. System Block Diagram of 65-W USB PD Reference Design**

## 2.2 Design Considerations {Required Topic}

{ "Elaborate on details of the design" }

## 2.3 Highlighted Products

### 2.3.1 LMG3624

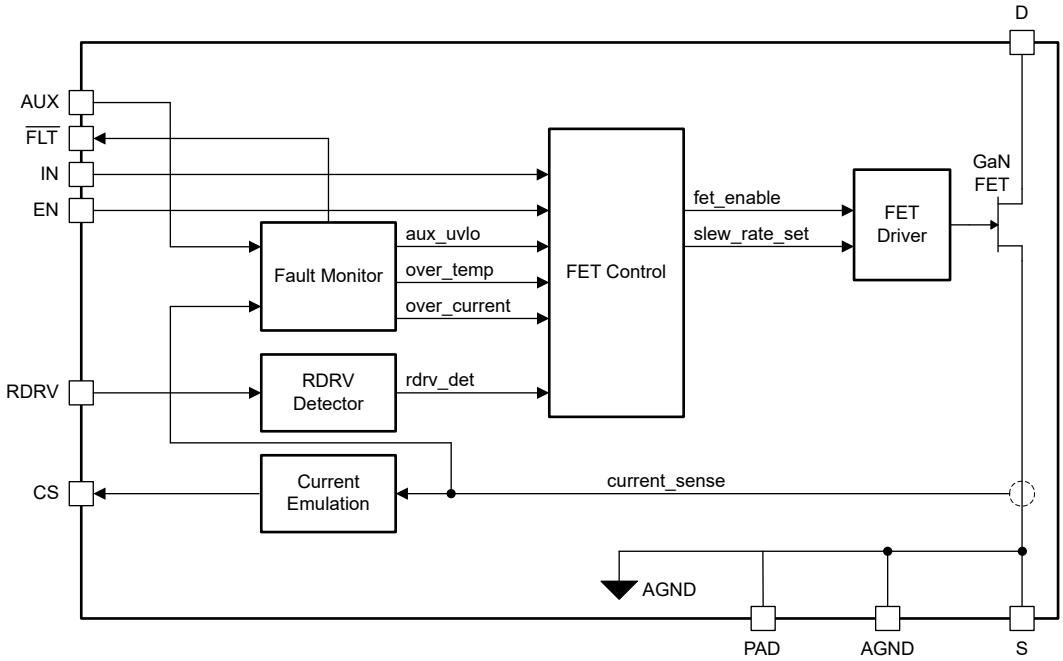



**Figure 2-2. LMG3624 Functional Block Diagram**

The LMG3624 is a 650-V 170-mΩ GaN power FET intended for switch-mode power-supply applications. The LMG3624 simplifies design and reduces component count by integrating the GaN FET and gate driver in a 8-mm by 5.3-mm QFN package.

Programmable turn-on slew rates provide EMI and ringing control. The current-sense emulation feature reduces power dissipation compared to the traditional current sense resistor and allows the low-side thermal pad to be connected to the cooling PCB power ground.

Low quiescent currents and fast start-up times support converter light-load efficiency requirements and burst-mode operation.

Extended feature descriptions are provided in the following list:

- 650-V, 170-mΩ GaN power FET
- Integrated gate driver with low propagation delays and adjustable turn-on slew-rate control
- Current-sense emulation with high bandwidth and high accuracy
- Cycle-by-cycle overcurrent protection
- Overtemperature protection with FLT pin reporting
- AUX quiescent current: 240 µA
- AUX standby quiescent current: 50 µA
- Maximum supply and input logic pin voltage: 26 V
- 8-mm × 5.3-mm QFN package with thermal pad

# 3 System Design Theory

## 3.1 Quasi-Resonant Operation

The quasi-resonant converter is chosen because this converter provides the best balance between cost, power loss, and simplicity.

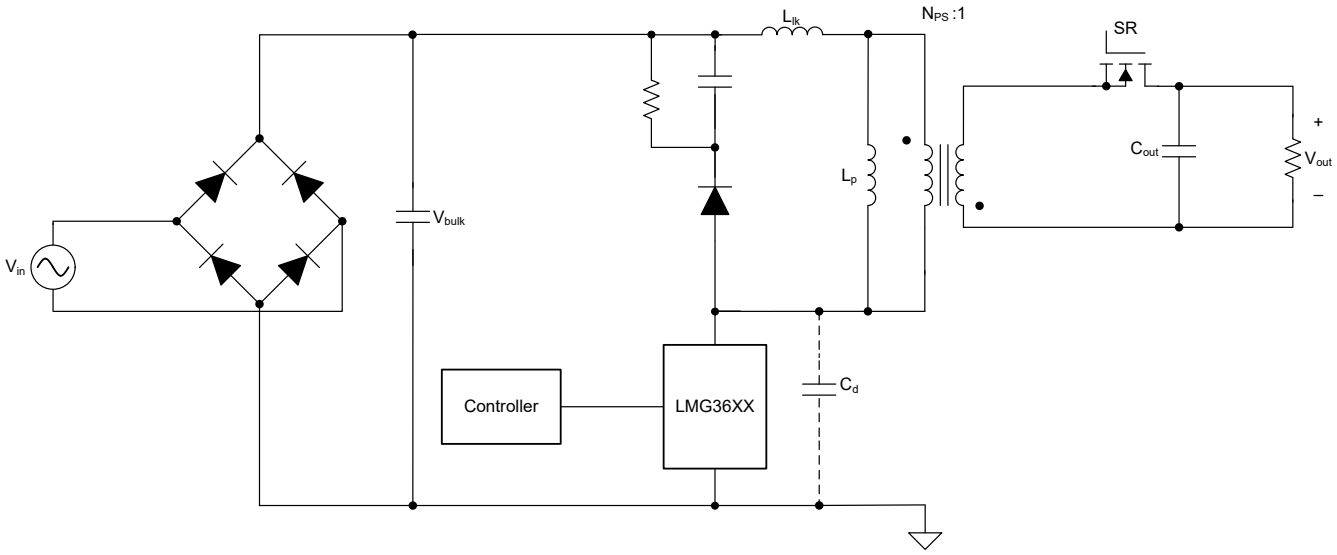



**Figure 3-1. Quasi-Resonant Converter Abstract Schematic**

The converter consists of a diode rectifier stage, switching FET, transformer with an inherent magnetizing inductance, passive RC clamp, synchronous secondary rectifier, and output capacitor.

The diode rectifier stage consists of the diode bridge and bulk capacitor. The diode bridge rectifies the ac line voltage and stores energy in the bulk capacitor, which maintains a relatively constant positive voltage.

The controller switches the FET on and off to deliver energy to the secondary side. While the FET is in the *on* state, current (energy) is built up in the magnetizing inductance of the transformer.

This is described by Equation 1:

$$E_{STORED} = \frac{1}{2} L_{MAG} \times I_{PK}^2 \quad (1)$$

The power delivered is calculated with Equation 2:

$$P = E_{STORED} \times f_{SW} \quad (2)$$

While the FET is in the *off* state, the rectifier on the secondary side of the transformer turns on and delivers the current to the load.

To maximize efficiency, the converter operates under *quasi-resonant* operation by turning on the FET at the resonant voltage valley formed by the resonance of the magnetizing inductance,$L_{MAG}$, and the total switch-node capacitance,$C_D$.

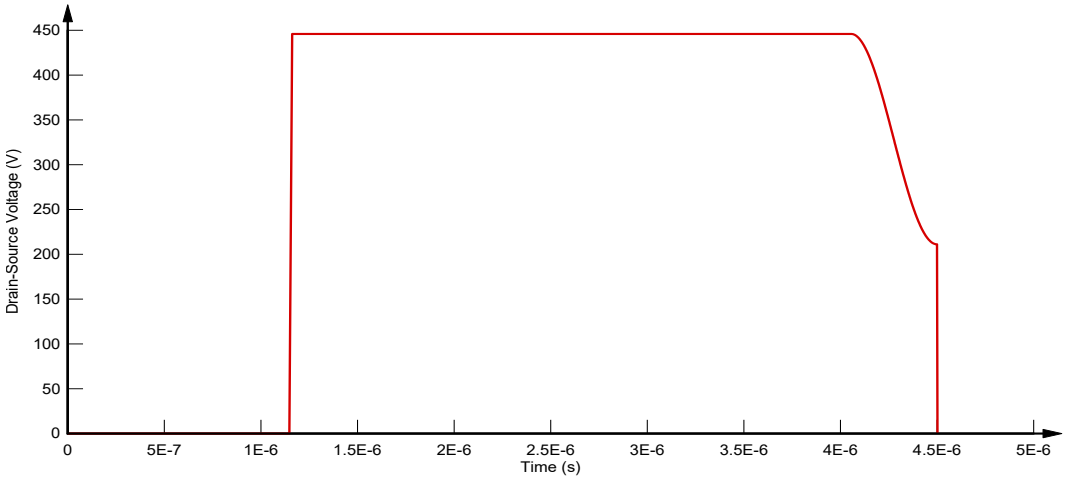



**Figure 3-2. Drain-Source Waveform Switching at Resonant Valley**

At this voltage valley, the FET suffers from the lowest possible turn-on switching power loss as described using Equation 3:

$$P_{LOSS,\,TURN-ON-ENERGY} = E_{COSS} \times f_{SW} = \frac{1}{2} C_D \times V_{VALLEY}^2 \times f_{SW} \quad (3)$$

where

- $C_D$ is the lumped capacitance at the switching node, consisting of FET output capacitance, transformer interwinding capacitance, and parasitic board capacitance
- $V_{Valley}$ is the drain-source voltage when the FET turns on
- $f_{sw}$ is the switching frequency

The minimum valley at which the converter can switch is given with Equation 4:

$$V_{VALLEY,MIN} = V_{IN,DC} - N_{PS} \times V_{OUT} = \sqrt{2} \times V_{AC} - N_{PS} \times V_{OUT} \quad (4)$$

Equation 4 illustrates that the $V_{VALLEY,MIN}$ reaches zero volts when the rectified input voltage, $V_{IN,DC}$, is equal to or less than the reflected voltage, $N_{PS} \times V_{OUT}$. Hence, the quasi-resonant converter operates with zero-voltage switching under conditions when the input voltage is low and the reflected voltage is high, meaning that device losses are only conduction-dominated.

## 3.2 Transformer Design

The benefit of GaN is the capability of higher switching frequency with lower losses. To improve the overall efficiency for high-density designs, the transformer design plays a key role.

The worst-case system efficiency occurs at the lowest input voltage condition of 90 $V_{AC}$. For a flyback topology, the main switch turns on to store energy in the magnetized inductance ($L_{MAG}$), and transfers the energy to the output when the device turns off. During the demagnetizing period, the secondary winding is clamped to the output voltage, $V_{OUT,}$ and the reflected voltage $V_{RF}$ from secondary to primary is calculated using Equation 5:

$$V_{RF} = V_{OUT} \times N_{PS} \quad (5)$$

where

- $N_{PS}$ is the turn ratio between primary and secondary

Equation 6 calculates the maximum duty cycle:

$$D_{MAX} = \frac{V_{RF}}{V_{DC\_MIN} + V_{RF}} \quad (6)$$

where

- $V_{DC\_MIN}$ is the minimum DC voltage at lowest AC input voltage condition

For the operation of QR flyback, the main device turns on after the magnetizing energy is discharged and the switch node voltage resonates to the lowest point. This means that the switching FET turns on with Zero Voltage Switch (ZVS) if $V_{RF} > V_{DC}$ and the conduction loss dominates the overall efficiency.

Suppose the running frequency, $f_{RUN\_MIN}$ is the minimum frequency at $V_{DC\_MIN}$, and the primary inductance of the transformer, $L_P$ is calculated with Equation 7:

$$L_P = \frac{(V_{DC\_MIN} \times D_{MAX})^2 \times \eta}{2 \times f_{RUN\_MIN} \times P_{OUT}} \quad (7)$$

where

- $P_{OUT}$ is the output power and η is the efficiency of the system

At this condition, the peak current, $I_{PK\_MAX}$ is found using Equation 8:

$$I_{PK\_MAX} = \frac{2 \times P_{OUT}}{V_{DC\_MIN} \times D_{MAX} \times \eta} \quad (8)$$

The primary RMS current, $I_{RMS}$ is determined with Equation 9:

$$I_{RMS} = \sqrt{\frac{D_{MAX}}{3}} \times I_{PK\_MAX} \quad (9)$$

These calculations show that, for a fixed output power, the conduction loss of the device depends on $V_{DC\_MIN}$ and $D_{MAX}$, which is only related to the turns ratio, $N_{PS}$. In summary, for a QR flyback design, the worst case is at the lowest AC input voltage. Under this condition, the switching device turns on with ZVS, which means conduction loss dominates the system losses, but these losses are related to the turns ratio only. In other words, a higher turns ratio leads to lower $I_{RMS}$. The loss on the switching device is fixed.

To facilitate the discussion on selection of switching frequency, Equation 7 can be re-written as:

$$L_P \times f_{RUN\_MIN} = \frac{(V_{DC\_MIN} \times D_{MAX})^2 \times \eta}{2 \times P_{OUT}} \quad (10)$$

The above shows higher frequency leads to lower a inductance value. In the transformer design, the flux density must be minimized to prevent saturation of the ferrite core. The maximum flux density, $B_{MAX}$ is found using Equation 11:

$$B_{MAX} = \frac{L_{MAG} \times I_{PK\_MAX}}{AE \times N_P} \quad (11)$$

where

- $A_E$ is the effective area of the ferrite core which depends on the core shape
- $N_P$ is the number of turns on the primary winding

From Equation 11, if $B_{max}$ and $A_E$ are held constant, the higher running frequency leads to a lower $L_{MAG}$ value with lower turns of winding. In this case, Litz wire can be used with more strands to reduce the copper loss to achieve better efficiency and thermal result.

In this reference design, the turns ratio is chosen to be 32:5 with a split primary winding method to minimize the leakage inductance. The primary winding is 0.1 mm × 15P Litz wire and the secondary winding is 0.05 mm × 320P triple isolation Litz wire.

### 3.3 GaN FET Switching Device

As the quasi-resonant converter is designed to minimize the transformer size with high switching frequencies, the switching device must be able to support high-frequency operation without suffering major additional power loss penalties.

There are two types of losses that must be considered when making the selection for the switching device: frequency-dependent *switching losses*, and current-dependent *conduction losses*.

In the quasi-resonant flyback application, the main component of the switching loss can be attributed to the turn-on stored energy loss, as described by using Equation 12:

$$P_{LOSS,\,TURN-ON-ENERGY} = = \frac{1}{2} C_D \times V_{VALLEY}^2 \times f_{SW} \quad (12)$$

Here, the $C_D$ term is highly-dependent on the output capacitance of the switching device. The LMG3624 integrated GaN FET is chosen to optimize for this switching loss, considering that the effective output capacitance, $C_{OSS}$, is drastically lower than a counterpart Silicon FET with a similar on-resistance.

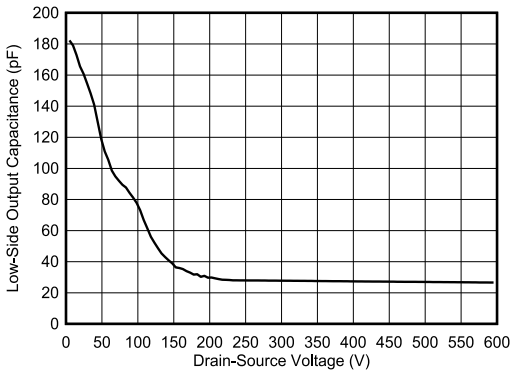



**Figure 3-3. LMG3624 $C_{OSS}$ vs $V_{DS}$ Characteristic**

Figure 3-3 shows the $C_{OSS}$ vs $V_{DS}$ characteristic for the LMG3624 device.

When switching from 400 V to 0 V, the effective energy-related output capacitance , $C_{O,ER}$of the device is only *29 pF*. Using Equation 12 and assuming $f_{SW}$= 150 kHz, this value of $C_{O,ER}$ yields a turn-on stored energy loss of 348 mW, or roughly 0.53% of the system efficiency. In practice, the design is switching lower than 400 V, due to the valley-switching operation, yielding higher power-loss savings.

The conduction loss component can be calculated with Equation 13:

$$P_{CONDUCTION} = I_{RMS}^2 \times R_{DS(on)} \quad (13)$$

where

- $I_{RMS}$ is the RMS current through the GaN device (1.2 A)
- $R_{DS(on)}$ is the on-resistance (170 mΩ)

In this 65-W application, the worst-case conduction loss at the 90 $V_{AC}$ input comes out to be 261 mW, or 0.40% of the system efficiency

When the main components of the switching loss and conduction loss are considered, the GaN device contributes less than 0.9% of the entire system losses, enabling a simple thermal design and a high system efficiency.

### 3.4 Current Sense Emulation Resistor

The current-sense resistor $R_{CS}$ is determined after initially calculating a value for a traditional current-sense resistor, $R_{CS(trad)}$. An initial value for $R_{CS(trad)}$ can be selected with considerations for the feedback voltage and other gain factors in the feedback loop as explained by Equation 14:

$$V_{FB} = K_{FB} \times I_{PK} \times R_{CS(TRAD)} \quad (14)$$

where

- $V_{FB}$ is the feedback voltage input to the controller
- $K_{FB}$ is a generic variables to account for additional gains in the feedback loop
- $I_{PK}$ is the peak current through the FET

$R_{CS}$ is then determined by solving for the traditional current-sense design resistance, $R_{CS(trad)}$, and multiplying by the inverse of $G_{CSE}$, the current sense gain, equal to 1,036 mA/A. The traditional current-sense design creates the current-sense voltage, $V_{CS(trad)}$, by passing the GaN power FET drain current, $I_D$, through $R_{CS(trad)}$. The LMG3624 creates the current-sense voltage, $V_{CS}$, by passing the CS pin output current, $I_{CS}$, through $R_{CS}$. The current-sense voltage must be the same for both designs.

$$V_{CS} = I_{CS} \times R_{CS} = V_{CS(trad)} = I_D \times R_{CS(trad)} \quad (15)$$

$$R_{CS} = I_D / I_{CS} \times R_{CS(trad)} = 1 / G_{CSE} \times R_{CS(trad)} \quad (16)$$

$$R_{CS} = 1{,}036 \times R_{CS(trad)} \quad (17)$$

# 4 Hardware, Testing Requirements, and Test Results

## 4.1 Required Hardware

### 4.1.1 Hardware

Figure 4-1 and Figure 4-2 show the TIDA-050072 boards with overall dimensions measuring 54 mm × 26 mm × 30 mm.

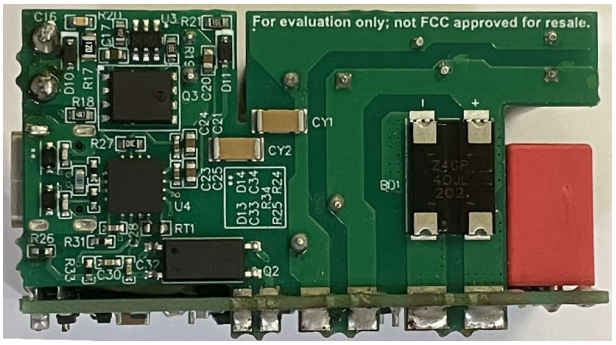



**Figure 4-1. TIDA-050072 Daughter Card View**

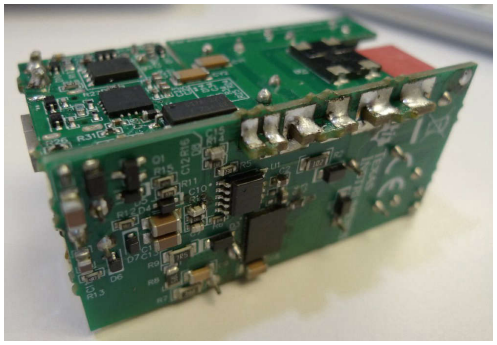


**Figure 4-2. TIDA-050072 Angled View**

### 4.1.2 Testing Equipment

The following test equipment is required when working with this reference design:

**Voltage Source:** Isolated AC source or variable AC transformer capable of 264 $V_{RMS}$ and capable of handling 100-W power level.

> **CAUTION**
> Do not apply DC voltage to this board when testing. Damage to equipment and components is possible.

**Voltmeter:** Digital voltage meter

**Power Analyzer:** Capable of measuring 1 mW to 100 W of input power and capable of handling 264-$V_{RMS}$ input voltage. Some power analyzers can require a precision shunt resistor for measuring input current to measure input power of 5 W or less. Read the user manual for the power analyzer for proper measurement setups for full power and for stand-by power.

**Oscilloscope:** 4-channel, 500-MHz bandwidth. Probes capable of handling 600 V.

**Load:** TIDA-050072 comes populated with a USB Type-C® PD controller and requires external connection through an onboard USB Type-C connector to a USB Type-C PD load to adjust the board output to obtain 5-V, 9-V, 15-V, or 20-V. A USB Type-C PD communicating load is required to make the board evaluation. An example of such a load is PM125, USB Power Delivery Tester and PassMark® Software. Without such a communication load, the board output USB Type-C connector does not provide a variable output voltage. To obtain the full load current 3.00-A from 5 V, 9 V, and 15 V, a standard USB Type-C cable can be used, but to obtain 3.25 A at 20-V output, an *E-marker* USB Type-C cable must be used. In case the EVM is desired to test on a load without USB Type-C PD communication, the output voltage can be obtained from C18 , but only 5 V and up to 3.00 A can be obtained.

## 4.2 Test Setup

This section describes the test setup of the reference design board.

**WARNING**

This reference design is not encapsulated and there are accessible voltages that are greater than 50 $V_{DC}$. Use appropriate handling precautions to avoid injury.

The AC input power goes through the power analyzer to support the reference design board. The output is taken from the USB Type-C receptacle to a USB Type-C load. The remote sense of the electronic load is connected to the output capacitor (C18) for accurate voltage measurement. See Figure 4-3for the test setup diagram.

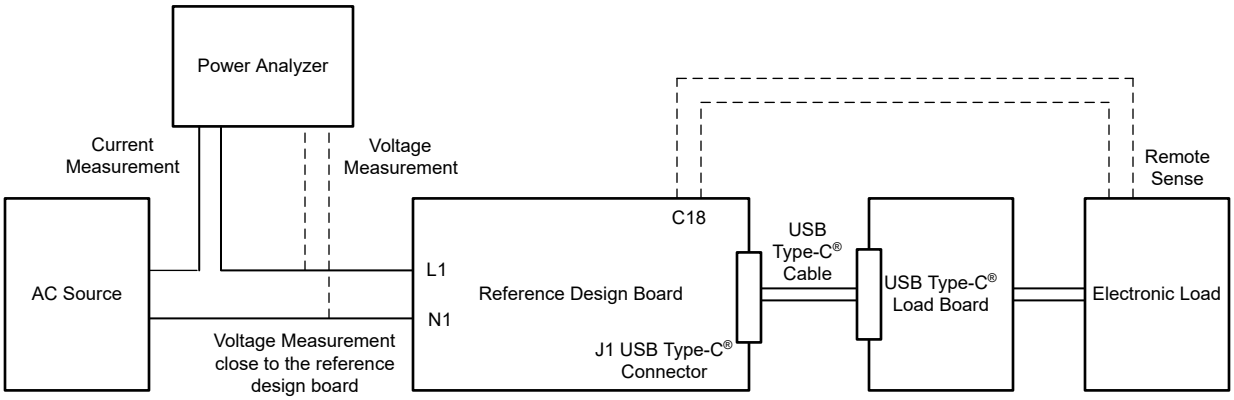



**Figure 4-3. Test Setup Diagram**

This reference design is a compact design without the use of any test points. The designer needs to connect the AC inlet on the L1 and N1 of the board close to F1 and CX1. L1 and N1 are the AC input connections and the voltage sense of power analyzer as shown in Figure 4-4. Place the voltage measurement of the power analyzer close to L1 and N1. When setting the input voltage range, check the power analyzer to get the right input voltage to reduce the effect of the AC cable drop. Read the input power with the average or integration function from the power analyzer.

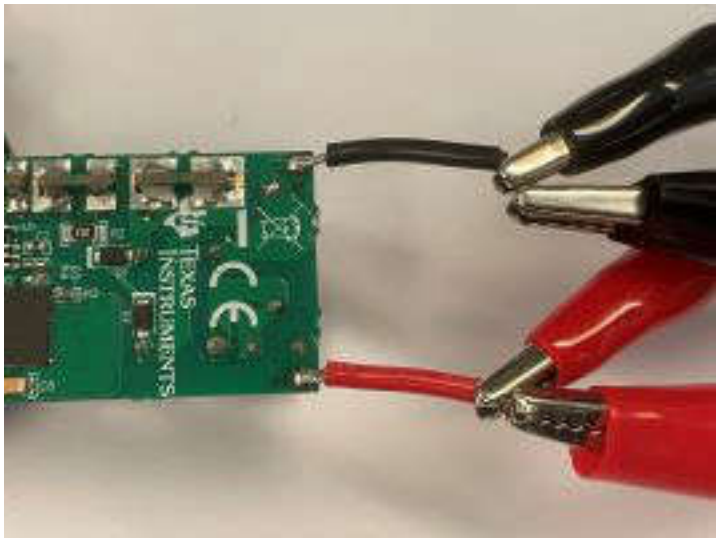


**Figure 4-4. Connection of AC Input**

For the output, use a USB Type-C cable from J1 connected to a USB PD load board, and then to the electronic load. As shown in Figure 4-5, the remote sense is connected to the terminals of C18 to reduce the loss of the output cable drop. Read the output power from the electronic load directly.

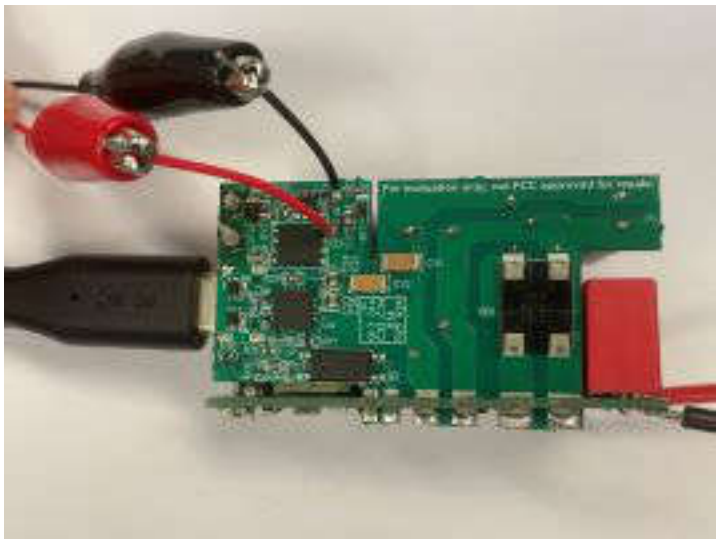


**Figure 4-5. Remote Sense Connection for Output**

## 4.3 Test Results

### 4.3.1 Efficiency Results

Figure 4-6, Figure 4-7, Table 4-1, and Table 4-2 show the efficiency data collected at 115 $V_{AC}$ and 230 $V_{AC}$ input. The setup described in the *Test Setup* section was used.

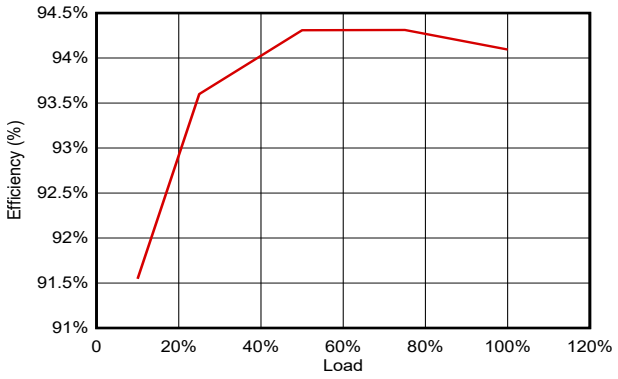



**Figure 4-6. 115 $V_{AC}$, 60 Hz Efficiency Across Load**

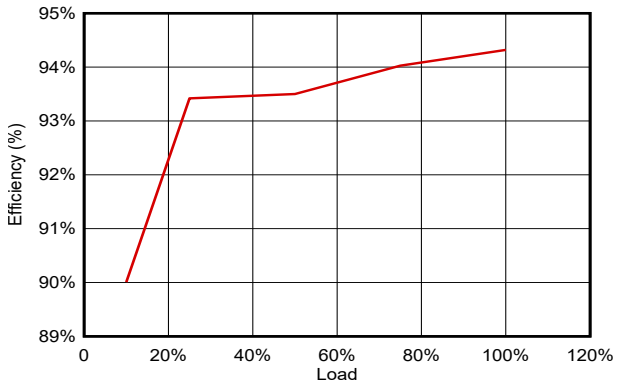



**Figure 4-7. 230 $V_{AC}$, 50 Hz Efficiency Across Load**

**Table 4-1. Efficiency at 115 $V_{AC}$, 60 Hz**

| LOAD | $V_{OUT}$ | $I_{OUT}$ | $P_{OUT}$ | $P_{IN}$ | EFFICIENCY |
|---|---|---|---|---|---|
| 100% | 20.133 | 3.2564 | 65.561 | 69.676 | 94.09% |
| 75% | 20.109 | 2.4306 | 48.877 | 51.825 | 94.31% |
| 50% | 20.074 | 1.6220 | 32.561 | 34.526 | 94.31% |
| 25% | 20.048 | 0.8120 | 16.278 | 17.391 | 93.60% |
| 10% | 20.034 | 0.3149 | 6.308 | 6.891 | 91.55% |
| Average | | | | | 94.08% |
| Standby Power | | | | | 29.498 mW |

**Table 4-2. Efficiency at 230 $V_{AC}$, 50 Hz**

| LOAD | $V_{OUT}$ | $I_{OUT}$ | $P_{OUT}$ | $P_{IN}$ | EFFICIENCY |
|---|---|---|---|---|---|
| 100% | 20.139 | 3.2550 | 65.552 | 69.501 | 94.32% |
| 75% | 20.111 | 2.4296 | 48.861 | 51.965 | 94.03% |
| 50% | 20.083 | 1.6200 | 32.534 | 34.796 | 93.50% |
| 25% | 20.055 | 0.8118 | 16.281 | 17.428 | 93.42% |
| 10% | 20.043 | 0.3148 | 6.310 | 7.011 | 90.01% |
| Average | | | | | 93.82% |
| Standby Power | | | | | 37.304 mW |

### 4.3.2 Thermal Results

Figure 4-8 through Figure 4-19 show the thermal captures of the system at full-load operation under various input voltage conditions. The soak-time was 30 minutes at an ambient temperature of 25°C. For mainboard images, Bx1 = LMG3624. For daughtercard images, Bx1 = SR controller, Bx2 = SR, Bx3 = diode bridge. For the top view images, Bx2, Bx3 = transformer.

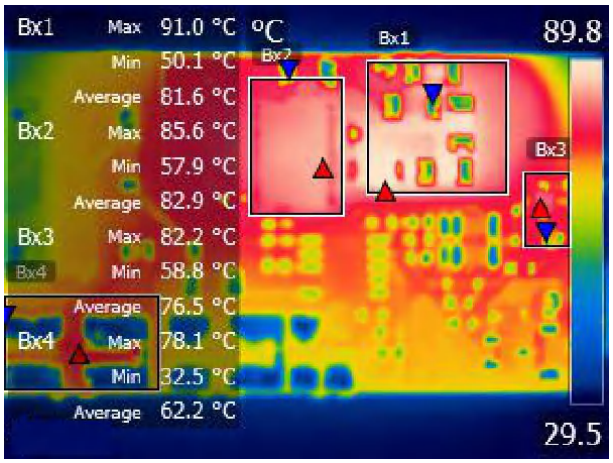



**Figure 4-8. $V_{IN}$ = 90 $V_{AC}$, Mainboard**

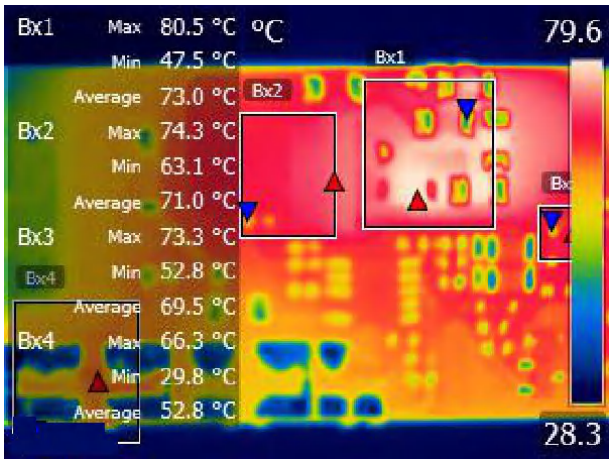



**Figure 4-9. $V_{IN}$ = 115 $V_{AC}$, Mainboard**

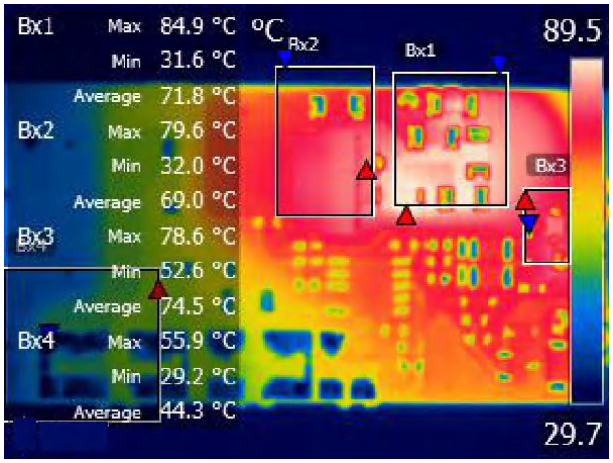



**Figure 4-10. $V_{IN}$ = 230 $V_{AC}$, Mainboard**

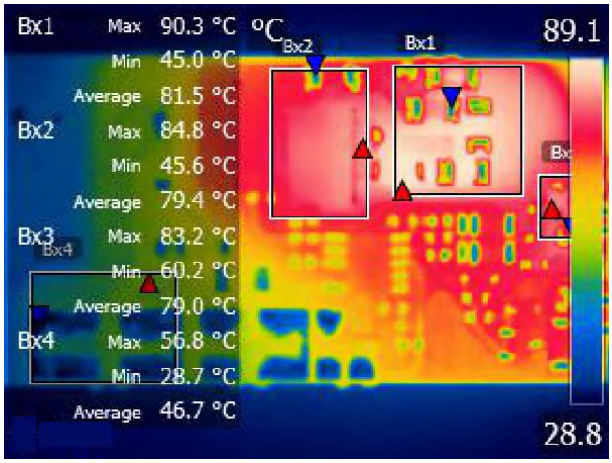



**Figure 4-11. $V_{IN}$ = 265 $V_{AC}$, Mainboard**

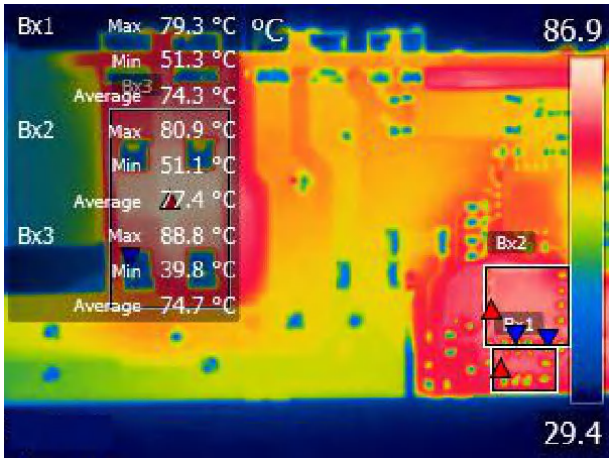



**Figure 4-12. $V_{IN}$ = 90 $V_{AC}$, Daughtercard**

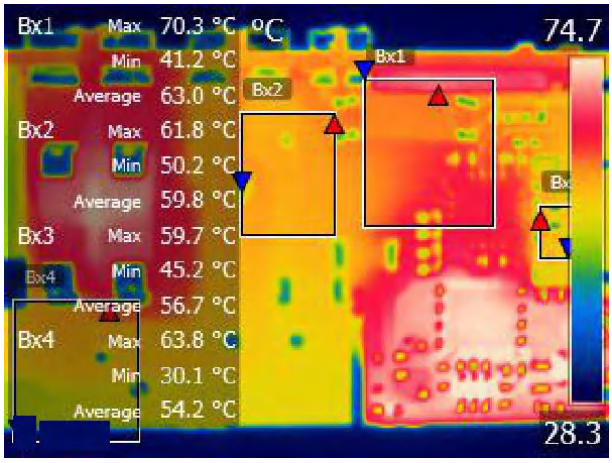



**Figure 4-13. $V_{IN}$ = 115 $V_{AC}$, Daughtercard**

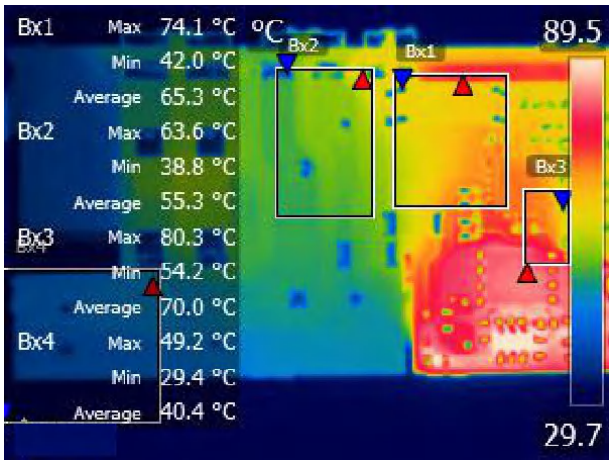



Figure 4-14. $V_{IN}$ = 230 $V_{AC}$, Daughtercard

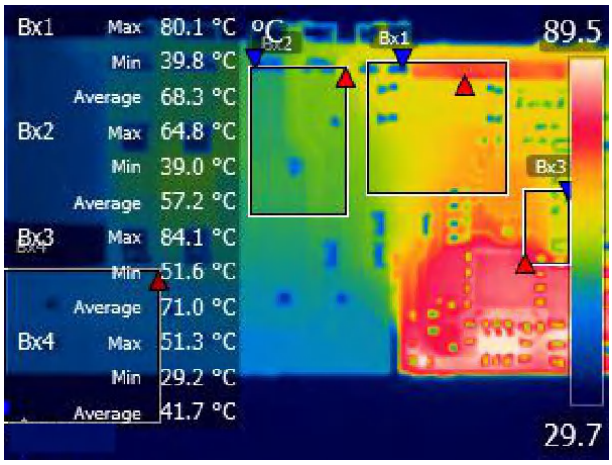



Figure 4-15. $V_{IN}$ = 265 $V_{AC}$, Daughtercard

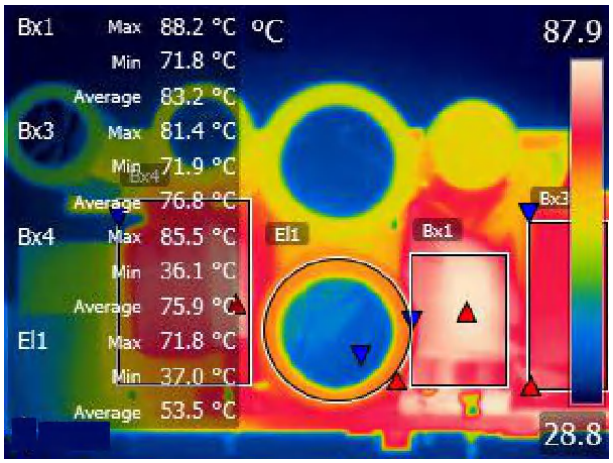



Figure 4-16. $V_{IN}$ = 90 $V_{AC}$, Top View

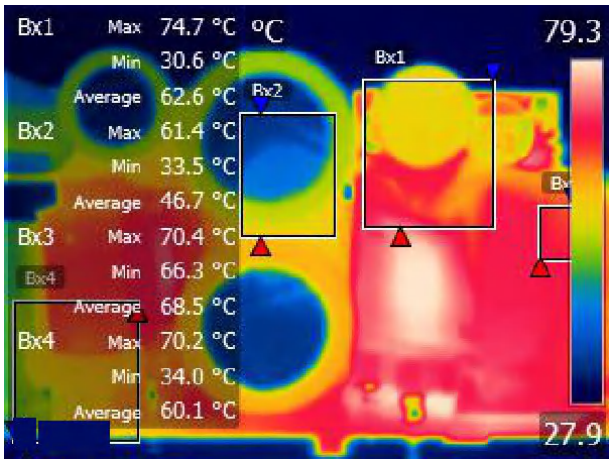



Figure 4-17. $V_{IN}$ = 115 $V_{AC}$, Top View

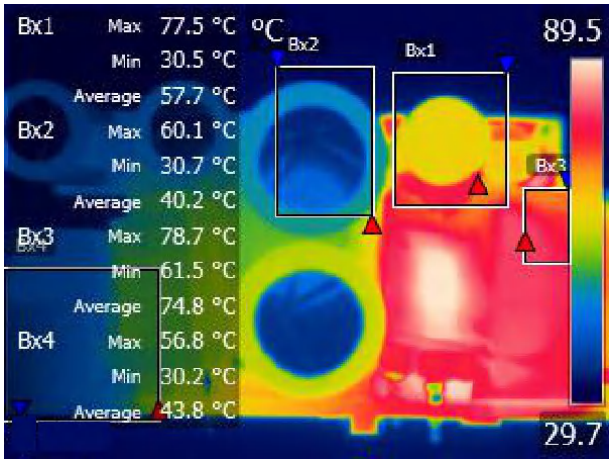



Figure 4-18. $V_{IN}$ = 230 $V_{AC}$, Top View

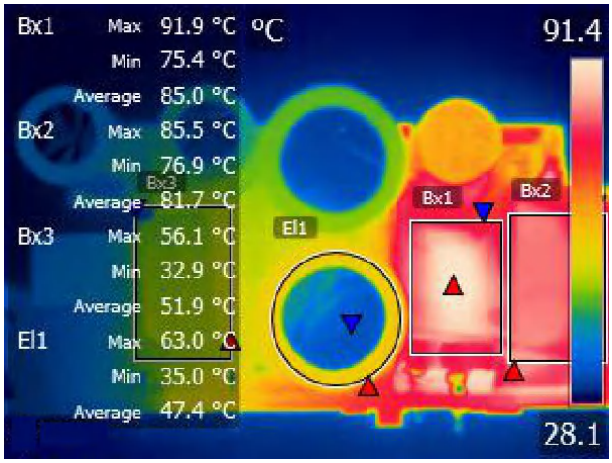



Figure 4-19. $V_{IN}$ = 265 $V_{AC}$, Top View

### 4.3.3 Switching Waveforms

Figure 4-20 through Figure 4-29 show the oscilloscope captures of the system switching waveforms under different input voltage and load conditions.

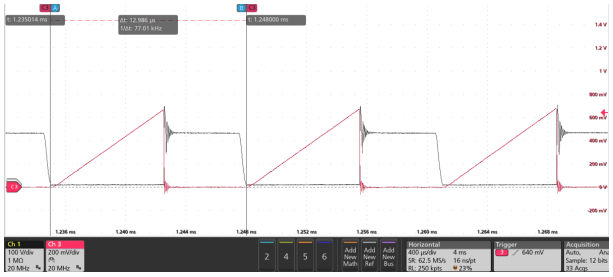


Figure 4-20. $V_{IN}$ = 90 $V_{AC}$, Output = 20 V / 3.25 A

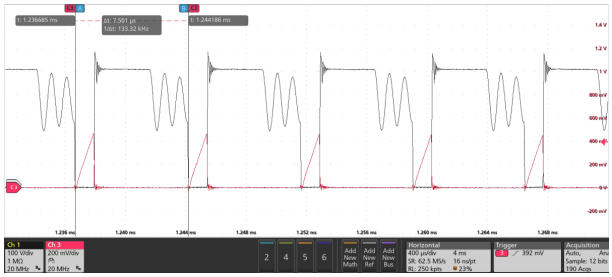


Figure 4-21. $V_{IN}$ = 264 $V_{AC}$, Output = 20 V / 3.25 A

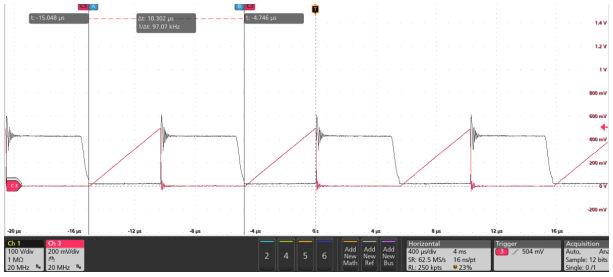


Figure 4-22. $V_{IN}$ = 90 $V_{AC}$, Output = 15 V / 3 A

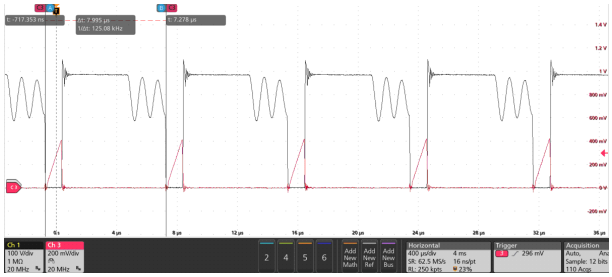


Figure 4-23. $V_{IN}$ = 264 $V_{AC}$, Output = 15 V / 3 A

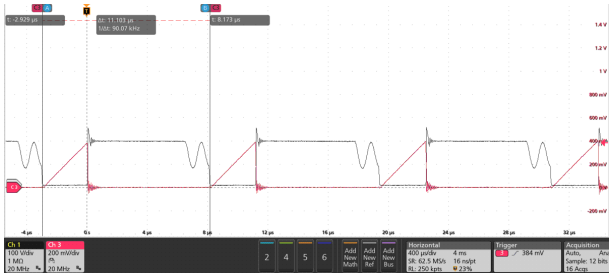


Figure 4-24. $V_{IN}$ = 90 $V_{AC}$, Output = 9 V / 3 A

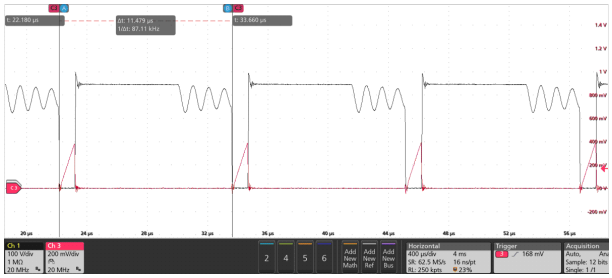


Figure 4-25. $V_{IN}$ = 264 $V_{AC}$, Output = 9 V / 3 A

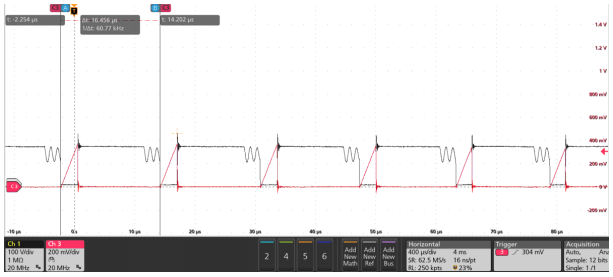


Figure 4-26. $V_{IN}$ = 90 $V_{AC}$, Output = 5 V / 3 A

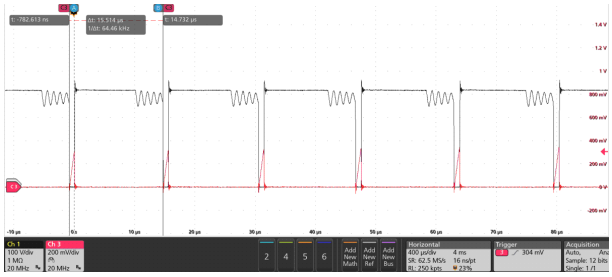


Figure 4-27. $V_{IN}$ = 264 $V_{AC}$, Output = 5 V / 3 A

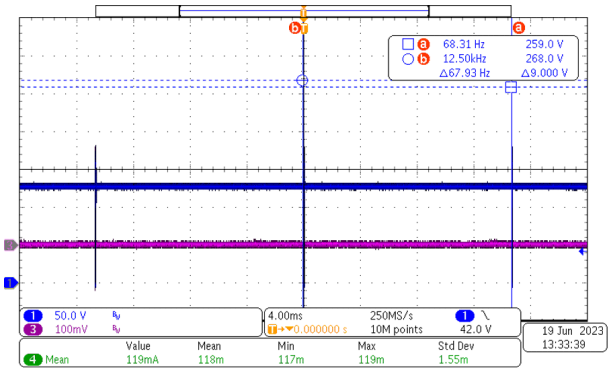



**Figure 4-28. $V_{IN}$ = 265 $V_{AC}$, Output = 0 W**

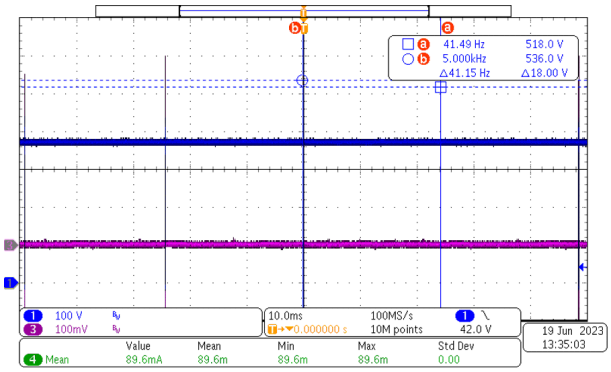



**Figure 4-29. $V_{IN}$ = 265 $V_{AC}$, Output = 0 W**

### 4.3.4 Switching Transients

Figure 4-30 through Figure 4-37 show the transient response from 10% load to 90% load at various output voltages. The transient duty cycle was set to 50% and the current slew rate was 2.5 A/µs.

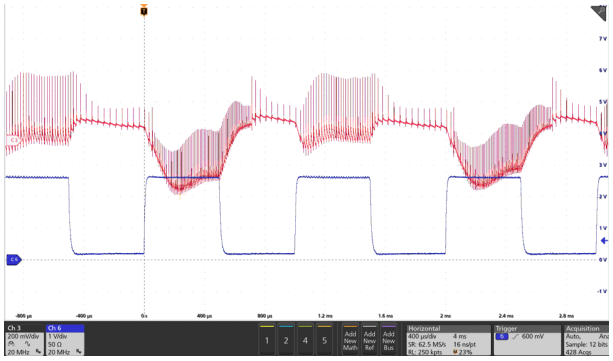


**Figure 4-30. Output = 20 V, $V_{IN}$ = 90 $V_{AC}$**

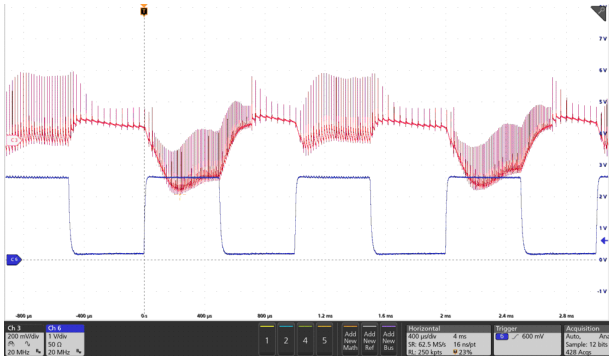


**Figure 4-31. Output = 20 V, $V_{IN}$ = 265 $V_{AC}$**

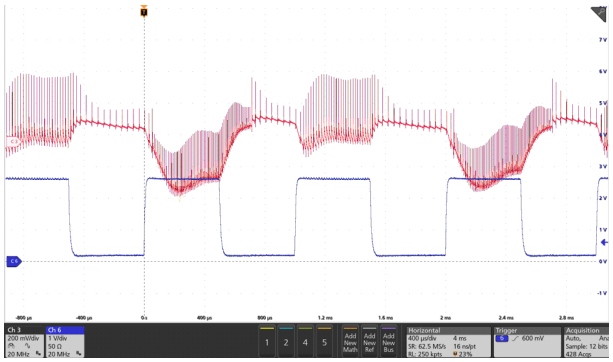


**Figure 4-32. Output = 15 V, $V_{IN}$ = 90 $V_{AC}$**

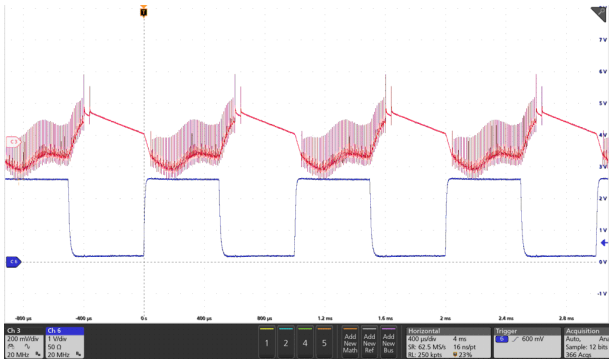


**Figure 4-33. Output = 15 V, $V_{IN}$ = 265 $V_{AC}$**

**Figure 4-34. Output = 9 V, $V_{IN}$ = 90 $V_{AC}$**

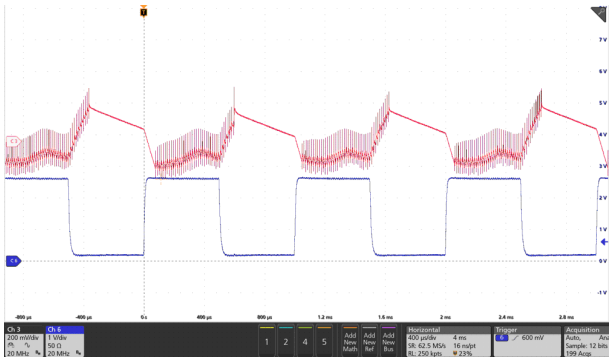


**Figure 4-35. Output = 9 V, $V_{IN}$ = 265 $V_{AC}$**

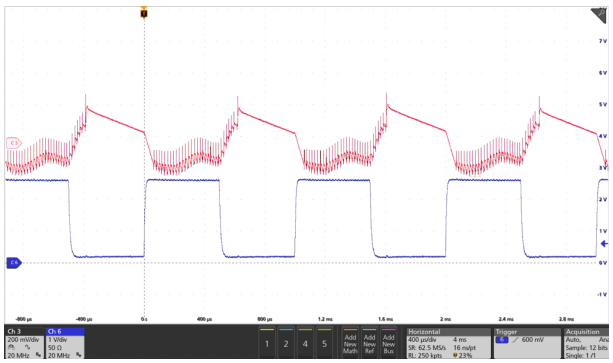


**Figure 4-36. Output = 5 V, $V_{IN}$ = 90 $V_{AC}$**

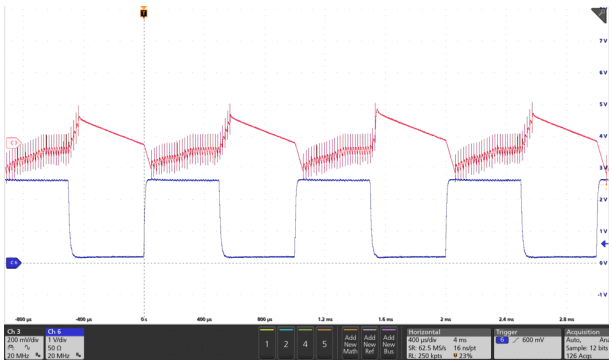


**Figure 4-37. Output = 5 V, $V_{IN}$ = 265 $V_{AC}$**

# 5 Design and Documentation Support

## 5.1 Design Files

### 5.1.1 Schematics

To download the schematics, see the design files at TIDA-050072.

### 5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050072.

## 5.2 Tools and Software

**Tools**

| | |
|---|---|
| LMG36XX-CALC | Quasi-Resonant Flyback Power Stage Design Calculator |

## 5.3 Documentation Support {Required Topic}

1. Texas Instruments, *LMG3624 650-V 170-mΩ GaN FET With Integrated Driver and Current-Sense Emulation* data sheet

## 5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 5.5 Trademarks

TI E2E™ are trademarks of Texas Instruments.
USB Type-C® is a registered trademark of USB Implementers Forum.
PassMark® is a registered trademark of PassMark Software Pty Ltd.
All trademarks are the property of their respective owners.

# 6 About the Author

**MARTIN HUANG** is an System-Applications Engineer for TI GaN.

**JOHN GOMEZ** is an Applications Engineer for TI GaN.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265