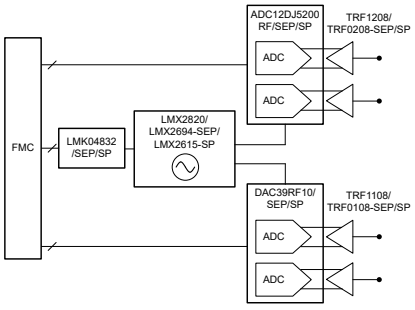
Design Guide: TIDA-010274

Space-Grade Discrete RF Sampling Transceiver Reference Design

Description

This reference design is a discrete RF sampling transceiver supporting instantaneous signal bandwidths up to 5GHz. The design utilizes -SEP (Space Enhanced Plastic) grade, radiation tolerant active devices designed for space applications. The receiver uses the ADC12DJ5200-SEP ADC (Analog-to-Digital Converter). The transmitter uses the DAC39RF10-SEP DAC (Digital-to-Analog Converter). The data converters support a variety of different JESD modes facilitating 1 or 2 output channels operating up to the lower part of X-band. The receiver includes the TRF0208-SEP active balun for transforming single-ended input to differential output. The transmitter includes the TRF0108-SEP active balun for transforming the differential output to single ended. The clocking design resides on a daughter-board that plugs into the top of the primary data converter board. The clock card includes the LMK04832-SEP for generating and distributing low frequency clock and reference signals to the synthesizer, data converters, and FPGA. The LMX2694-SEP RF synthesizer provides the 10GHz sample clock to the DAC and the 5GHz sample clock to the ADC. The power design resides on a daughter card that plugs into the bottom of the board and handles power distribution to all of the active devices on the board.



Resources

TIDA-010274	Design Folder
ADC12DJ5200-SEP	Product Folder
DAC39RF10-SEP	Product Folder
LMK04832-SEP	Product Folder
LMX2694-SEP	Product Folder
TRF0208-SEP	Product Folder
TRF0108-SEP	Product Folder
TPS7H4010-SEP	Product Folder
TPS7H1111-SEP	Product Folder
TPS7H1210	Product Folder

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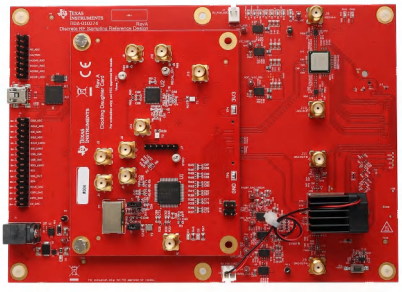
Features

- Up to 5GHz instantaneous bandwidth
- Operation up to X-band
- 10 / 5GHz clocking design
- Broadband active data converter interface
- Swappable clocking design
- Swappable power design

Applications

- Communications payload
- Radar imaging payload
- Command and data handling (C&DH)



1 System Description

Satellite payload applications related to communications and radar utilize wide instantaneous bandwidth signals to support large amounts of data. The applications require flexible, configurable solutions that can quickly reconfigure in different bands. For applications up to around 8GHz, the RF sampling architecture supports directly. For applications through Ka-band (27 - 40GHz), The RF sampling architecture is used as an IF stage to up/down convert to/from the higher frequency. These systems operate in Low Earth Orbit (LEO) applications and require radiation tolerant active devices.

1.1 Terminology

- ADC: Analog-to-Digital Converter
- DAC: Digital-to-Analog Converter
- NCO: Numerically Controlled Oscillator
- IF: Intermediate Frequency
- LO: Local Oscillator
- BW: Bandwidth

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of the reference design. Figure 2-2 shows the block diagram of the power design.

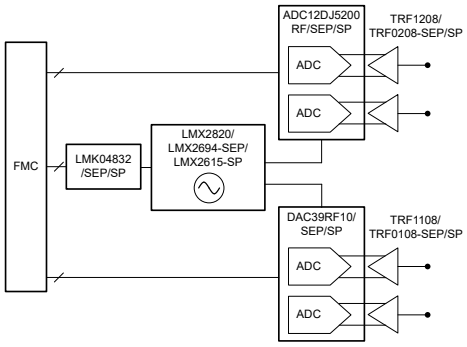


Figure 2-1. TIDA-010274 Block Diagram

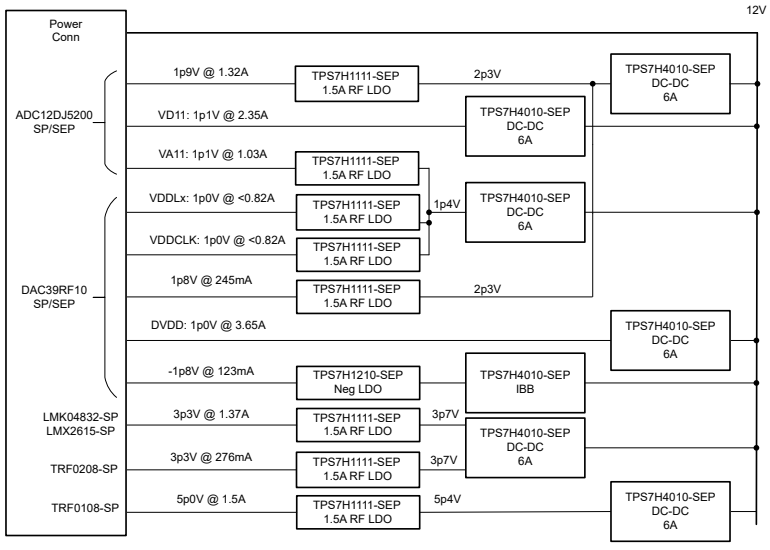


Figure 2-2. TIDA-010274 Power Block Diagram

2.2 Design Considerations

The design is centered on the discrete DAC and ADC devices that support wide instantaneous bandwidth signals. The receive channels utilize active baluns to convert single-ended inputs to differential outputs to interface with the ADC input. The transmit channels utilize a different active balun to convert the differential interface to single-ended. Because industrial, -SEP, and -SP grade parts related to the data converters and active baluns are all in plastic with the same pin-out, a single PCB design supports all grade flavors.

The clocking design is on a daughter card that snaps onto the top of the data converter board. The clocking daughter card houses the LMK04832-SEP and the LMX2694-SEP. The LMK provides a low frequency reference to the LMX synthesizer. The LMK also provides the low frequency clock signals for the FPGA and the SysRef signals to the data converters and FPGA to support the JESD204B digital interface protocol. The LMX2694-SEP provides the low phase noise, high frequency sampling clock to the data converters. Because both DAC an ADC clocks come from the same device, the ADC clock must be an integer divider of the DAC clock.

A power design is on a daughter card that snaps into the bottom of the board. The power board provides all the power rails for the DAC, ADC, clock chips, RF active baluns, and current sensors. The approach generally provides LDOs on the sensitive analog rails to maintain the best performance. DC-DC converter provide direct power to less sensitive digital rails.

2.3 Highlighted Products

2.3.1 DAC39RF10-SEP

The DAC39RF10-SEP is a radiation tolerant RF sampling DAC. The DAC39RF10-SEP supports a sampling rate up to 10.24GSPS. The DAC39RF10-SEP operates in a variety of JESD204B/C modes supporting wide instantaneous bandwidth up to 10GHz and wide freqeuncy of operation up to 10GHz. The device boasts very low phase noise performance. On-chip DDS function facilitates generating a CW tone without the need for an FPGA pattern generator.

2.3.2 ADC12DJ5200-SEP

The ADC12DJ5200-SEP is a radiation tolerant RF sampling ADC. The ADC12DJ5200-SEP supports a sampling clock up to 5.2GHz. In the nominal operating mode the ADC samples up to 5.2GSPS and has two outputs. With dual edge sampling (DES), the effective sample clock doubles (by using both falling and rising edge of the clock). In this mode, the device has only one channel output but supports 5GHz of instantaneous bandwidth. The device operates in a variety of JESD204B/C modes with a wide frequency of operation up to 8GHz.

2.3.3 LMK04832-SEP

The LMK04832-SEP is a radiation tolerant, high performance clock conditioner with JESD204B/C support. The LNK04832-SEP has 14 clock outputs configurable as clock or SysRef outputs and has two PLLs (Phased Locked Loops). The first PLL operates as a jitter cleaner to lock a localized low jitter reference source, like a VCXO, to a low frequency system reference. The second PLL locks the internal VCO (Voltage Controlled Oscillator) to the low jitter reference. The device supports dual PLL, single PLL, or clock distribution modes.

2.3.4 LMX2694-SEP

The LMX2694-SEP device is a radiation tolerant, low phase noise, wideband phase-locked loop (PLL) with an integrated voltage-controlled oscillator (VCO) supporting a frequency between 39.3MHz and 15.1GHz. The device has two outputs with independent output divider control.

2.3.5 TPS7H4010-SEP

The TPS7H4010-SEP is a radiation tolerant synchronous step-down DC/DC converter capable of driving up to 6A of load current from a supply voltage ranging from 3.5V to 32V. The device provides exceptional efficiency and output accuracy in a very small design size.

2.3.6 TPS7H1111-SEP

The TPS7H1111-SEP is a radiation tolerant low drop-out (LDO) regulator. The device can output up to 1.5A of current. The TPS7H1111-SEP is very low noise which makes the device an excellent choice to power sensitive analog and RF devices.

2.3.7 TPS7H1212-SEP

The TPS7H1210 is a radiation tolerant low drop-out (LDO) negative voltage regulator. The device can output up to 1.0A of current. The TPS7H1210 operates with a wide negative voltage input. The low noise output makes the device an excellent choice for sensitive analog and RF power rails.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

Evaluation of the reference design requires the following hardware.

- TIDA-010274 Reference Design Board
- TSW14J59EVM Rev B (or later)
- Agilent PSA E4445A Spectrum Analyzer or equivalent
- Rohde and Schwarz SMA100B Signal Generator or equivalent for input
- Signal Generator for 10MHz reference (optional)
- Fixed or variable attenuator
- TSW14J59 Power Supply (12V, 2A)
- TIDA-010274 Reference Design Power Supply (12V, 2A)

3.2 Software Requirements

Evaluation of the reference design requires the following software.

- TIDA-010274_GUI_v2p0 (or later)
- HSDC Pro GUI (5.0.3 or later)
- AMD Vivado: Xilinx_HW_Server_Win_2019.1_0524_1430
- TI JESD FW: j59_ui.exe

3.3 Test Setup

Figure 3-1shows a block diagram of the test set-up.

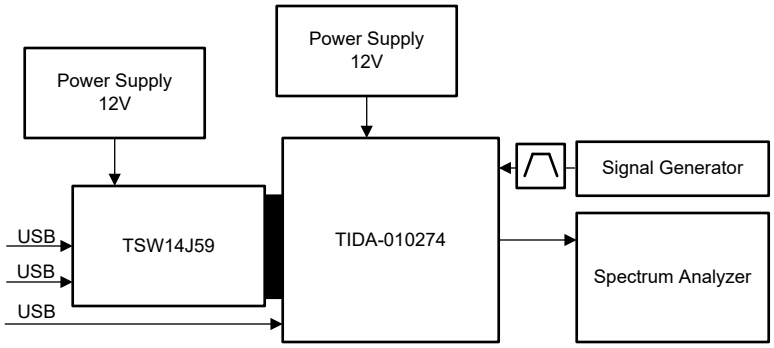


Figure 3-1. TIDA-010274 Test Set-up Block Diagram

3.4 Test Procedure

Initial Hardware Setup

- Connect TIDA-010274 Reference Design to 'J59 Pattern/Capture card
- Connect RF cable from DAC output J9 to ADC input J8 through 20dB attenuator
- Connect 10MHz reference to connector J5 on the clocking board (optional)
- Connect both USB cables to 'J59; connect USB cable to TIDA-010274
- Connect 12V supply to 'J59; confirm current limit is set to 2A or higher
- Connect 12V supply to TIDA-010274; confirm current limit is 2A or higher
- Connect Spectrum Analyzer to J11 to monitor DAC output (optional)

Initial Power Up

- Engage 12V supply for 'J59
- Engage 12V supply for TIDA-010274; expect initial current to be 0.85A

Initial Software Setup

- Launch HSDC Pro GUI version 5.3.03 or later
  - Select Device: ADC

  - Set ADC Output Data Rate to: 10G
- Launch j59_ui. gui
  - Verify software connects to 'J59 board

Software Execution

- Launch TIDA-010274 GUI
- Select / verify Case0 is selected for wideband mode
- On TIDA-010274 GUI: Press Run button
  - Verify comm error indicator is not on;
  - If so, re-run and/or check the USB connections and power to the device.
  - Verify current increases to 1.8A
  - Verify current monitor indicates DAC power at 3.3W and ADC power at 3.8W

Transceiver Capture Procedure

- On j59_ui.exe: Run script file "Master Transceiver"
- Wait for code script to load pattern, capture data, and transfer to HSDC Pro
- Verify FFT capture display on the HSDC Pro GUI

3.5 Test Results

The test signal is a wideband OFDM (Orthogoanl Frequency Division Multiplexed) modulated signal operating at a 5GSPS data rate. The patterns are configured with a 2GHz and 4GHz signal bandwidth. Figure 3-2 and Figure 3-3 show the spectrum performance out of the transmitter.

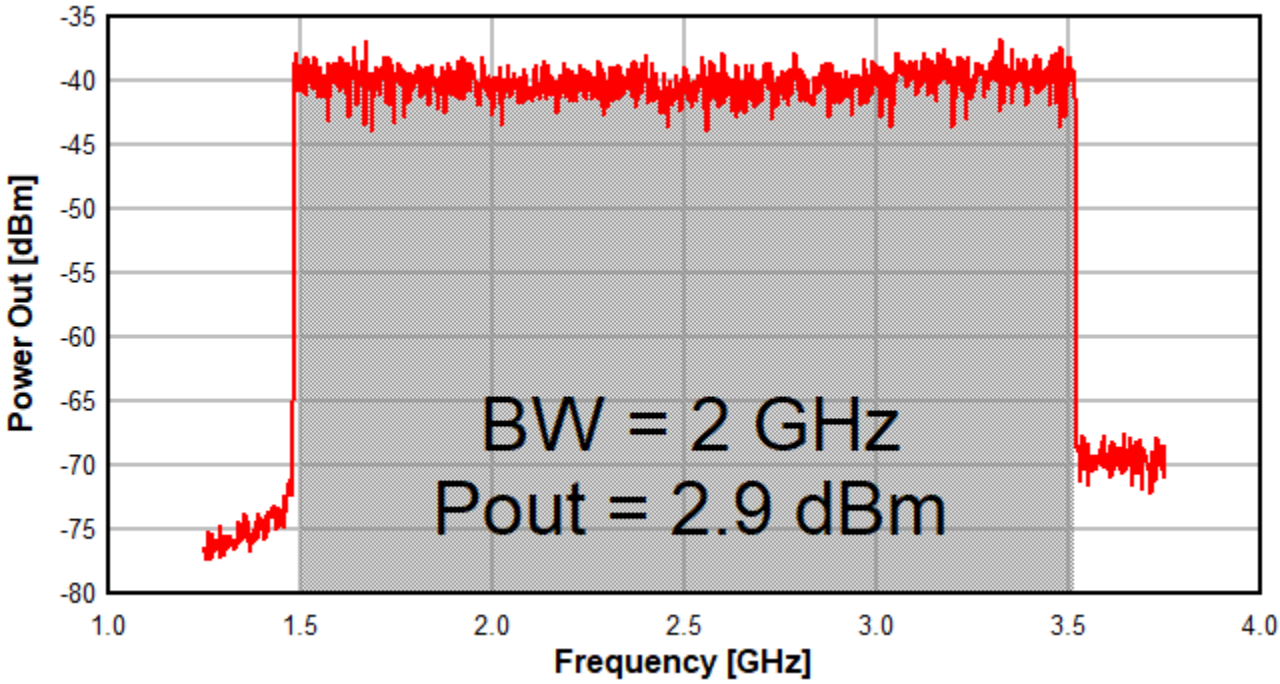


Figure 3-2. DAC Output With 2GHz Wide OFDM Signal

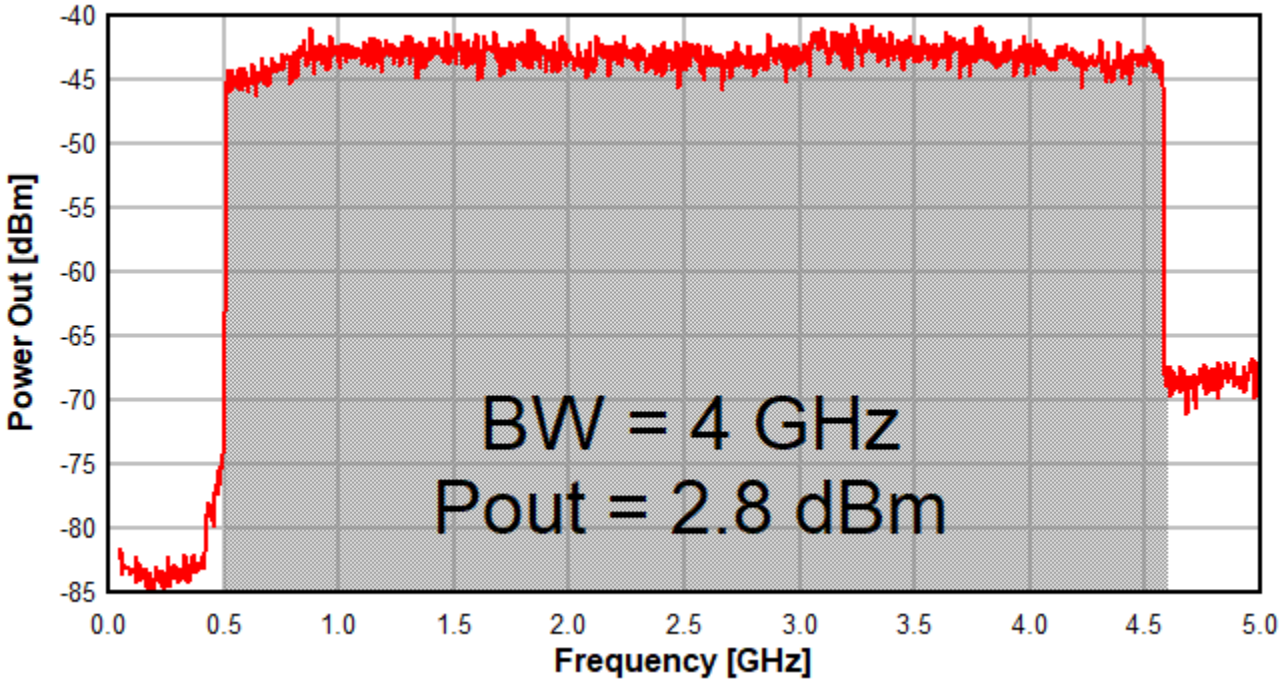


Figure 3-3. DAC Output with 4GHz Wide OFDM Signal

The modulated output signal is looped back to the transmitter through a 20dB attenuator to maintain that the receiver is not over-driven. Figure 3-4 and Figure 3-5 show the FFT spectrum of the captured waveform from the receiver.

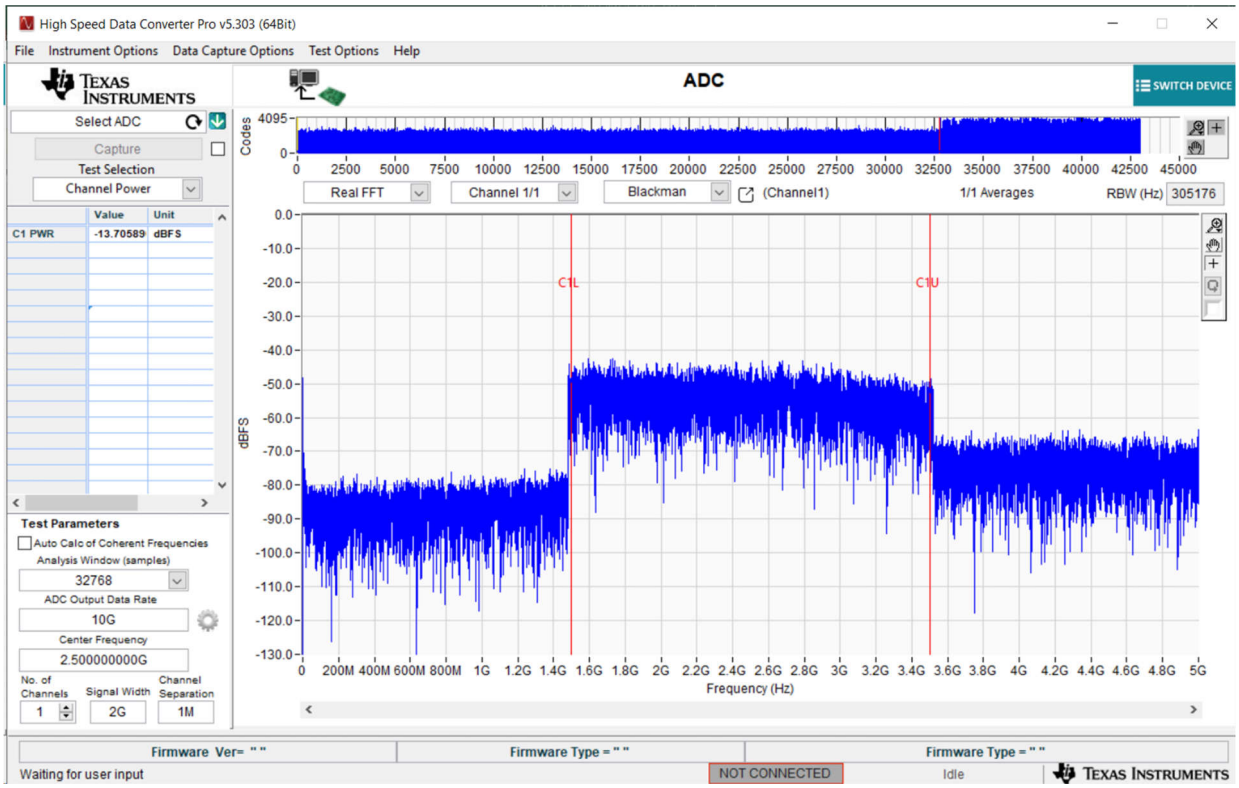


Figure 3-4. ADC Capture of 2GHz Wide OFDM Signal (Loopback)

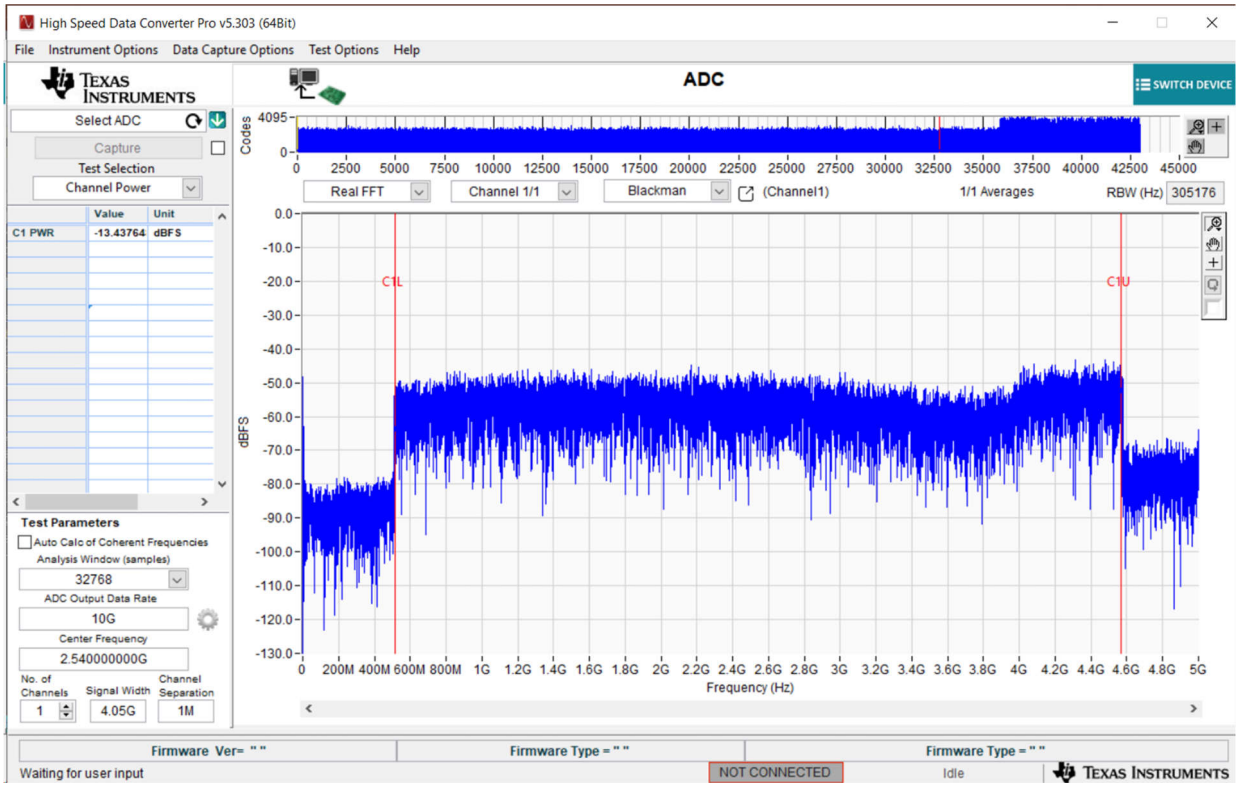


Figure 3-5. ADC Capture of 4GHz Wide OFDM Signal (Loopback)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010274.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010274.

4.2 Tools and Software

Tools

TSW14J59	JESD204B/C Pattern/Capture Card

Software

HSDC Pro	TSW14J59 GUI
TIDA-010274_GUI_v2p0	TIDA-010274 Programming GUI (version 2.0 or later)

4.3 Documentation Support

1. Texas Instruments, *DAC39RF10, DAC39RFS10 10.24, 20.48-GSPS, 16-bit, Dual and Single Channel, Multi-Nyquist Digital-to-Analog Converter (DAC) with JESD204B, C Interface Data Sheet*
2. Texas Instruments, *ADC12DJ5200-SEP 10.4-GSPS Single-Channel or 5.2-GSPS Dual-Channel, 12-bit,RF-Sampling Analog-to-Digital Converter (ADC) Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

Russell Hoppenstein is a system engineer in the System Engineering Marketing (SEM) group supporting the Aerospace and Defense sector. He has over 20 years of semiconductor experience working with high-performance RF devices and RF sampling data converters for the communication and defense markets. He previously designed RF transceivers, active antenna systems, and linearized power amplifiers for the wireless infrastructure market. Russell earned his BSEE from the University of Texas at Austin and his MSEE from University of Texas at Arlington.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2024) to Revision A (May 2024)	Page
• Updated block diagram	1

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