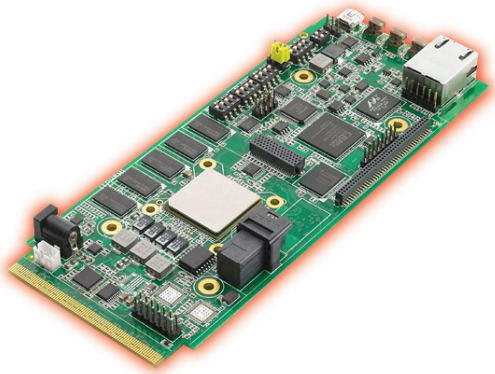
KeyStone Multicore DSPs for High-Performance Radar and Avionic Systems

Texas Instruments

Many of today's radar, military telecom and avionics systems require high complexity within a constrained size, weight and power (SWaP). These systems are signal processing intensive and heavily rely on the efficient implementation of digital signal processing algorithms.

The rapid move to new waveforms, video standards, and higher network densities requires flexible programmable implementations. The ability to provide field upgrades or configurability is critical for the next generation of radar, military telecom and avionics systems.

Texas Instruments' multicore processors offer the high-performance processing capabilities that these applications require, with full programmability and compelling performance per watts. In production now are TI's TMS320C6678 and TMS320C6657 DSPs, based on TI's KeyStone architecture, which are available on multiple COTS formats like PCIe, AMC, 3U VPX, XMC, and ATCA. To ease development, TI also offers a low-cost Evaluation Module (EVM) that includes a Multicore Software Development Kit (MCSDK) and Code Composer Studio integrated development environment, allowing programmers to quickly come up to speed on the devices (see Figure 1).



▲ *Figure 1. Low cost multicore evaluation module (EVM).*

The 66AK2H12 System-on-Chip (SoC) based on TI's Keystone II architecture is now sampling and features the industry's first, infrastructure-class, quad ARM® Cortex™-A15 MPCore™ processor cluster. The 66AK2H12 also features eight TMS320C66x TI DSP cores and multiple high-speed SERDES interfaces. This device allows for new, optimized embedded processor architectures to be designed for this market.

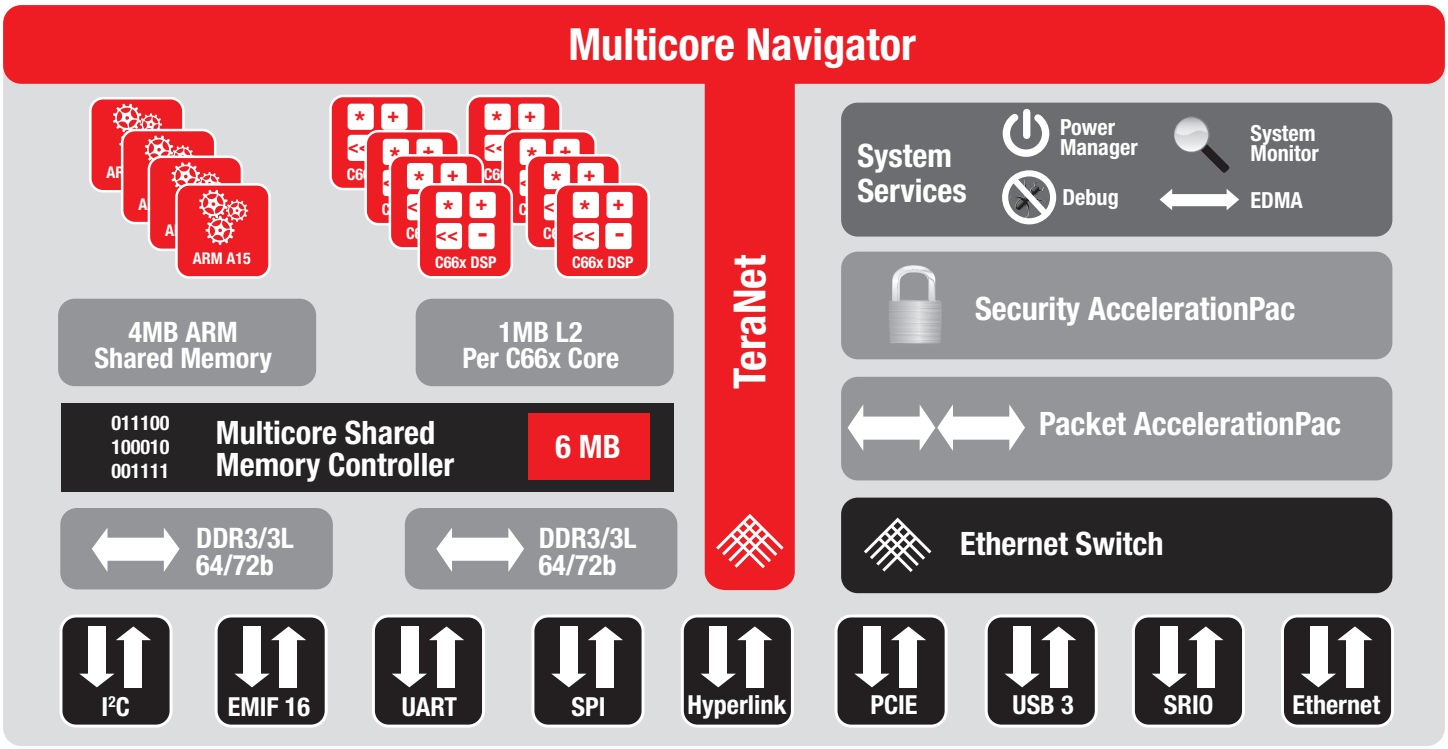
Floating point and Accelerators

As signal processing requirements continue to increase in waveform-intensive applications like sonar, radar, signals intelligence (SIGINT) and software defined radio (SDR), the use of multiple digital signal processor (DSP) cores is a key enabler, offering unmatched GFlops/W performance. Each C66x core provides up to 20 GFlops of single-precision IEEE floating point performance and up to 5 GFlops of native, IEEE double-precision performance. Multicore further enables these applications with the increased performance of multiple cores while keeping the power at acceptable levels.

The ability to support native floating point operations is another key advantage of TI's Keystone devices. Previously most, multicore, high-end digital signal processors focused mainly of fixed-point performance which did not meet the requirements of the radar and avionics markets. Floating point processors enable higher dynamic range and increased precision which fixed-point processors cannot achieve easily. Since the C66x core supports both fixed and floating point precision, designers can choose which format best suits their system (or algorithm) and dynamically switch back and forth as well.

Dedicated accelerators also play a role in boosting the overall efficiency of a system designed with the KeyStone architecture. In addition to the DSP performance, the TMS320C6657/55 features a Viterbi CoProcessor (VCP) and Turbocode Decoder CoProcessor (TCPd) accelerators for speeding up the forward error correction used in communications systems. These accelerators operate independently to minimize DSP use and reduce latencies. While developers take advantage of these accelerators, the DSP core is free to perform other signal processing.

TI's TMS320C6657 is based on 40-nm process technology and delivers up to 80 GMACs and/or 40 GFLOPs at 1.25 GHz. TI's TMS320C6678 is based on 40-nm process technology and delivers up to 320 GMACs and/or 160 GFLOPs at 1.25 GHz. TI's 66AK2H12 is based on 28nm process technology and delivers up to almost 200 GFLOPS at 1.25 GHz.



▲ *Figure 2. TI's 66AK2H12 system-on-chip*

Providing the right mix of I/O bandwidth

Mission critical-based applications also require a great deal of high-speed interoperability with equipment and devices from other multiple vendors and with currently deployed legacy equipment. Data transfers between sensor equipment and signal processing units is high in many of these applications. TI's KeyStone architecture has a high-performance peripheral set with everything needed to develop a robust avionic, radar, or SDR system. The peripherals include:

- PCI Express port with two lanes supporting GEN2 up to 5 GBaud per lane
- Four lanes of Serial RapidIO® (SRIO), compliant with RapidIO 2.1 spec for up to 5-Gbps operation per lane
- Hyperlink supporting up to 50 GBaud direct connection with other KeyStone devices
- Gigabit Ethernet (GbE) port or switch depending on the device with one or more SGMII ports, each supporting up to 1000Mbps
- 32-bit and 64-bit DDR3 with ECC interfaces at up to 1,333 MHz speed
- 16-bit external memory interface (EMIF) for connecting to flash memory (NAND andNOR) and asynchronous SRAM

SRIO, PCIe, and Hyperlink all provide the high-speed interconnects between multiple DSPs and/or FPGAs. The Hyperlink interface, supporting up to 50 Gbps, provides a point to point high speed interconnect that offers low protocol and high-speed communication and connectivity to other KeyStone devices or FPGA. FPGA IP cores are also available for this interface. All told, TI's KeyStone devices provide a scalable solution that meets the needs of today's radar, SDR, and avionics systems.

66AK2H12 SoC offers new architecture possibilities

The quad Cortex-A15 processor cluster on the 66AK2H12 allows efficient systems to be built without the need for a separate host processor (see figure 2). With full support of Linux (both commercial and open) the 66AK2H12 allows existing code to be ported simply and easily to the new SoC. The processing power of the DSPs can then be easily accessed using standard multicore programming protocols such as OpenMP and OpenCL, both of which are supported on TI processors. In addition, the quad Cortex-A15 cluster can run full networking and protocol stacks taking advantage of the on-board network coprocessors.

The combination of the Cortex-A15 processors and C66x DSPs will allow a new generation of solutions with unmatched performance at equivalent power, size and area levels for the mission critical market.

For more information about TI's KeyStone-based DSPs and SoCs, please visit **www.ti.com/multicore.**

Get Started Quickly with TI Software Tools and Optimized Codecs

- Multicore Software Development Kit (MCSDK)
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