Power Supply Design Seminar

Accelerating Power-Supply Compliance to Specification

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Accelerating Power-Supply Compliance to Specification

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ABSTRACT

Efficient and reliable power conversion is the foundation for everything electronic today. From automobiles to mobile phones and everything in-between, power electronics drives our world. Developing an efficient and reliable power converter necessitates a systemic understanding of the complexities of power electronics and the system-level design considerations for which the power converter is being designed. Equipped with this knowledge, mathematical models and/or simulations can help achieve a comprehensive understanding of the circuit under nominal and worst-case conditions. This topic offers a practical approach for advancing a power-supply design through SPICE-based power-supply analysis and advanced measurement techniques.

I. Converter Specification and Analysis

A. Specifying Circuit Behavior

Regardless of complexity, writing a power-supply specification is the essential first step to advancing a robust design. From three-terminal linear regulators to complex switching regulators, the specification sheet should detail the design requirements throughout the product lifetime – a design affected by layout, packaging, component selection, interconnects, environment and more.

Table 1 lists the typical design objectives in a power-supply worst-case circuit analysis (WCCA), a rigorous approach to verifying functional reliability through comprehensive mathematical- and simulation-based analysis. A WCCA encompasses not only the obvious considerations but more subtle behavior influenced by circuit and component impedances.

Although a power converter typically regulates output voltage, power or current, it is circuit impedance that you are controlling. Transient response, electromagnetic compatibility (EMC) and input/output stability are a few foundational power-supply considerations strongly influenced by circuit impedance, both controlled and parasitic. Thus, my topic focuses heavily on understanding and quantifying circuit and component impedances and their effect on power-supply operation.

Specifications Design Objectives	Analysis Method
Gain/Phase Margin, Input/Output Impedance	SPICE
Conducted Susceptibility	SPICE
Input Conducted Emissions	Math
Input Filter – Damping, Attenuation	SPICE
UVLO Threshold/Latch Off, No Oscillations	Math
Output Ripple	Math/ SPICE
Switching Frequency Tolerance/Sync	SPICE
Efficiency	Math/ SPICE
Primary Overcurrent Trip Thresholds	Math
Short-Circuit Analysis/Turn-Off – (Survival)	SPICE
Output Overvoltage	SPICE
Isolation Resistance and Capacitance	Math
Bus Off State Leakage Current	Math
Load Step (Natural and Forced Responses)	SPICE
Output Response Bus Transient	SPICE
On/Off Command Overshoot/Delay/Rise	SPICE
In-Rush/Out-Rush	SPICE
Gate Drive Analysis	SPICE
Magnetics Characteristics	Math
Power Sequencing	SPICE
Regulation	Math

Table 1 – Design specification checklist.

B. Circuit Analysis Options

To perform a successful power-supply analysis, you should be familiar with the subtleties of power converter design – control theory, EMC, component selection and component stress tolerance, to name a few. Figure 1 illustrates the speed of an analysis relative to the model abstraction level.

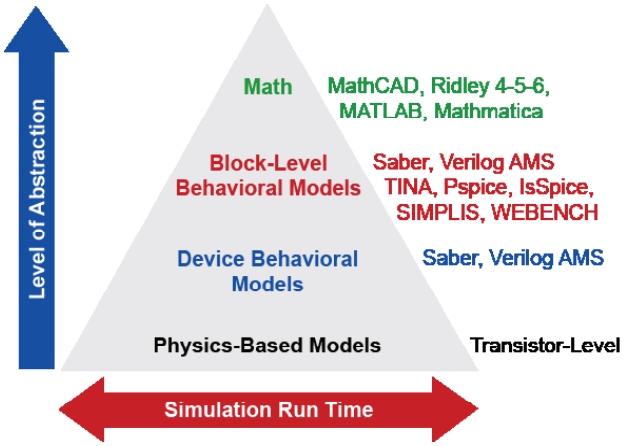

Figure 1 – Analysis run time vs. abstraction.

If a device or circuit model is built purely in mathematics, the abstraction level from physical behavior will be high and the analysis run time will be fast (not inclusive of the time to build the analysis), particularly when applied to switch-mode power conversion. In contrast, transistor-level simulations used in the design of integrated circuits reveal subtle circuit behavior over temperature and process, but the simulations can take hours and in some cases even days to complete.

To address long simulation run time at the circuit level, behavioral modeling has evolved to where transistor-level functionality is replaced with controlled voltage and current sources that define device behavior as logical and/or mathematical functions. These behavioral constructs – although abstractions themselves – can greatly simplify the development of complex device models and accelerate circuit development and simulation run time while also achieving excellent fidelity.

When analyzing complex or subtle circuit behavior, behavioral modeling coupled with targeted mathematical analysis offers the most comprehensive approach with which to execute a power-supply analysis. It should be emphasized that simulation is not a method for designing a power supply but rather a means of analyzing it. And although experienced designers may not want or need simulation, simulation tools today – along with the computers they run on – have evolved in ways that make it an efficient means of verifying a power-supply design [1].

Designers unfamiliar with simulation and the mathematics behind power conversion may rely on highly intelligent design synthesis and analysis tools. Design tools like Power 4-5-6 from Ridley Engineering, PowerESIM and Texas Instruments' WEBENCH® circuit designer help novice and experienced designers quickly develop power-supply solutions and analyze behavior without the burden of building a custom analysis.

These tools offer an effective means for starting a design, as they integrate many power-supply design considerations including stability, thermals, magnetic component selection, circuit board size and efficiency. However, even the best power-supply synthesis tools cannot anticipate all of the considerations and complexities of your design. As such, every design built in synthesis must be understood and validated on the bench before it is committed to production.

To summarize, a thoroughly specified, analyzed and tested power converter is the principle method of advancing a robust power converter.

C. To Simulate or Not to Simulate …

As Figure 1 illustrates, there are many simulation tools to choose from. However, your simulator "choice" may be mandated by the company you work for. Standardization within a company facilitates engineering collaboration and re-use, but with so many power-centric software tools available, this mandate can work against the power-supply designer. For example, SIMPLIS, IsSpice, PSIM and TINA are simulation tools that

may not be endorsed by an organization, but may be far more useful in a power-supply analysis than other top-tier simulation software tools.

SPICE is arguably the most widespread simulation program for circuit analysis. With dozens of variants to choose from – several that are free of charge – it is also an economical choice. Another reason to choose SPICE over other simulators is that the vast majority of semiconductor and component suppliers make SPICE models of their devices freely available. Beware, however – just because a model is available does not mean it is suitable for your application. It is up to you as the designer to understand and validate a model's behavior and augment it where necessary.

In general, SPICE models are defined to represent "typical" behavior, so they are generally not appropriate for worst-case or extreme value-type simulations. In most cases the only way to achieve a representative WCCA in SPICE is to develop your own parameterized component models and circuit simulations. Take an inductor model, for example. The inductor may include a parasitic DC resistance (DCR), but it probably does not model AC winding losses or saturation effects, and capacitor models rarely include DC bias effect or temperature-dependent equivalent series resistance (ESR). To address these limitations, it becomes necessary to construct a composite "macro-model" for the device based on the component data sheet and your own device characterization where necessary.

Another caveat associated with effectively using circuit simulation is that you must be familiar with the simulation tool as well as the circuit topology you are analyzing. Suppose you are analyzing a high-power boost or flyback converter. When simulating the control loop, you should be aware that as the load increases, a right-half-plane zero (RHPZ) moves toward the origin. Neglecting to consider this effect can result in an abrupt reduction in control-loop phase margin and instability. Although the location of the RHPZ can be expressed mathematically [2], a small-signal SPICE simulation like the one presented in reference [3] facilitates a far greater understanding of the RHPZ and its impact on stability.

Other effects often missed in a power-supply analysis are capacitor ESR variance over temperature and DC bias [4]. These effects can represent the difference between a stable converter and one that is unpredictable under variations in temperature, DC bias and life. Developing a model that accurately represents a capacitor's behavior is essential for accurate modeling of a power converter [5]. Ultimately, it is the integration of power-supply experiences into an intelligent simulation that makes it a powerful approach in advancing a robust design. Over time, your understanding of SPICE and your confidence in simulation will improve; this will facilitate design creativity and design insight that ultimately will help differentiate your products and accelerate product time to market.

II. Inside SPICE

A. The SPICE Convergence Algorithm

Understanding how SPICE works is essential to getting the most out of your simulations. Figure 2 is a simplified block diagram of the SPICE algorithm, where nodal analysis (blocks 3 and 4) is accomplished by formulating a linear matrix of the circuit and solving nodal equations for the circuit voltages. The iterative inner loop (blocks 2-6) finds the solution for nonlinear circuit elements. To do this, SPICE must create linear "companion models" for all nonlinear devices at each time-step interval, h(n). Together with the inner loop, the outer loop (7-9) makes transient analysis of nonlinear circuits possible in SPICE.

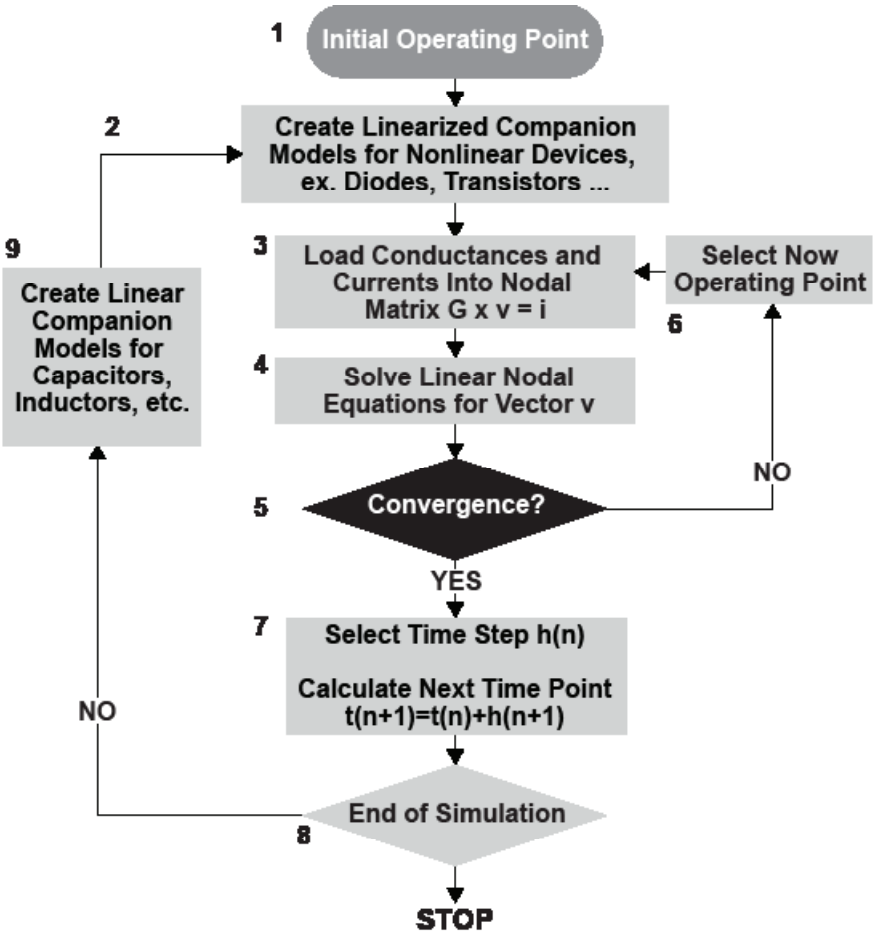

Figure 2 – SPICE basic matrix solver algorithm.

The primary analyses in SPICE used to evaluate a power supply include DC, transient (time domain) and AC (small-signal frequency domain); a brief description for each follows. SPICE is also capable of other analyses, including Sensitivity, Fourier, Monte Carlo and Noise analysis. Some versions of SPICE include Smoke analysis, where SPICE evaluates each component according to predefined stress tolerances.

B. DC Analysis

DC analysis calculates the DC operating point – the initial solution to a transient analysis and bias point for an AC analysis. A "DC sweep" analysis performs a DC analysis multiple times while sweeping a selected component parameter across a defined range, ignoring all energy-storage components including semiconductor charge mechanisms.

One of the simpler tasks for SPICE is performing a DC analysis on a linear circuit. Only two of the blocks from Figure 2 are needed: load the nodal matrix (block 3) and solve the nodal equations (block 4). For nonlinear circuits, SPICE creates an equivalent linear model for each nonlinear device. The loop (blocks 1-6) iteratively finds the solution by inferring an operating point from the circuit, creating equivalent linear models, and solving the nodal matrix for the circuit voltages that satisfy analysis parameters. When changes in circuit voltages and currents have fallen below predefined limits, the solution is said to have "converged."

C. Transient Analysis

A transient analysis of a linear circuit completes the output loop (blocks 3-9), ignoring blocks 2 and 5. After finding the initial operating point, the energy-storage components (capacitors, inductors, semiconductor junctions) are transformed into linear companion models to facilitate nodal analysis. For nonlinear circuits, SPICE completes the nonlinear loop (blocks 2-6) at each time step of the transient analysis. To improve accuracy while reducing simulation run time, SPICE dynamically adjusts the time step. When circuit voltages and currents are changing rapidly, the time step is reduced to improve accuracy. On the other hand, if changes are small, SPICE increases the time step to reduce simulation run time.

D. AC Analysis

AC analyses are a family of frequency-domain analyses that include transfer function analysis and noise analysis. To perform an AC analysis, the SPICE algorithm must first evaluate the nonlinear circuit loop (blocks 1-6) to find a DC operating point. The analysis then moves to blocks 3 and 4, where SPICE loads the nodal matrix with the real and imaginary parts of impedances for the resistors, capacitors and inductors. Power supplies are set to zero, the signal source is set to unity, and blocks 3 and 4 are repeated over all specified frequencies. The result of the analysis is calculated in terms of signal magnitude and signal phase for each node.

E. SPICE control

One of the more frustrating aspects of running a simulation in SPICE is when a solution cannot be found and the algorithm sputters to a halt. To help avert this, you must know how to set the analysis parameters (Table 2). These options adjust algorithm behavior such as:

- The maximum iterations allowed in the nonlinear loop.
- The criteria for when a solution has converged.
- How to select the initial operating point.
- How the time steps are chosen in a transient analysis.
- The method used to create linear companion models.
- The maximum/minimum time step, and transient and DC relative error.

Temperature of Environment °C	27°C
DC ABSTOL Abs. Current Error	1 μA
DC VNTOL Abs. Voltage Error	1 μV
DC Abs. Base-Current Error	1 pA
DC RELTOL Relative Error (%)	1 m
GMIN	1 p
DC Max. Iteration #	1,000
DC Min. Iteration #	40
TR Max. Time Step (s)	1 Gs
TR Min. Time Step (s)	1E-30
Shunt Conductance	0

Table 2 – SPICE analysis parameters (abbreviated).

F. Convergence

Until recently, running a SMPS circuit simulation in SPICE was time-inefficient and convergence errors were common. But convergence and simulation speed in SPICE have more to do with the model/circuit constructs than with a presumed weakness in SPICE. This is true today more than ever, with SPICE algorithms running on faster computers that have nearly "unlimited" memory. However, if a model or circuit asks SPICE to solve a circuit matrix that is "irregular" or contradictory, a convergence error will occur.

A simple example of an irregular circuit is one containing a shorted voltage source or an open current source, but the effect can be more subtle. Idealized reactive devices or poorly defined behavioral constructs inside macro-models can create a transient "short" or "open" that looks

irregular to the SPICE matrix solver. In either case, these circuits have a topology that contradicts the definition of the parts, resulting in unsolvable equations. Adding DC resistance to reactive components can help resolve many irregular circuit convergence errors.

In a transient analysis, the size of the linear matrix is defined by the circuit and is a function of the number of circuit nodes. The more nodes in the circuit, the bigger the matrix and the longer simulation may take to complete. Clearly a switch-mode power supply is far from a linear circuit and the analysis is computationally intensive. As such, it is essential to carefully select the analysis parameters to decrease simulation run time and improve convergence while not compromising simulation fidelity [6].

Although the list of analysis parameters is long (to address a wide range of circuits), relative error (RELTOL) and maximum time step (see Table 2) have the most significant effect on switching regulator simulations. For example, if a simulation is running slowly, consider relaxing RELTOL and restricting TR MAX (more on this later). But for now, let's illustrate the effectiveness of a SPICE by considering the SEPIC power converter in Figure 3. Although the SEPIC is widely regarded as one of the more difficult topologies to analyze [7], a validated time-domain simulation of a SEPIC in SPICE can be highly effective in ensuring that you meet your design objectives.

The simulation circuit in Figure 3 uses a highly accurate behavioral model of the Texas Instruments TPS40210 boost controller configured as a 300-kHz buck-boost SEPIC. Output response is evaluated over line and load variations and includes startup behavior and a transient load step. The simulation completes in less than 30 seconds, revealing a wealth of information about the expected circuit behavior even under extreme operating conditions.

The key to achieving speed in any SMPS simulation is to minimize the number of rejected time steps that can occur if the analysis parameters are not set correctly. Often, you can improve the performance of an SMPS simulation by increasing RELTOL from 1 m to 5 m and/or reducing tmax to <<1 µs. And since the mathematics underlying power-supply operation are well documented, it is always a good idea to confirm simulation waveform results (peak inductor current, duty cycle, etc.) with a few calculations. A good mathematical analysis of the SEPIC topology can be found at http://www.ti.com/lit/an/snva168d/snva168d.pdf.

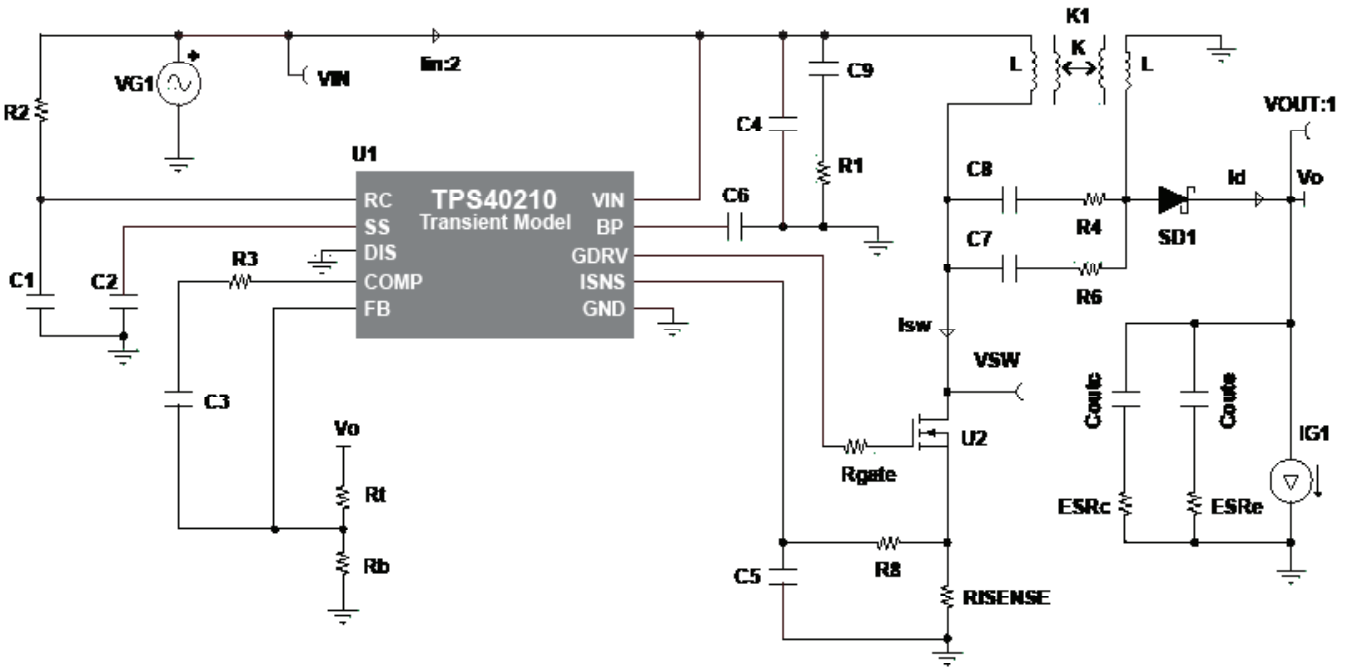

Figure 3 – SEPIC transient analysis circuit simulation model.

G. Solving the Nodal Voltages – Numeric Integration

Figure 4 illustrates the basic idea behind numeric integration, the method used by SPICE to solve nodal voltages in complex linear and nonlinear circuits. Suppose the waveform in Figure 4 represents a charging capacitor. To solve for the voltage at t(n+1), you could calculate the slope at t(n), multiply it by the time step h = Δt = (t(n+1) – tn), and add it to the voltage at t(n). This is known as the Forward-Euler (FE) integration.

The approximation approaches the exact solution as Δt goes to zero:

$$x_{n+1} \quad x_n + h \times \frac{dx_n}{dt} \tag{1}$$

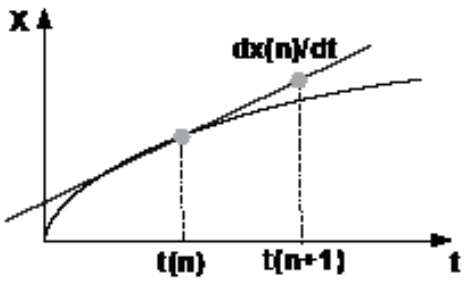

Figure 4 – Forward-Euler integration.

Clearly, there is error between the actual curve and the estimated point t(n+1), but reducing the time step will reduce the error. Another method, the Backward-Euler (BE), uses the slope at t = (n+1) (see Figure 5), rather than the one at t(n), to predict the next voltage. BE is mathematically expressed in Equation 2 and is more accurate and less sensitive to the size of the time step.

$$x_{n+1} - x_n + h \times \frac{dx_{n+1}}{dt} \tag{2}$$

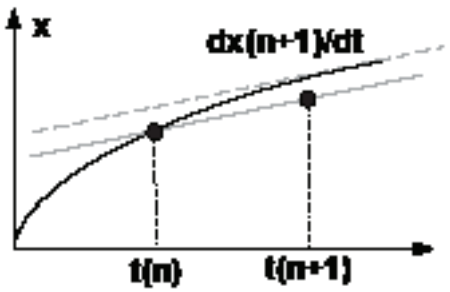

Figure 5 – Backward-Euler integration.

The trapezoidal integration method shown in Equation 3 calculates the average slope of the present and next time point to approximate the next solution.

$$x_{n+1} - x_n + h \times \frac{\left(\dot{x}_{n+1} + \dot{x}_n\right)}{2} \dot{x} - \frac{dx}{dt} \tag{3}$$

Gear-2, named after its author Steven Gear, is shown in Equation 4 and predicts the next point using information from the present and two from the past:

$$x_n - \frac{4}{3} \times x_{n-1} - \frac{1}{3} \times x_{n-2} + \frac{2}{3} \times h \times \dot{x}_n \tag{4}$$

Each method has its own strengths and weaknesses based on:

- Accuracy: how much error (local truncation error) each method introduces.
- Stability: Does the error accumulate or decrease over time?

One integration method may have an advantage over another; however, in SMPS analysis, Gear-2 is least susceptible to numeric oscillations and is generally recognized as the most effective method for the SPICE algorithm. (For a detailed discussion on integration methods, see http://docs.lib.purdue.edu/cgi/viewcontent.cgi?article=1301&context=ecetr.)

To summarize:

- Backward Euler – average accuracy and stability.
- Trapezoidal – better accuracy than stability, may oscillate in some cases.
- Gear-2 – most stable method with some trade-off in accuracy. Best method for SMPS.

H. Deriving the Linear Companion Model

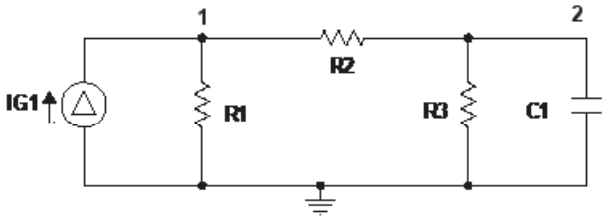

Figure 6 – Nonlinear circuit.

Suppose you wanted to find the time response of the circuit in Figure 6. You could formulate a set of differential equations and analyze the nodal voltages mathematically, or you could build the circuit in SPICE. SPICE, however, is not a differential equation solver, but as we saw earlier, it can solve for nonlinear behavior using numeric integration and linear companion models for the nonlinear devices. Let's examine two examples, the capacitor and diode.

I. Capacitor Companion Model

A capacitor is transformed into a linear element by applying numeric integration to the current-versus-voltage relationship.

Equation 5 defines the capacitor's voltage-charge relationship.

$$V_C = \frac{Q}{C} \tag{5}$$

Applying BE integration (Equation 2), you can express the capacitor voltage in terms of the differential equation below:

$$V_{n+1} - V_n + h \times \frac{1}{C} \times \frac{dQ_{n+1}}{dt}$$

can express the capacitor's voltage in terms of voltages and currents only:

$$V_{n+1} - V_n + \frac{h}{C} \times I_{n+1}$$

To create the linear companion model, rearrange the expression above such that the current is in terms of voltage:

$$I_{n+1} - \frac{C}{h} \times V_{n+1} + \frac{C}{h} \times V_n$$

Now you can think of (C / h) as an equivalent conductance, Geq, because multiplying it by V produces a current:

$$I_{n+1} - Geq \times V_{n+1} + Geq \times V_n$$

This expression can be represented with the SPICE primitives shown below in Figure 7.

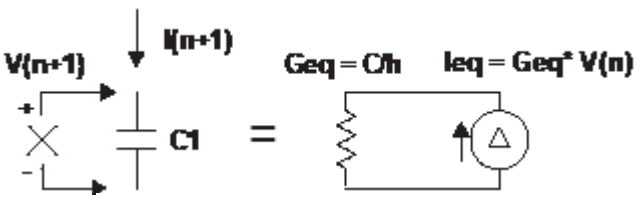

Figure 7 – Capacitor companion model.

Conductance, Geq, describes the part of C1's current dependent on its new voltage Vn+1; the current source, Ieq, describes the other part based on the past voltage, Vn.

SPICE can now solve the nonlinear circuit in Figure 6 using the iterative method described previously and the limits equations for voltage and current change shown in Equations 6 and 7:

$$|V(n) - V(n-1)| < VLIMIT = V(n) \times RELTOL + VNTOL$$

$$|I(n) - I(n-1)| < ILIMIT = I(n) \times RELTOL + ABSTOL \tag{7}$$

By default, RELTOL is set to 0.1 percent (1 m). So if the expected voltage is 5 V, the change in node voltage must fall below 5 mV to reach a solution. However, if the voltage swings near zero, such as 0.1 mV, then the voltage change has to fall below 0.1 µV for convergence – possibly an unrealistic demand that can cause convergence errors.

VNTOL is another analysis parameter used to limit the expectation of the RELTOL parameter for convergence. VNTOL has a default value of 1 µV to ensure that as voltages approach 0 V, RELTOL doesn't preclude convergence. RELTOL and ABSTOL play a similar role for the current change limits. The default value for ABSTOL is 1 pA. In a switching regulator, designers are not usually interested in 1-pA or even 1-µV signals, so these can be relaxed unless they are part of an internal macro-model that requires this level of sensitivity.

J. The Diode Companion Model

Like the capacitor, a diode's nonlinear behavior must be represented in a linear way.

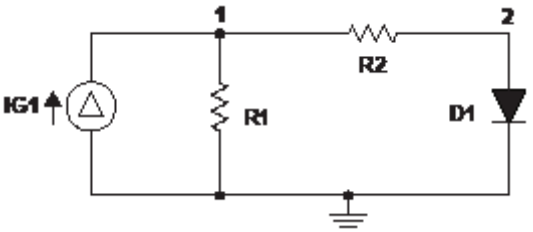

Figure 8 – Nonlinear diode circuit.

Mathematically, the I-V relationship of the diode is expressed in Equation 8:

$$Id = IS \times \left(e^{\frac{Vdo}{Vt}} - 1 \right) \tag{8}$$

where IS is the saturation current and Vt is the thermal voltage.

Limiting your focus to the forward voltage, Vdo, you can approximate the behavior with a line tangent to its ideal curve (the blue line in Figure 9).

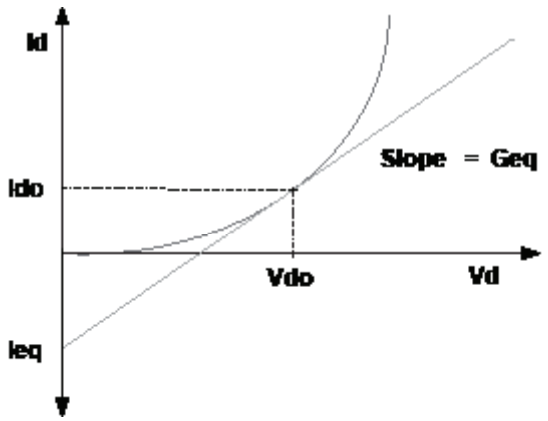

Figure 9 – Diode I-V analysis.

The straight line can then be modeled using a parallel combination of a conductance, Geq, and a current source, Ieq – a linear model. By inspecting Equation 9, Geq is the slope of the tangent at the operating point, Vdo.

$$Geq \quad \frac{dId}{dVd} \quad \frac{IS}{Vt} \times e^{\frac{Vdo}{Vt}} \tag{9}$$

Ieq is the point where the tangent intersects the y-axis (Equation 10).

$$Ieq \quad Ido \quad Geq \times Vdo \tag{10}$$

Figure 10 illustrates the SPICE components used to create the diode linear companion model. Figure 11 illustrates how it would be used in the circuit shown in Figure 8.

Figure 10 – Diode companion model.

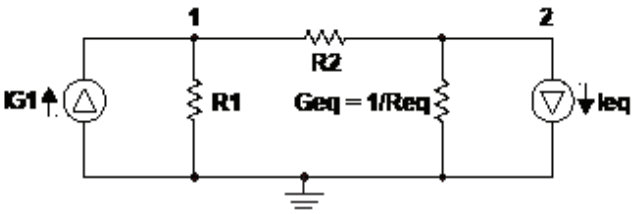

Figure 11 – Diode linear equivalent circuit.

K. Nodal Analysis at Work

As with the capacitor companion model, you can now treat the diode like any other linear component and formulate the nodal equations (Equations 11 and 12).

$$\frac{1}{R1} + \frac{1}{R2} \times V_1 + \left(-\frac{1}{R2} \right) \times V_2 = Is \tag{11}$$

$$\left(-\frac{1}{R2} \right) \times V_1 + \left(\frac{1}{R2} + Geq \right) \times V_2 = -Ieq \tag{12}$$

Since the reciprocal of resistance is conductance, let G11 = 1/R1 + 1/R2, G12 = -1/R2, G21 = -1/R2, G22 = 1/R2+Geq, I1 = Is and I2 = - Ieq.

Thus, the equations reduce to:

$$G_{11} \times V_1 + G_{12} \times V_2 \quad I_1$$

$$G_{21} \times V_1 + G_{22} \times V_2 \quad I_2$$

The diode voltage at node 2 is expressed in Equation 13:

$$V_2 = \frac{\left(I_2 - \frac{G_{21}}{G_{11}} \times I_1\right)}{\left(G_{22} - \frac{G_{21}G_{12}}{G_{11}}\right)} \tag{13}$$

Finally, substitute the calculated V2 value into Equation 14 to get V1:

$$V_1 \quad \frac{I_1 \quad G_{12} \times V_2}{G_{11}} \tag{14}$$

Remember, the diode's companion model was created at a trial operating point with a specific integration method. After solving the nodal equations, the voltage found across the diode serves as the next trial operating point and a new companion model is created. When changes in circuit voltages and currents between iteration (n) and the last iteration (n-1) are smaller than the limit defined below, you've arrived at a solution. Figure 12 illustrates the flow diagram.

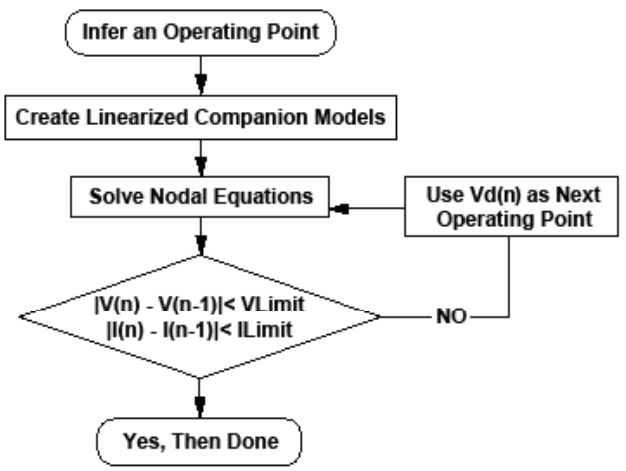

Figure 12 – Nonlinear iterative "linearizer."

If the changes are greater than the defined limits, VLIMIT/ILIMIT, then use the calculated voltage as the trial operating point for the next iteration and jump to Step 2. The simulator will ultimately converge and satisfy the predefined limits set. For a more complete discussion on the SPICE algorithm and many introductory examples of using SPICE, see www.ecircuitcenter.com.

L. Is SMPS Simulation in SPICE Slow?

The nonlinearity of switching regulators – including fast dV/dt, di/dt and abrupt changes in impedance – can severely burden a SPICE matrix solver. However, today SPICE can easily handle SMPS analysis both accurately and quickly.

As an analysis tool, SPICE offers a high level of signal fidelity (perhaps too high for SMPS). But contrary to popular opinion, a SPICE simulation of a switching regulator does not have to be slow or painful when you understand how SPICE works and have access to good SPICE models. In fact, in this paper I will develop a current-mode PWM model that operates in multiple modes (fixed frequency at 1.25 MHz and frequency fold-back) and simulates startup to steady-state with a transient load step in 10 seconds.

There are many SPICE simulators from which to choose. The most popular are PSpice, IsSpice, SIMetrix, LTspice and my personal favorite, TINA. TINA is a full-featured SPICE simulator that is intuitive to use and powerful. TINA-TI™ is a limited-feature, free version of the TINA software developed for Texas Instruments, and although feature-limited, it is not node-limited, so there is no restriction with regard to the size of a circuit you can analyze. TINA version 9 is among the fastest simulators for SMPS applications available today and is fully compatible with SPICE models built in Berkeley 3F5 SPICE, XSpice, and PSpice, the most widely deployed and recognized SPICE simulator.

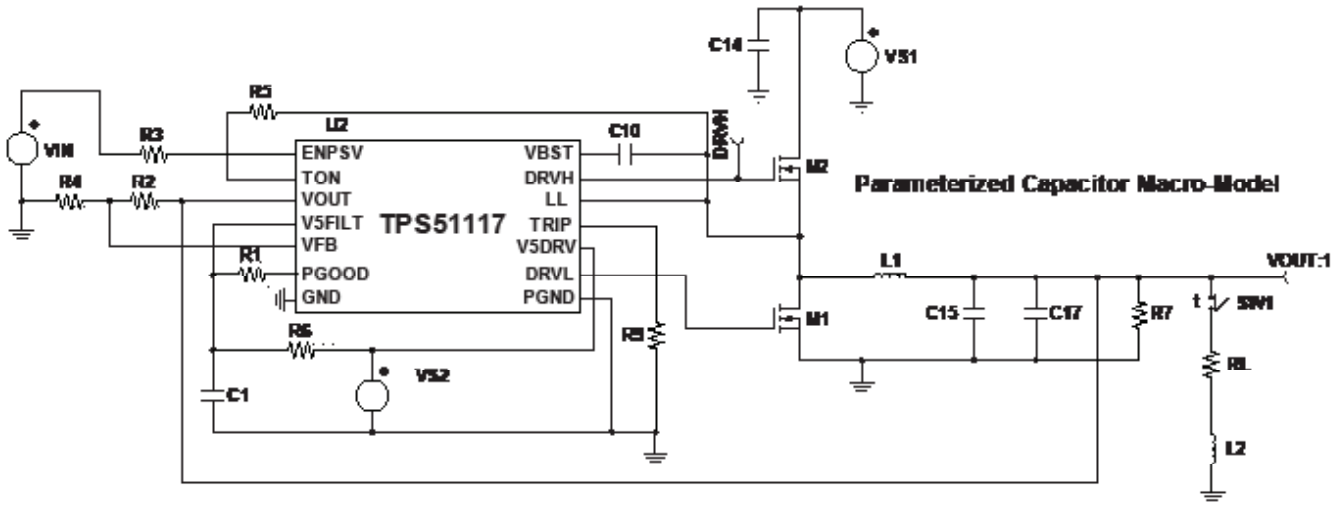

Figure 13 – Adaptive on-time transient analysis schematic.

Some simulators, including LTspice, use built-in "code models" that help a simulation run faster, and LTspice is a fast simulator when using their models. However, if a SPICE model has not been optimized with these specialized primitives, an SMPS simulation may run much slower. For example, the simulation in Figure 13 uses the Texas Instruments TPS51117 adaptive on-time synchronous rectifier controller running a startup to steady-state analysis and load step. TINA-TI software v9 completes the simulation (Figure 14) in 15 seconds using standard Berkeley 3F5 SPICE primitives, whereas the same circuit takes more than 6 minutes in LTSpice.

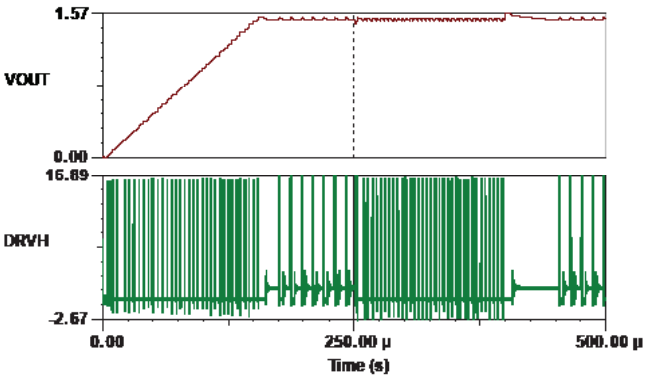

Figure 14 – Startup to steady-state simulation (high fidelity, 15-s run time).

It is important to understand that a transient SMPS model in SPICE is not suitable for a small-signal analysis. A small-signal analysis is a linear analysis and requires a separate linear or "average" model of the switching regulator. Therefore, to evaluate loop stability and switching behavior in SPICE, you will need two models:

- A transient model to predict time-domain behavior including switching waveforms, transient load-step response, voltage sequencing, fault response and output voltage ripple.
- A linear average model to predict small-signal frequency-domain behavior including loop stability, output impedance and PSRR.

Note, however, that an average model can predict a transient load-step response if the model is self-biasing and operates in both CCM and DCM [8].

A significant advantage of the "SPICE-like" simulator SIMPLIS is that a single model can be used to predict both transient switching and small-signal behavior. In fact SIMPLIS is one of the most power-centric simulation tools available today. Their design verification module (DVM) enables users to automate the execution of a suite of tests and compare the measured results to a design performance specification [9].

Armed with this basic understanding of SPICE, I will now move to the development of a SPICE simulation for a current-mode, buck power supply. It is worth mentioning that component modeling is both art and engineering and that each model in a simulation should be understood and validated mathematically where possible; a circuit simulation is only as good as its weakest component model, and creativity in modeling facilitates time-efficient simulations.

M. SPICE Building Blocks

Table 3 represents the more commonly used SPICE building blocks. In addition to the idealized component models (resistors, inductors, capacitors, etc.), there are dependent sources (including voltage- and current-controlled sources) and behavioral structures that are exceptionally useful in building high-level macro-models. A behavioral source is a voltage or current source with inputs and outputs defined as mathematical, logical or list/table functions, mimicking complex transistor-level functionality while simulating much faster. There are many references on the Web explaining SPICE components and component syntax, including this one sponsored by the University of California at Berkeley: http://bwrc.eecs.berkeley.edu/classes/icbook/spice/.

For specific insight into using SPICE for SMPS analysis, few better resources exist than those provided by Basso [10] and Sandler and Hymowitz [11].

Elementary SPICE Primitives	Inductors, Capacitors, Resistors, Transistors/Diodes …
Dependent Sources	Voltage- and Current-Controlled Sources
Voltage-Controlled Switches	With and Without Hysteresis
Behavioral-Controlled Sources	Mathematical, Table, Boolean, List, If-Then-Else, etc.
Non-Standard SPICE Primitives	Coded Models to Accelerate Simulation

Table 3 – SPICE building blocks.

To illustrate a behavioral construct, let's create a Boolean AND gate as a voltage expression E1:

E1 3 0 VALUE= {IF ((V(1)>2.5) & (V(2)>2.5),5V,0)}

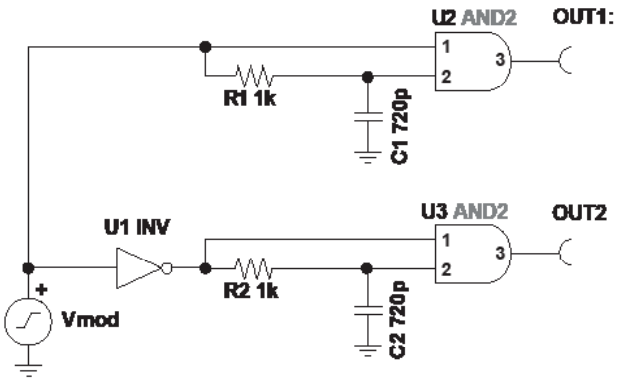

Figure 15 – Half-bridge behavioral gate driver with programmable dead time.

This expression defines a voltage source, E1, from node 3 to the circuit ground (0 is an absolute circuit reference) using the SPICE if-then-else statement. Translated, it states: "IF the voltage at node 1 is greater than 2.5 V AND the voltage at node 2 is greater than 2.5 V, THEN E1 = 5 V, else E1 = 0 V."

A practical example of using this structure is in the half-bridge, gate-drive circuit, as illustrated in Figure 15. The time constants made up of R1 and C1 and R2 and C2 will set the dead time (Delay) by the expression:

C1 = Delay/(0.693 x R1)

III. PWM Converter and Circuit Model

A. PWM Modeling Blocks

The principle building blocks associated with modeling a SMPS are the:

- Error amplifier (EA).
- Modulator.
- Power MOSFET output transistor.
- Gate driver with dead time.
- Output filter.

The development of these blocks as behavioral elements will be discussed in detail. In addition, I will also show how frequency fold-back can be added using a TINA-formulated voltage-controlled-oscillator (VCO).

B. The Error Amplifier (EA)

Depending on the device you are modeling, the EA can be a simple operational transconductance amplifier (OTA) or a SPICE parameterized voltage amplifier defined in terms of its operating characteristics. An OTA can be defined as a simple voltage-controlled current source (VCCS) where the output current is proportional to the differential input voltage and specified transconductance, gm. In a simulation, this voltage is presented to the pulse-width modulator (PWM) that compares the error signal to a ramp signal. Since the output of the modulator is proportional to the converter duty cycle and hence the output response, it is important to limit the EA output bandwidth, output current and voltage according to the actual device performance defined in the data sheet.

The minimum/maximum behavioral expression shown here limits the output current to +/-7 µA. The output current is then presented to a parallel RC, which sets the open-loop bandwidth of the EA.

if(I(V1)>0, -1*min(I(V1),7u),-1*max(I(V1),-7u))

If the output current of the EA is not limited, the output transient response will likely be erroneous.

The syntax reads, “If the current through the zero volt voltage source V1 is > 0, [i.e., EA sinking] then make the output current to be the lesser of I(V1) and 7 µA; otherwise the current is sourcing and make it to be the greater of -7 µA and I(V1).” Ideal diodes on the output clamp the output voltage, thereby limiting the output voltage of the EA. The complete EA macro is shown in Figure 16.

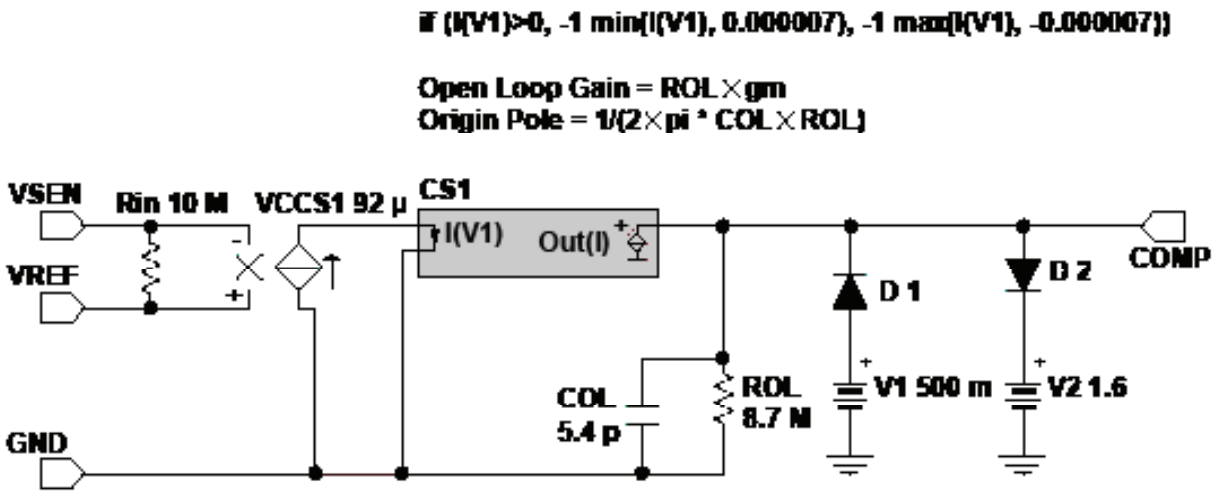

Figure 16 – Current- and voltage-limited OTA.

C. The Modulator

The PWM compares the output of the EA to a ramp signal. In voltage-mode control, this ramp can be generated as an independent voltage source with the following syntax:

Vn N1 N2 PULSE(V1 V2 Td Tr Tf PW T)

Where N1 and N2 are circuit nodes, V1 and V2 represent the start/stop voltage levels, Td is a time delay, Tr/Tf are the rise and fall times and PW is the pulse width.

Example: Figure 17

VRAMP 1 0 PULSE(0 5 0 10u 1u 0 11u)

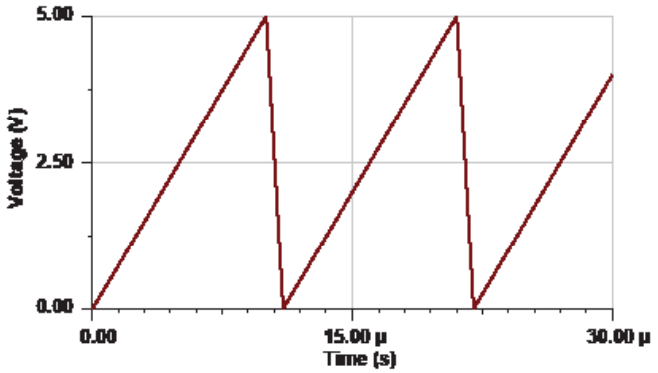

Figure 17 – Pulse-width modulator ramp.

The modulator can be represented as a simple behavioral voltage "compare" between the error signal and the ramp.

if(V(EA)-V(RAMP) > 0 5, 0)

The syntax reads, "If the voltage at EA minus the voltage at the RAMP is greater than zero, then the output of the modulator is 5 V; else it is 0 V." The output of any behavioral block is often presented as a 10- to 100-ps time constant to remove numerical noise and address race conditions in sequential circuits. In addition, a delay block should be added to the output of the modulator to represent the expected propagation delay through the comparator; it can be modeled in SPICE by a transmission line, unit time delay (UTD).

It is important to consider the delay because it does impact phase margin, especially as the crossover frequency approaches the switching frequency. For example, a 70-ns propagation delay is represented in Figure 18 as a ~3° reduction in phase margin at 125 kHz. A simple AC sweep on a UTD was used to generate this plot. Notice that the propagation-delay effect on phase margin increases at higher frequencies.

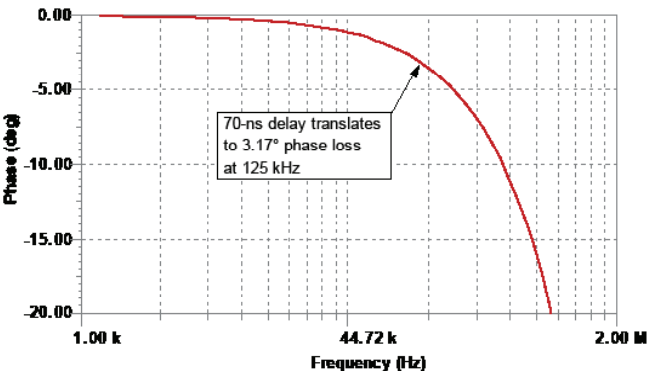

Figure 18 – Modulator delay effect on phase.

The modulator also represents a control-loop gain term defined as Gm = Vin/Vramp for the buck topology. To maintain a fixed gain over the input-voltage range, many voltage-mode controllers vary the ramp amplitude as a function of the input voltage. This is known as "voltage feed forward" [12], and helps ensure a constant response over line variations. The function can be modeled in SPICE by altering the slope of the PWM pulse as a function of the input voltage.

D. The Latch

The modulated error signal is presented to a reset-set (RS) latch holding the state between clock periods. This block can be created as a behavioral structure with two NAND functions or with discrete transistors, as shown in Figure 19.

A behavioral latch uses fewer nodes, however, and may run faster than the transistor-level circuit. The behavioral expression in netlist form is shown below:

```
SUBCKT FFLOP S R Q Qn
EQn 10 0 VALUE={IF ( (V(R)<1) &
(V(Q)>1),0,5)}
EQ 20 0 VALUE={IF ( (V(S)<1) &
(V(Qn)>1),0,5)}
RDa 10 Qn 100
CDa Qn 0 10P IC=5
RDb 20 Q 100
CDb Q 0 10P IC=0
ENDS FFLOP
```

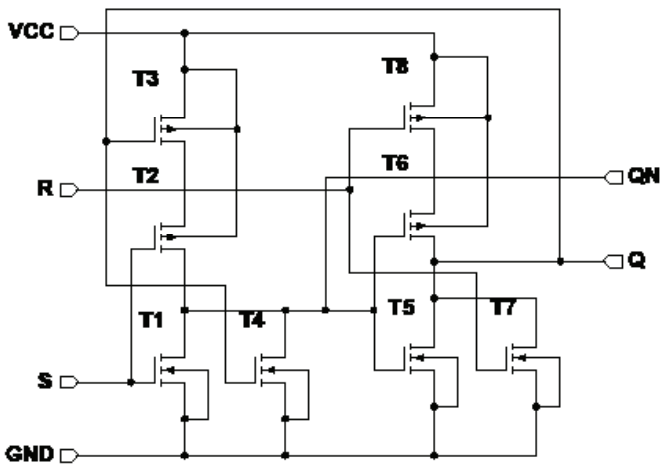

Figure 19 – Transistor model of an RS latch.

The subckt nodes S, R, Q and Qn are defined on the first line and two Boolean if-then-else statements interconnect the NAND gates to form the RS latch. This structure, however, is prone to instability in SMPS applications, so a clocked or dominant reset latch is often used.

E. MOSFET Transistor Switch Model

There are several options for modeling the behavior of a MOSFET switch depending on the fidelity required. In a linear regulator, for example, the pass element is more critical to the simulation than in an SMPS simulation. A MOSFET model for a switching regulator can be as simple as a voltage-controlled switch defined by an on-resistance, off-resistance and turn-on threshold.

An ideal diode is usually placed in parallel with the switch, making it suitable for a variety of analyses including synchronous rectification and voltage stress analysis. When greater fidelity is needed, lateral SPICE MOSFET structures are an option, but these offer poor correlation with the vertical DMOS structures typically used in power electronics, particularly at low and high current densities. Other nonlinear effects not modeled with these devices include input, output, Miller capacitances and thermal effect. To address these limitations, BSIM 3.3 models have evolved that are modifiable with external behavioral constructs to achieve exceptional correlation with measured results. A model of this level of fidelity can examine subtle behavior including switching losses, BVDSS breakdown, body-diode reverse recovery and Miller turn-on effect. A thermally compensated behavioral MOSFET model is presented in reference [13], and although the model had convergence issues when it was developed at Harris Semiconductor in the 1990s, it can be easily simulated on computers today.

F. Output Filter Response

A power-supply transient response to a load step is its peak output impedance times the change in load current. Figure 20 presents a simplified model of the open-loop power-supply power stage with the resulting output impedance and phase response in Figure 21. The voltage source, Vg, represents the power supply. The output impedance of the filter is determined with an AC sweep while measuring the output voltage. The filter output impedance at low frequency is set by the output inductor DCR and increases with frequency, as shown in Figure 21. The impedance rises until the output inductor and capacitor resonate.

At this frequency, the magnitude of the impedance is determined by the Q of the circuit and can be many times the impedance of the filter elements. Once past resonance, the output impedance drops with increasing frequency until the capacitor ESR is reached. At higher frequencies, there is a parasitic or equivalent series inductance (ESL) in the capacitor that causes the impedance to increase.

The output-voltage variation to a rapid load step can be quickly estimated (Figure 22), neglecting the effect of any feedback network. If the load step has a rate of rise much greater than the inverse of the resonant frequency, the filter characteristic impedance sets the maximum impedance and the voltage variation in the open circuit case is expressed in Equation 15:

$$V_1 \quad Zout \times Istep \tag{15}$$

where

$Zout = \sqrt{\frac{Lout}{Cout}}$ is the characteristic impedance.

The SPICE circuit in Figure 20 can be used to optimize the output capacitance necessary to address transient load-step behavior [14].

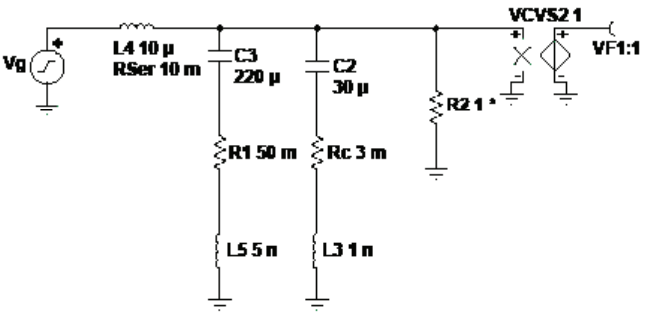

Figure 20 – Modeling the output filter.

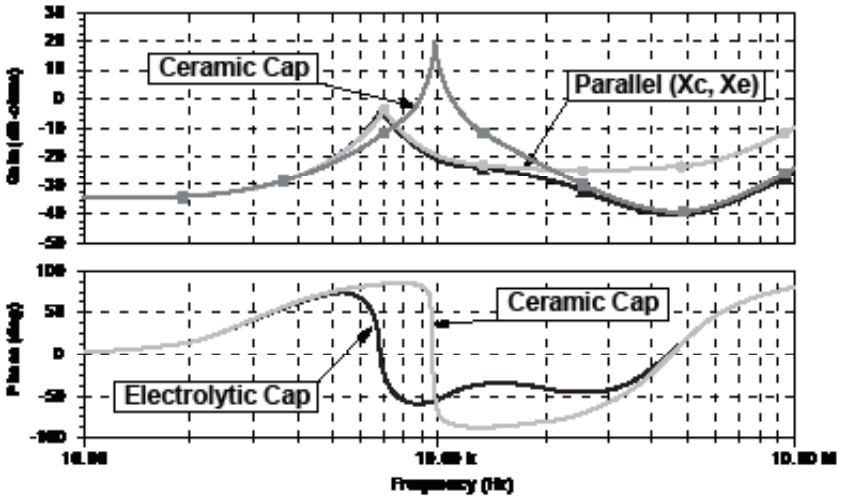

Figure 21 – AC output filter response.

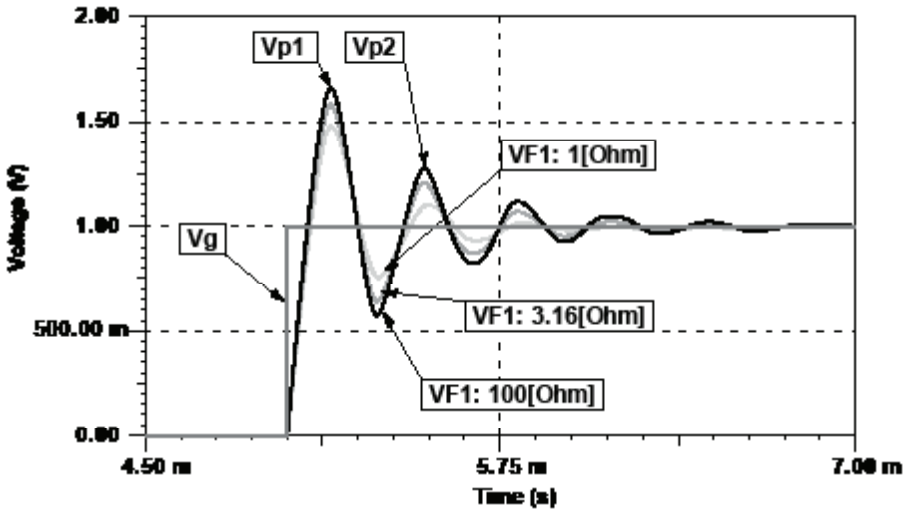

Figure 22 – Output filter time response and Q.

From the filter phase response in Figure 21 and corresponding time response in Figure 22, you can see why the all-ceramic filter capacitor output with high Q (low DC resistances) is more difficult to compensate than a lossy filter with higher ESR and inductor DCR.

The resonant tank quality coefficient, Q, can be calculated from the peak ringing waveforms in Equation 16.

$$Q = \sqrt{\left(\frac{\pi}{\ln k}\right)^2 + \frac{1}{4}} \Rightarrow k = (vp2\text{-}vin)/(vp1\text{-}vin) \quad (16)$$

Clearly, the open-loop circuit resonances impact filter ringing, but as I will show later, the stability of a closed-loop system is in fact quantifiable in terms of the closed-loop quality coefficient, Qc. In short, if you can measure Qc, you can assess stability.

G. Completed SPICE model

At this point, you have all the SPICE elements necessary to build a behavioral macro-model of a switching buck regulator. Using the data sheet block diagram for the TPS40222 buck converter, you can see how to interconnect the SPICE sub-circuits.

The TPS40222 current-mode block diagram in Figure 23 illustrates how the modulator ramp is created from the sensed switch current (I_{DRAIN}) using a current-controlled current source summed together with the slope compensation ramp ($I(V_{OSC})$) and an offset bias current.

All of the gain parameters illustrated in this block diagram are available from the data sheet parameter table; use the TI E2E Community at http://e2e.ti.com to request parameters when they are not available. Note that the TPS40222 data sheet also defines a frequency fold-back mode, whereby the switching frequency is reduced at light load conditions to improve efficiency. When the EA output is less than 0.5 V, frequency fold-back applies as explained in the data sheet. It is implemented in the model with a voltage-controlled oscillator (VCO); otherwise the oscillator operates at a fixed frequency of 1.25 MHz.

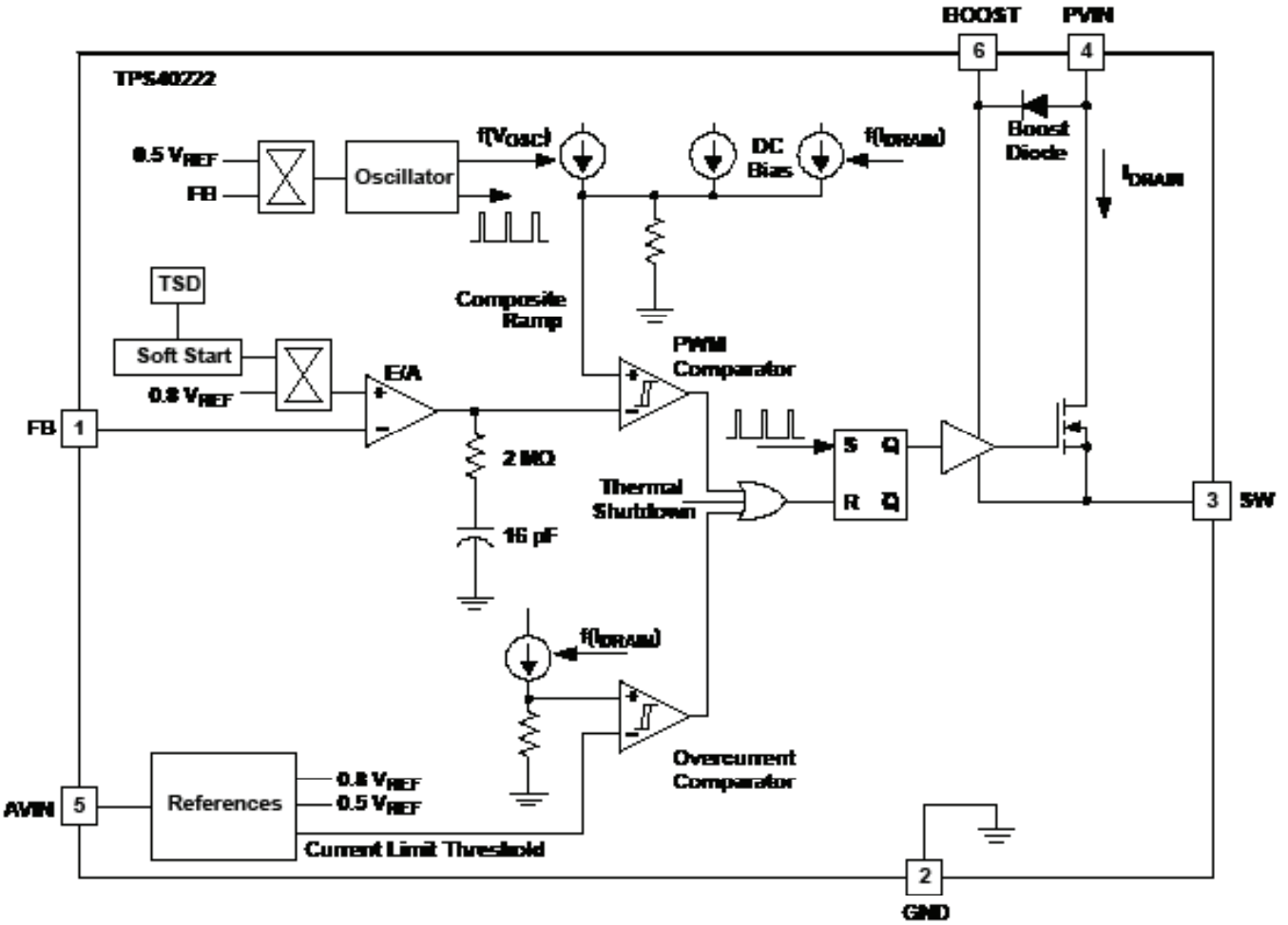

Figure 23 – TPS40222 functional block diagram.

Clearly understanding SPICE building block primitives – and in particular controlled-dependent and behavioral sources – is essential in building a PWM SPICE model. The completed TPS40222 behavioral macro-model is shown in Figure 24a with interconnects that match the data sheet block diagram shown in Figure 23. A top-level circuit representative of the TPS40222 EVM is shown in Figure 24b, where a pieces-wise-linear (PWL) voltage source with a 10-mΩ source resistance is used as the input voltage. The PWL input voltage is recommended in SMPS simulations to help avert convergence errors associated with abrupt changes when the simulation starts. Setting initial conditions on capacitors and inductors is also an option to help convergence. Note that the latch inside a PWM controller generally has its output state pre-set with initial conditions on holding capacitors, generally speaking, use initial conditions when running an SMPS simulation.

You can use a time-activated load switch with a representative inductance to examine the load-step response. The simulation uses an external catch diode downloaded from the Web. The diode I-V characteristic was verified using a current source and DC sweep analysis.

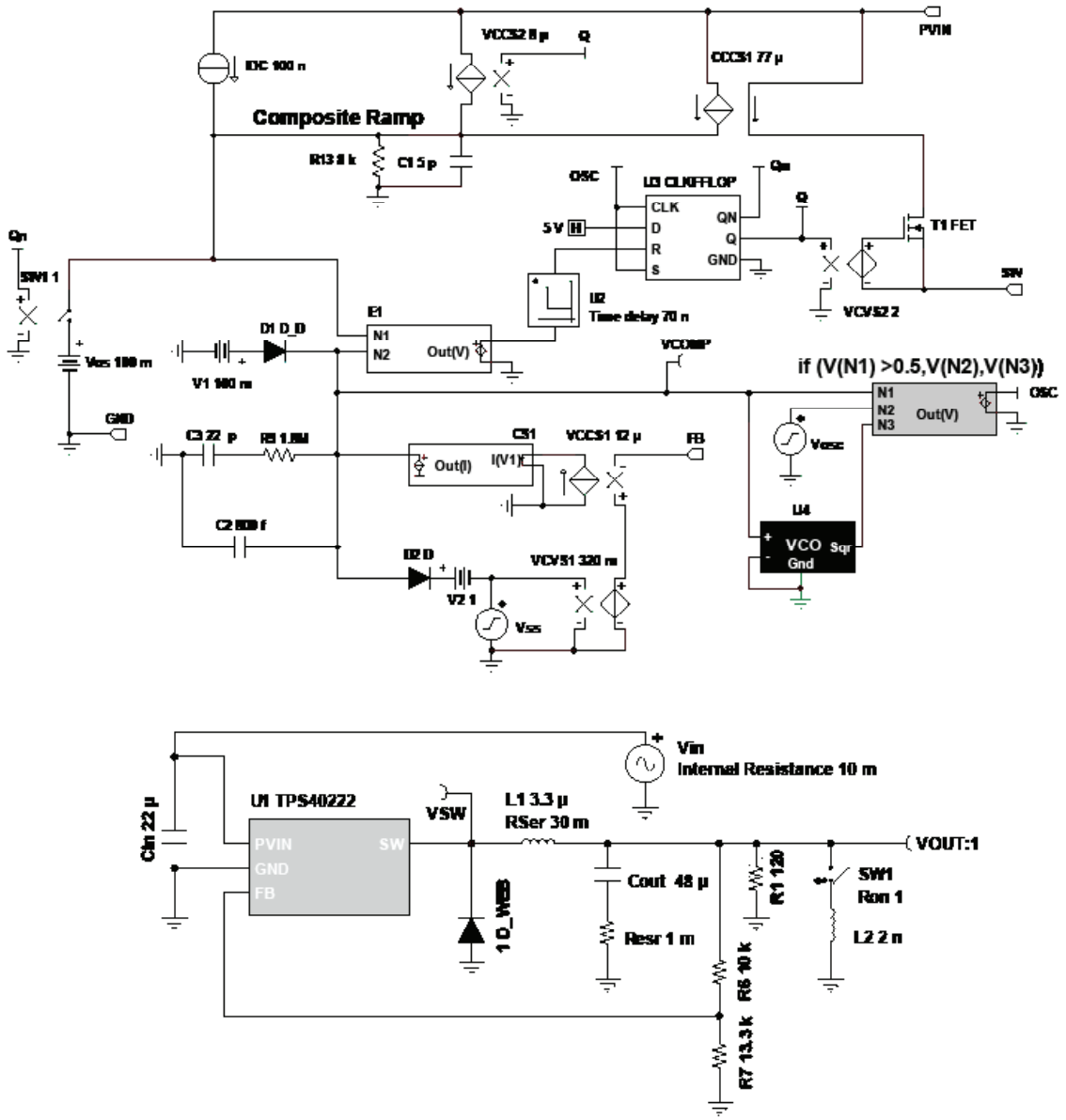

Figure 24 – Behavioral model of the TPS40222 (a) and top-level circuit (b).

H. Transient Load-Step Response

The best way to inspect a time-domain model is to run a transient analysis over line and load variations including startup; a load step on the output will typically expose instabilities and resonances if the circuit and component parasitic impedances have been modeled. But what load step di/dt in a simulation is representative of the actual load, and are the filter parasitic impedances accurately accounted for? Unless the load generator and circuit impedances are modeled correctly, correlation may not be as good as what is shown in Figure 25. This is especially true when inspecting the small-signal output impedance of the converter, where very small resistance and resonances are analyzed.

The load generator for a small-signal frequency analysis is modeled as an AC current source, but in a transient analysis it can be modeled as a current sink made with a voltage-controlled switch in series with an inductance to limit di/dt.

Figure 25a illustrates the startup-to-steady-state behavior of the buck converter. After charging the output capacitance, the converter enters frequency fold-back operating at ~100 kHz and is in DCM. When the load step occurs, the converter is forced into CCM operating at 1.25 MHz. The load-step behavior illustrated in Figure 25b suggests a critically damped response, correlating nicely with the EVM-measured phase margin of 70°. The entire simulation from startup to steady state completes in 10 seconds in TINA-TI software v9.

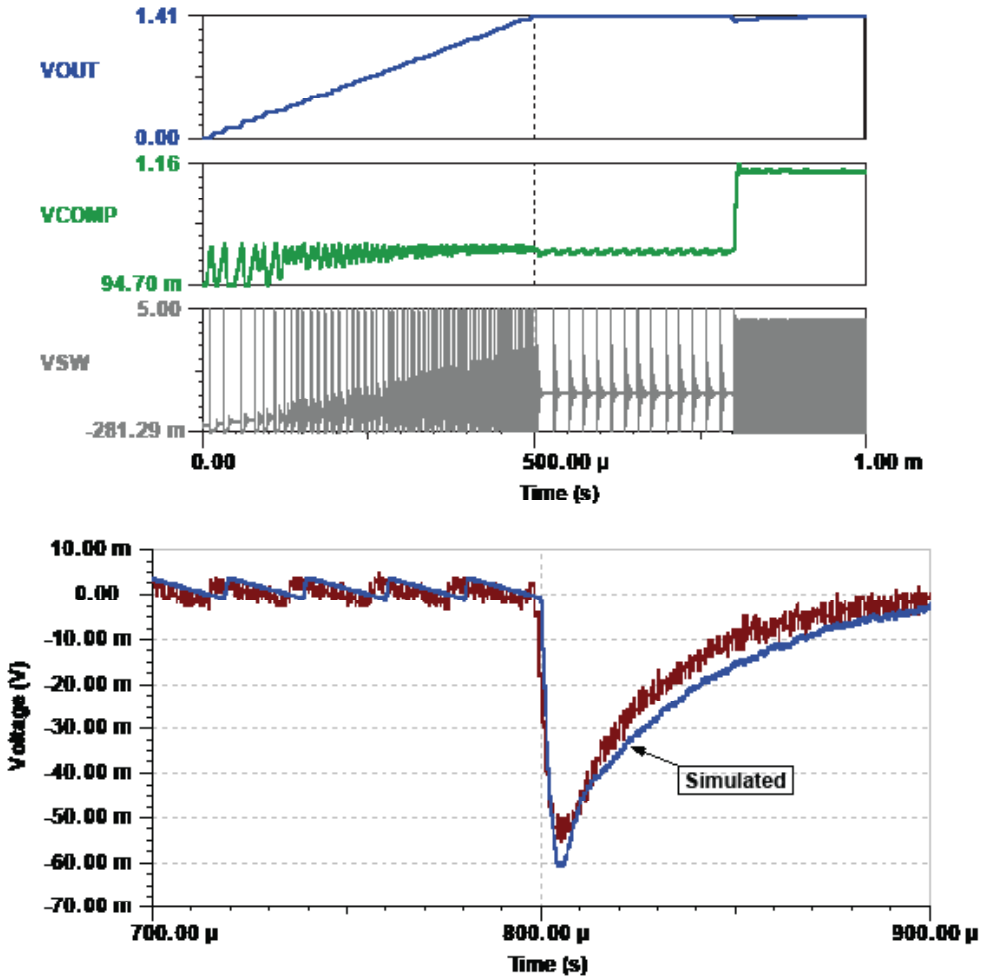

Figure 25 – Time-domain transient analysis (startup [a], load step [b]).

IV. Frequency-Domain Analysis in SPICE

A. Small-Signal Analysis

Let's move now from the time domain to the frequency domain by considering the frequency-dependent characteristics of a switching regulator. Unfortunately, frequency and spectral-domain behavior of a switching regulator are typically not examined sufficiently, and yet there is arguably more to know about the converter in the frequency domain than the time domain. The SPICE analysis of a switching regulator in the frequency domain requires a linearization of the switching behavior. After defining the circuit gain elements and linearizing the switching elements in terms of duty cycle, you can then sweep the frequency of dependent sources and inspect a wide array of power-supply behavior, including:

- Output impedance.
- Control loop phase and gain margin.
- Power-supply rejection ratio.
- Reverse transfer.

Note that a linear model of a switching regulator in SPICE is topology-dependent and should be done in a way to accommodate both CCM and DCM. Once a model is correlated on the bench with actual circuit performance, you can use the model to predict behavior over line, load and component variation. The actual technique for linearizing a switching regulator was originally proposed by Cuk, Middlebrook and Bello in the 1970s and advanced by Vorperian and Meares, Ridley, Basso and others in the 1980s and 1990s. The technique is well beyond the scope of this paper, but let's take a look at how to use the PWM switch model.

B. The PWM Switch Model

Figure 26 illustrates the Vorperian/Meares PWM switch model, a significant advancement in small-signal analysis of switching regulators. The block is parameterized to accommodate voltage- and current-mode control as well as CCM and DCM of the four principle topologies including buck, buck-boost, boost and SEPIC/CUK.

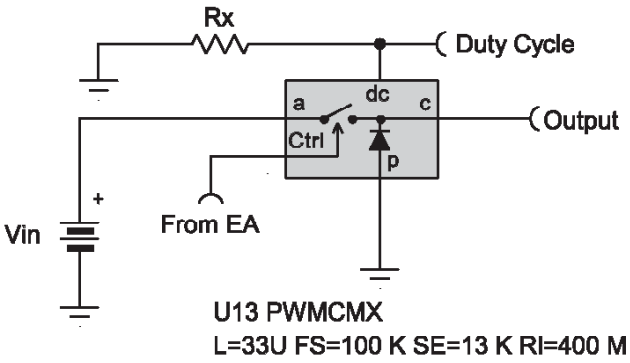

Figure 26 – PWM switch model.

The advancement of this model construct was in its simplification over the complex state-space averaging method first proposed by Middlebrook and Cuk. Furthermore, a rearrangement of external components supports alternate topologies; a detailed explanation of the model can be found in references [15] and [16]. To generate the control-to-output transfer function Vout/VF1 in Figure 27, a large inductor is placed on the output of the EA to break the loop when an AC sweep is performed. Inserting Vstim between the output and the upper feedback resistor (Rupper) will result in a simulation of the phase and gain response commonly referred to as a Bode plot.

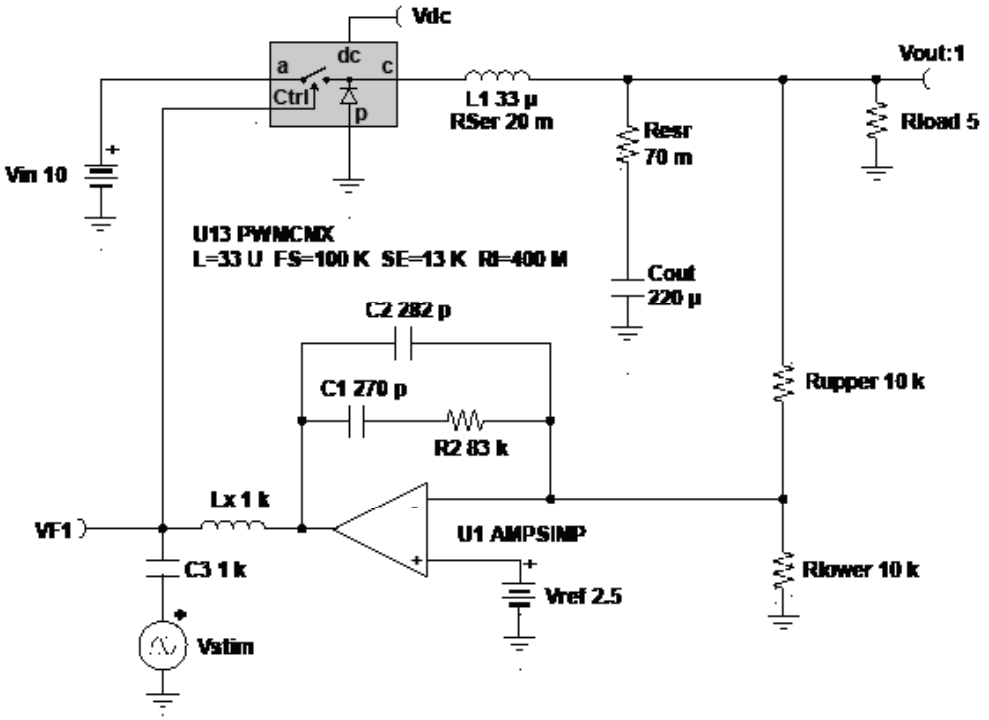

Figure 27 – Current-mode PWM buck.

As this is a current-mode control function, the model includes a parameterized term for the slope compensation ramp, SE. Using the open-loop gain and phase at the desired crossover frequency in Figure 28 (-48.76°, -12.5 dB), you can then use the Venable K-factor equations shown in Solution Set 1 to calculate the EA compensation.

Here, I selected a phase margin of 60° and a crossover of 10 kHz [17].

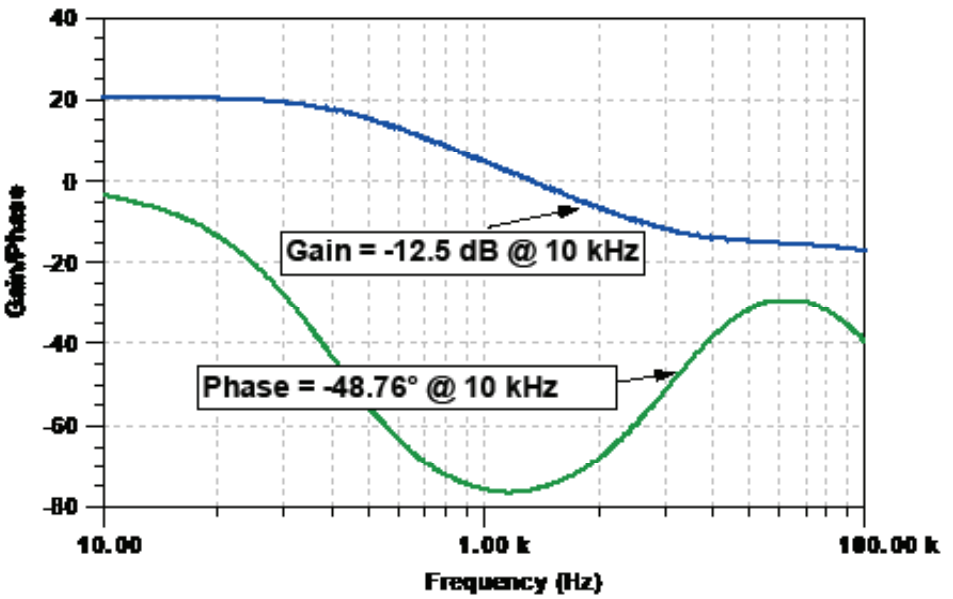

Figure 28 – Open-loop transfer function.

$$Rupper := 10\times10^{3} \quad Fc := 10\times10^{3} \quad pm := 60$$

$$pfc\_oloop := -48.8 \qquad Gfc\_oloop := -12.14$$

$$Gain := 10^{\frac{-Gfc\_oloop}{20}} \qquad Gain = 4.046$$

$$boost := pm - pfc\_oloop - 90 \qquad boost = 18.8$$

$$Kf := \tan\left[\left(\frac{boost}{2}+45\right)\times\frac{\pi}{180}\right] \qquad Kf = 1.397$$

$$C2 := \frac{1}{2\times\pi\times Fco\times Gain\times Kf\times Rupper} \qquad C2 = 281.638\times10^{-12}$$

$$C1 := C2\times\left(Kf^{2}-1\right) \qquad C1 = 267.84\times10^{-12}$$

$$R2 := \frac{Kf}{2\times\pi\times Fco\times C1} \qquad R2 = 82.999\times10^{3}$$

Solution Set 1 – Venable equations to calculate loop compensation.

Using the prescribed compensation and Vorperian switch model, you can generate the small-signal Bode plot shown in Figure 29a and verify the 10-kHz crossover frequency and 60° of phase margin. Because this model automatically calculates the DC bias operating point and can auto-toggle between CCM/DCM, it is said to be a "large signal, average model" that is capable of simulating the large-signal load-step behavior shown in Figure 29b.

A large-signal average model is arguably more valuable than a transient-domain switching model in that it can predict time-domain, load-step response and frequency-domain behavior. Notice the good correlation between predicted small-signal phase margin (slightly under-damped) and the time-domain load-step response.

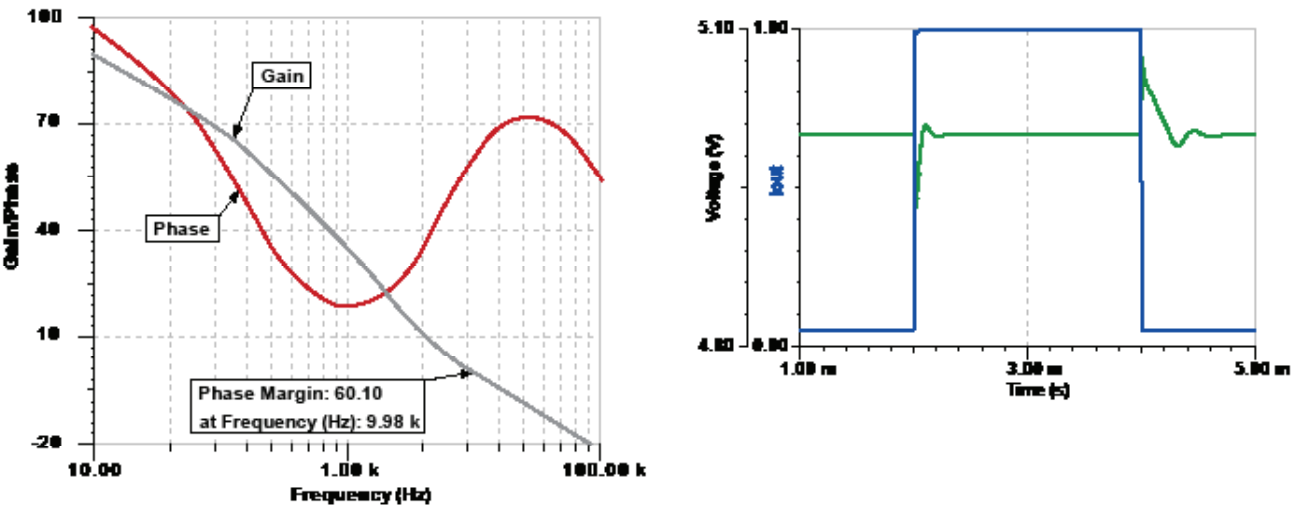

Figure 29 – Vorperian predicted small- (a) and large-signal (b) responses.

C. Output Impedance

The basic power supply is often thought of as having low output impedance (good load regulation) for all frequencies. However, to ensure stability, the feedback amplifier's gain must decrease as you approach crossover. The closed-loop output impedance is defined as the open loop divided by 1 plus the frequency-dependent gain terms and is expressed in Equation 17. The output impedance approaches the open-loop impedance as the gain falls toward crossover (0 dB).

$$Rcl(s) = \frac{Rol}{1 + aG(s) \times H(s)} \tag{17}$$

D. Analyzing Output Impedance

Using the PWM switch model, it is possible to fix the output voltage duty cycle (Ctrl) and sweep the output with a current source to unveil the closed-loop output impedance.

Figure 30 illustrates the output impedance of the converter while varying the output capacitor filter ESR and load.

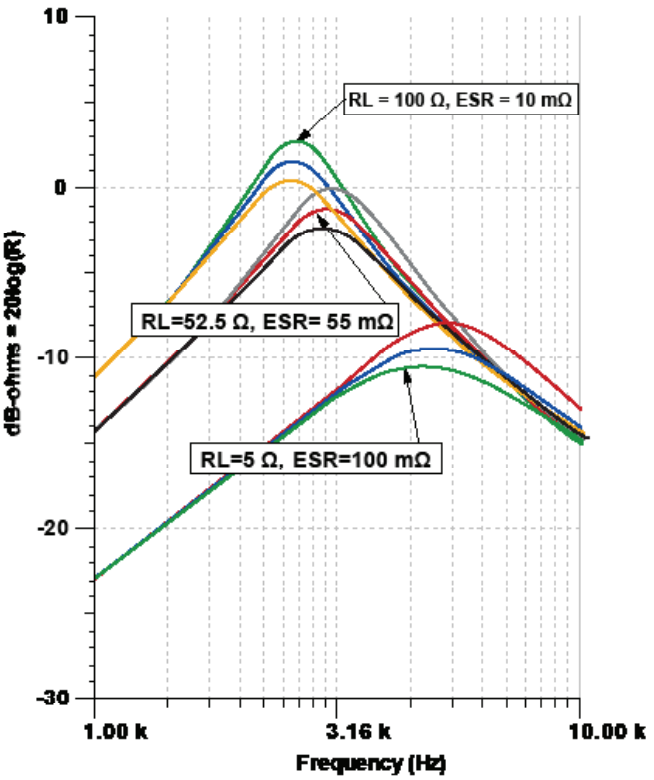

Figure 30 – Predicting output impedance from Vorperian PWM switch model.

Notice that in Figure 30 there are three curve families, each corresponding to a different load. The highest Q family is at light load while the lowest Q family is at the highest load. The capacitor ESR also affects the Q, as it adds a zero in the transfer function. The higher the ESR, the lower the frequency of the zero, and the more damped the response will be.

E. Circuit Q and Control-Loop Stability

Just as there is a relationship between the phase response of an LC output filter and the resonant Q of that filter, so too is there a relationship between the closed-loop Q, Qc, of a converter and phase margin [18] [19]. In fact the relationship can be mathematically quantified in terms of group delay, τ_g. Group delay in this context is the first derivative of the phase angle between the voltage and current waveforms used to create an impedance plot and are expressed in Equation 18.

$$\tau_g \quad \frac{d\theta}{d\omega} \text{ and } Q \quad \tau g \times \pi \times f \tag{18}$$

Phase margin is then calculated in terms of the closed-loop Q as expressed in Equation 19. It is graphically represented in Figure 31.

$$Qc = \frac{360}{2 \times \pi} \times \tan^{-1}\left\{\sqrt{\frac{2}{\left(-1 + \sqrt{1 + 4 \times Qc^4}\right)}}\right\} \tag{19}$$

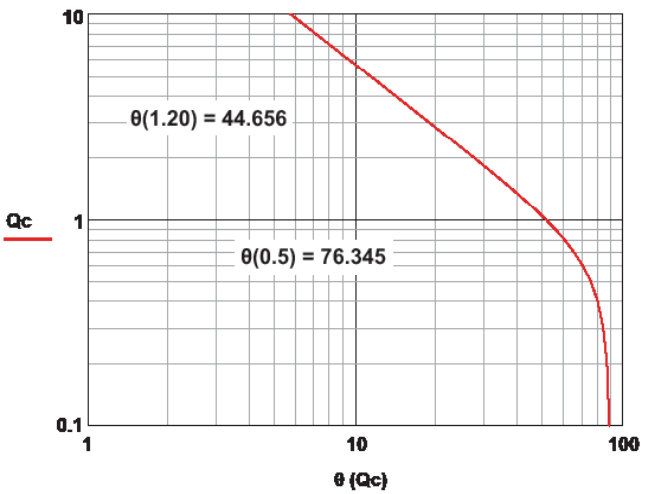

Figure 31 – Phase margin as a function of closed-loop Qc.

The expression approaches a 90° asymptote as Qc approaches zero. From a practical standpoint, a closed loop Qc > 0.5 represents an over-damped response with no imaginary roots in the transfer function. Consequently, this method for determining phase margin is limited to applications where the phase margin is less than about 60-70°. The mathematics presented here are applied to a small-signal SPICE analysis of the TPS40222 EVM in Sections VI-F and VI-G and empirically correlated.

V. Power-Supply Measurement

A. Equipping the Power-Supply Designer

Newer oscilloscopes like the Tektronix MDO4000 mixed-domain oscilloscope and Lecroy Waverunner 610Zi combine a time-synchronized spectrum analyzer with a >1-GHz bandwidth. Optional modules are also available to calculate power-centric behavior including switching and magnetic losses, eye diagrams for phase-noise measurements, safe operating area, power factor and even EMC harmonic pre-compliance measurements [20]. These oscilloscopes are increasingly useful in high-fidelity systems where time and spectral domains need to be examined closely.

Power conversion in RF and precision data-acquisition systems must be carefully analyzed not only in the time domain, but also in the frequency and spectral domains. Time-domain measurements alone are no longer sufficient for characterizing power-supply behavior – even for experienced power-supply designers who can generally "read between the lines." At a minimum, power-supply designers should have access to a spectrum analyzer, network analyzer, function generator and the appropriate signal injectors for measuring power-supply AC behavior [21].

Although a great deal of information can be understood from time-domain measurements, power-supply engineers must now look to the frequency domain to consider power distribution network (PDN) impedance measuring techniques. High-power and high-bandwidth systems found on motherboards and high-fidelity signal processing necessitate a broader understanding of a power converter's RF signature and transient response. The management of a PDN is complex, requiring sensitivity to power-plane impedances, decoupling and the impedance of the voltage regulator itself. Note that PDN impedances are generally below 1 mΩ, and even at high frequencies ESL is typically below 100 pH. The measurement sensitivities are detailed in references [22] and [23].

B. Component Measurement

When it comes to designing a power converter, a theoretical and topological understanding of a converter's behavior is a good starting point, but it is only a starting point. The practical considerations include experience in component selection, component tolerance, component thermal considerations, aging variances and parasitic effects, all of which have a profound impact on circuit performance and reliability. Understanding the effect of leakage inductance in transformers, capacitor self-resonance, ESR, ESL and the DC bias effect of ceramic capacitors are a few more basic considerations that come to mind. Semiconductor component tolerances must also be understood and characterized where possible, particularly in high-volume and high-reliability systems. As such, the artistry of power-supply design is in understanding and developing solutions that address circuit requirements while accounting for subtle component behavior. But how do you determine that behavior when it is often not specified in a data sheet?

Take for example the current transfer ratio (CTR) of the optocoupler often used in isolated control loops. The minimum CTR is generally specified; however the maximum is not. The setup in Figure 32 shows how a DC bias injector and a vector network analyzer (VNA) are configured to accurately measure the CTR gain over frequency. Reference [24] details how to make this measurement.

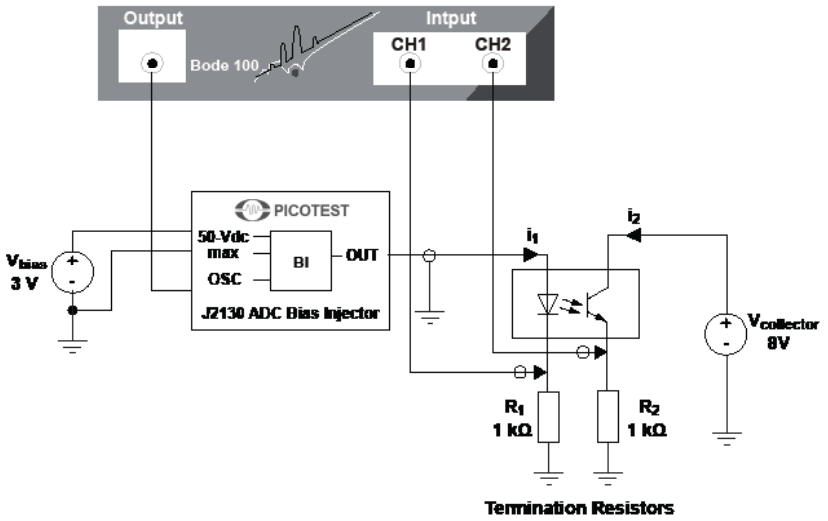

Figure 32 – Measuring an optocoupler's maximum CTR.

In general, power-supply designers tend to underutilize their network analyzers. A VNA equipped with the appropriate signal and bias injectors can be used for a wide range of frequency-dependent measurements, including magnetic leakage inductance, capacitor parasitic inductance (ESL), skin effect, diode emission coefficients, MOSFET impedances and PDN circuit-board impedances with sensitivity in the pico-Henries [25]. For an introduction to signal injectors that can be used to measure component characteristics, see https://www.picotest.com/articles/Introduction%20to%20Signal%20Injectors.pdf. Registration is required to access their application material.

C. High-Fidelity Ripple Measurements

Noise from power-supply regulators and references can limit performance in precision analog and communication products. The noise from regulators contributes to clock jitter that can degrade analog-to-digital (ADC) performance, including bit error rate (BER) and signal-to-noise ratio (SNR). In communication products, phase noise introduces modulating effects in low-noise amplifiers (LNA) [26]. For a topological list of high-fidelity sensitivities associated with linear regulators, see reference [27].

Power-supply ripple and noise measurements are difficult with low-sensitivity oscilloscopes, especially with the trend toward all-ceramic output capacitance where the ripple is typically <10 mV. When making time-domain measurements of low-voltage signals, it is important to consider oscilloscope sensitivity, probe attenuation, system noise, probe grounding, probe input impedance, AC coupling, probe offset and probe bandwidth.

A far better approach is to use a high-sensitivity spectrum analyzer to characterize ripple. Figure 33 shows the output ripple of the TPS40222 evaluation board in the time and frequency domains; this is the same device modeled in the previous section. A higher-sensitivity X2 Tek probe was used to capture the time-domain ripple measurement. The probe has a low attenuation factor to maximize the oscilloscope's vertical sensitivity. See reference [28] for details on probe selection of low-voltage signals. Using a mixed-domain oscilloscope helps to characterize ripple and noise more thoroughly, including parasitic ringing and circuit resonances.

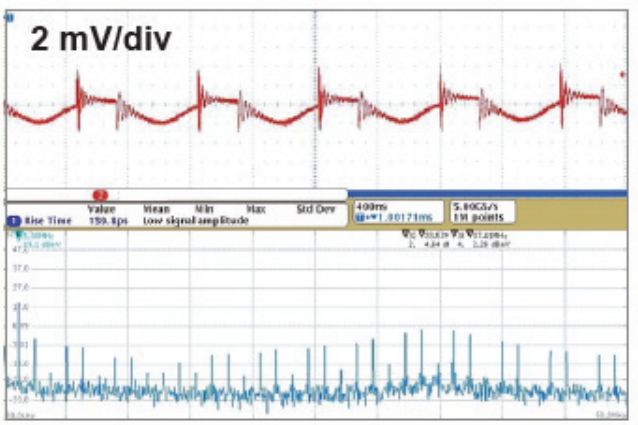

Figure 33 – High-fidelity output ripple measurements.

D. Transient Load-Step Measurements

The bandwidth of a control loop is generally insufficient to address dynamic load changes found in high power processing. To address this limitation, banks of ceramic capacitors are used to quiet the regulator output during load transitions that easily exceed 100 A/µs. Unfortunately, characterizing this behavior on the bench has been performed erroneously, failing to consider the effect of interconnect impedance, resistive load ESL and electronic load output capacitance.

Table 4 compares a solid-state current injector, the J2111A, to a typical electronic load (e-load). Although highly effective for characterizing a converter's efficiency, the e-load rise/fall and interconnect impedance limit their effectiveness in measuring processor load-step behavior. In addition, the output impedance of some e-loads can be invasive (usually capacitive), altering the overall loop response of the regulator under test. As such, it is important to characterize the output impedance of your e-load or use noninductive, resistive loads when measuring load-step response and control-loop stability.

	J2111A Injector	**E-Load**
Rise/Fall	20 nsec	0.5 µ-20 µsec
Bandwidth	40 M	10 k-100 kHz
Polarity	Bipolar	Unipolar
Resolution	<1 µA	10 µA-10 mA
Monitor	1 V/A, 40 MHz	Varied
Invasive?	No	Yes

Table 4 – Comparing a current injector to an electronic load (e-load).

VI. Frequency-Domain Measurements

This brings us to frequency-domain measurements. I will use the TPS40222 evaluation module (EVM) and an OMICRON Lab Bode 100 VNA with various Picotest signal injectors. In this section, I will show how to setup and measure:

- Input filter stability.
- Traditional Bode plots.
- Power-supply rejection ratio (PSRR) and reverse transfer.
- Output impedance.
- Noninvasive phase measurement.

A. Converter/Input Filter Impedance

Switching regulators exhibit negative input impedance that is most severe at maximum output power and minimum input voltage. The effect can cause sustained input oscillations and overvoltage stress if the net impedance between the filter and the negative resistance of the converter become equal. This is often referred to as the Middlebrook Stability Criteria, named after R.D. Middlebrook, who originally developed the mathematics in the mid 1970s [29].

Current-mode-controlled converters generally have higher sensitivity to input stability due to their higher negative resistance bandwidth. You can apply a "loaded Q" specification to tame the effect where input damping is applied to the filter [30]. Characterizing the impedance of an input filter and power-supply input/output impedances is a straightforward exercise with the appropriate equipment.

Figure 34 illustrates the use of a high-bandwidth current injector, the J2111A, interfacing with a VNA that presents a variable-frequency-load current to the filter while examining the response on CH1 and CH2. The load current is mirrored at the IMON BNC output of the J2111A and is connected to CH1 of the VNA. The input filter voltage is presented to channel two (CH2) and the result is the output impedance of the filter. If the output impedance of the filter is greater than the open-loop input impedance of the power supply at any frequency, sustained oscillations may occur at that frequency. Figure 35a illustrates the negative input impedance to the converter feed by an 18-inch power cord. Figure 35b plots the filter response.

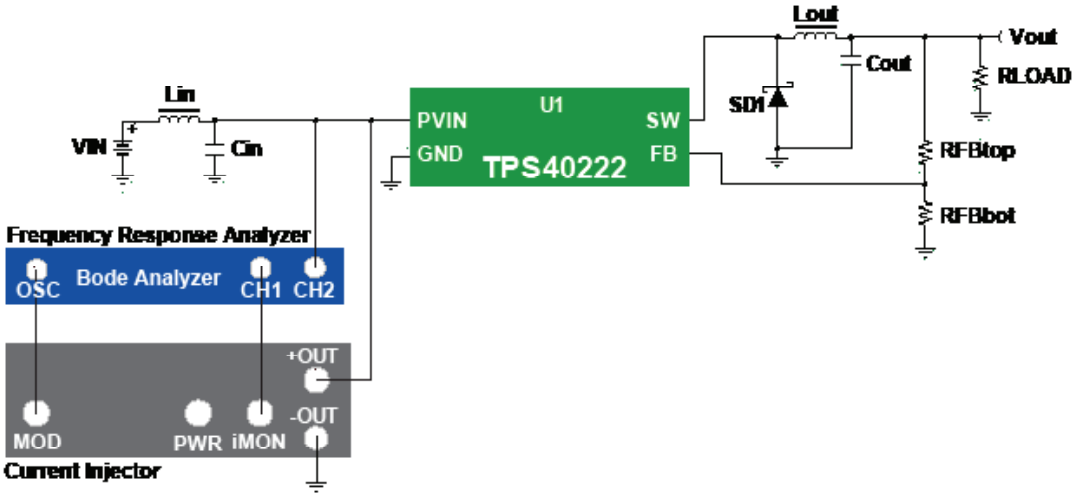

Figure 34 – Filter/converter impedance measurement setup.

Coupled with a network analyzer, the current injector can measure the output impedance of all types of circuits and systems including voltage regulators, power buses and batteries. It can also noninvasively measure the stability of a combined input filter and negative resistance of a switching power supply, or the phase margin of a linear or switching regulator without the need to break the control loop. See http://www.picotest.com for application details; registration is required to access their application material.

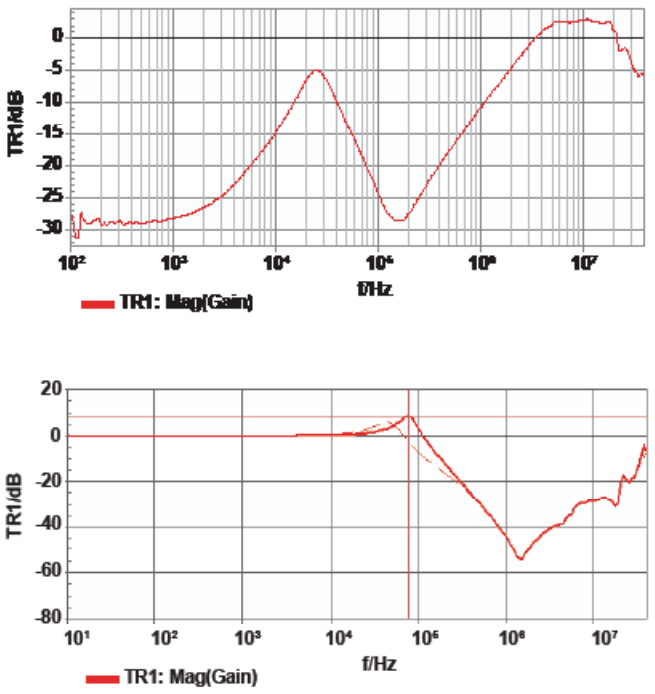

Figure 35 – Converter negative input impedance (a) and filter response (b).

B. Bode Plot

The Bode plot is a measure of the open-loop gain/phase response of a closed-loop system, an essential measurement in verifying a stable response to line and load changes. Making this measurement requires a network analyzer. Figure 36a illustrates the basic setup and Figure 36b illustrates a typical response. The dark gray trace is the gain and the light gray trace is the phase.

The analyzer's variable-frequency oscillator is applied to an injection transformer to introduce a small-signal perturbation into the control loop while measuring the voltage at each side of the injection transformer. One side of the transformer is the input signal while the other side is the output signal. The division of the two results in the loop gain and phase commonly referred to as a Bode plot.

Remember that the Bode plot is a "small-signal" analysis, and as such, the injected signal must be small relative to the AC output of the error amplifier. Excessive signal amplitude will cause an erroneous result [31] [32]. In general, start with a -20-dBm signal into a 4.99-ohm injection resistor and increase until changes in gain or a nonlinearity are observed. Once you observe a gain change, lower the injection signal by 3 dBm and take your final measurement.

The criterion for stabilizing a negative-feedback control loop requires that the phase lag in the control loop does not exceed 360°. Some margin to accommodate line and load variation,

variations in temperature and component tolerance is also required; in general, many power-supply designers believe that 45° of margin from 360° is adequate. But if you test your converter over temperature, can you then get away with less? Unfortunately phase margin impacts more than stability – PSRR and output impedance are also affected by phase margin, so in general maintaining a minimum of 45° of phase margin is good practice for high-fidelity systems.

Transient load-step analysis as a means to characterize stability is a mistake for several reasons, not the least being that it affords designers no insight into the impending doom associated with control-loop sensitivities (including but not limited to the RHPZ previously discussed) [33].

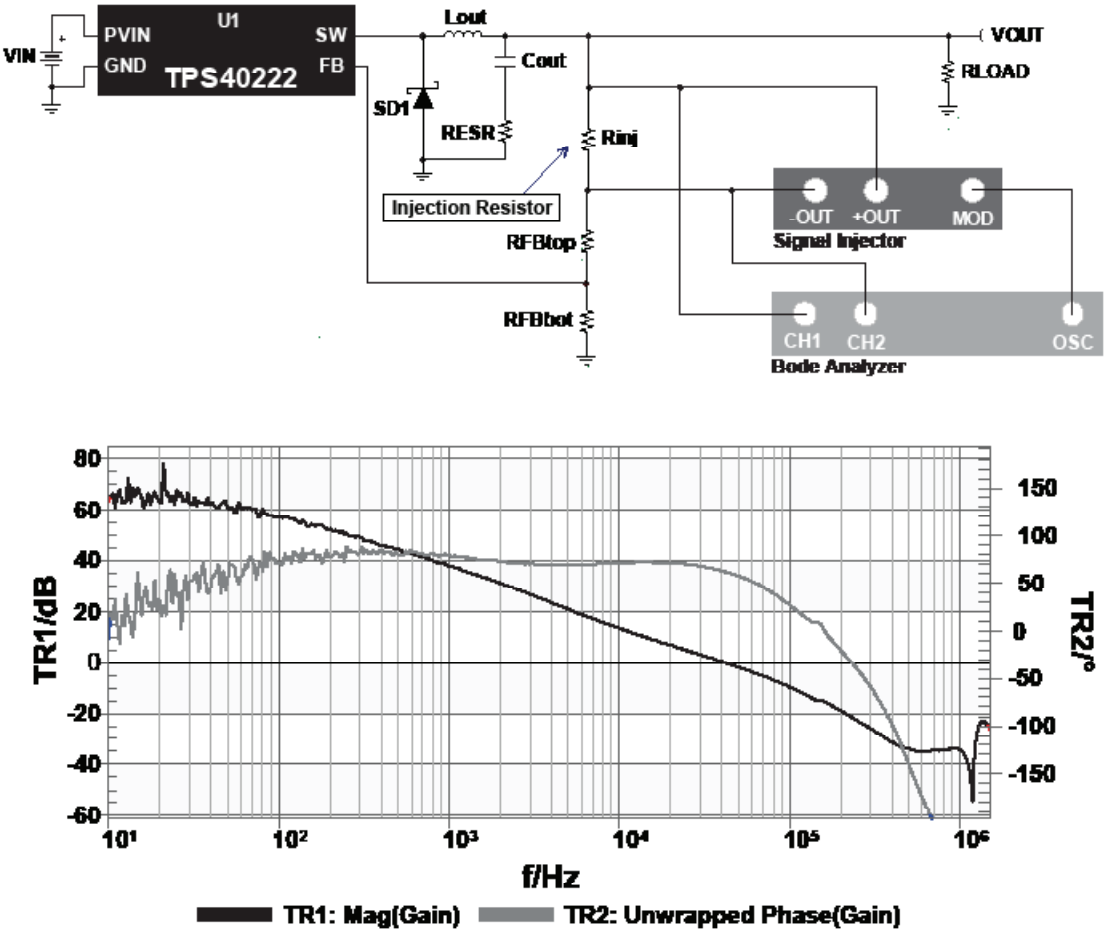

Figure 36 – Bode plot measurement setup (a) and typical response (b).

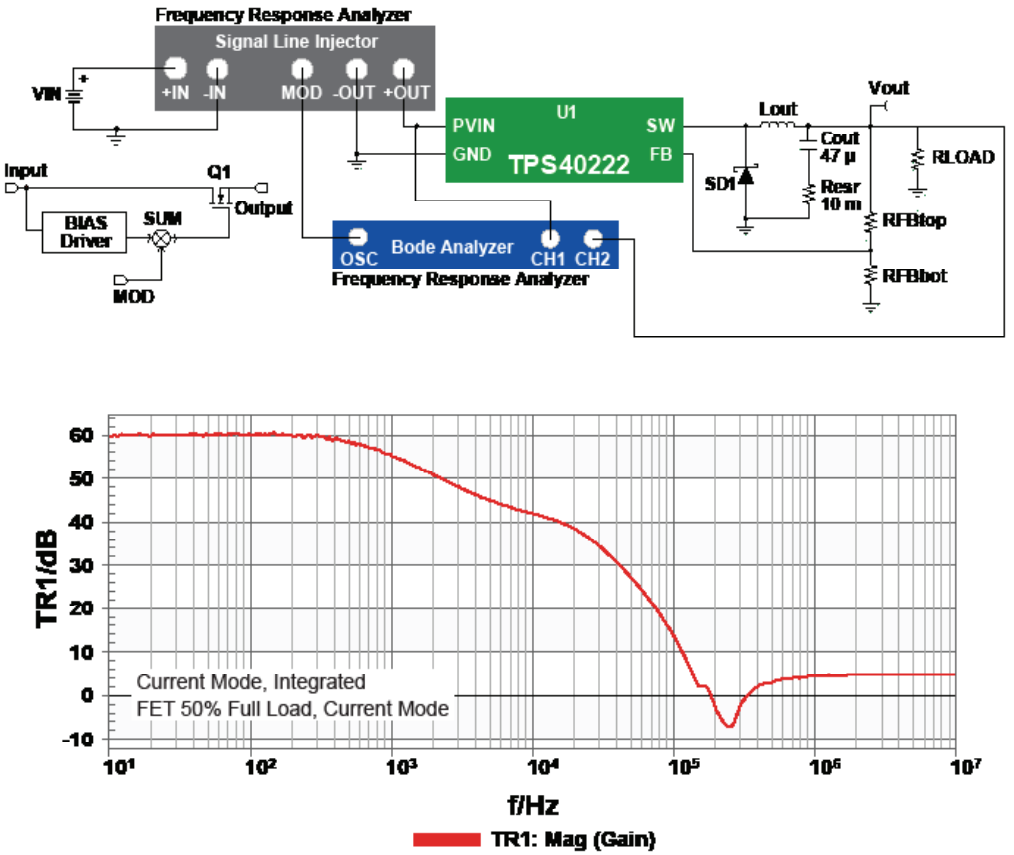

Figure 37 – PSRR measurement setup and example of a typical plot.

C. PSRR Measurement

PSRR is a delicate measurement requiring a low noise floor. The output amplitude can be significantly impacted by the operating current and the total storage capacitance at the input and load. Using a line injector that interfaces with a network analyzer is an effective way to achieve an accurate measurement; the measurement setup is shown in Figure 37 and a detailed explanation on the setup is given in references [34] and [35].

D. Reverse Transfer

Reverse transfer is essentially the inverse of PSRR, where PSRR is the ability of a power converter to attenuate input noise as seen at the output. Reverse transfer is the attenuation of output disturbances as seen at the input; this measurement is especially important in distributed power architectures. Reverse transfer is the assessment of I_{in}/I_{out} or the input current resulting from a perturbation of the output current. This is more often an issue with linear regulators, as the stability of linear regulators tends to be poor compared to switching regulators. At low frequency, the input and output currents are approximately equal in a linear regulator, resulting in a 0-dB reverse transfer. Poor regulator stability, however, results in a gain near the bandwidth of the regulator that can compromise EMI and distributed power systems. Figure 38a illustrates a typical setup for measuring the I_{in}/I_{out} transfer function and Figure 38b illustrates the measured effect that phase margin has on reverse transfer. A detailed discussion can be found in reference [36].

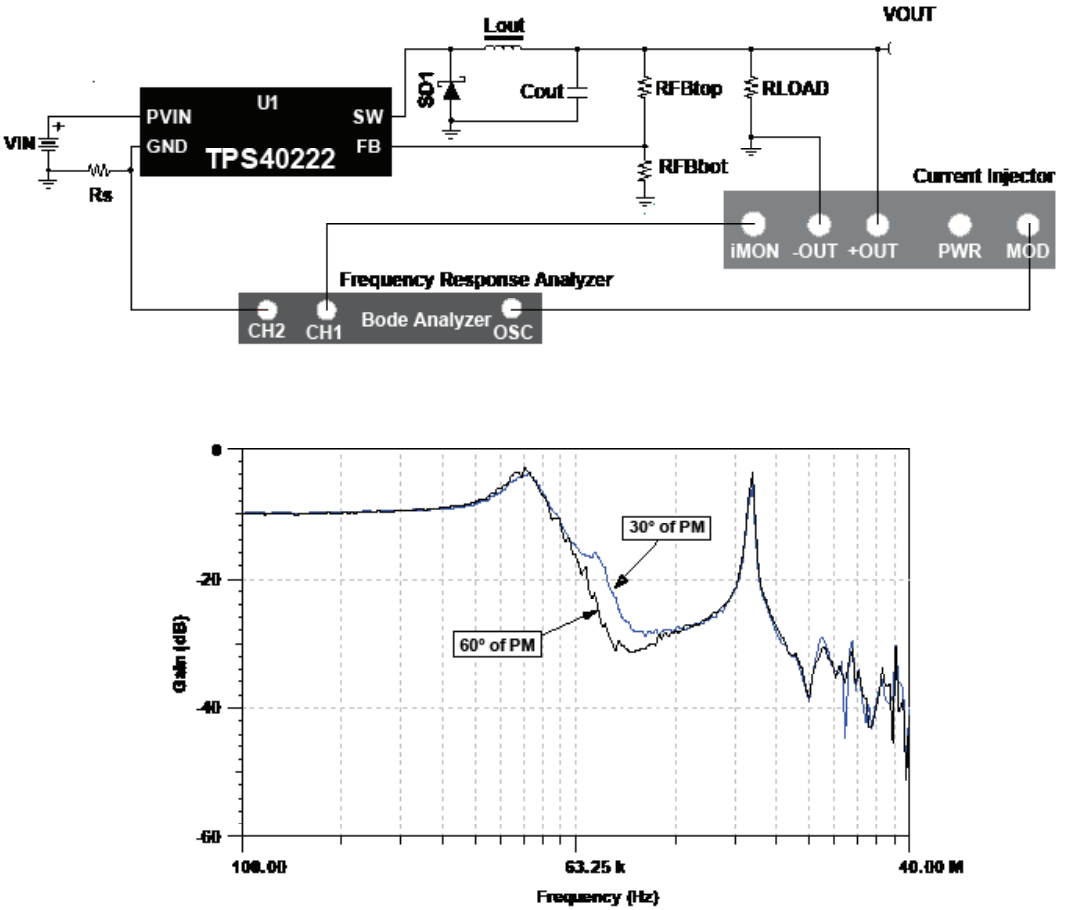

Figure 38 – Reverse transfer setup (a) and measurement (b) at 30° and 60° of phase margin.

E. Output Impedance

As you saw earlier, the closed-loop output impedance of a regulator is a frequency-dependent parameter given by Equation 20.

$$Rcl(s) \quad \frac{Rol}{1+\alpha G(s)\times H(s)} \tag{20}$$

The output impedance is one of the most informative and easiest measurements you can make of a power converter. Output impedance affects regulation, transient response and stability. To plot this frequency-dependent function, use a network analyzer to sweep the frequency of the load current and measure it along with the output voltage to calculate Rcl(s).

Figure 39 illustrates the basic setup using the J2111A current injector and network analyzer, as well as the typical behavior. Notice that the output impedance (dark gray trace) is very low at DC (because of DC, gain is high), but increases with frequency.

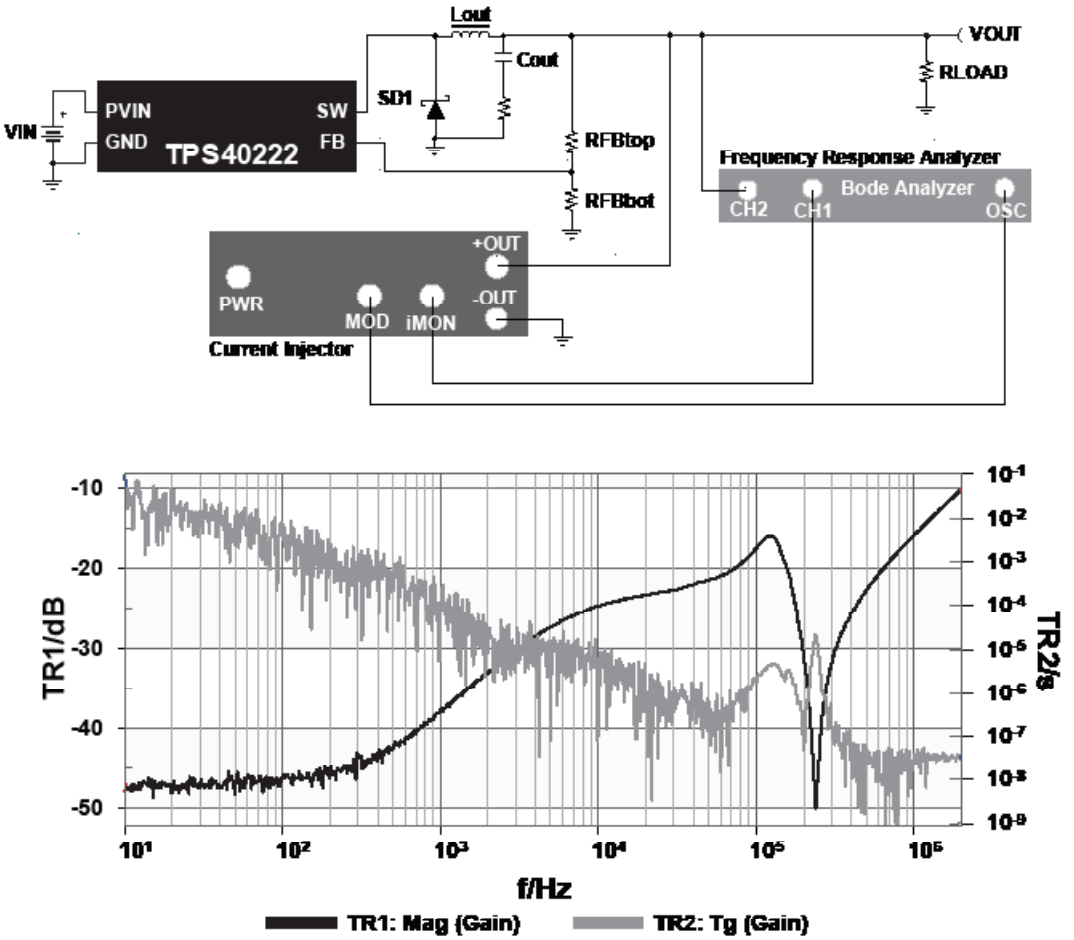

Figure 39 – Output impedance measurement setup and typical response. The light gray trace is a measure of group delay measured in seconds.

F. Noninvasive Phase Measurement

Many linear voltage regulators and some switching converters (with integrated FET) are of the fixed-output variety, with an internal feedback voltage divider to set the output voltage. Although this helps eliminate external components and improve output-voltage regulation tolerance, it also makes it impossible to do traditional Bode stability measurement. Section III-F discussed how the phase response of the output filter is dependent on the filter Q. Similarly, the closed-loop quality coefficient, Qc, of the regulator is representative of a converter's stability.

One manufacturer, OMICRON Lab, uses the relationship between Qc and phase margin to noninvasively predict stability (NIP). You can examine circuit resonances and infer stability from a plot of output impedance and group delay. But how does this method compare with traditional Bode plots in measuring stability?

To answer this question, the TPS40222 EVM (the same device used for previously developing a time-domain model) was measured using both the NIP technique and the conventional Bode plot method. Note that the TPS40222 is internally compensated and the evaluation module has >60° of phase margin. Also recall that when approaching >60° of phase margin, it becomes increasingly difficult to measure phase margin with the NIP technique, as imaginary roots in the transfer function are lost (see Section IV-E).

To adequately compare the two methods requires reducing the phase margin of the EVM. Since the TPS40222 is internally compensated, the stability was lowered by reducing the output capacitance from 3 x 22 µF to 1 x 22 µF. The Bode plot of the modified TPS40222 EVM is shown in Figure 40. The measured phase margin is 31.6° at a crossover frequency of 100 kHz.

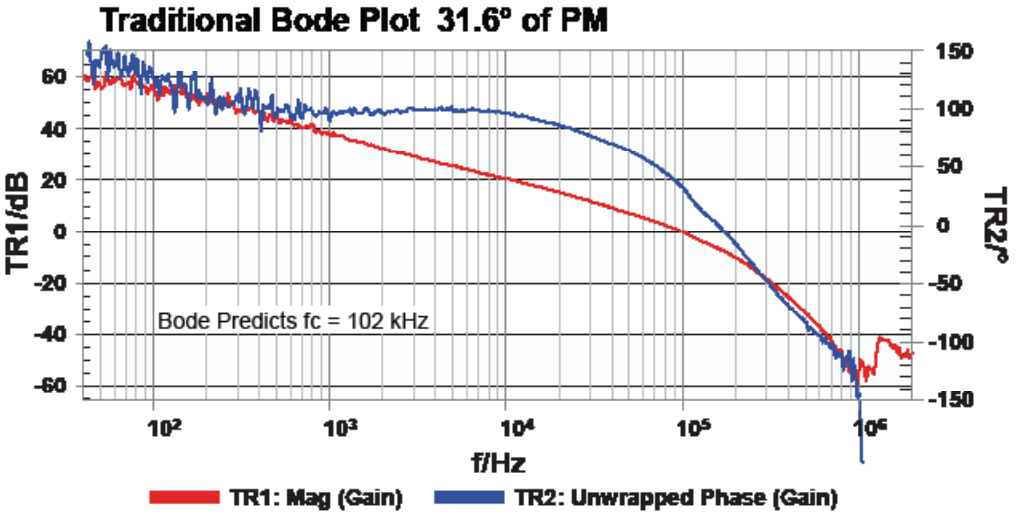

Figure 40 – Bode plot of modified TPS40222 EVM.

G. Bode/NIP Correlation in SPICE

To further illustrate the NIP technique and compare it with a Bode analysis, I developed an average model of the TPS40222 using the Vorperian PWM switch model. The circuit model of the EVM is shown in Figure 41 and predicts the Bode plot, output impedance and group delay for comparison with measurement results. The output capacitance in the simulation was reduced to from 22 µF to 15 µF to include the effect of DC bias.

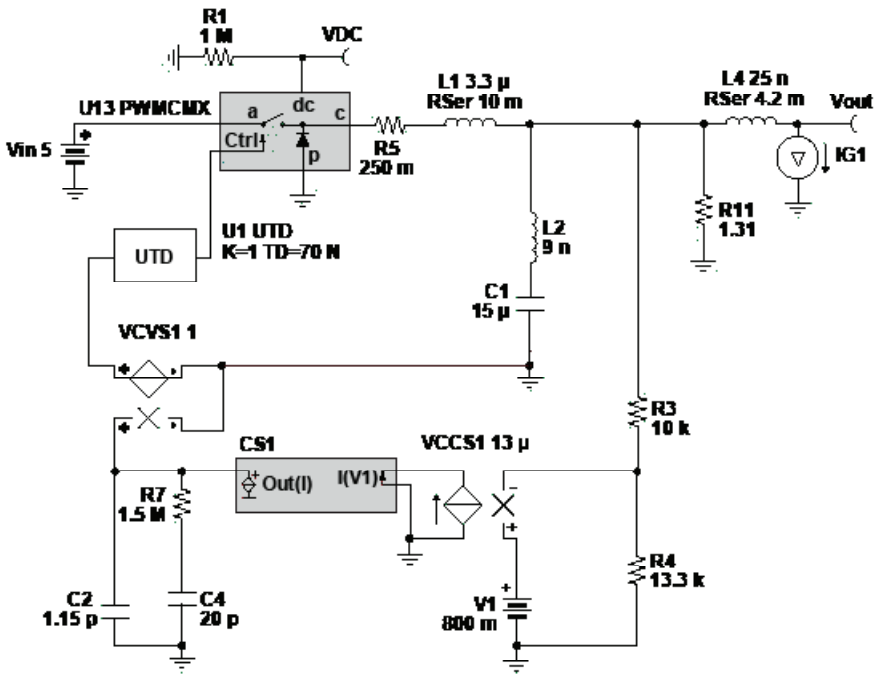

Figure 41 – TPS40222 EVM small-signal average model used to compare Bode and NIP.

Figure 42 shows the correlation between measured and simulated output impedance. Clearly the model is highly representative of the EVM, and with this correlated SPICE model it is possible to plot and compare the predicted Bode response and group delay. Figure 43a and 43b show the result. You can use the peak group delay to calculate closed-loop Qc (see Section IV-E), from which you can then calculate phase margin.

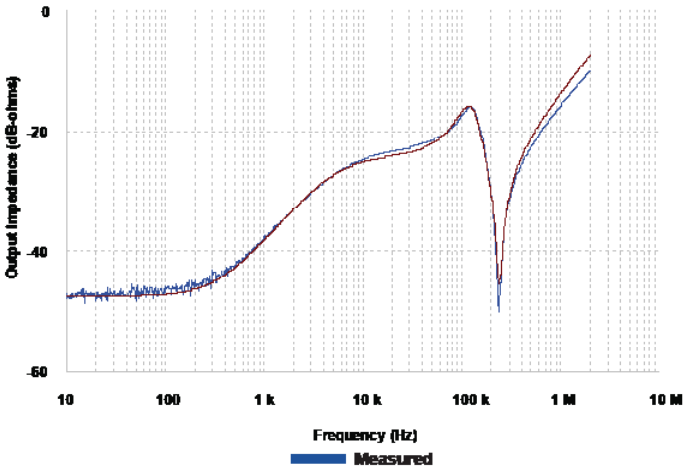

Figure 42 – Simulated and measured output impedance of modified TPS40222 EVM.

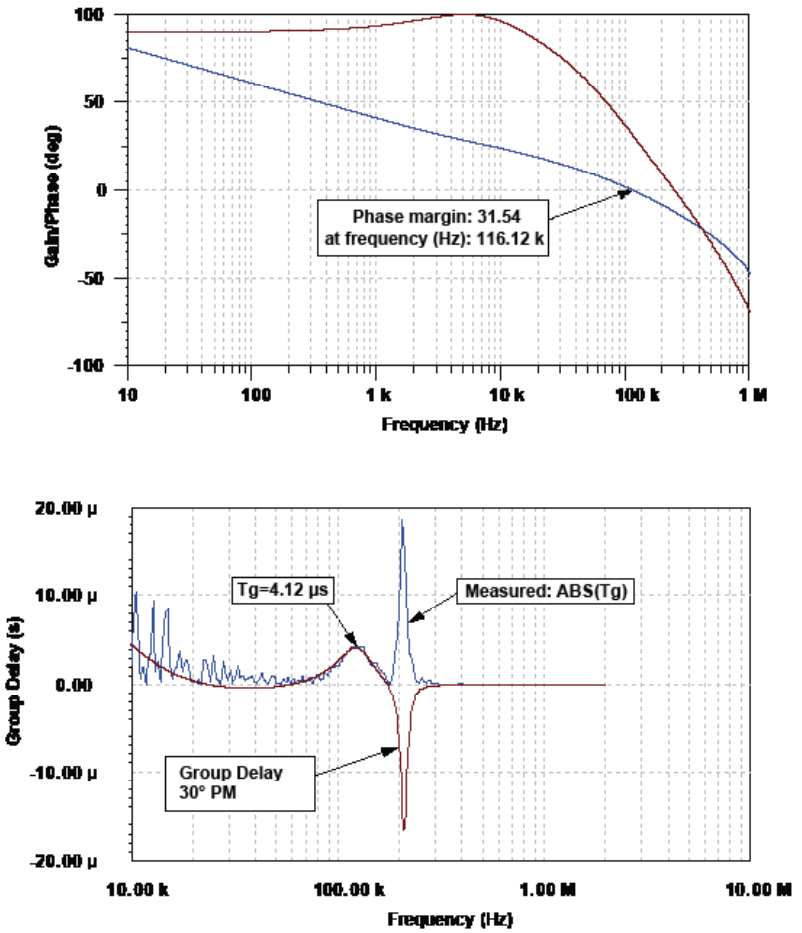

Figure 43 – Bode plot correlation (a) with noninvasive phase measurement (b).

Recall that a Bode plot assumes that the worst-case stability point of a control loop occurs at the crossover frequency (Gain = 0 dB) and that the phase margin at this point would give you your worst-case stability figure of merit. But this is not necessarily true. For example, the modified TPS40222 evaluation board exhibits a Bode plot phase margin of 32° and a loop crossover of 100 kHz. From this, you can calculate a closed-loop Qc of 1.814 using the expression in Equation 21.

If you measure the output impedance and group delay, you can determine closed-loop Qc directly. That measurement was taken on the TPS40222 EVM (Figure 39) where the Bode predicted 32° of phase margin and -6.8 dB of gain margin.

The peak group delay occurs at 126 kHz, corresponding to the maximum response (point closest to [1,0] on a Nyquist plot), not at 100 kHz as the Bode plot predicted. At that frequency, the Bode plot indicates 14.2° of phase margin and -3.5 dB of gain. If you evaluate Qc at this point (Equation 22), you realize that the length of the vector to [1,0] is shorter at this frequency; hence it is the actual worst-case stability point.

In cases such as this one, the NIP method offers a **better** assessment of stability than the traditional Bode plot [37].

$$T \quad 10^{\frac{0}{20}}, T \quad 1 \quad Qc \quad \left| \frac{1}{1 \quad T \times \cos(32°) + \sin(32°) \times i} \right| Qc \quad 1.814 \tag{21}$$

$$T \quad 10^{\frac{3.5}{20}}, T \quad 0.668 \quad Qc \quad \left| \frac{1}{1 \quad T \times \cos(14.2°) + \sin(14.2°) \times i} \right| Qc \quad 2.575 \tag{22}$$

H. Design Analysis vs. Design Synthesis

Web-based design synthesis and analysis tools like WEBENCH designer tools accelerate the design and analysis process. In a highly developed server-based environment, a power-converter solution can be synthesized, mathematically analyzed and cost-/performance-optimized based on simple input and output design specifications. With WEBENCH circuit design tools, users specify key design parameters including desired solution size, efficiency and input-output requirements. The tool then sorts through thousands of possible solutions; once a solution is selected, it completes a detailed performance analysis including component stress analysis, AC stability, transient analysis and thermal analysis. Although designed to be accurate, the results must always be carefully validated on a real bench and in the field before production.

VII. Conclusions

The writing of a power-supply specification sheet is the essential first step in advancing a robust power-converter design – a design that affects every electronic subsystem. As such, the development of the specification sheet needs to be a collaborative effort. Developing mathematical and/or behavioral models for a power converter helps designers advance their solutions more quickly with higher levels of design confidence.

However, the effective simulation of a power supply requires experience, both in power-supply design and in the simulation tool used for the analysis. Any component model used in a simulation must be understood and verified to ensure simulation fidelity. This paper demonstrated by example that SPICE is a practical simulation environment in which to build a power-supply analysis, but ultimately performance must be validated on the bench. Over time, models in your library improve, and this further helps accelerate product-to-market cycle time.

Lastly, as measurement fidelity becomes increasingly important in RF and high-performance analog circuits, power-supply designers must be equipped with the latest measurement equipment and measurement techniques outlined in this paper. Collectively, SPICE analysis and careful measurement techniques help accelerate a power-supply design to specification compliance.

VIII. Acknowledgement

I would like to thank my colleagues Mike Segal, John Betten and Chanakya Mehta for their excellent review of this paper and presentation. In addition I would also like to thank Bill Brady of Tektronix Inc. for lending support and test equipment to build this presentation, including a powerful mixed-domain oscilloscope and high-fidelity test probes. I am especially grateful to Steve Sandler and Charles Hymowitz of Picotest and AEi Systems for the many hours they spent discussing SPICE and the principles of high-fidelity power-supply measurement.

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