Technical Article

Understanding MOSFET Data Sheets, Part 6 – Thermal Impedance

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It' s been a while since posting entries 1 through 5 in this series, but I find myself still fielding several questions about FET data sheets, particularly those parameters found in the thermal information table. That's why today, I want to address the data-sheet parameters of junction-to-ambient thermal impedance and junction-to-case thermal impedance that seem to be the cause of much confusion. Note that if you are more of a visual learner, you can watch the video "Understanding MOSFET data sheets - thermal impedance".

First, let's define exactly what these parameters mean. When it comes to thermal impedance, it's hard to find consistency in the nomenclature of these parameters within the FET industry – sometimes even within the same company. For the sake of this post, I will use the parameters defined in Figure 2 and Table 1. If you think of heat flow as analogous to current, it's easy to envision the resistance network by which the heat can dissipate from the junction or die shown in Figure 2. The sum of this network is what we call the junction-to-ambient thermal impedance ($R_{\theta JA}$) of the device.

Described mathematically by Equation Figure 1, $R_{\theta JA}$ is the parallel summation of impedance through the top of the package to the ambient environment and through the bottom of the package, then through the printed circuit board (PCB):

$$R_{\theta JA} = \left(\frac{1}{R_{\theta JB} + R_{\theta BA}} + \frac{1}{R_{\theta JT} + R_{\theta TA}} \right)^{-1} \qquad (1)$$

Figure 1. (1)

Of the four parameters that sum up to $R_{\theta JA}$, the FET itself dictates only two: $R_{\theta JB}$ and $R_{\theta JT}$. Because in practice it is much easier to dissipate heat through the PCB, $R_{\theta JB} + R_{\theta BA}$ is usually much smaller than $R_{\theta JT} + R_{\theta TA}$, and you can neglect the latter term in Equation Figure 1. (This is may not be the case if the device has DualCool™ packaging or an exposed metal top. Typical $R_{\theta JT}$ for a standard 5mm-by-6mm quad flat no-lead (QFN) package is on the order of 12-15˚C/W, but you can reduce it to 2-3˚C/W with an exposed metal top and techniques that put the silicon die closer to the top of the package. All of this is for naught, however, unless you employ some technique to reduce $R_{\theta TA}$, such as applying a heat sink to the device or administering airflow.)

When FET vendors discuss junction-to-case thermal impedance ($R_{\theta JC}$) in the data sheet, while technically they could be referring to $R_{\theta JB}$ or $R_{\theta JT}$, you can usually assume that they are talking about $R_{\theta JB}$.

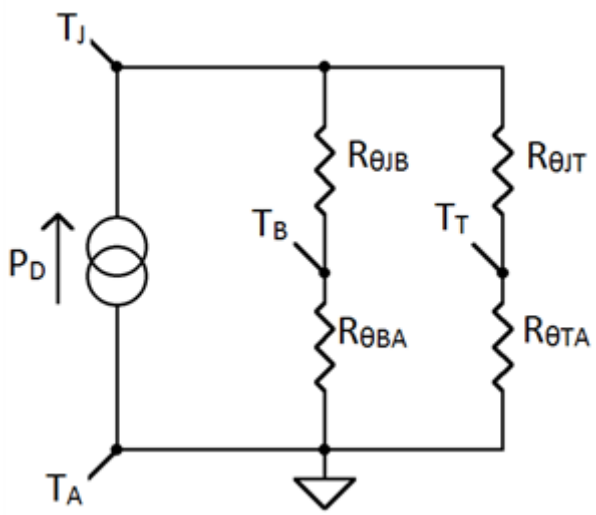

Figure 1. Resistance Network between the Silicon Junction and Ambient Environment

Parameter	Definition
P_D	Power dissipated in the metal-oxide semiconductor field-effect transistor (MOSFET) silicon die
T_J	Temperature of the silicon junction
T_A	Ambient temperature
T_B	Temperature of the bottom of the MOSFET package
T_T	Temperature of the top of the MOSFET package
$R_{\theta JB}$	Thermal impedance from the MOSFET junction to the bottom of the package
$R_{\theta BA}$	Thermal impedance from the bottom of the package to the ambient environment, usually dictated by the PCB
$R_{\theta JT}$	Thermal impedance from the MOSFET junction to the top of the package
$R_{\theta TA}$	Thermal impedance from the top of the package to the ambient environment
$R_{\theta JA}$	Thermal impedance from the MOSFET junction to the ambient environment, comprising the four previous thermal impedances in a resistance network

Because $R_{\theta BA}$ is completely dependent on board conditions (PCB size, copper thickness, number of layers) it is impossible to know the total $R_{\theta JA}$ without knowing $R_{\theta BA}$ as well. Regardless, $R_{\theta BA}$ will be the dominant impedance dictating $R_{\theta JA}$. In practical applications, it can be as high as 40˚C/W, all the way down to ~10˚C/W for well-designed systems. FET vendors can only guarantee $R_{\theta JC}$, but typically, they do provide some $R_{\theta JA}$ for worst-case scenarios. For example, transistor outline (TO)-220 or TO-263 (D2PAK) data sheets list the measured $R_{\theta JA}$ with the device suspended in air (see Figure 3). QFN devices, on the other hand, are measured on 1-inch copper and min Cu minimum copper board (see Figure 4). The maximum values provided in the data sheet and shown in Figure 4 are 25% above those values measured in characterization. Because they are almost entirely dependent on the package's interaction with the surrounding board, and less on die size or thermal mechanics inside the device, they are more or less industry standards for a given package.

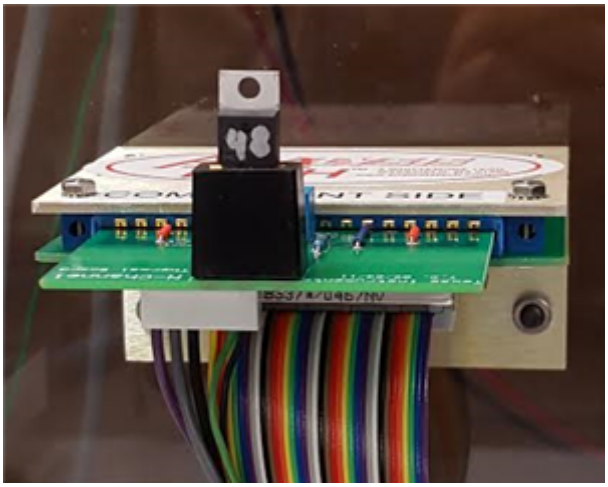

Figure 2. TO-220 Device Suspended in the Air for $R_{\theta JA}$ Measurement

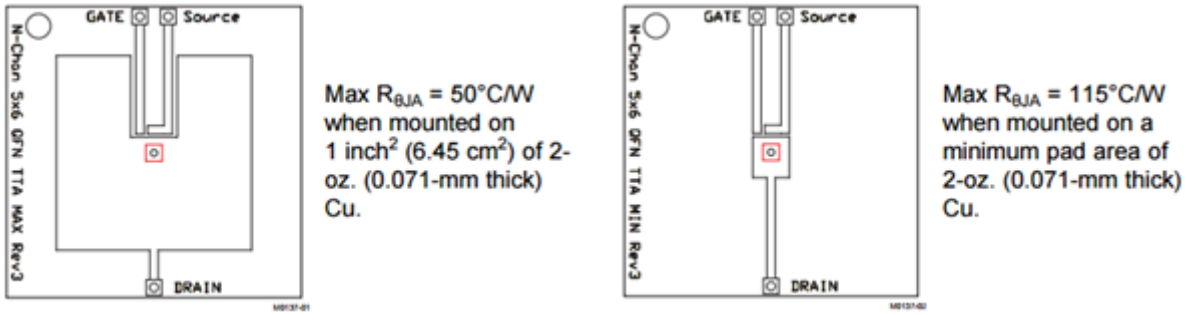

Figure 3. Small Outline No-lead (SON) 5mm-by-6mm $R_{\theta JA}$ Measurements as They Appear in the Device Data Sheet

I could write another 13 pages elaborating on these values, but since Darvin Edwards beat me to the punch with an excellent application note, I'll just redirect you there.

Also, please check out Manu Balakrishnan's similar breakdown of these thermal parameters (part 1 and part 2), particularly regarding how they pertain to selecting the right FETs for power tools where thermal performance is critical.

Visit TI's Thermal Analysis landing page for access to the tools and information needed to understand and design thermal systems including design tools, lab analysis recommendations, education, and FAQs.

I think this should be the final entry of this series, which I never anticipated would grow to six installments. But hey, that's what spinoffs are for, right? Please join me next month, when I will discuss MOSFET selection methods for a wide array of applications. In the meantime, consider one of TI's MOSFETs for your next design.

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