User's Guide

TPS7A14EVM Evaluation Module

ABSTRACT

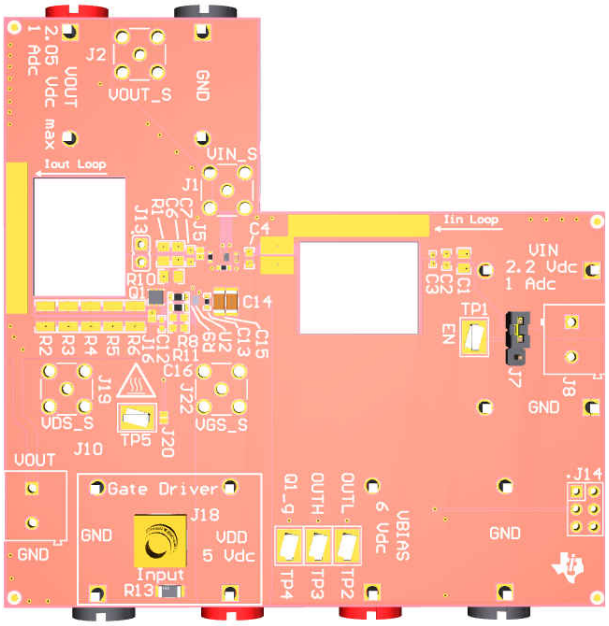

Figure 1-1. TPS7A14EVM-058 Evaluation Module

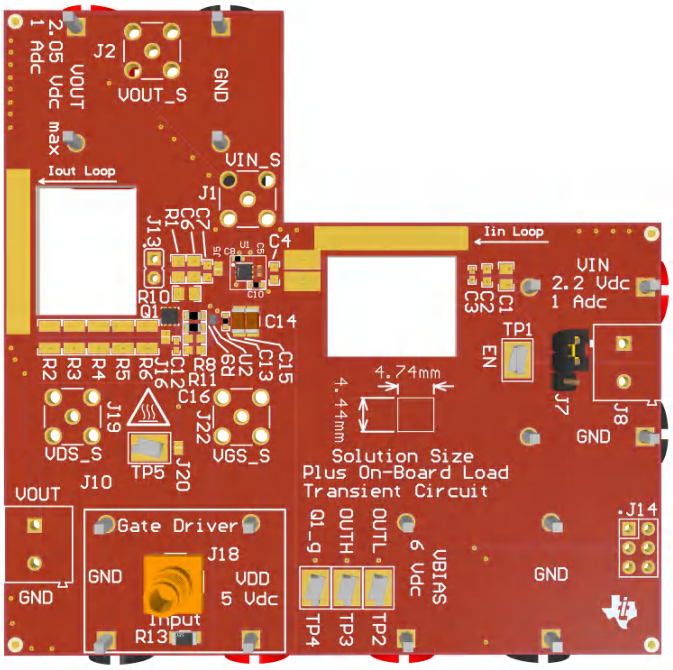

Figure 1-2. TPS7A14EVM-095 Evaluation Module

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Trademarks

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1 Introduction

The Texas Instruments TPS7A14EVM-058 and TPS7A14EVM-095 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7A14 LDO voltage regulator. As shown in Table 1-1, the TPS7A14EVM-058 contains one TPS7A14 LDO voltage regulator in the DSBGA package and the TPS7A14EVM-095 contains one TPS7A14 LDO voltage regulator in WSON package . An optional load transient circuit is also included to assist the user with high-speed load transient testing. An input current loop is included that allows fast measurements of the input current.

Table 1-1. Device Information

EVM ORDERABLE NUMBER	V_{OUT}	PART NAME	PACKAGE
TPS7A14EVM-058	0.8 V	TPS7A1408PYBKR	6-pin DSBGA
TPS7A14EVM-095	1.8 V	TPS7A1418PDRVR	6-pin WSON

2 Setup

This section describes the jumpers and connectors on the EVM, and how to properly connect, set up, and use the TPS7A14EVM-058 and TPS7A14EVM-096. Section 2.1 and Section 2.3 describe the test setup and operation for the TPS7A14 LDO. Section 2.2 and Section 2.4 describe the test setup and operation of the optional load transient circuit.

2.1 LDO Input/Output Connector Descriptions

2.1.1 VIN and GND

VIN and GND are the connection terminals for the input supply. The VIN terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.1.2 BIAS and GND

BIAS and GND are the connection terminals for the bias supply. The BIAS terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.1.3 VOUT and GND

VOUT and GND are the connection terminals for the output load. The VOUT terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.1.4 EN

EN is a 3-pin header used to enable or disable the TPS7A14.

The center pin of the 3-pin header is tied to the TPS7A14 EN input. When the 2-pin shunt is placed across the top two pins of the header, VIN is shorted to EN, and the TPS7A14 is enabled. When the 2-pin shunt is placed across the bottom two pins of the header, GND is shorted to EN, and the TPS7A14 is disabled.

When driving the EN terminal with an off-board supply or signal generator, the applied voltage must be kept between 0 V and 5.5 V.

2.2 Optional Load Transient Input/Output Connector Descriptions

2.2.1 VDD and GND

VDD and GND are the connection terminals for the input supply of the load transient circuit. The VDD terminal is the positive connection, and the GND terminal is the negative (that is, ground) connection.

2.2.2 J13

J13 is an optional connection for the user to make measurements or apply loads to the output of the LDO.

2.2.3 J15

J15 is an optional connection to insert a damping circuit across the load transient MOSFET drain to source voltage.

2.2.4 J16

J16 is an optional connection to insert capacitance or additional load across the drain to source of the load transient MOSFET.

2.2.5 J18

J18 is the connection for the function generator to drive the gate driver device. J18 is terminated by the 50-Ω resistor, R13.

2.2.6 J19

J19 is a high-frequency kelvin connection that allows accurate measurements of the load transient MOSFET drain to source voltage.

2.2.7 J22

J22 is a high-frequency kelvin connection that allows accurate measurements of the load transient MOSFET gate to source voltage.

2.2.8 TP2, TP3, and TP4

TP2, TP3, and TP4 allow the user to measure the gate drive resistances R8 and R9 when power is turned off to the EVM.

2.2.9 TP5

TP5 is the enable pin to enable the gate driver device. Tie this pin to GND to enable the gate driver.

2.3 TPS7A14 LDO Operation

The TPS7A14EVM-058 and TPS7A14EVM-095 evaluation module contains the TPS7A14 LDO with input, bias, and output capacitors installed. These four components provide the minimum required solution size, as illustrated by the white boxes in Figure 1-1 and Figure 1-2. Additional pads are available to test the LDO with additional input, bias, and output capacitors beyond what is already installed on the EVM. The TPS7A14 LDO can be enabled or disabled by using the J7 3-pin header.

1. Place a 2-pin shunt across the header to tie VIN to EN to enable the device.
2. Place a 2-pin shunt across the header to tie GND to EN to disable the device.

Alternatively, by connecting an external function generator to TP1 (EN) and a nearby GND post (J11), the user can enable or disable the TPS7A14 LDO after VIN is applied. Figure 2-1 shows the result of the TPS7A14EVM-058 during turn on. The blue trace is the enable voltage, and the red trace is the output voltage.

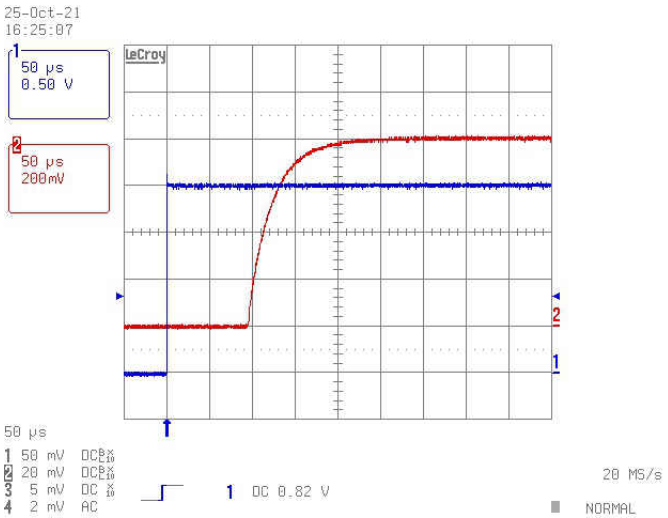

Figure 2-1. TPS7A14EVM-058 Turn On

If desired, a current probe can be inserted in the EVM as shown in Figure 2-2 to measure the input and output current. The slots were sized to fit most current probes, such as the LeCroy™ AP015 or CP031 current probes.

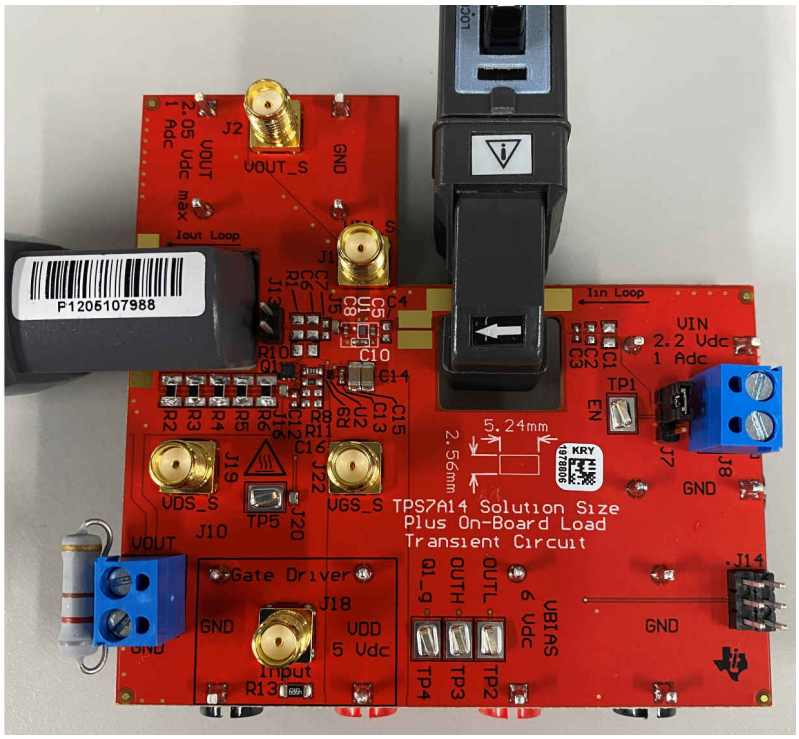

Figure 2-2. TPS7A14EVM-058 With Current Probes Attached

The user has two options for providing a DC load on the output of the TPS7A14. J10 can be used to place a DC load that flows through the current sense path on the output of the LDO. Alternatively, the J4 (VOUT) and J12 (GND) banana connectors can be used for external measurements and loading; however, the IOUT loop does not sense current flowing through these connectors. In cases where very fast transient tests are performed, ringing can be observed on VIN or VOUT as a result of the parasitic inductance within the PCB of the EVM. A strip of wire placed on the exposed copper in the current path can reduce this ringing. Select the correct size of additional wire to fill the volume of the current probe. For most current probes, a 10 AWG wire can be used.

WARNING

The sensors of some current probes are tied to GND and cannot come into contact with energized conductors. See the user manual of your current probe for details. If your current probe has this limitation, use a thin strip of electrical or Kapton® tape to isolate the current sense path from the current probe.

Optional kelvin sense points are provided using the SMA connectors J1 (VIN) and J2 (VOUT).

2.4 Optional Load Transient Circuit Operation

The TPS7A14EVM-058 and TPS7A14EVM-095 evaluation modules contains an optional high-performance load transient circuit to allow efficient testing of the TPS7A14 LDO load transient performance. To use the optional load transient circuit, install the correct components in accordance with the application. Modify the input and output capacitance connected to the TPS7A14 LDO to match the expected operating conditions. Determine the desired peak current to test, and modify the parallel resistor combination of R2, R3, R4, R5, and R6 as shown:

$$I_{Peak} = \frac{V_{OUT}}{R_2 \| R_3 \| R_4 \| R_5 \| R_6} \quad (1)$$

The slew rate of the load step can be adjusted by C11, R7, R8, and R9. In this section, only R8 and R9 is adjusted to set the slew rate. For a 0-mA to 1-A to 0-mA load step, use Table 2-1 to select a value of R8 and R9 that results in the desired rise or fall time.

Table 2-1. Suggested Ramp Rate Resistor Values

R8	R9	Rise/Fall Time
97.6 kΩ	86.6 kΩ	10 µs
52.3 kΩ	40.2 kΩ	5 µs
31.6 kΩ	20.5 kΩ	2.5 µs
12.4 kΩ	8.06 kΩ	1 µs
6.19 kΩ	4.02 kΩ	500 ns
3.74 kΩ	2.43 kΩ	300 ns
2.49 Ω	1.62 Ω	200 ns
806 Ω	806 Ω	100 ns

After the EVM is modified (if needed), connect a power supply to banana connectors J17 (VDD) and J21 (GND) with a 5-V DC supply and a 1-A DC current limit. As illustrated in Figure 2-3 and Figure 2-4, the TPS7A14 transient response is very fast and the output voltage recovers in well under 1 ms after the initial load transient. Therefore, use a load transient pulse duration limit of 1 ms to prevent excessive heating of the pulsed resistors (R2, R3, R4, R5, and R6). Configure a function generator for the 50-Ω output, in a 0-V DC to 5-V DC square pulse. If necessary, burst mode can be configured in the function generator for repetitive, low duty cycle, load transient testing.

A 10.7-kΩ resistor is installed on the EVM at R8, and a 10-kΩ resistor is installed on the EVM at R9. These resistors provide approximately 1 A/µs slew rate from 0 mA to 1 A. Figure 2-3 and Figure 2-4 provide example test data with R8 = 10.7 kΩ and R9 = 10 kΩ. The red trace is the output voltage and the blue trace is the output current. J10 provides 1 mA of DC load current and R2, R3, R4, R5, and R6 provide 949 mA of pulsed load. The resulting test data shows a 1-mA to 950-mA load step on VOUT of the LDO, with only a 2.2-µF capacitor on the output of the LDO.

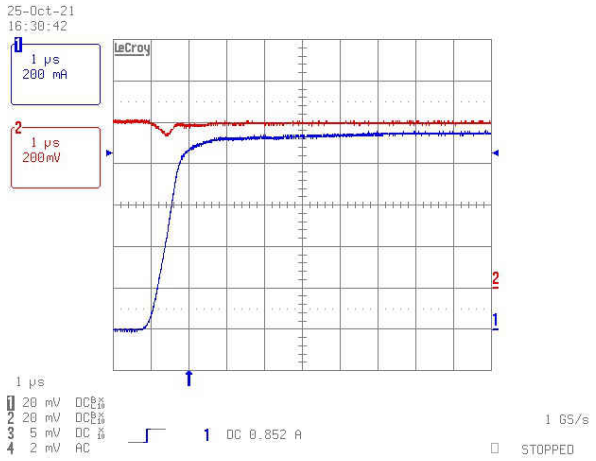

Figure 2-3. TPS7A14EVM-058 Load Transient Results: 1-mA to 950-mA Load Step

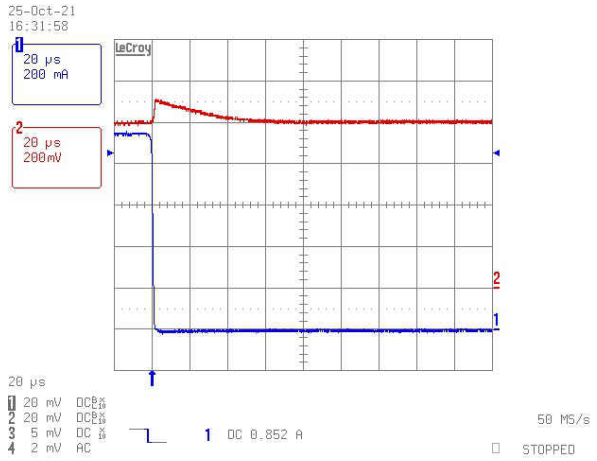

Figure 2-4. TPS7A14EVM-058 Load Transient Results: 950-mA to 1-mA Load Step

3 Board Layout

Figure 3-1 through Figure 3-6 illustrate the board layout for the TPS7A14EVM-058 PCB.

Figure 3-7 through Figure 3-12 illustrate the board layout for the TPS7A14EVM-095 PCB

The TPS7A14EVM-058 and TPS7A14EVM-095 dissipate power, which can cause some components to experience an increase in temperature. The TPS7A14 LDO, LMG1020YFFR gate driver, and pulsed resistors R2, R3, R4, R5, and R6 are most at risk of raising to a high junction temperature during normal operation.

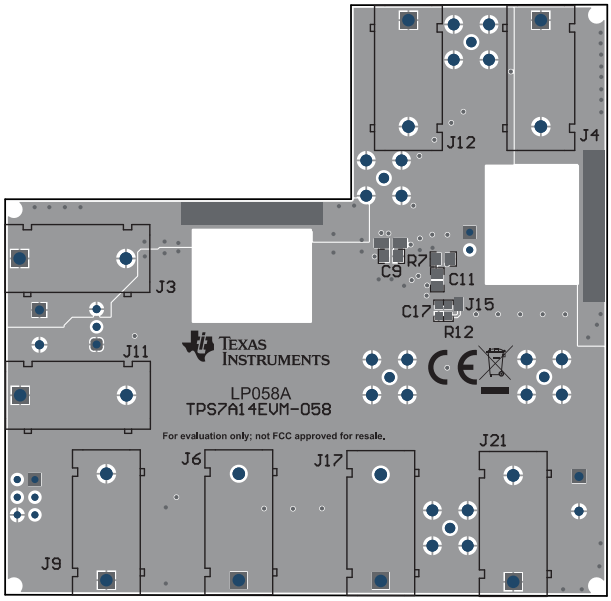

Figure 3-1. TPS7A14EVM-058 Top Assembly Layer and Silk Screen

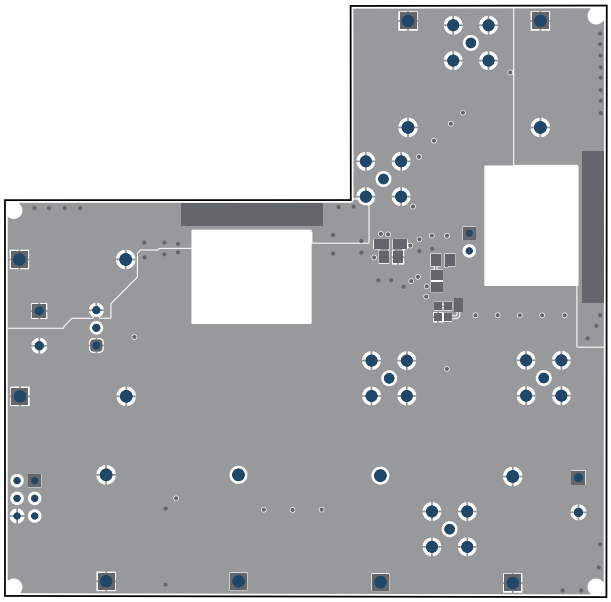

Figure 3-2. TPS7A14EVM-058 Top Layer Routing

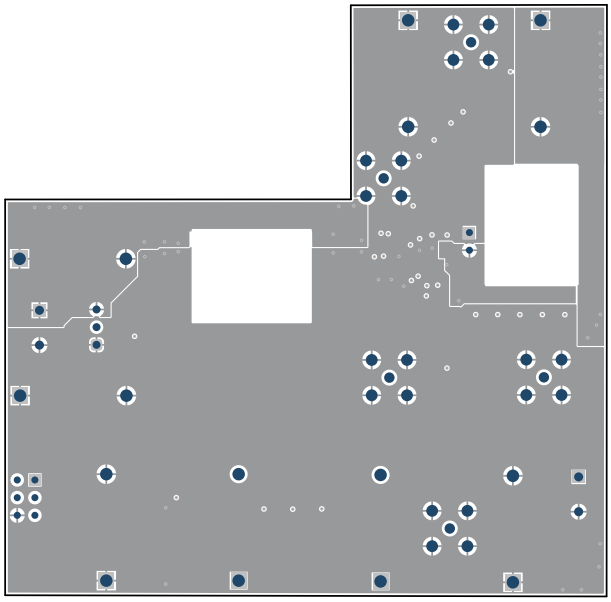

Figure 3-3. TPS7A14EVM-058 Layer 2

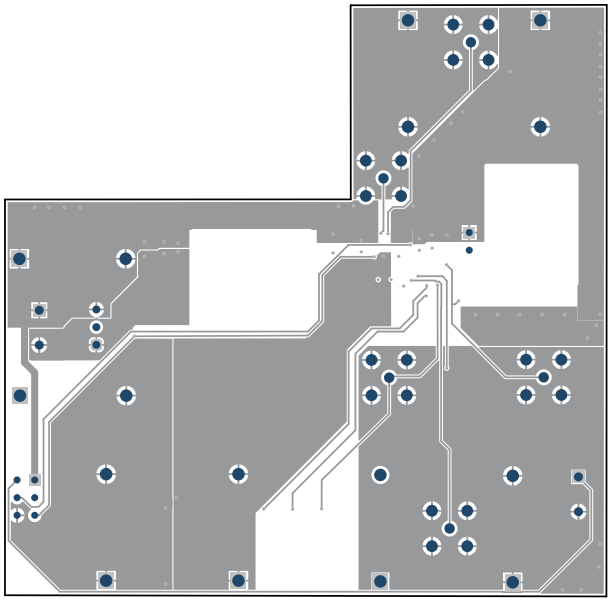

Figure 3-4. TPS7A14EVM-058 Layer 3

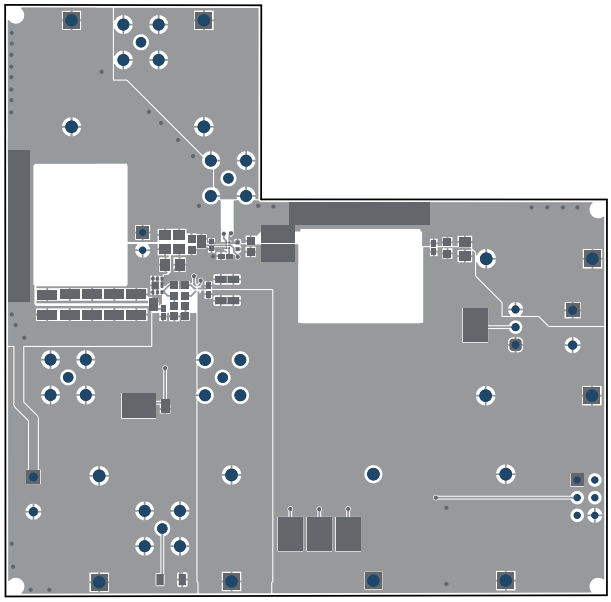

Figure 3-5. TPS7A14EVM-058 Bottom Layer Routing

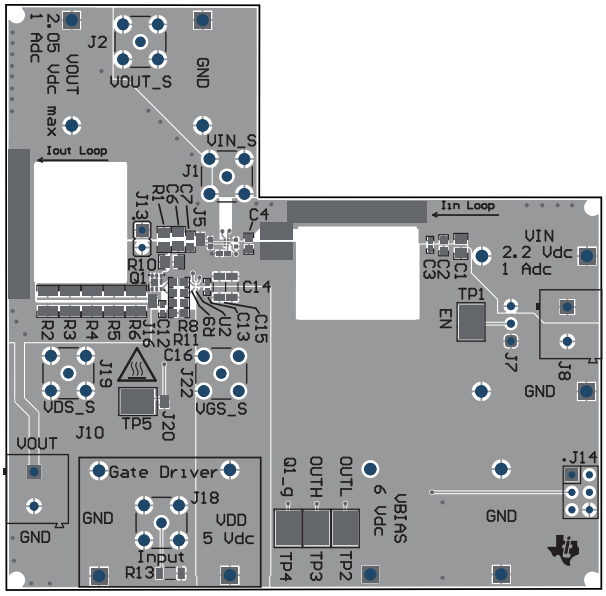

Figure 3-6. TPS7A14EVM-058 Bottom Assembly Layer and Silk Screen

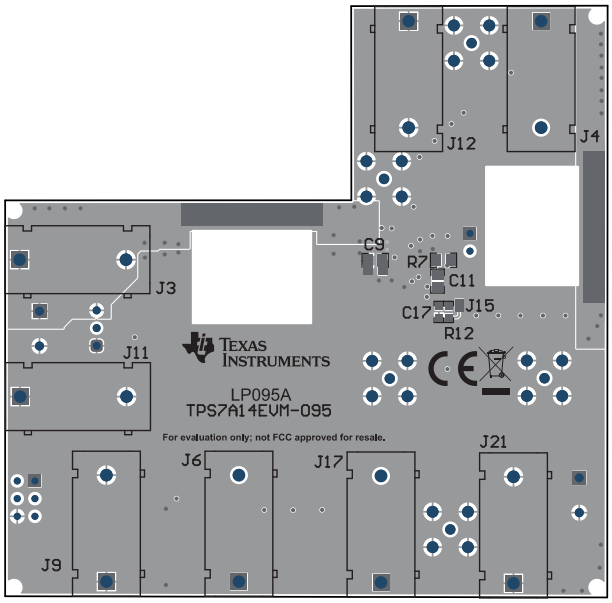

Figure 3-7. TPS7A14EVM-095 Top Assembly Layer and Silk Screen

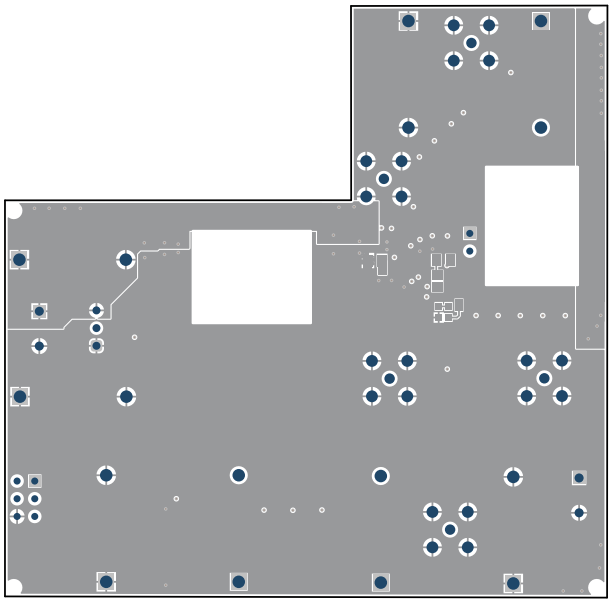

Figure 3-8. TPS7A14EVM-095 Top Layer Routing

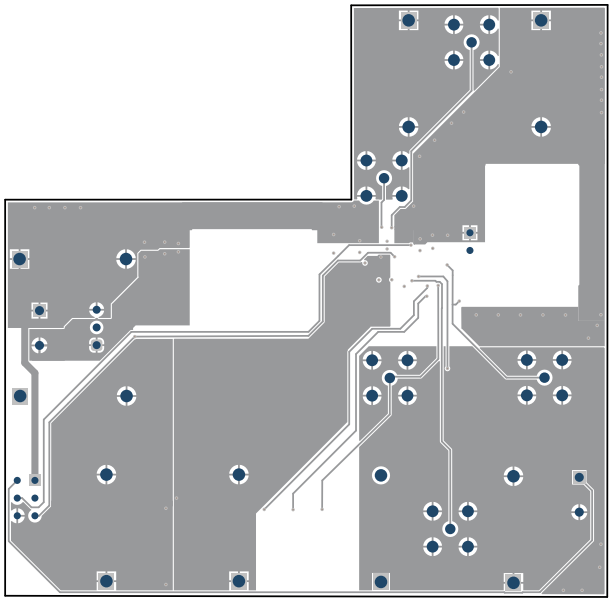

Figure 3-9. TPS7A14EVM-095 Layer 2

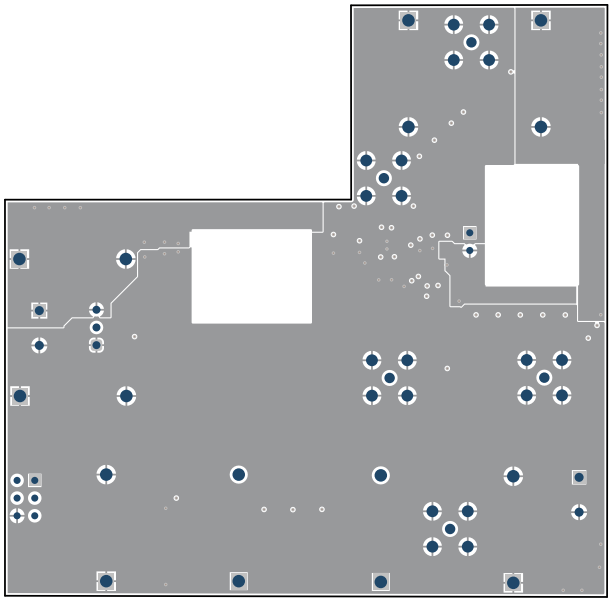

Figure 3-10. TPS7A14EVM-095 Layer 3

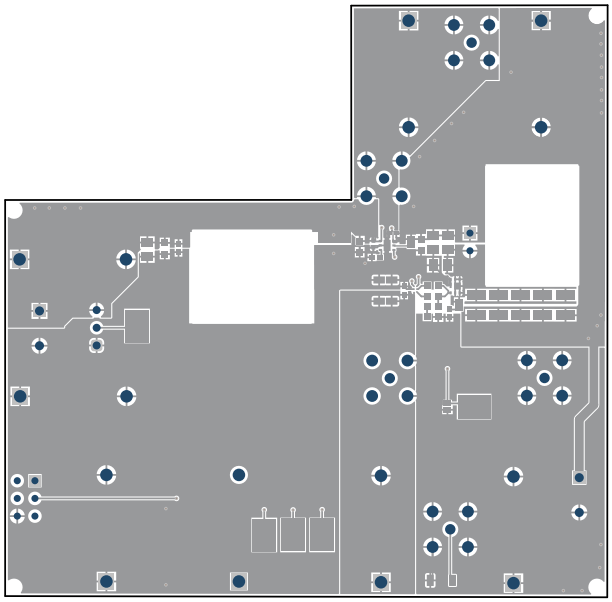

Figure 3-11. TPS7A14EVM-095 Bottom Layer Routing

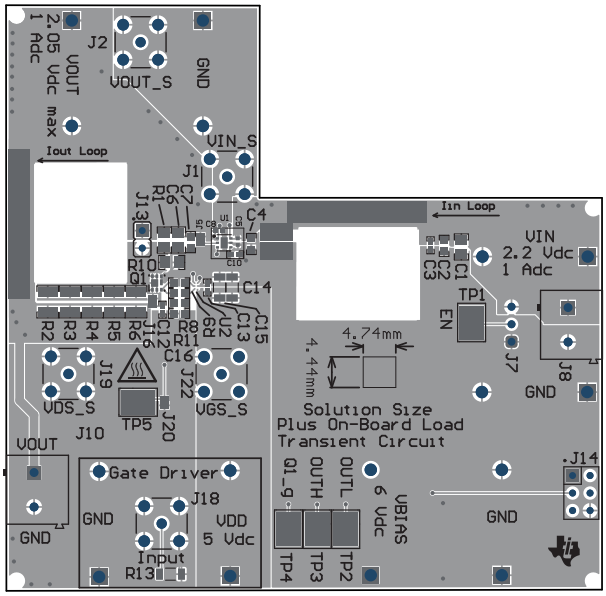

Figure 3-12. TPS7A14EVM-095 Bottom Assembly Layer and Silk Screen

4 TPS7A14EVM Schematic

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

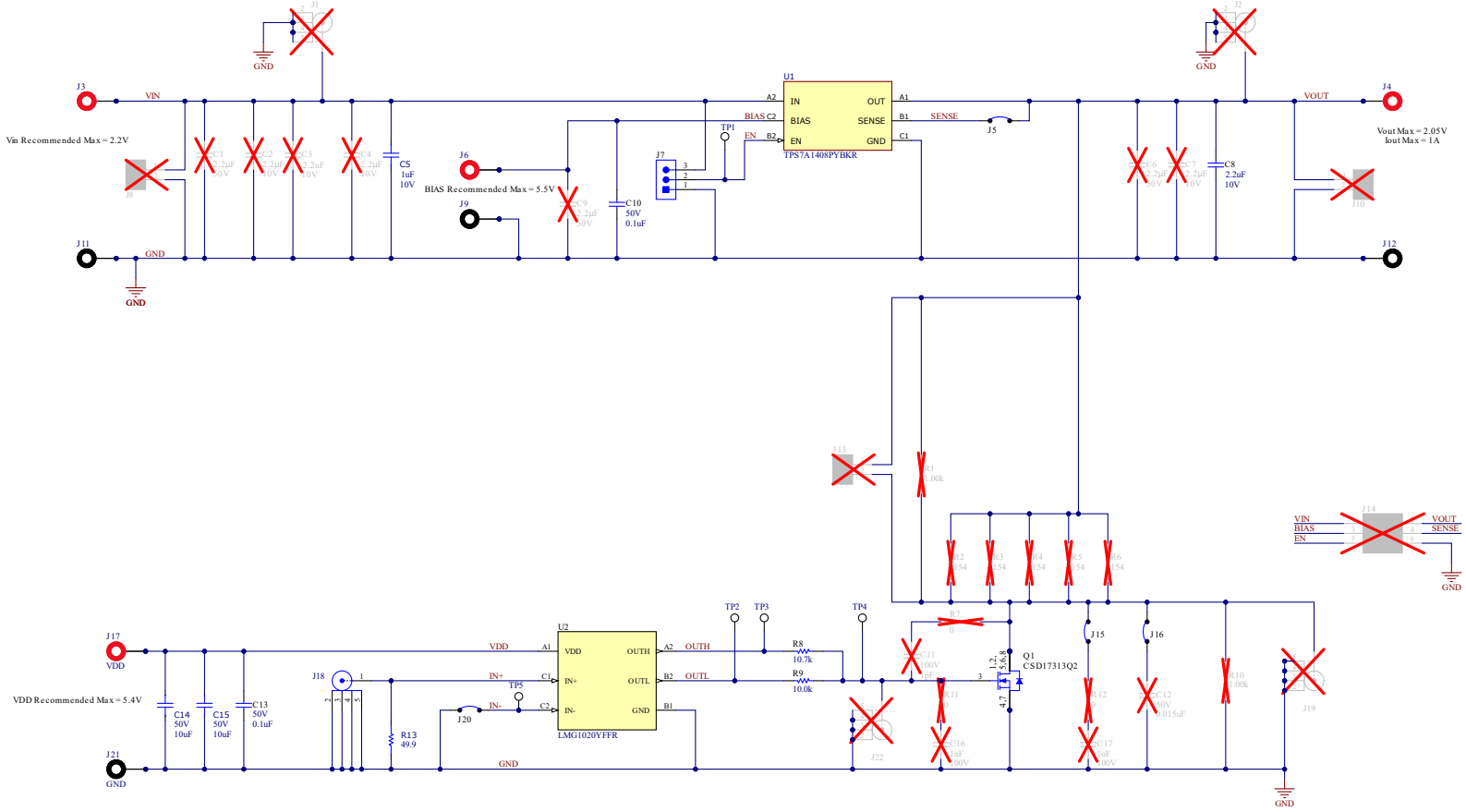

Figure 4-1. TPS7A14EVM-058 Schematic

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

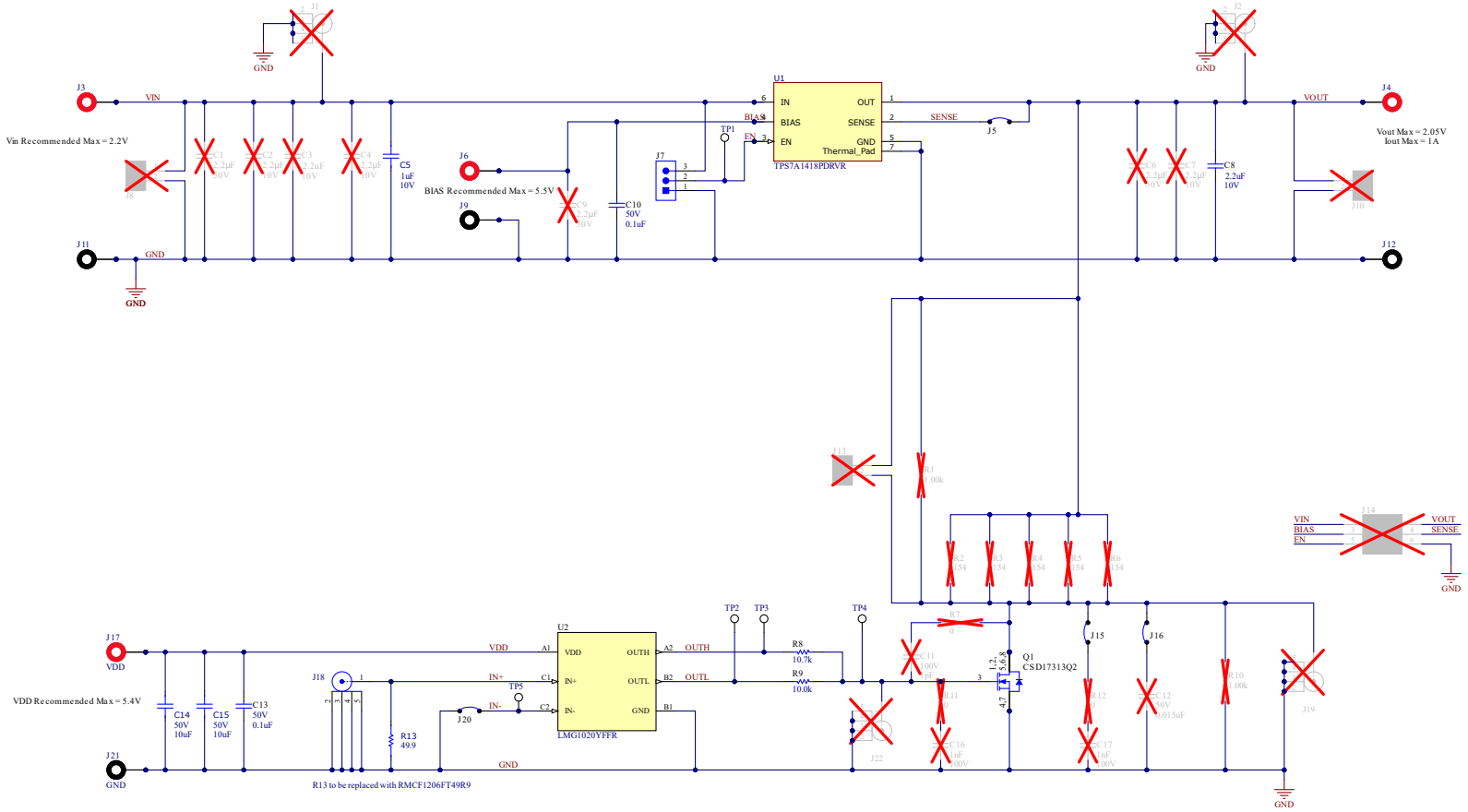

Figure 4-2. TPS7A14EVM-095 Schematic

5 Bill of Materials

Table 5-1 shows the bill of materials for the TPS7A14EVM-058 and TPS7A14EVM-095.

Table 5-1. Bill of Materials

Designator	Quantity		Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
	LP058 EVM	LP095 EVM							
!PCB1	1	-		Printed Circuit Board		LP058	Any		
!PCB1	-	1		Printed Circuit Board		LP095	Any		
U1	1	-		Ultra-Low Dropout Regulator, 0.8V 1 A, DSBGA6	DSBGA6	TPS7A1408PYBKR	Texas Instruments		
U1	-	1		Ultra-Low Dropout Regulator, 1.8V 1 A, WSON6	WSON6	TPS7A1418PDRVR	Texas Instruments		
C5	1	1	1 µF	1 µF ±10% 10 V Ceramic Capacitor X7R 0402 (1005 Metric)	402	GMC04X7R105K10NT	Cal-Chip Electronics		
C8	1	1	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 20%, X5R, 0402	402	885012105013	Wurth Elektronik		
C10, C13	2	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	402	C1005X7R1H104K050BB	TDK		
C14, C15	2	2	10 µF	10 µF ±10% 50 V Ceramic Capacitor X7R 1206 (3216 Metric)	1206	GMC31X7R106K50NT	Cal-Chip Electronics		
J3, J4, J6, J17	4	4		Standard Banana Jack, insulated, 10 A, red	571-0500	571-0500	DEM Manufacturing		
J5, J15, J16, J20	4	4		Jumper, SMT	shorting jumper, SMT	JMP-36-30X40SMT	Any		
J7	1	1		Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH	61300311121	Wurth Elektronik		
J9, J11, J12, J21	4	4		Standard Banana Jack, insulated, 10 A, black	571-0100	571-0100	DEM Manufacturing		
J18	1	1		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
Q1	1	1	30 V	MOSFET, N-CH, 30 V, 5 A, DQK0006C (WSON-6)	DQK0006C	CSD17313Q2	Texas Instruments		None
R8	1	1	10.7k	RES, 10.7 k, 1%, 0.1 W, 0603	603	RC0603FR-0710K7L	Yageo		
R9	1	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0710KL	Yageo		
R13	1	1	49.9	Res Thick Film 1206 49.9 Ohm 1% 1/4W ±100ppm/°C Molded SMD SMD Paper T/R	1206	RMCF1206FT49R9	Stackpole Electronics		
SH-J1	1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5	5	5		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U2	1	1		5 V, 7 A/5 A Low Side GaN Driver With 60 MHz/1ns Speed, YFF0006AEAE (DSBGA-6)	YFF0006AEAE	LMG1020YFFR	Texas Instruments	LMG1020YFFT	Texas Instruments

Table 5-1. Bill of Materials (continued)

Designator	Quantity		Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
	LP058 EVM	LP095 EVM							
C1, C6, C9	0	0	2.2uF	CAP, CERM, 2.2 uF, 50 V, +/- 20%, X7R, 0805	805	C2012X7R1H225M125AC	TDK		
C2, C4, C7	0	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603	603	C1608X7R1A225K080AC	TDK		
C3	0	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7S, 0402	402	C1005X7S1A225K050BC	TDK		
C11	0	0	1 pF	CAP, CERM, 1 pF, 100 V, +/- 5%, C0G/NP0, 0805	805	GQM2195C2A1R0CB01D	MuRata		
C12	0	0	0.015uF	CAP, CERM, 0.015 uF, 50 V, +/- 10%, X7R, 0402	402	GRM155R71H153KA12D	MuRata		
C16, C17	0	0	1000 pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	603	06031C102JAT2A	AVX		
FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8	0	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1, J2, J19, J22	0	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
J8, J10	0	0		Terminal Block, 5 mm, 2x1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik		
J13	0	0		Header, 100mil, 2x1, Gold, TH	Sullins 100mil, 1x2, 230 mil above insulator	PBC02SAAN	Sullins Connector Solutions		
J14	0	0		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec		
R1, R10	0	0	1.00k	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1001V	Panasonic		
R2, R3, R4, R5, R6	0	0	154	RES, 154, 1%, 0.5 W, 1210	1210	RC1210FR-07154RL	Yageo		
R7	0	0	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic		
R11, R12	0	0	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	RMCF0603ZT0R00	Stackpole Electronics Inc		

5 Bill of Materials

Table 5-1 shows the bill of materials for the TPS7A14EVM-058 and TPS7A14EVM-095.

Table 5-1. Bill of Materials

Designator	Quantity		Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
	LP058 EVM	LP095 EVM							
!PCB1	1	-		Printed Circuit Board		LP058	Any		
!PCB1	-	1		Printed Circuit Board		LP095	Any		
U1	1	-		Ultra-Low Dropout Regulator, 0.8V 1 A, DSBGA6	DSBGA6	TPS7A1408PYBKR	Texas Instruments		
U1	-	1		Ultra-Low Dropout Regulator, 1.8V 1 A, WSON6	WSON6	TPS7A1418PDRVR	Texas Instruments		
C5	1	1	1 µF	1 µF ±10% 10 V Ceramic Capacitor X7R 0402 (1005 Metric)	402	GMC04X7R105K10NT	Cal-Chip Electronics		
C8	1	1	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 20%, X5R, 0402	402	885012105013	Wurth Elektronik		
C10, C13	2	2	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	402	C1005X7R1H104K050BB	TDK		
C14, C15	2	2	10 µF	10 µF ±10% 50 V Ceramic Capacitor X7R 1206 (3216 Metric)	1206	GMC31X7R106K50NT	Cal-Chip Electronics		
J3, J4, J6, J17	4	4		Standard Banana Jack, insulated, 10 A, red	571-0500	571-0500	DEM Manufacturing		
J5, J15, J16, J20	4	4		Jumper, SMT	shorting jumper, SMT	JMP-36-30X40SMT	Any		
J7	1	1		Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54mm, 3x1, TH	61300311121	Wurth Elektronik		
J9, J11, J12, J21	4	4		Standard Banana Jack, insulated, 10 A, black	571-0100	571-0100	DEM Manufacturing		
J18	1	1		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
Q1	1	1	30 V	MOSFET, N-CH, 30 V, 5 A, DQK0006C (WSON-6)	DQK0006C	CSD17313Q2	Texas Instruments		None
R8	1	1	10.7k	RES, 10.7 k, 1%, 0.1 W, 0603	603	RC0603FR-0710K7L	Yageo		
R9	1	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	603	RC0603FR-0710KL	Yageo		
R13	1	1	49.9	Res Thick Film 1206 49.9 Ohm 1% 1/4W ±100ppm/°C Molded SMD SMD Paper T/R	1206	RMCF1206FT49R9	Stackpole Electronics		
SH-J1	1	1	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	3M
TP1, TP2, TP3, TP4, TP5	5	5		Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
U2	1	1		5 V, 7 A/5 A Low Side GaN Driver With 60 MHz/1ns Speed, YFF0006AEAE (DSBGA-6)	YFF0006AEAE	LMG1020YFFR	Texas Instruments	LMG1020YFFT	Texas Instruments

Table 5-1. Bill of Materials (continued)

Designator	Quantity		Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
	LP058 EVM	LP095 EVM							
C1, C6, C9	0	0	2.2uF	CAP, CERM, 2.2 uF, 50 V, +/- 20%, X7R, 0805	805	C2012X7R1H225M125AC	TDK		
C2, C4, C7	0	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603	603	C1608X7R1A225K080AC	TDK		
C3	0	0	2.2uF	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7S, 0402	402	C1005X7S1A225K050BC	TDK		
C11	0	0	1 pF	CAP, CERM, 1 pF, 100 V, +/- 5%, C0G/NP0, 0805	805	GQM2195C2A1R0CB01D	MuRata		
C12	0	0	0.015uF	CAP, CERM, 0.015 uF, 50 V, +/- 10%, X7R, 0402	402	GRM155R71H153KA12D	MuRata		
C16, C17	0	0	1000 pF	CAP, CERM, 1000 pF, 100 V, +/- 5%, X7R, 0603	603	06031C102JAT2A	AVX		
FID1, FID2, FID3, FID4, FID5, FID6, FID7, FID8	0	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1, J2, J19, J22	0	0		SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH	901-144-8RFX	Amphenol RF		
J8, J10	0	0		Terminal Block, 5 mm, 2x1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik		
J13	0	0		Header, 100mil, 2x1, Gold, TH	Sullins 100mil, 1x2, 230 mil above insulator	PBC02SAAN	Sullins Connector Solutions		
J14	0	0		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec		
R1, R10	0	0	1.00k	RES, 1.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6ENF1001V	Panasonic		
R2, R3, R4, R5, R6	0	0	154	RES, 154, 1%, 0.5 W, 1210	1210	RC1210FR-07154RL	Yageo		
R7	0	0	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	805	ERJ-6GEY0R00V	Panasonic		
R11, R12	0	0	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	603	RMCF0603ZT0R00	Stackpole Electronics Inc		

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2021) to Revision A (June 2023)	Page
• Added *TPS7A14EVM-095 Evaluation Module* figure	1
• Added LP095 to *Device Information* table	3
• Added figures to *Board Layout* section	8
• Added *TPS7A14EVM-095 Schematic* figure	11

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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