User's Guide

TMUX741xEVM and TMUX746EVM User's Guide

ABSTRACT

This document is the EVM user's guide for the TMUX741-746EVM which provides a board for quick DC parmeter testing for the TMUX741x and TMUX746x families in the QFN and TSSOP package families.

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Trademarks

1 1. Introduction

This user's guide describes the TMUX741-746 evaluation module (EVM) and its intended use. This board allows for the quick prototyping and DC characterization of TI's TMUX741x/TMUX746x Line of parts in either QFN (RRP) or TSSOP (PW) packages. Figure 1-1 and Figure 1-2 show the top and bottom sides of the board respectively.

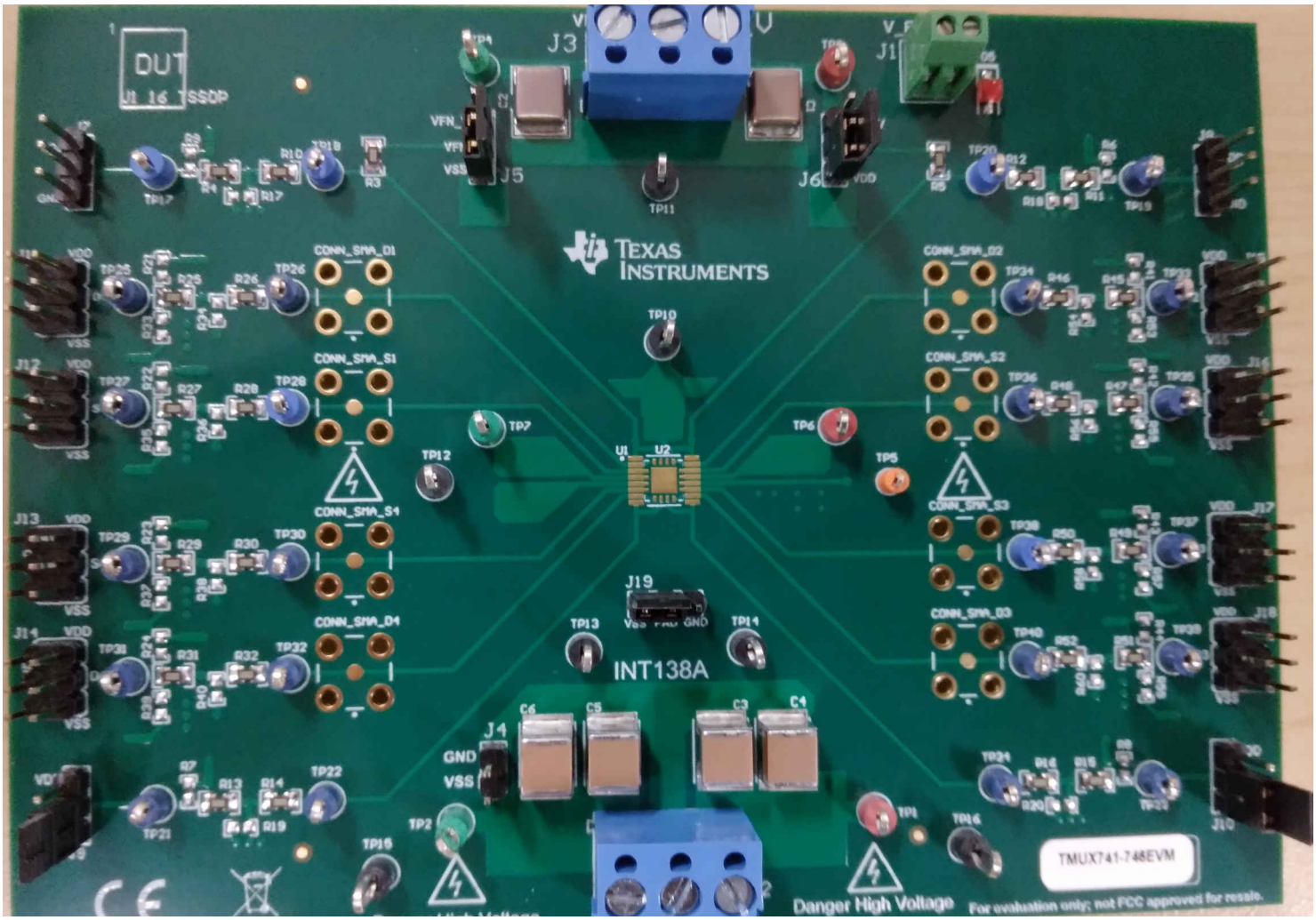

Figure 1-1. TMUX741-746EVM Top Side View

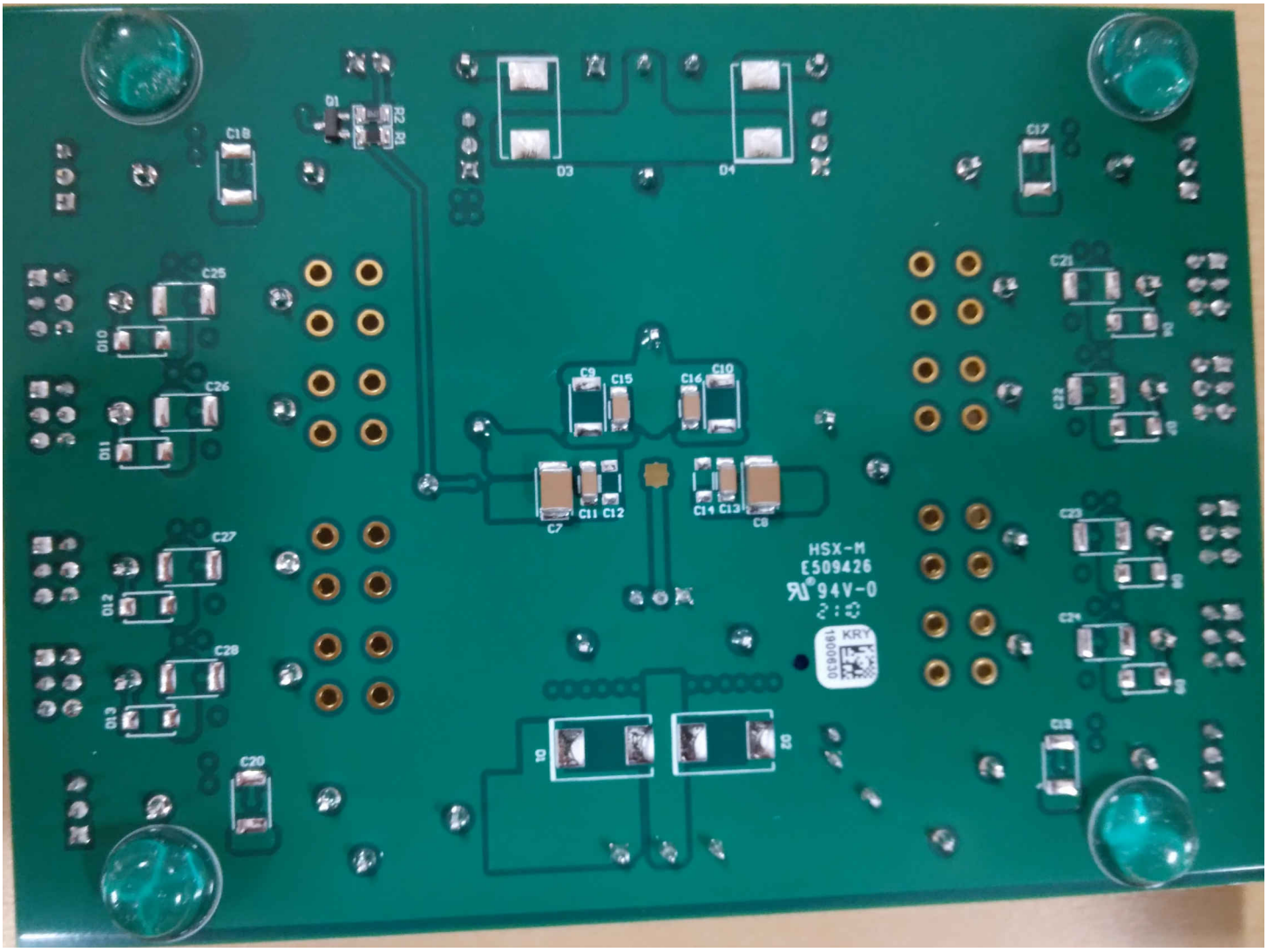

Figure 1-2. TMUX741-746EVM Bottom Side View

1.1 Information About Cautions and Warnings

The information in the warning statement is provided for personal protection and the information in the caution statement is provided to protect the equipment from damage. Read each caution and warning statement carefully.

This EVM contains components that can ptentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bad when not in suse. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, see Electrostatic Discharge (ESD).

2 3. Features of This EVM

The EVM has the following features:

- Four power supply decoupling capacitors from VDD to Ground (2 × 3.3 µF, 1 µF, 0.1 µF)
- One additional power supply decoupling capacitor pad from VDD to Ground (0.1 µF)
- One power supply decoupling capacitors from VSS to Ground (2 × 3.3 µF, 1 µF, 0.1 µF)
- One additional power supply decoupling capacitor pad from VDD to Ground (0.1 µF)
- Protection diode pads available near VDD and VSS input.
- 10 µF supply decoupling capacitor to Ground on both VFP and VFN supplies
- Protection diode pads available near VFP and VFN inputs
- Up to four auxiliary pathways available with jumpers
- Up to eight analog I/O pathways available
- All analog I/O pathways have pads available to load device
- All analog I/O pathways have pads available to support SMA connections to device.
- Fault indicator flag LED circuit included on EVM

3 4. TMUX741-746EVM Setup

1. If the default conditions on the board is not what you desired please refer to the following table to set up the Auxiliary pathways which can be either VFP, VFN, SEL, DR, or NC depending on device installed.

Jumper on Pathway	Possible Signal	Pull Up Resistor Pad ID	Load Resistor Pad ID	Load Capacitor Pad ID	Additional Capacitor Pad ID
J7	VFN / SEL	R4	R17	C17	C10
J5	VFN / SEL	N/A	N/A	N/A	N/A
J8	VFP / SEL	R6	R18	C18	C9
J6	VFP / SEL	N/A	N/A	N/A	N/A
J9	DR / SEL	R7	R19	C19	N/A
J10	NC / SEL	R8	R20	C20	N/A

2. If VFP and VFN are used in the application, attach a shunt on J5 and J6 to the appropriate VFP/VFN source.
3. Next, use the following table to set up the desired configuration of the analog channels:

Jumper on Pathway	Pull Down Resistor Pad ID	Pull Up Resistor Pad ID	Load Resistor Pad ID	Load Capacitor Pad ID	TVS Diode Pad ID
J11	R33	R21	R34	C21	D6
J12	R35	R22	R36	C22	D7
J13	R37	R23	R38	C23	D8
J14	R39	R24	R40	C24	D9
J15	R53	R41	R54	C25	D10
J16	R55	R42	R56	C26	D11
J17	R57	R43	R58	C27	D12
J18	R59	R44	R60	C28	D13

4. Next, solder down the chosen TMUX74xx in either a PW or QFN package that is to be tested.
5. If using dual supplies, connect shunt from VSS to PAD on J19.
6. If using single supplies, connect shunt from VSS to GND on J4.
7. Next, power the board through J2. Follow the specific device data sheet as to what range the voltage should be set to.
8. If VFP/VFN pins are used in the application and are using an external source power this through J3.
9. If the fault flag voltage (VFF) is used in the application, connect and power up this source through J1.

4 5. TMUX741-746EVM Jumper Connections and Test Points

1. The auxiliary lines on the EVM have 3 prong jumpers attached to them. These are labeled on the board but are also listed in the following table:

Jumper ID	Jumper Pin 1	Jumper Pin 2	Jumper Pin 3	Test Point 1	Test Point 2
J7	VDD	VFN/SEL	GND	TP17	TP18
J8	VDD	VFP/SEL	GND	TP19	TP20
J9	VDD	DR/SEL	GND	TP21	TP22
J10	VDD	NC/SEL	GND	TP23	TP24

2. The analog lines on the have 6 prong jumpers attached to them in a 2 × 3 formation. Only 4 pins have signals attached to them. For reference this document refers to jumper pins that are closest to the IC as *Interior Jumper Pins* and pins that face away from the IC as *Exterior Jumper Pins*. All interior pins are used, only the middle exterior pin is used. Please see the following table for connections.

Jumper ID	Top Interior Pin	Mid. Interior Pin	Bottom Interior Pin	Mid. Exterior Pin	Test Point 1	Test Point 2
J11	VDD	D1	VSS	GND	TP25	TP26
J12	VDD	S1	VSS	GND	TP27	TP28
J13	VDD	S4	VSS	GND	TP29	TP30
J14	VDD	D4	VSS	GND	TP31	TP32
J15	VDD	D2	VSS	GND	TP33	TP34
J16	VDD	S2	VSS	GND	TP35	TP36
J17	VDD	S3	VSS	GND	TP37	TP38
J18	VDD	D3	VSS	GND	TP39	TP40

3. Finally, the remaining test points and their location on board.

Test Point ID	Signal Net Attached to Test Point
TP4	VFN_V
TP3	VFP_V
TP11	GND
TP10	GND
TP7	VSS
TP6	VDD
TP5	VFF
TP12	GND
TP13	GND
TP14	GND
TP2	VSS
TP1	VDD
TP15	GND
TP16	GND

5 6. Schematics

Figure 5-1 shows the schematic without DNP/DNI markings. Figure 5-2 shows the scheamtic with DNP/DNI markings. Figure 5-3 shows mechanical hardware and overlays.

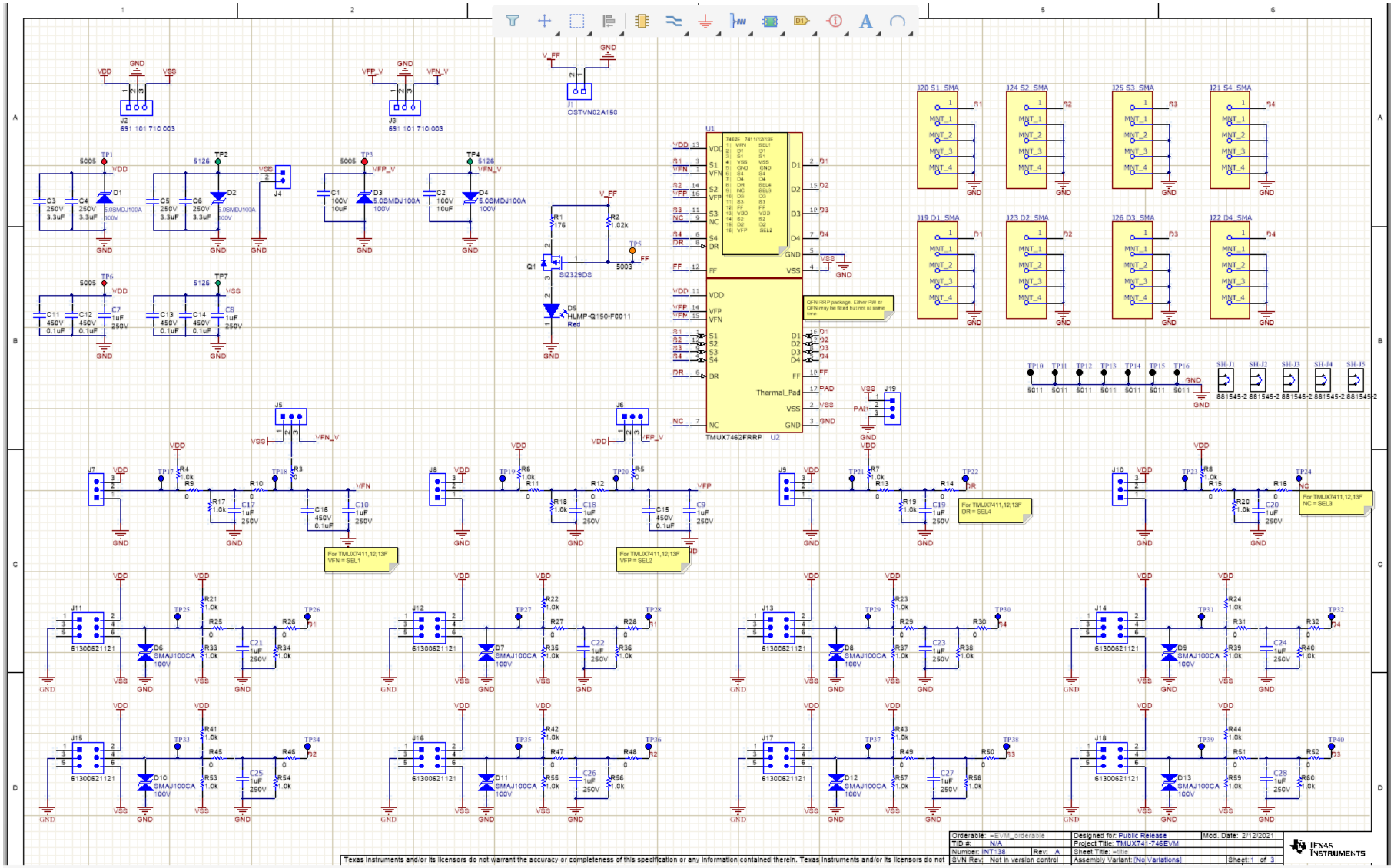

Figure 5-1. TMUX741-746EVM Schematic without DNP/DNI Markings

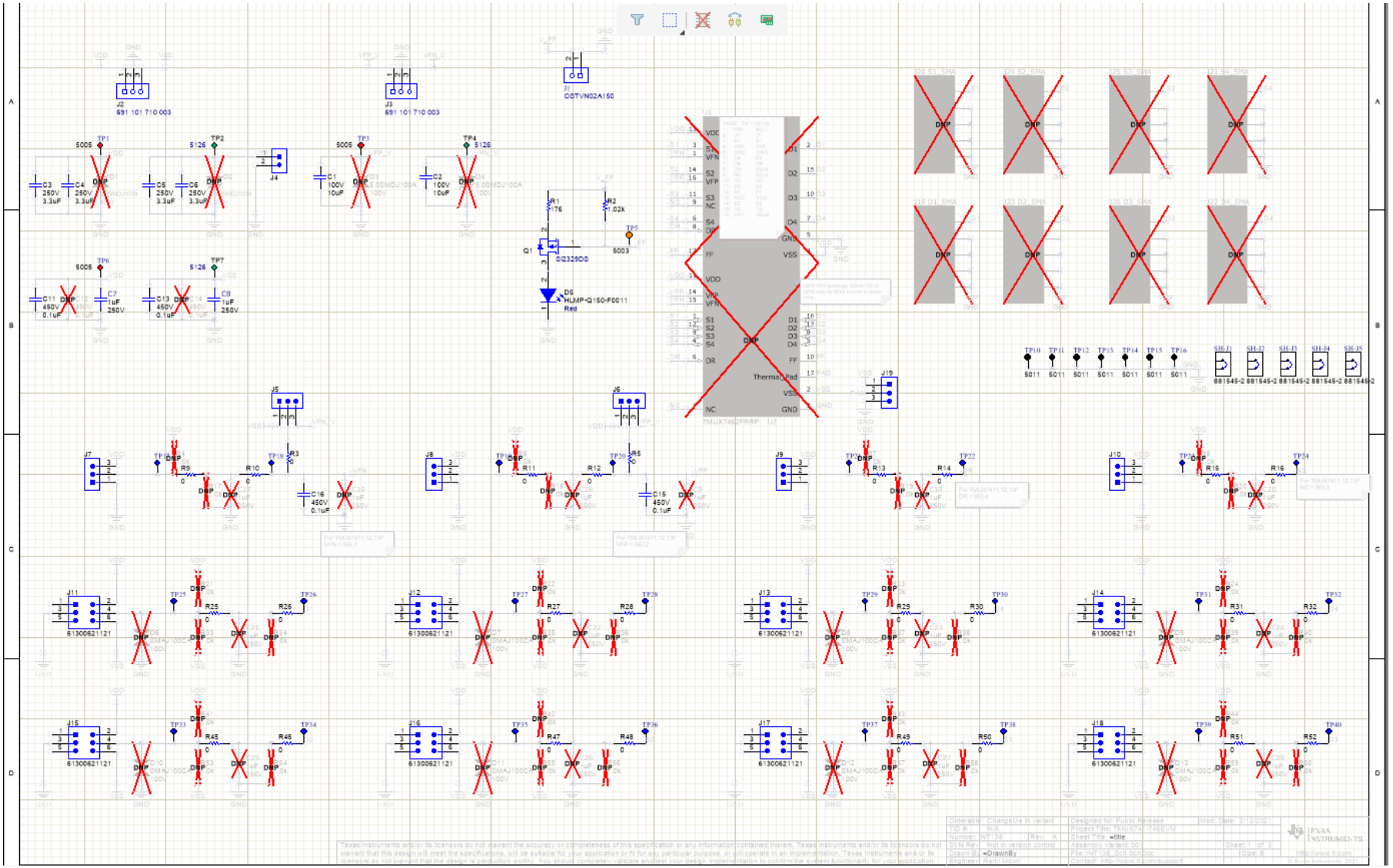

Figure 5-2. TMUX741-746EVM with DNP/DNI Markings

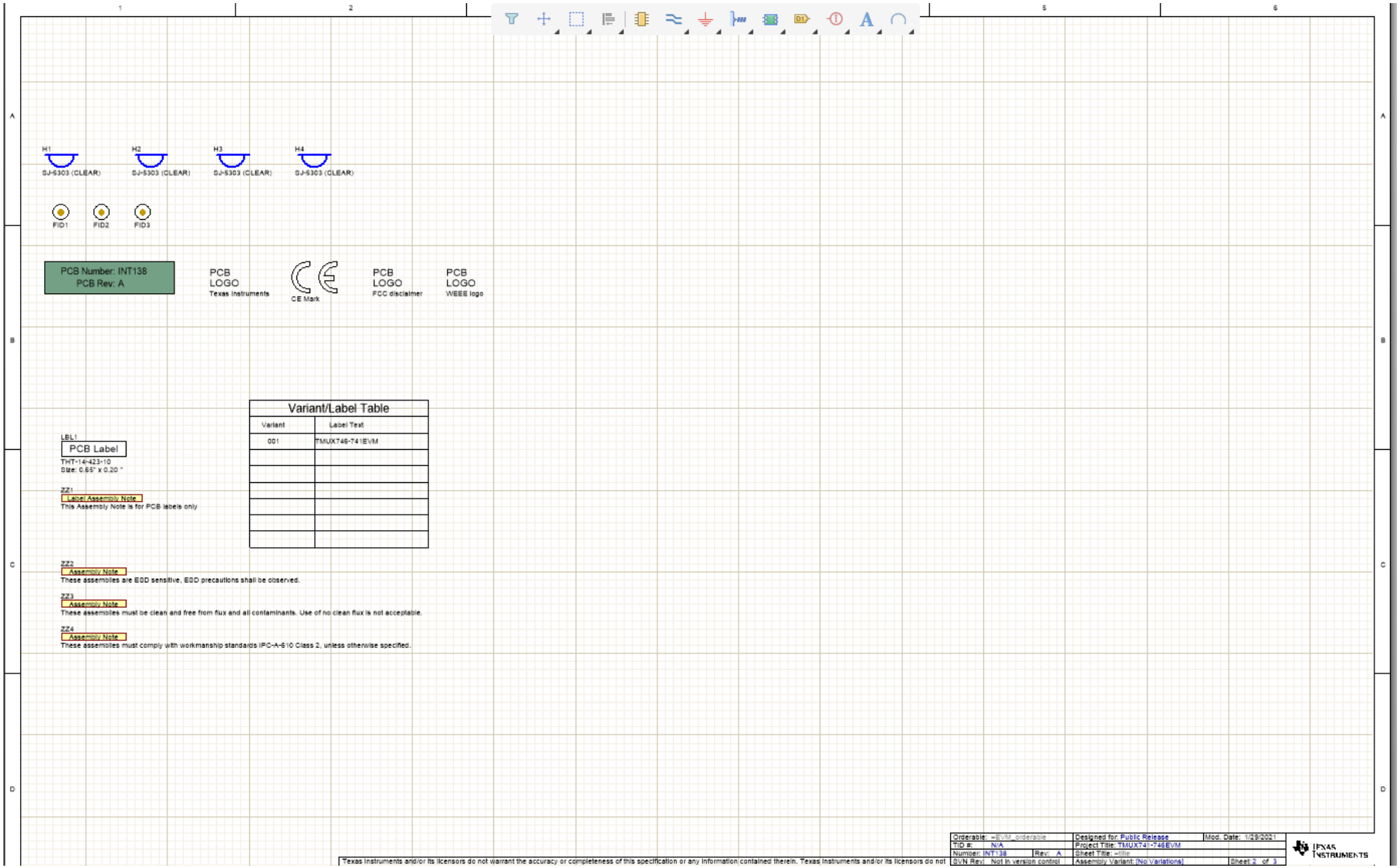

Figure 5-3. TMUX741-746EVM Mechanical Hardware and Overlays

6 7. Bill of Materials

Designator	Quantity	Value	Part Number	Manufacturer	Description	Dimensions
C1, C2	2	10 µF	C5750X7S2A106 K230KB	TDK	CAP, CERM, 10 µF, 100 V, ± 10%, X7S,	
C3, C4, C5, C6	4	3.3 µF	CKG57NX7T2E33 5M500JH	TDK	CAP, CERM, 3.3 µF, 250 V, ± 20%, X7T, AEC-Q200 Grade 1, 6 × 5 × 5mm	6 × 5 × 5 mm
C7, C8	2	1 µF	C4532X7T2E105K 250KA	TDK	Multilayer Ceramic Capacitors 1 µF ±10% 250 V X7T SMD 1812	1812
C11, C13, C15, C16	4	0.1 µF	C3216X7T2W104 K160AE	TDK	CAP, CERM, 0.1 µF, 450 V, ± 10%, X7T, 1206	1206
D5	1	Red	HLMP-Q150-F0011	Avago	LED, Red, SMD	2.08 × 2.21 mm
H1, H2, H3, H4	4		SJ-5303 (CLEAR)	3M	Bumpon, Hemisphere, 0.44 × 0.20, Clear	Transparent Bumpon
J1	1		OSTVN02A150	On-Shore Technology	Terminal Block, 2.54 mm, 2 × 1, Brass, TH	Terminal Block, 2.54 mm, 2-pole, Brass, TH
J2, J3	2		691 101 710 003	Wurth Elektronik	Terminal Block, 5 mm, 3 × 1, Tin, TH	Terminal Block, 5 mm, 3 × 1, TH
J4	1		PEC02SAAN	Sullins Connector Solutions	Header, 100 mil, 2 × 1, Tin, TH	Header, 2 PIN, 100 mil, Tin
J5, J6, J7, J8, J9, J10, J19	7		PBC03SAAN	Sullins Connector Solutions	Header, 100 mil, 3 × 1, Gold, TH	PBC03SAAN
J11, J12, J13, J14, J15, J16, J17, J18	8		61300621121	Wurth Elektronik	Header, 2.54 mm, 3 × 2, Gold, TH	Header, 2.54 mm, 3 × 2, TH
LBL1	1		THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650 inch W × 0.200 inch H - 10,000 per roll	PCB Label 0.650 × 0.200 inch
Q1	1	-8V	Si2329DS	Vishay-Semiconductor	MOSFET, P-CH, -8 V, -5.3 A, SOT-23	SOT-23
R1	1	176	RT0805BRD0717 6RL	Yageo America	RES, 176, 0.1%, 0.125 W, 0805	0805
R2	1	1.02k	CRCW08051K02F KEA	Vishay-Dale	RES, 1.02 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805
R3, R5, R9, R10, R11, R12, R13, R14, R15, R16, R25, R26, R27, R28, R29, R30, R31, R32, R45, R46, R47, R48, R49, R50, R51, R52	26	0	PMR10EZPJ000	Rohm	RES, 0, 0%, W, AEC-Q200 Grade 0, 0805	0805
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	5		881545-2	TE Connectivity	Shunt, 100 mil, Gold plated, Black	Shunt 2 pos. 100 mil
TP1, TP3, TP6	3		5005	Keystone	Test Point, Compact, Red, TH	Red Compact Testpoint

Designator	Quantity	Value	Part Number	Manufacturer	Description	Dimensions
TP2, TP4, TP7	3		5126	Keystone	Test Point, Multipurpose, Green, TH	Green Multipurpose Testpoint
TP5	1		5003	Keystone	Test Point, Miniature, Orange, TH	Orange Miniature Testpoint
TP10, TP11, TP12, TP13, TP14, TP15, TP16	7		5011	Keystone	Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint
TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40	24		5122	Keystone	Test Point, Compact, Blue, TH	Blue Compact Testpoint

7 8. PCB Layouts

The PCB layouts are shown below. Figure 7-1 shows the 2D top view layout of the EVM, whereas Figure 7-2 shows the 2D bottom view. Figure 7-3 and Figure 7-4 show the 3D represenation of the layout for both top and bottom respectively.

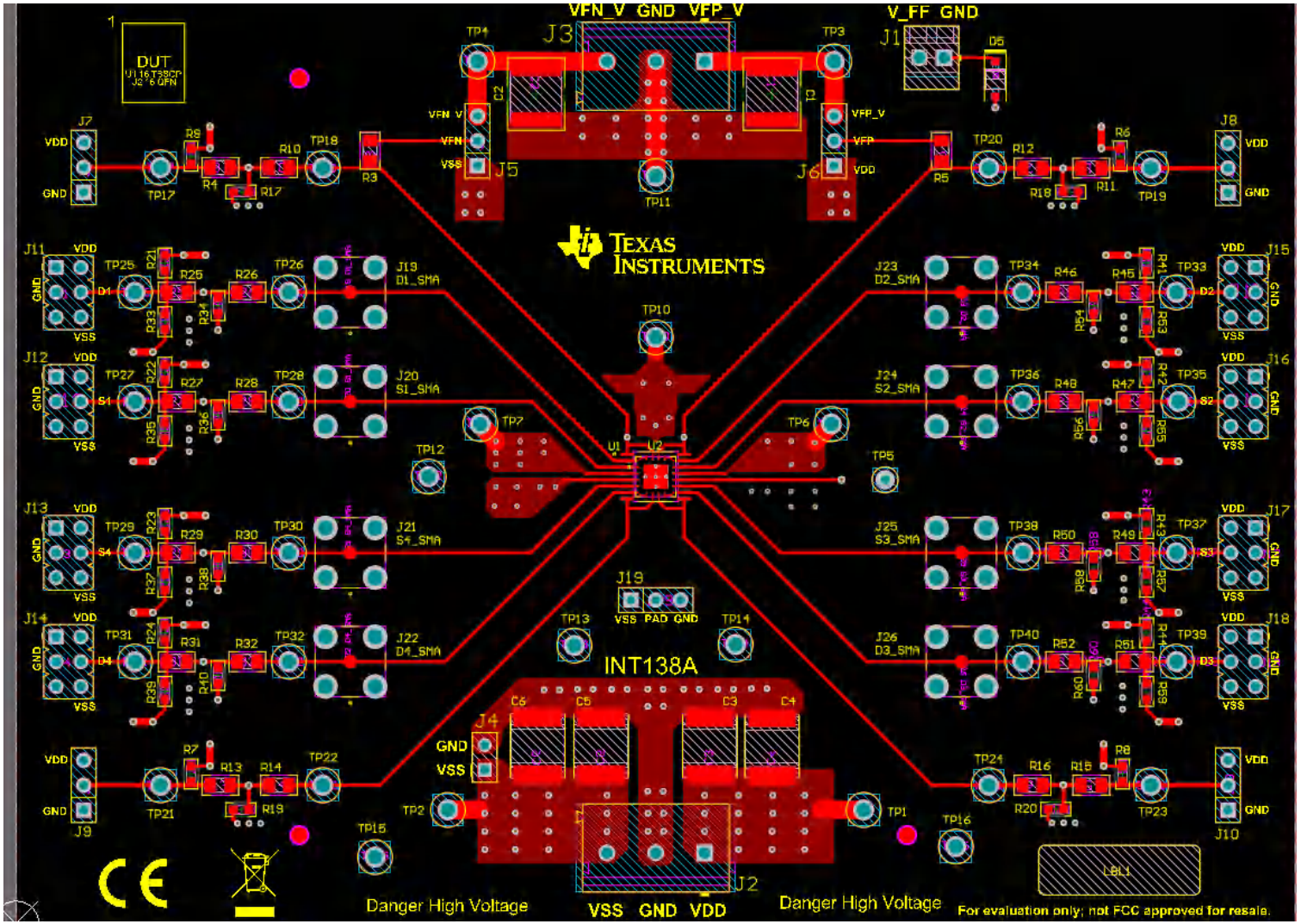

Figure 7-1. 2D Top Side Layout View

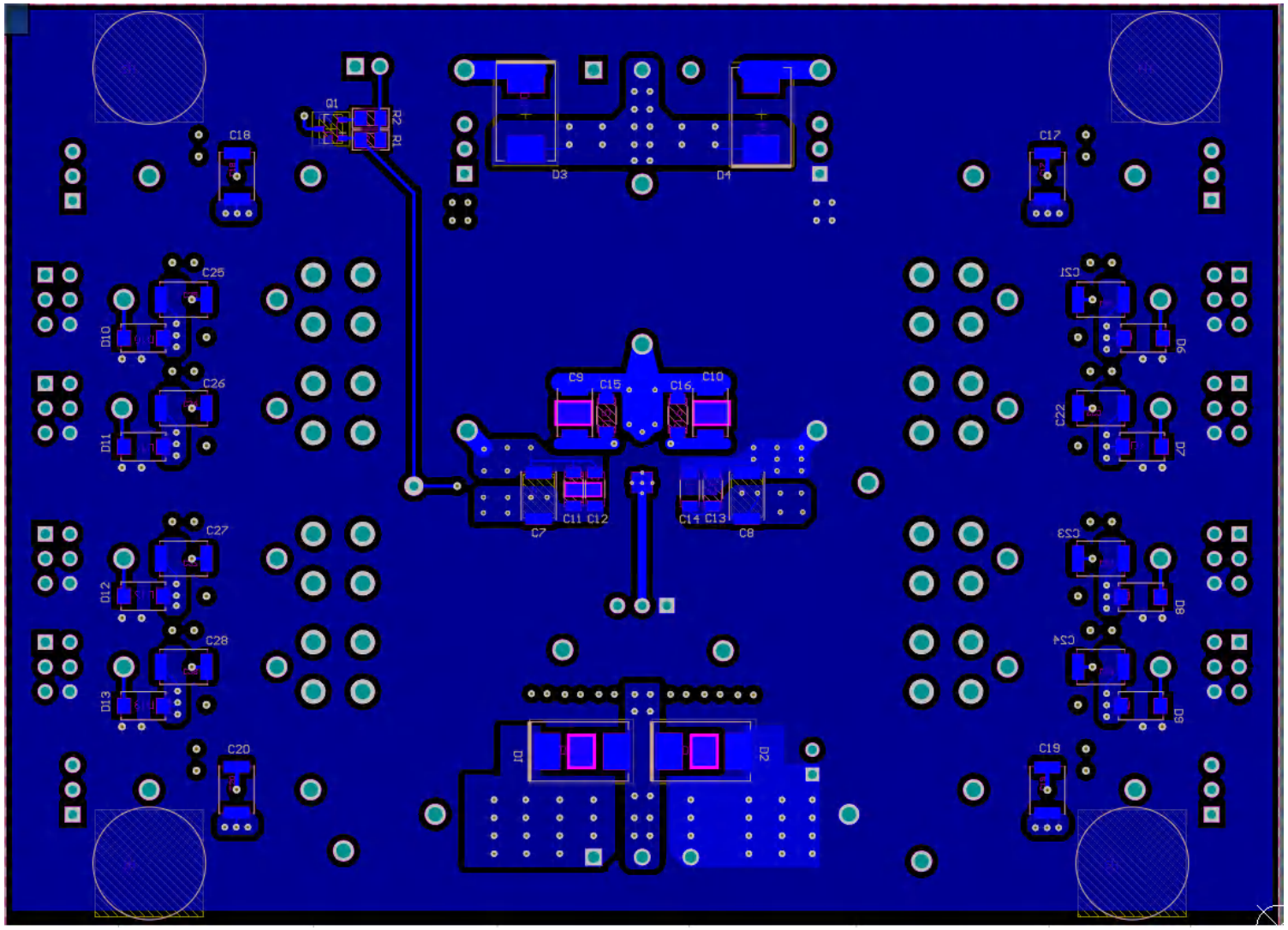

Figure 7-2. 2D Bottom View Layout

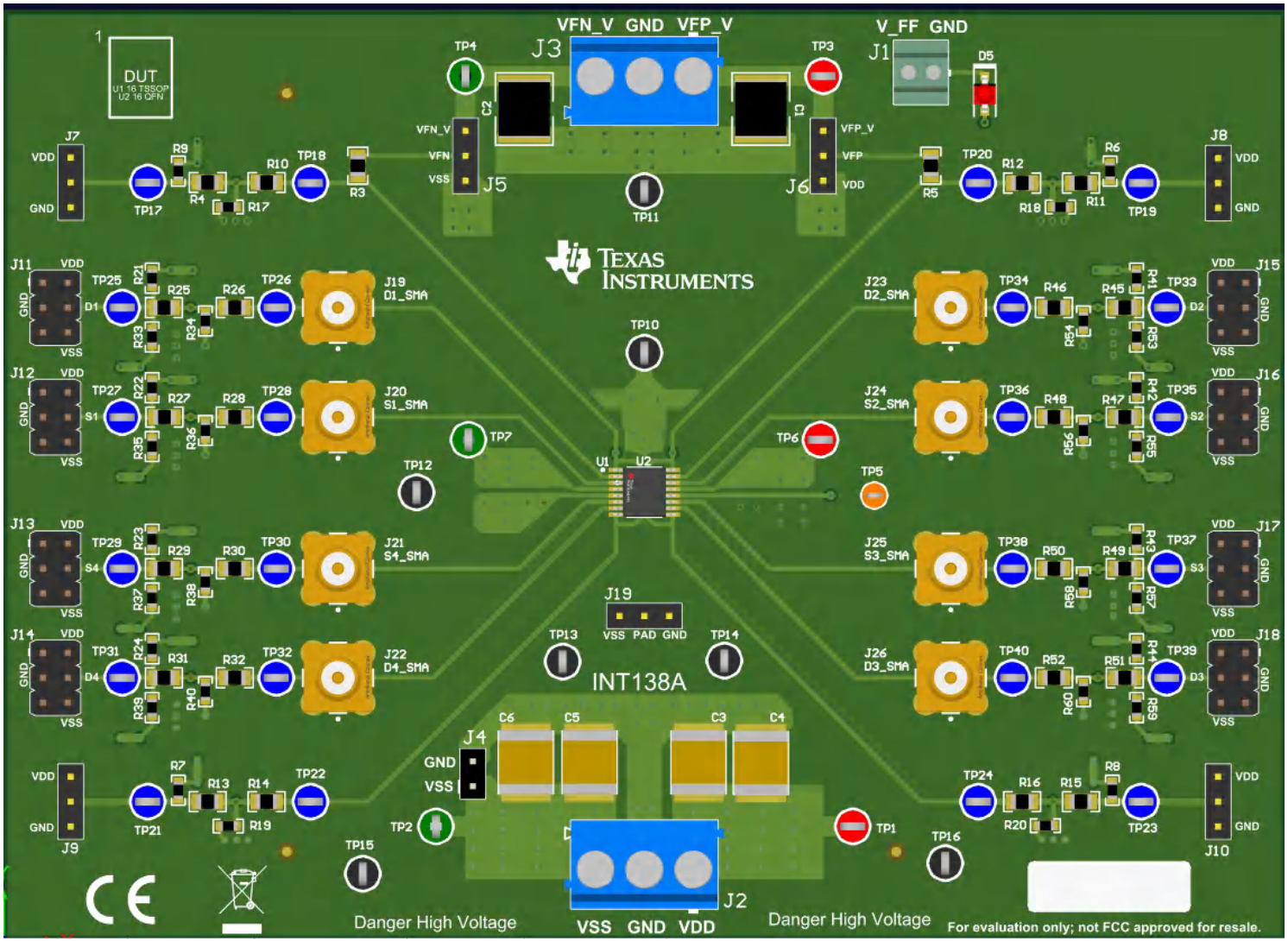

Figure 7-3. 3D Top View of Layout

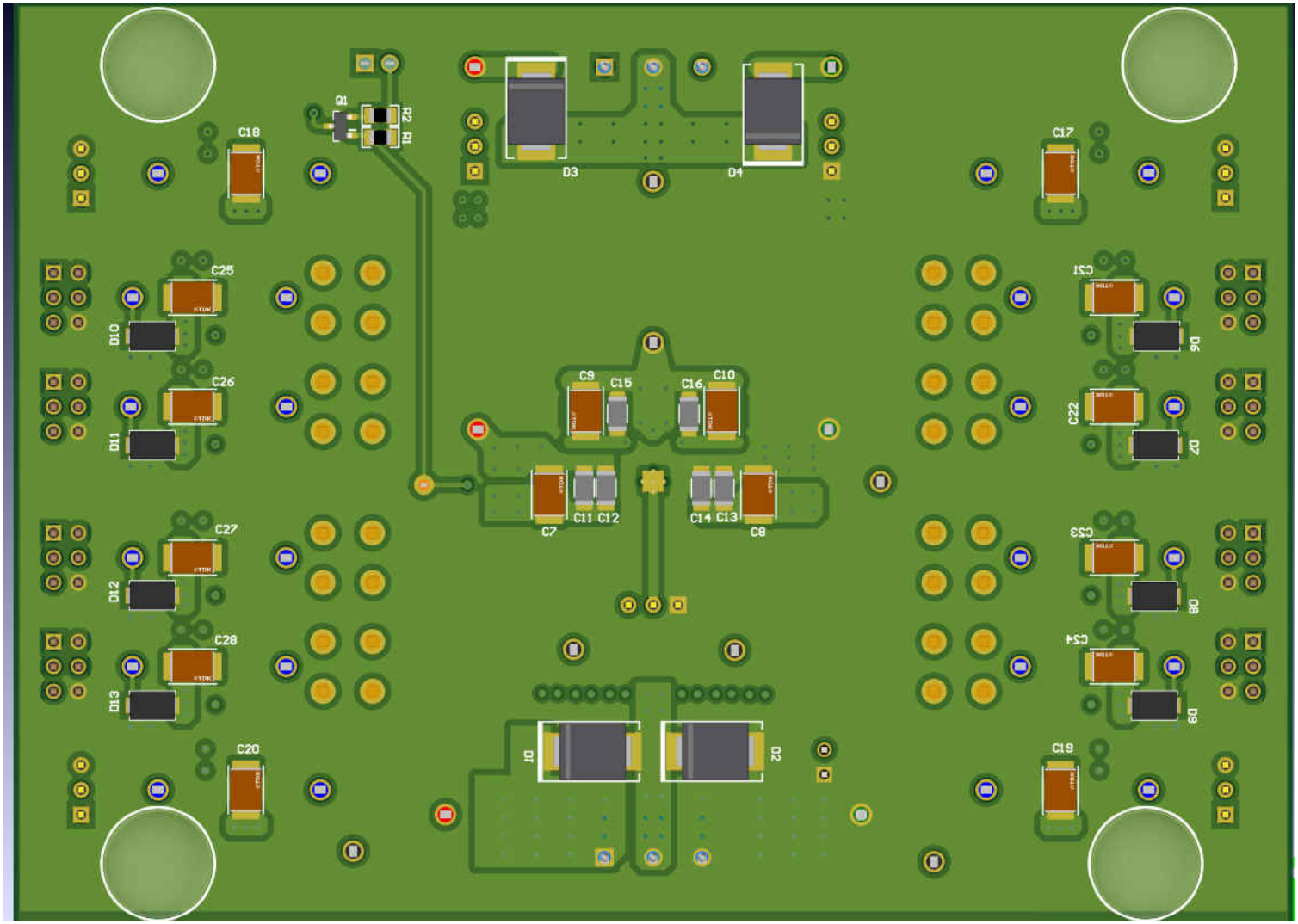

Figure 7-4. 3D Bottom View Of Layout

8 Related Documentation

- Texas Instruments, *TMUX7412F ±60-V Fault-Protected, 1:1 (SPST), Four-Channel Switches with 1.8-V Logic (Four Active High)*
- Texas Instruments, *TMUX7462F ±60-V Fault-Protected, Latch-Up Immune, 4-Channel Protector, Adjustable Fault Threshold, 1.8-V Logic*
- Texas Instruments, *TMUX741xF ±60 V Fault-Protected, 1:1 (SPST), 4-Channel Switches with 1.8-V Logic* data sheet

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