TEXAS INSTRUMENTS

TLV320AIC27 EVM

User's Guide

August 2000

AAP Data Conversion

SLAU051

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Preface

Read This First

About This Manual

This manual presents the user's guide for the TLV320AIC27 evaluation module.

How to Use This Manual

This document contains the following chapters and appendixes:

Chapter 1 – System Description
Chapter 2 – Modes of Operation
Appendix A –TLV320AIC27 Register Block Diagram
Appendix B –DSP Interface
Appendix C –Audio Control Block Diagram
Appendix D –EVM Shared Clock Configuration
Appendix E –Serial Interface Register Map
Appendix F –Software Drivers
Appendix G –PC Board and Bill of Materials
Appendix H –Schematics

Trademarks

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Chapter 1

System Description

Topic Page

1.1 Introduction

The TLV320AIC27 EVM is designed to be a daughterboard that directly plugs into the peripheral connector of any or TI's DSP DSK or EVM boards that have the 80-pin common-connector configuration. The TLV320AIC27 EVM also has an AMR connector available for use without the need of a DSP as a controller. The AIC27 EVM board is populated with one TLV320AIC27 device. The EVM is powered by either a 3.3-V or a 5-V power supply.

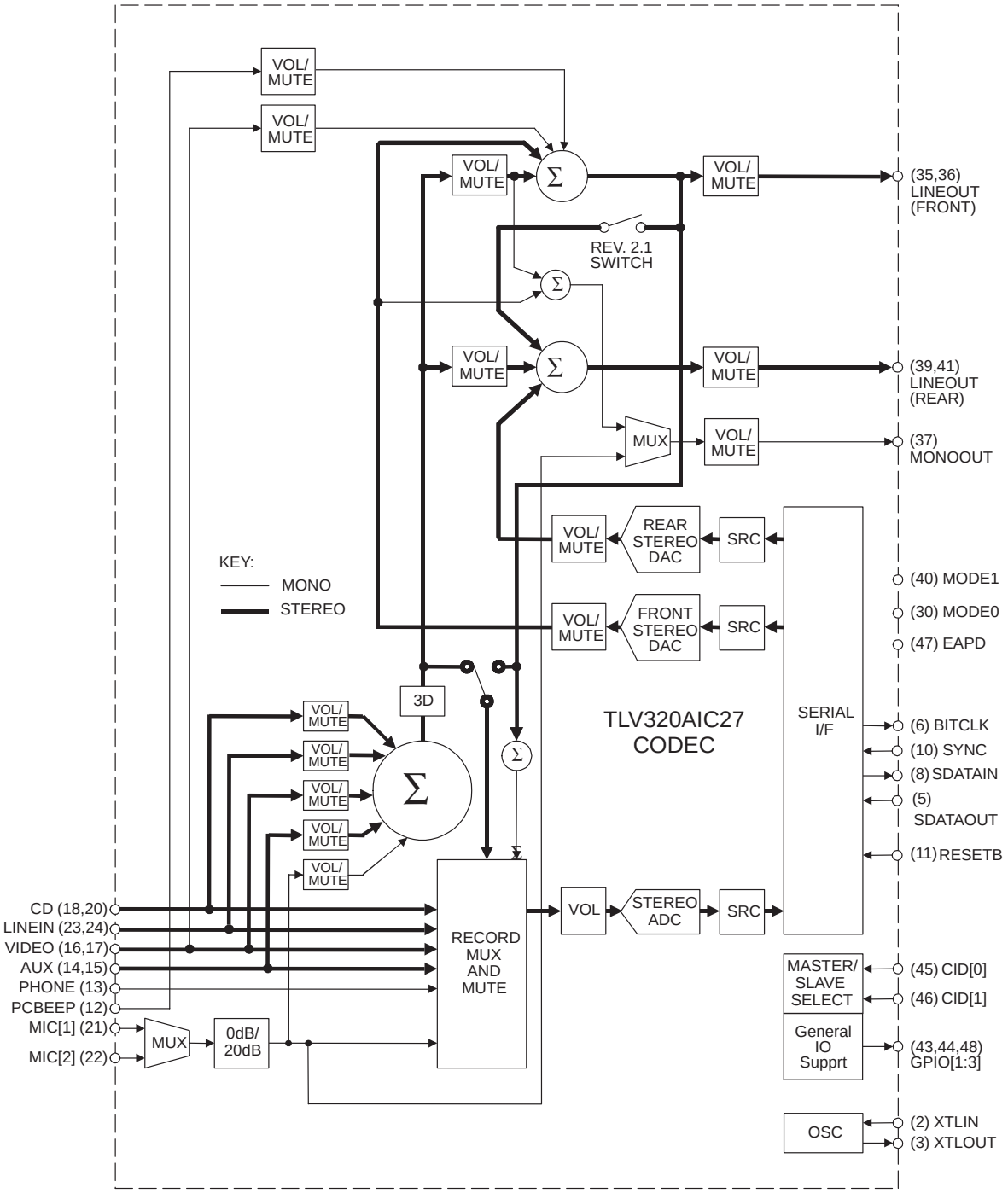
The TLV320AIC27 is a high-performance, AC'97 compliant audio CODEC specifically designed for use with TIs digital-signal processors (DSPs). This new 18-bit linear DSP codec transmits data at up to 48 kilosamples per second, contains a powerful serial interface, has four modes of operation, allows for variable sampling rates, and consumes only 139 mW of power at 3.3 V. This CODEC is well suited for audio applications such as telecommunications, surround sound, teleconferencing, and USB.

The TLV320AIC27 EVM manual assumes that the user has a working knowledge of Revision 2.1 of the AC97 CODEC standard.

1.2 TLV320AIC27 Device Block Diagram

Figure 1–1 shows the block diagram of the TLV320AIC27.

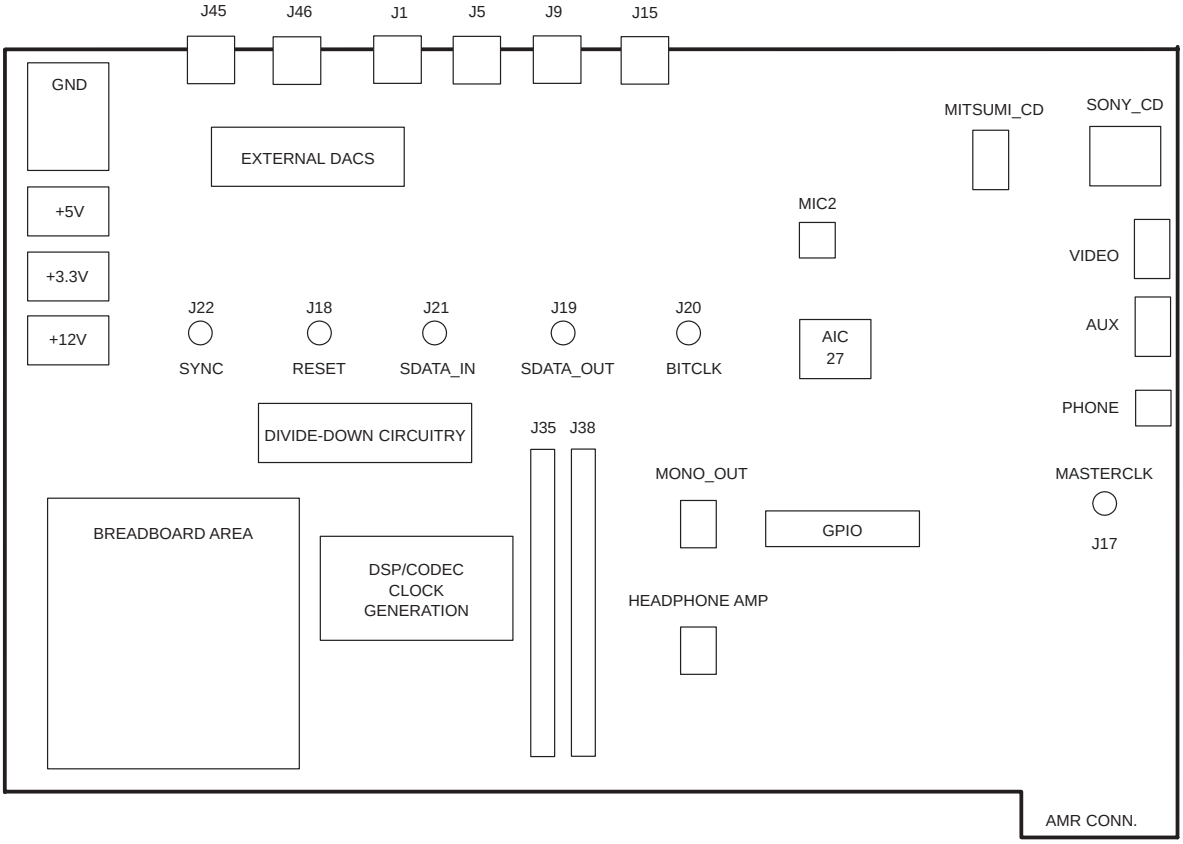
Figure 1–1. TLV320AIC27 Block Diagram



1.3 EVM Layout

Figure 1–2 shows the EVM layout

Figure 1–2. EVM Layout



1.4 TLV320AIC27 Jumper Description

The TLV320AIC27 EVM is designed to provide maximum flexibility to end users. It can be used with any DSP design kit that uses the common 80-pin connector as the controller. However, this EVM can also be used with a controller other than the DSP by using the AMR connector that allows access to critical signals and clocks. Control signals and clocks are also available to users via connectors and jumpers.

1.4.1 Summary of the Jumpers

Refer to the EVM schematics in Appendix H for the desired position of jumpers.

Quad and six-channel I^2S mode (jumpers J1–J12):
The quad and six-channel I^2S modes use external DACs. These jumpers offer users the flexibility to use these external DACs and to configure the surround-sound options as desired.

SYNC pulse generation (jumpers J13–J15, J29–J31):
There is more than one way to configure the DSP and CODEC. These jumpers provide flexibility in creating the SYNC pulse from BITCLOCK, and provide reset capability.

Mode selection (jumpers J19–J20):
These jumpers provide users control of the desired mode selection. Refer to the TLV320AIC27 data sheet and section 2.1 of this user's manual for more information.

Power options (jumpers J21, J22, J43–J44):
These jumpers are used for the selection of the power options.

Shared master clock (jumpers J16–J18):
These jumpers are used to control the shared master-clock options.

DSP/CODEC configuration (jumpers J23, J24, J34, J36, J37, J39–J41):
These jumpers provide users access to signals and clocks to allow flexibility in configuring the DSP or any other controller with the TLV320AIC27 CODEC.

Table 1–1. Jumper Description

TLV320AIC27 DELIVERED DEFAULT JUMPER POSITIONS		
J18	DSP 1.8-V master clock	Pins 1–2 shorted
J22	DSP regulator	Pins 1–2 shorted
J23	SYNC signal	Pins 1–2 shorted
J36	RESETB signal	Pins 1–2 shorted
J39	SDATA_IN0	Pins 1–2 shorted
J7	3-V or 5-V option	Pins 1–2 shorted
J17	CODEC 3.3-V master clock	Pins 1–2 shorted
J44	5 V from DSP power	Pins 1–2 shorted
J19	Mode pin	Open
J20	Mode pin	Open

1.4.2 Jumper List

JUMPER	NAME	DESCRIPTION
J1	D1_GPIO1	DAC #1 GPIO1 pin
J2	D1_GPIO3	DAC #1 GPIO3 pin
J3	D1_BITCLOCK	DAC #1 BITCLOCK
J4	D1_FORMAT	DAC #1 format control
J5	D1_DEEMPH	DAC #1 DEEMPH control
J6	D1_MUTE	DAC #1 mute control
J7	D2_GPIO1	DAC #2 GPIO1 pin
J8	D2_GPIO2	DAC #2 GPIO2 pin
J9	D2_BITCLOCK	DAC #2 BITCLOCK
J10	D2_MUTE	DAC #2 mute control
J11	D2_DEEMPH	DAC #2 DEEMPH control
J12	D2_FORMAT	DAC #2 format control
J16	CODEC_CRYSTAL	Control to onboard CODEC-only crystal
J17	CODEC_MC	Control to onboard DSP-only crystal
J18	DSP_MC	Control to onboard DSP-only crystal
J19	MODE0	Mode control pin 30
J20	MODE1	Mode control pin 40
J21	5V_ISOL	Prevent 5 V to regulator
J22	DSP_REG	Sets up DSP for needed voltages
J24	SDATAOUT	Serial data out of DSP
J36	RESETB	Reset
J34	CRYSTAL	Master clock for AMR connector
J37	X_FSRO	DSP frame-sync receive control
J23	SYNC	AC97 sync control
J39	SDATA_IN0	DSP serial data into DSP
J40	X_CLKXO	DSP CLK transmit
J41	X_CLKRO	DSP clock receive
J43	12V	12-V control
J44	5V	5-V control
J31	DIVIDE_IN	Create frame-sync-circuitry control
J32	DIVIDE_HI	Create frame-sync-circuitry control
J33	DIVIDE_RESET	Create frame-sync-circuitry control
J28	DIVIDE_HIJ	Create frame-sync-circuitry control
29	DIVIDE_RESET	Create frame-sync-circuitry control
J15	DIVIDE_G	Create frame-sync-circuitry control
J14	DIVIDE_OUT	Create frame-sync-circuitry control
J13	DIVIDE_G_OUT	Create frame-sync-circuitry control
J42	STEP_UP_IN	Step-up clock level control
J26	STEP_UP_OUT	Step-up clock level control

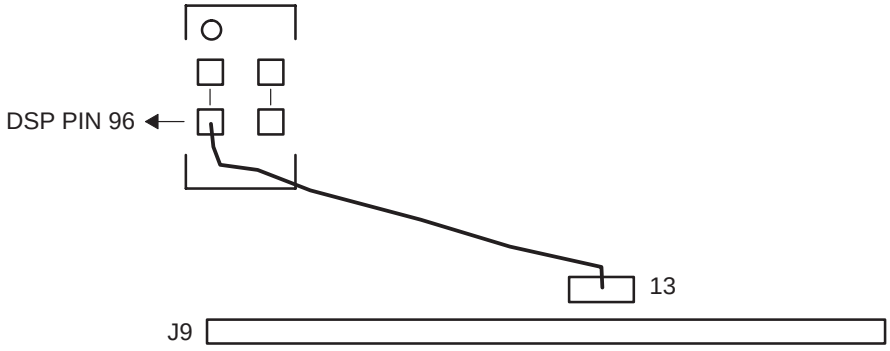
1.5 Getting Started

1.5.1 DSP DSK Setup

This procedure uses the TI C5402 DSK. If another 80-pin common-connector type DSP DSK is used instead of the C5402, refer to the specific manuals for the necessary signal connections to the board. This getting-started procedure uses a configuration of DSP and AIC27 CODEC running from the same clock (see *Shared Clock Configurations* in Appendix D). Complete the following two steps:

1) On the TI DSP5402 DSK, remove crystal Y2 and capacitors CAP57 and CAP70. A connection needs to be made from pin 96 of the DSP to J9–13 of the DSP DSK. The now unused crystal pad closest to pad CAP70 can be used to connect to DSP pin 96. This connection to J9–13 will allow the CODEC EVM master clock to be connected to the DSP (see Figure 1–3).

Figure 1–3. Pin 96 to DSK J9–13 Connection



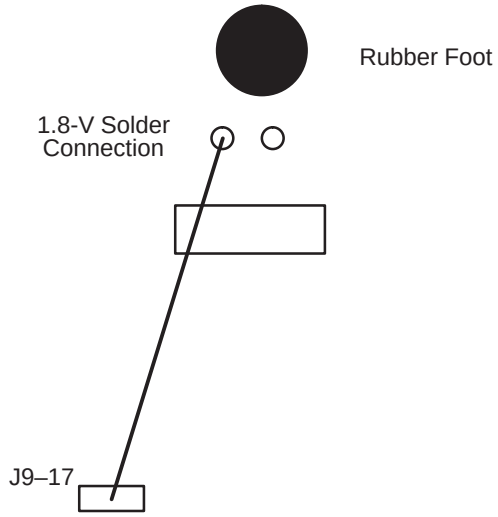
2) Connect J9–17 to the 1.8-V solder connection. This connection allows 1.8 V to be used on the CODEC EVM board (see Figure 1–4).

   a) Power up the C5402 DSK board and place the DSK with the side with the rubber feet facing up.

   b) With a voltmeter, measure the 1.8 V from the solder connection as shown below.

   c) Connect a wire from J9–17 to the 1.8-V solder connection as shown below.

Figure 1–4. Connection of J9–17 to 1.8 V



3) Connect the DSP DSK's parallel port to the PC using the DSK cable provided.

4) Set the dip switch (SW1) on the DSP DSK accordingly:

   a) If using parallel port DSP to PC connector,
      1 = Down
      2 = Down
      3 = Down
      4 = Up
      5 = Down
      6 = Up
      7 = Down
      8 = Down

   b) If using DSP JTAG to PC connector,
      1 = UP
      2 = Down
      3 = Down
      4 = Up
      5 = Down
      6 = Up
      7 = Down
      8 = Down

1.5.2 TLV320AIC27 EVM Setup

1) Attach the TLV320AIC27 EVM board to the DSP 5410 DSK using the two common 80-pin connectors.

2) Connect the following jumpers on the TLV320AIC27 EVM:

   a) J7 – Selects either 3 V or 5 V (short two pins)

   b) J17 – Codec master clock (3.3 V) (short two pins)

   c) J18 – DSP master clock (1.8 V) (short two pins)

   d) J22 – DSP regulator (short two pins)

   e) J23 – SYNC signal (short two pins)

   f) J36 – RESETB signal (short two pins)

   g) J39 – SDATA_IN0 (short two pins)

   h) J44 – 5 V from DSP power (short two pins)

   i) J19 – Mode pin (open)

   j) J20 – Mode pin (open)

3) Turn power on DSP DSK (power to both DSP DSK and CODEC EVM from DSP power).

4) Load Code Composer Studio.

5) Under File, select Load Program. Load AIC27driver.out (updates located on TI web site).

6) Under Project, select Open and Load AIC27driver.mak (updates located on TI web site).

7) Hit F5 (Run) or select Run under Debug.

8) To stop the program from running, select Halt under Debug.

9) To make changes to signal path, programmable gain amplifier (PGA), or modes, edit file taic27_ob.c contained in directory Project/Source (displayed in code composer). Refer to data sheet for register descriptions and values. The serial interface register map is located in Appendix E.

10) The TLV320AIC27 EVM has the available hardware on board to run in configurations b and c, as shown in Figure 1–5.

1.6 DSP-CODEC Configurations

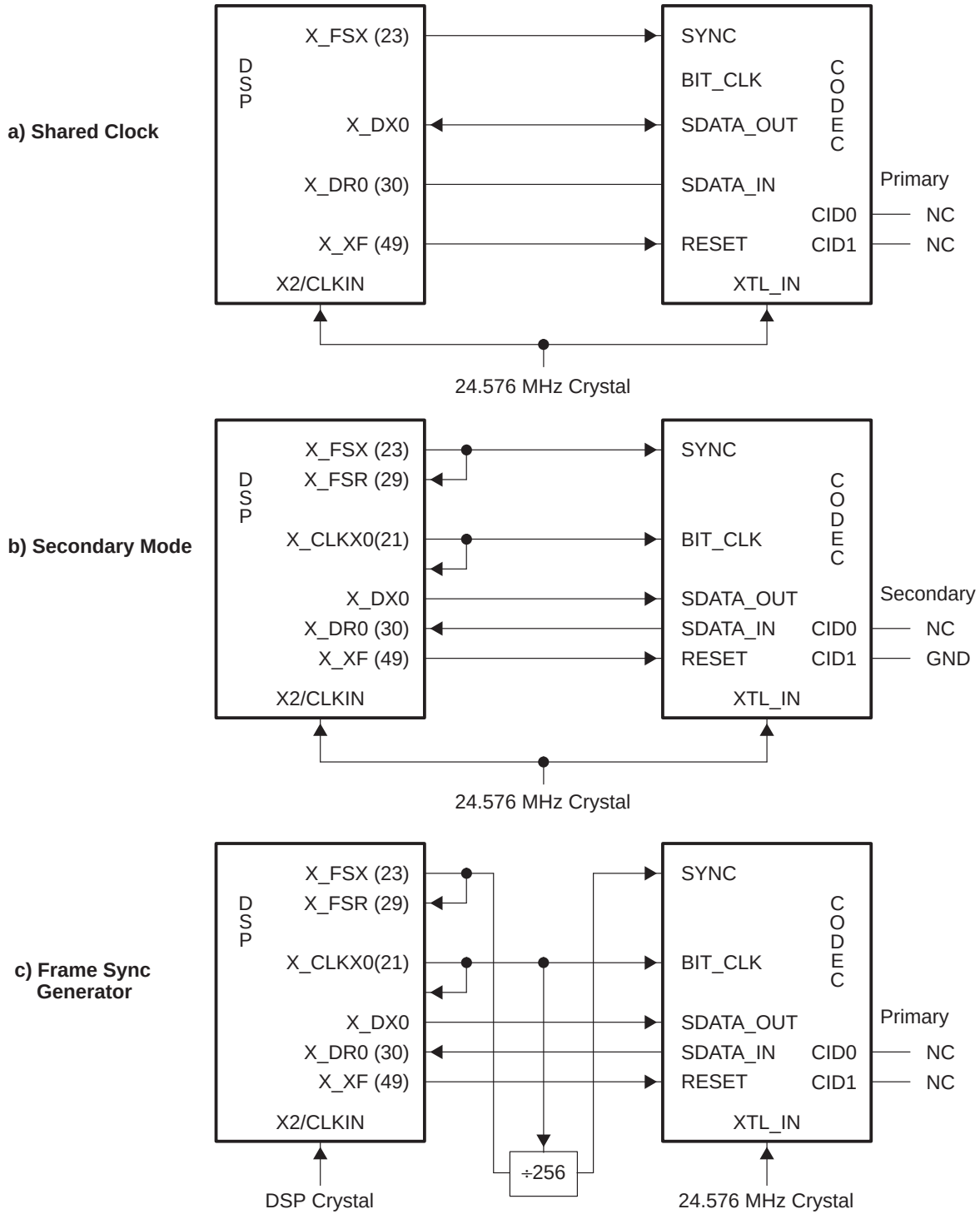
Figure 1–5 illustrates three possible DSP and CODEC configurations. They are:

1) DSP and CODEC sharing the same master clock. This is the configuration used in this manual. The configurations used to drive both DSP and CODEC are shown in Appendix D.

2) DSP and CODEC sharing the same master clock, with the CODEC in secondary mode. To place the CODEC in secondary mode, populate R9 with a resistor with a value between 1 Ω and 50 Ω. Both FRAME SYNC and BITCLOCK are from the DSP.

3) The DSP and CODEC run at their own unique master clocks. The frame sync is created by the BITCLOCK by divide-down circuitry provided on the EVM board. Jumpers 13 to 15, and 29 to 31 are used to implement this configuration. Refer to the schematics on page 8 of Appendix H for additional information.

Figure 1–5. DSP-CODEC Configurations



Chapter 2

Modes of Operation

This chapter describes the modes of operation of the TLV320AIC27 EVM.

Topic **Page**

2.1 Introduction to the TLV320AIC27 Modes

The TLV320AIC27 has four modes of operation. The EVM will allow any of the four modes by configuring jumpers J19 and J20. The four modes are:

1) Basic two-channel mode
2) I^2S six-channel mode
3) Quad mode
4) Modem mode

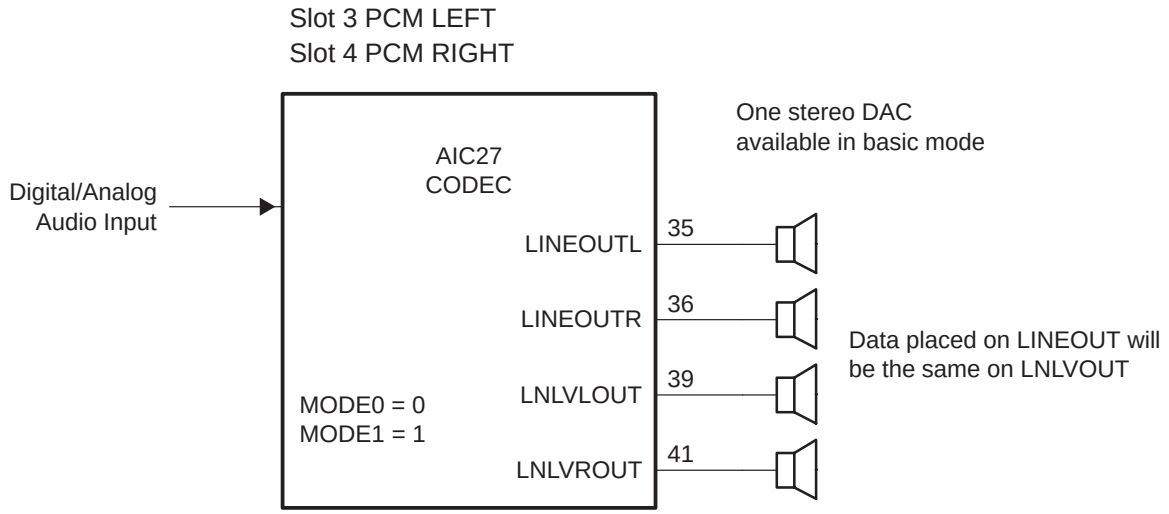
Table 2–1. TLV320AIC27 Modes

Mode1 J20	Mode0 J19	Operational Mode	Resulting Device Behavior
0	0	Basic	Two-channel mode codec
0	1	Six-channel I^2S	Six-channel I^2S mode codec
1	0	Quad	Quad DAC mode (with I^2S six-channel support)
1	1	Modem	Modem DAC mode

2.2 Basic Mode

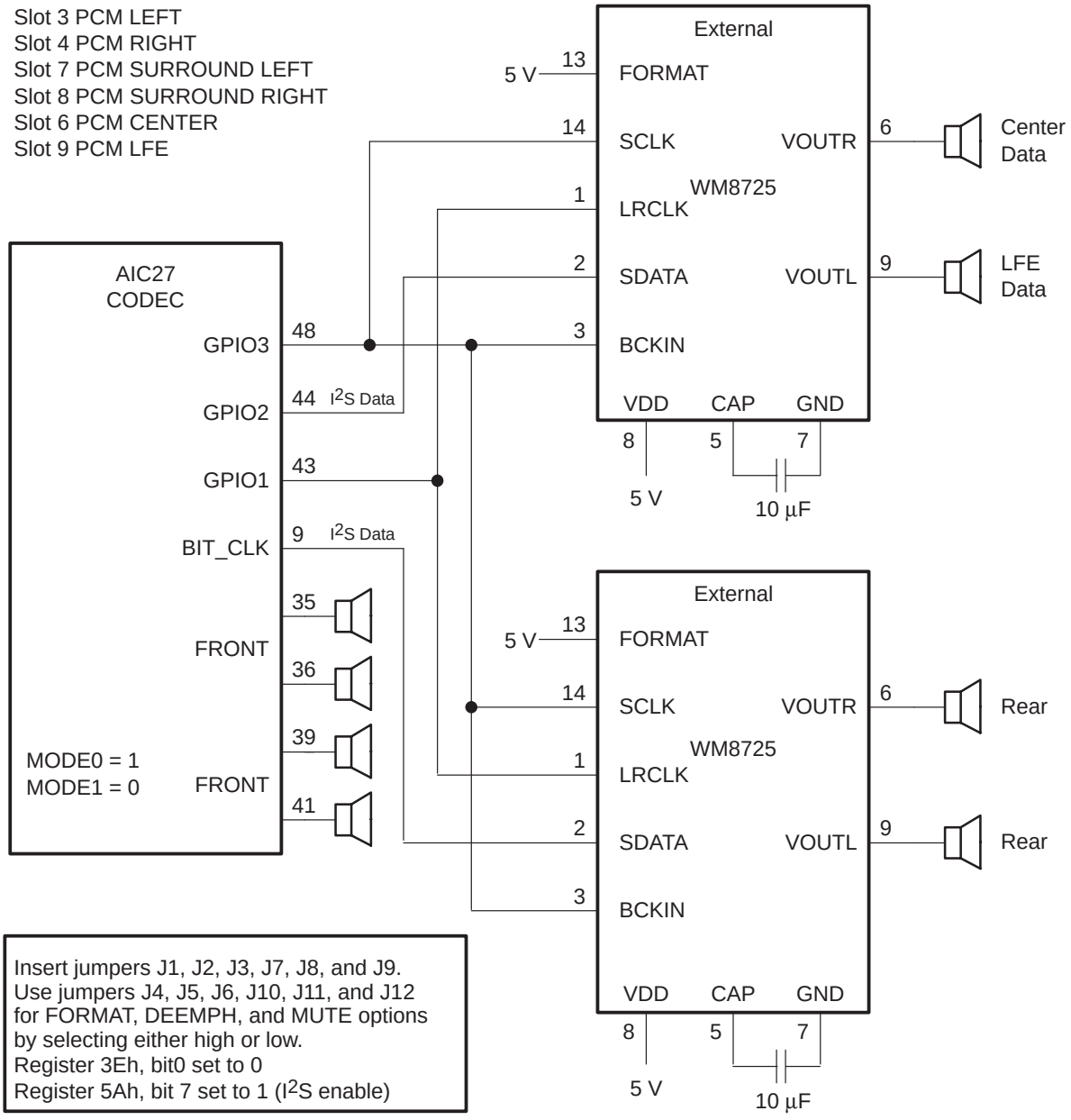
The basic mode is illustrated in Figure 2–1.

Figure 2–1. Basic Mode



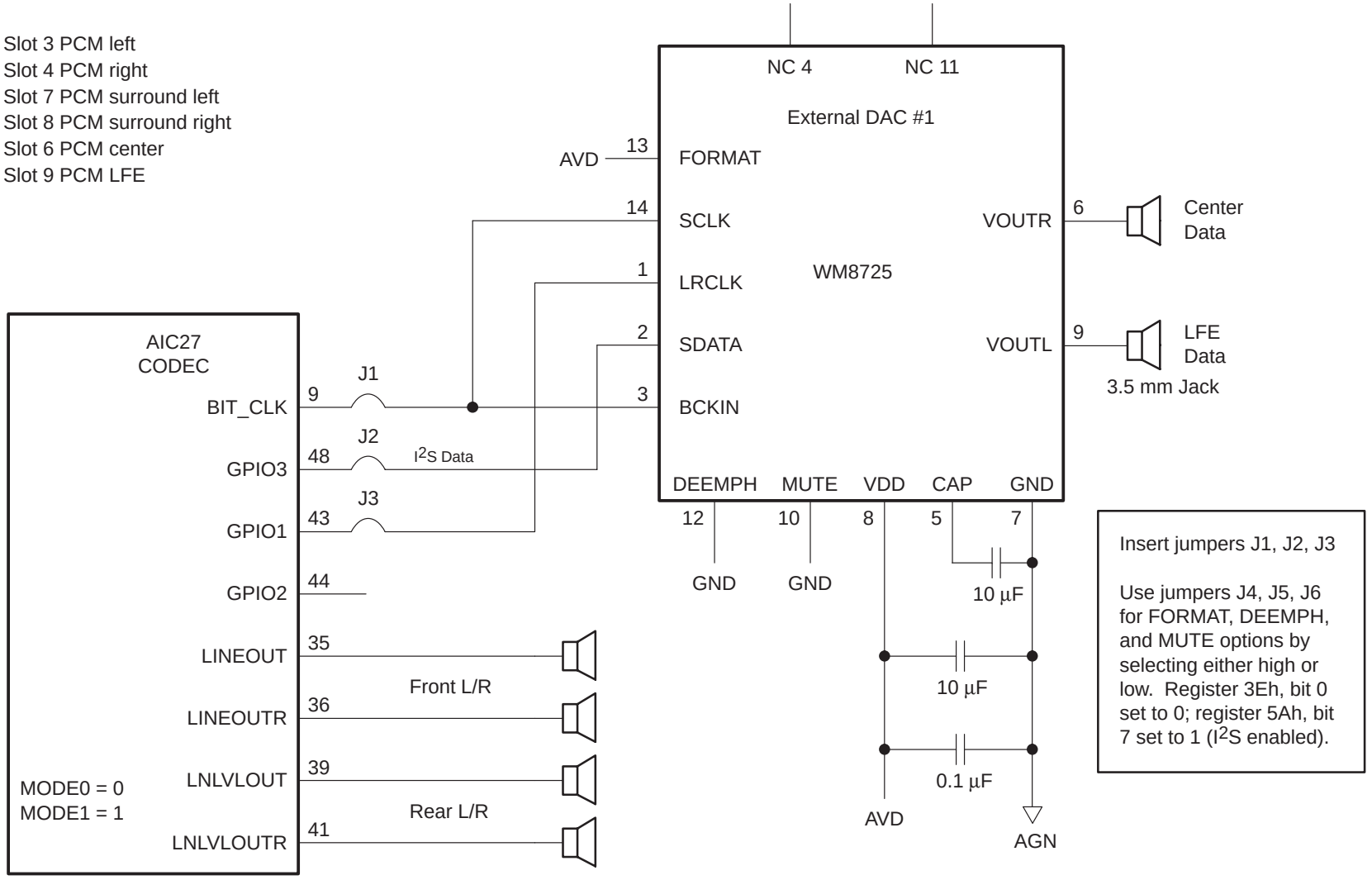
2.3 Six-Channel I2S Mode

Figure 2–2. Six-Channel I2S Mode



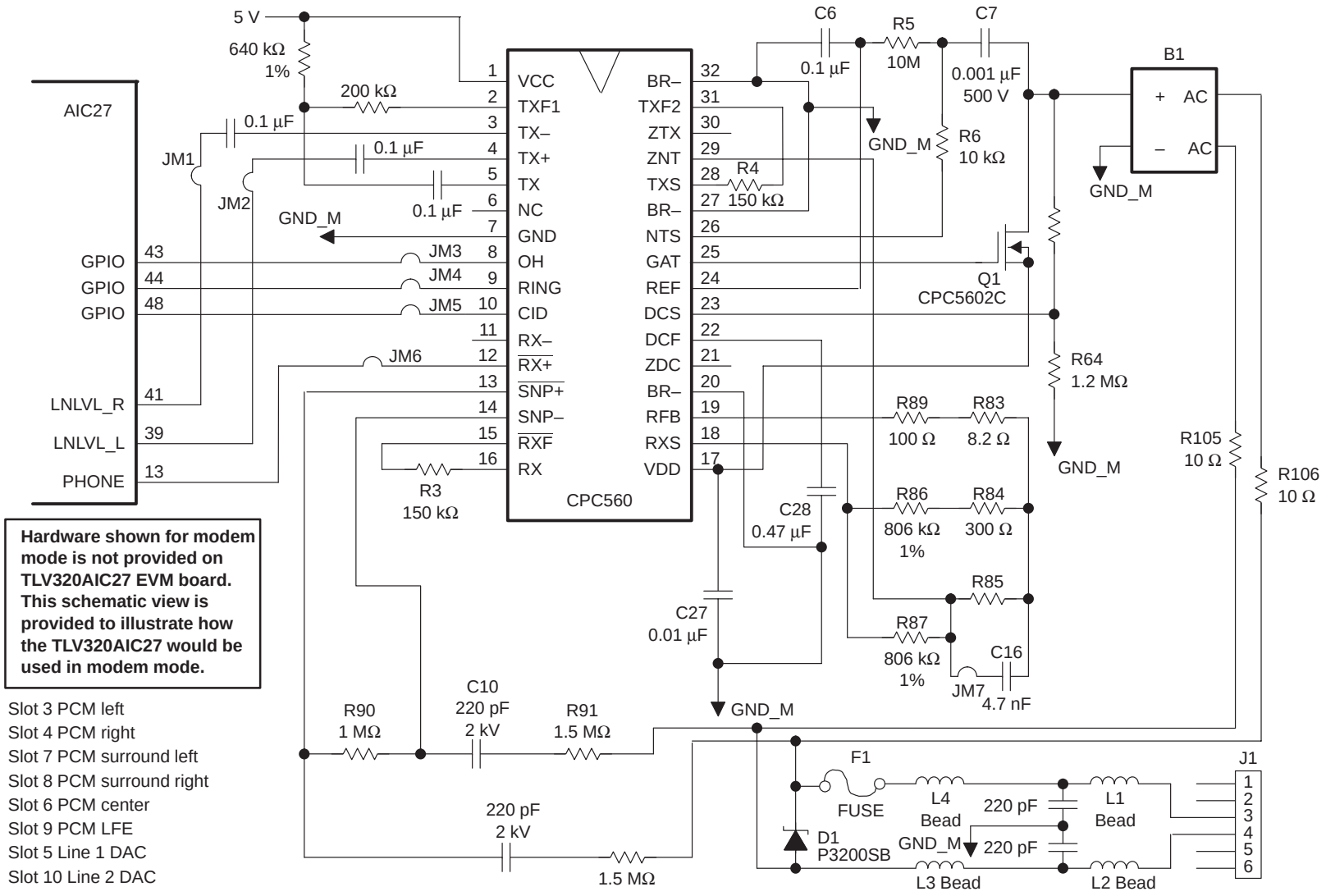
2.4 Quad Mode

Figure 2–3. Quad Mode



2.5 Modem Mode

Figure 2–4. Modem Mode



Hardware shown for modem mode is not provided on TLV320AIC27 EVM board. This schematic view is provided to illustrate how the TLV320AIC27 would be used in modem mode.

Slot 3 PCM left
Slot 4 PCM right
Slot 7 PCM surround left
Slot 8 PCM surround right
Slot 6 PCM center
Slot 9 PCM LFE
Slot 5 Line 1 DAC
Slot 10 Line 2 DAC

2.6 Power Supply Description

The TLV320AIC27 EVM receives its power from the DSP EVM board. The voltages supplied to the EVM from the DSP are 1.8 V, 3.3 V, 5 V, and 12 V. The voltage sources are as follows:

- ❑ The 1.8 V comes from the DSP (5-V power plug regulated to 1.8 V).
- ❑ The 3.3 V comes from the DSP (5-V power plug regulated to 3.3 V).
- ❑ The 5 V comes from the DSP.
- ❑ The 12 V comes from the AUX power connection on the DSP.

The voltage used on the EVM is DV_{DD} (digital) and AV_{DD} (analog), and VDSP18 (DSP clock voltage).

DV_{DD} is either 3.3 V or 5 V, as determined by a jumper (J7) which comes from the DSP.

AV_{DD} is 5 V, and comes from either the DSP by using J44, or from the 12-V AUX power connector on the DSP, which is regulated to 5 V on the CODEC EVM board using J43.

2.6.1 DSP Power Options

If using external 12 V from the DSP DSK AUX connector:

- ❑ Connect J43 (short pins 1 and 2) and J21 (short pins 1 and 2).

If using 5 V from the DSP power supply:

- ❑ Connect J44 (short pins 1 and 2) and leave J21 off.

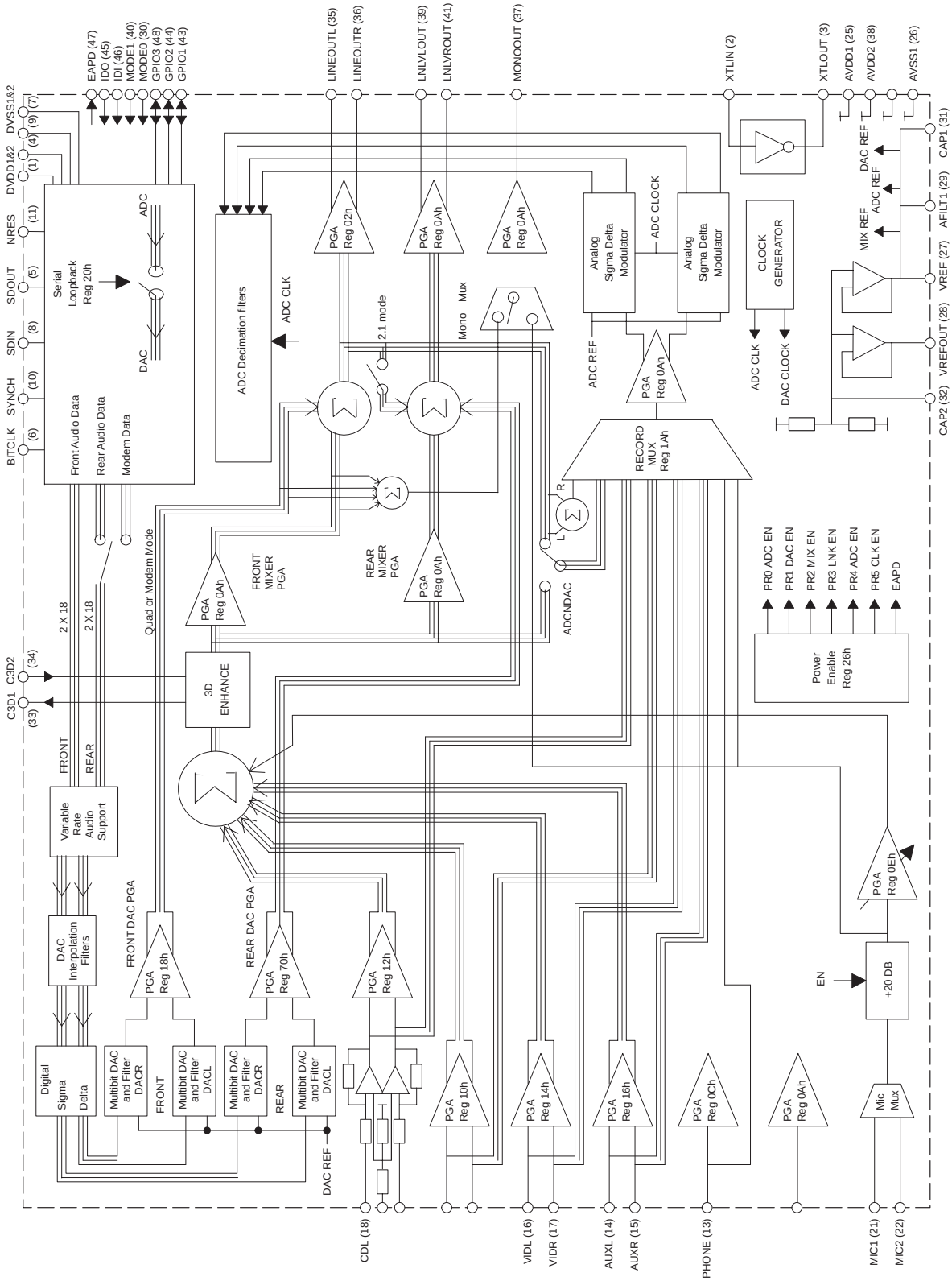
2.6.2 Power Connections When Not Using the DSP as a Controller

- ❑ Use the 12-V, 5-V, and 3.3-V connections available on the breadboard area as required.

Appendix A

TLV320AIC27 Register Block Diagram

This appendix presents the TLV320AIC27 register block diagram.


EAPD (47)
IDO (45)
IDI (46)
MODE1 (40)
MODE0 (30)
GPIO3 (48)
GPIO2 (44)
GPIO1 (43)
LINEOUTL (35)
LINEOUTR (36)
LNLVLOUT (39)
LNLVROUT (41)
MONOOUT (37)
XTLIN (2)
XTLOUT (3)
AVDD1 (25)
AVDD2 (38)
AVSS1 (26)
DVSS1&2
DVDD1&2
NRES (11)
SDOUT (5)
SDIN (8)
SYNCH (10)
BITCLK (6)
CAP1 (31)
AFILT1 (29)
VREF (27)
VREFOUT (28)
CAP2 (32)
C3D2 (34)
C3D1 (33)
Serial Loopback Reg 20h
ADC
DAC
Front Audio Data
Rear Audio Data
Modem Data
ADC Decimation filters
ADC CLK
2:1 mode
Mono Mux
PGA Reg 02h
PGA Reg 0Ah
Analog Sigma Delta Modulator
ADC CLOCK
CLOCK GENERATOR
DAC REF
ADC REF
MIX REF
ADC CLK
DAC CLOCK
RECORD MUX Reg 1Ah
Quad or Modem Mode
2 X 18
FRONT MIXER PGA
REAR MIXER PGA
ADCNDAC
PR0 ADC EN
PR1 DAC EN
PR2 MIX EN
PR3 LNK EN
PR4 ADC EN
PR5 CLK EN
EAPD
Power Enable Reg 26h
3D ENHANCE
FRONT
REAR
Variable Rate Audio Support
DAC Interpolation Filters
FRONT DAC PGA
REAR DAC PGA
PGA Reg 18h
PGA Reg 70h
PGA Reg 12h
PGA Reg 0Eh
EN
+20 DB
Digital Sigma Delta
Multibit DAC and Filter DACR
Multibit DAC and Filter DACL
PGA Reg 10h
PGA Reg 14h
PGA Reg 16h
PGA Reg 0Ch
Mic Mux
CDL (18)
VIDL (16)
VIDR (17)
AUXL (14)
AUXR (15)
PHONE (13)
MIC1 (21)
MIC2 (22)

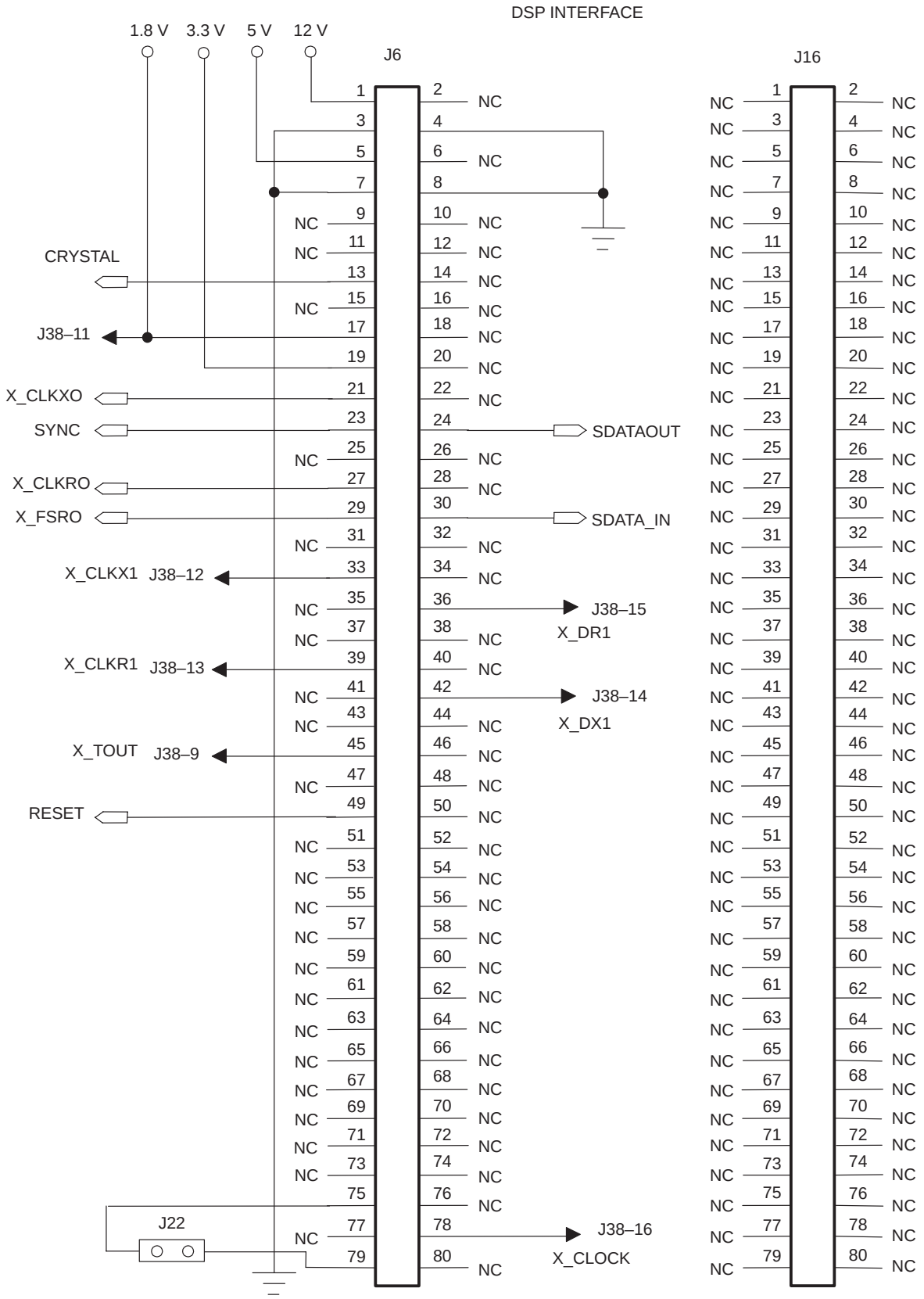
Appendix B

DSP Interface

This appendix presents the DSP interface schematic diagram.

Topic **Page**

B.1 DSP Interface Diagram



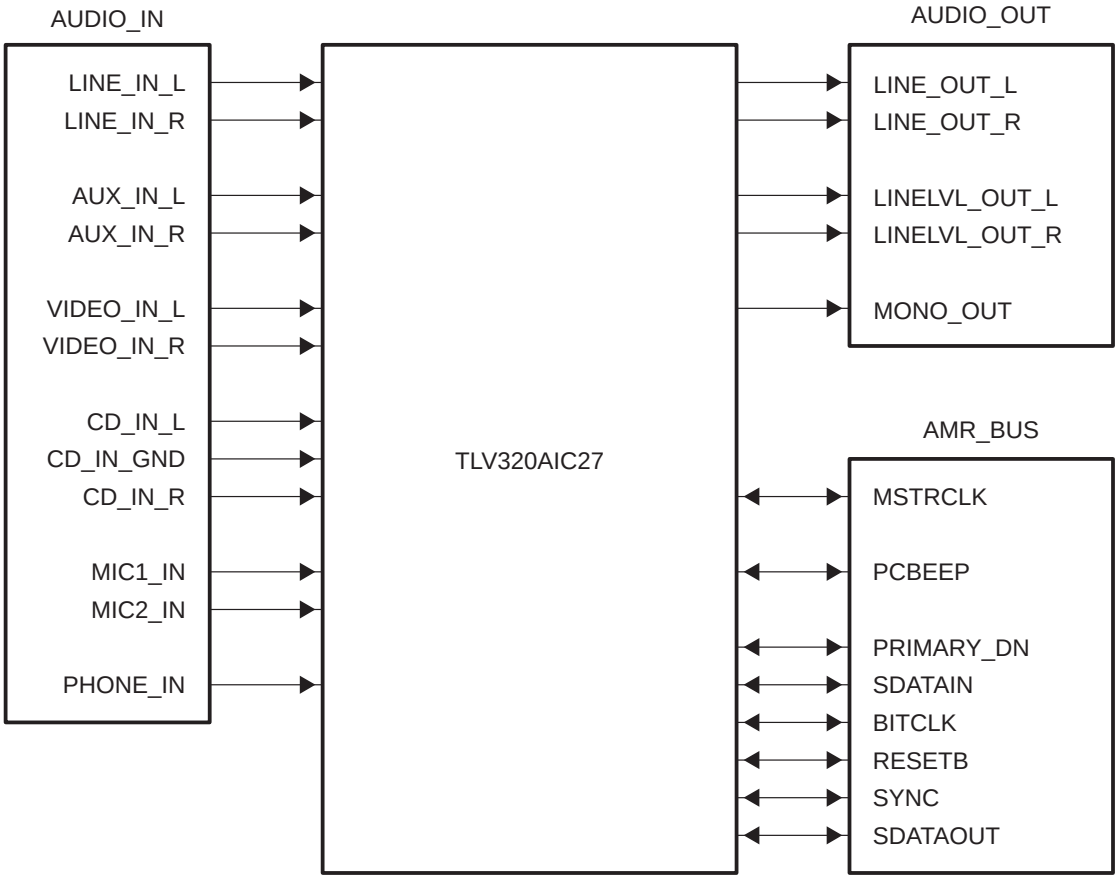
Appendix C

Audio Control Block Diagram

This appendix presents the audio-control block diagram.

Topic **Page**

C.1 Audio-Control Block Diagram



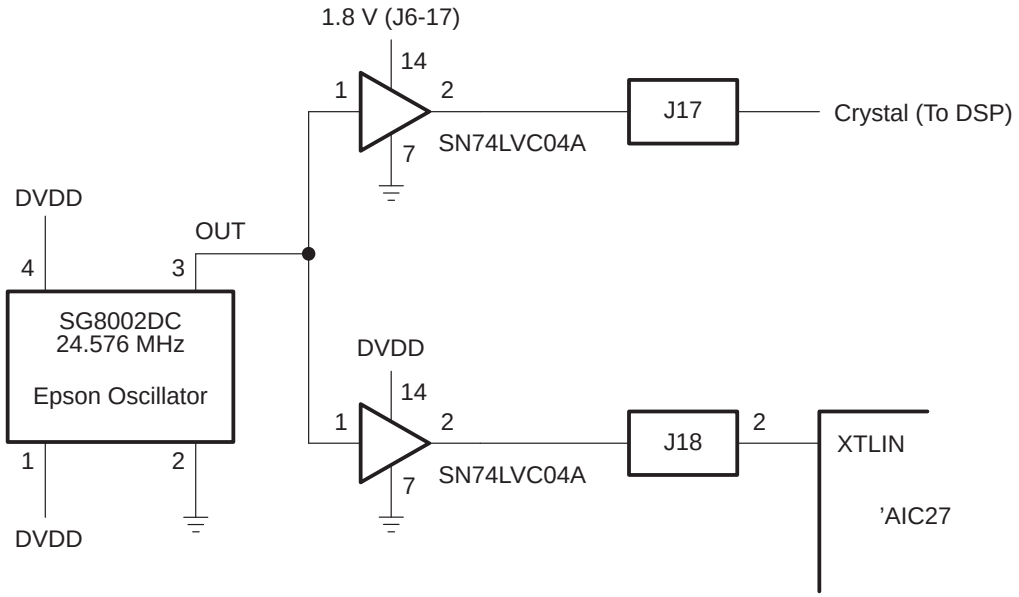
Appendix D

EVM Shared Clock Configuration

The following illustration shows the TLV320AIC27 shared clock configuration.

Topic **Page**

D.1 Shared Clock Configuration



Appendix E

Serial Interface Register Map

The following table shows the functions and addresses of the various control bits that are loaded through the serial interface during write operations.

Topic **Page**

Table E–1.Serial Interface Register Map Description

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6150h
02h	Master volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master volume mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PCBEEP volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	8000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic volume	Mute	X	X	X	X	X	X	X	X	20 dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line-in volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	Front PCM out volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Receiver select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Receiver gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General purpose	POP	ST	3D	ID	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	8000h
22h	3D control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
24h	Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0000h
26h	Power-down ctrl/stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended audio ID	ID1	ID0	X	X	X	X	Amap	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0281h
2Ah	Extended audio ctrl/stat	X	PRL	PRK	PRJ	PRI	X	Madc	Ldac	Sdac	Cdac	X	X	VRM	X	DRA	VRA	0080h
2Ch	Front DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
2Eh	Rear DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
30h	LFE DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	Audio ADC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
36h	Six channel vol. C, LFE	Mute	x	x	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	x	x	CNT4	CNT3	CNT2	CNT1	CNT0	8080h
38h	Six channel vol. L, R surround	Mute	x	x	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	x	x	RSR4	RSR3	RSR2	RSR1	RSR0	8080h

Table B–1.Serial Interface Register Map Description (Continued)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	CID2	CID1	HSET	LIN2	LIN1	x00xh
3Eh	Extended modem stat	PRH	PRG	PRF	PRE	PD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	0100h
40h	Line1 sample rate ADC/ DAC	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line2 sample rate ADC/ DAC	Sample rates written to 42h will alias onto 40h																
46h	Line1 DAC/ADC level	Not supported – set TX modem levels by writing to rear DAC PGA 04h																
48h	Line2 DAC/ADC level	Not supported – set TX modem levels by writing to rear DAC PGA 04h																
4Ch	GPIO pin configuration	0	0	GW13	GW12	GW1	0	0	0	0	0	0	0	0	0	0	0	000Eh
4Eh	GPIO pin type	1	1	GC13	GC12	GC11	1	1	1	1	1	1	1	1	1	1	1	FFFFh
50h	GPIO pin sticky	0	0	GP13	GP12	GP11	0	0	0	0	0	0	0	0	0	0	0	0000h
52h	GPIO wake-up	0	0	GS13	GS12	GS11	0	0	0	0	0	0	0	0	0	0	0	0000h
54h	GPIO pin status	0	0	GI13	GI12	GI11	0	0	0	0	0	0	0	0	0	0	0	000xh
56h	Misc. modem ctrl/stat	CID2	CID1	CIDR	MLNK	x	HSB2	HSB1	HSB0	x	L2B2	L2B1	L2B0	x	L1B2	L1B1	L1B0	0000h
5Ah	Vendor reserved test	ATST	DTST	AFTS	DFTS	RTST	DDS	AMD	DLM	I2S	R2S	AND	HIM	HIC	TRM	BB	AEV	0000h
70h	Rear PCM out volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	0808h
72h	Front mixer volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
74h	Rear mixer volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
7Ah	Vendor reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574Dh
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0	4C0xh

Appendix F

Software Drivers

This appendix presents the software drivers.

Topic **Page**

F.1 Software Drivers

The TLV320AIC27 software package may be downloaded from the TLV320AIC27 EVM product page web site.

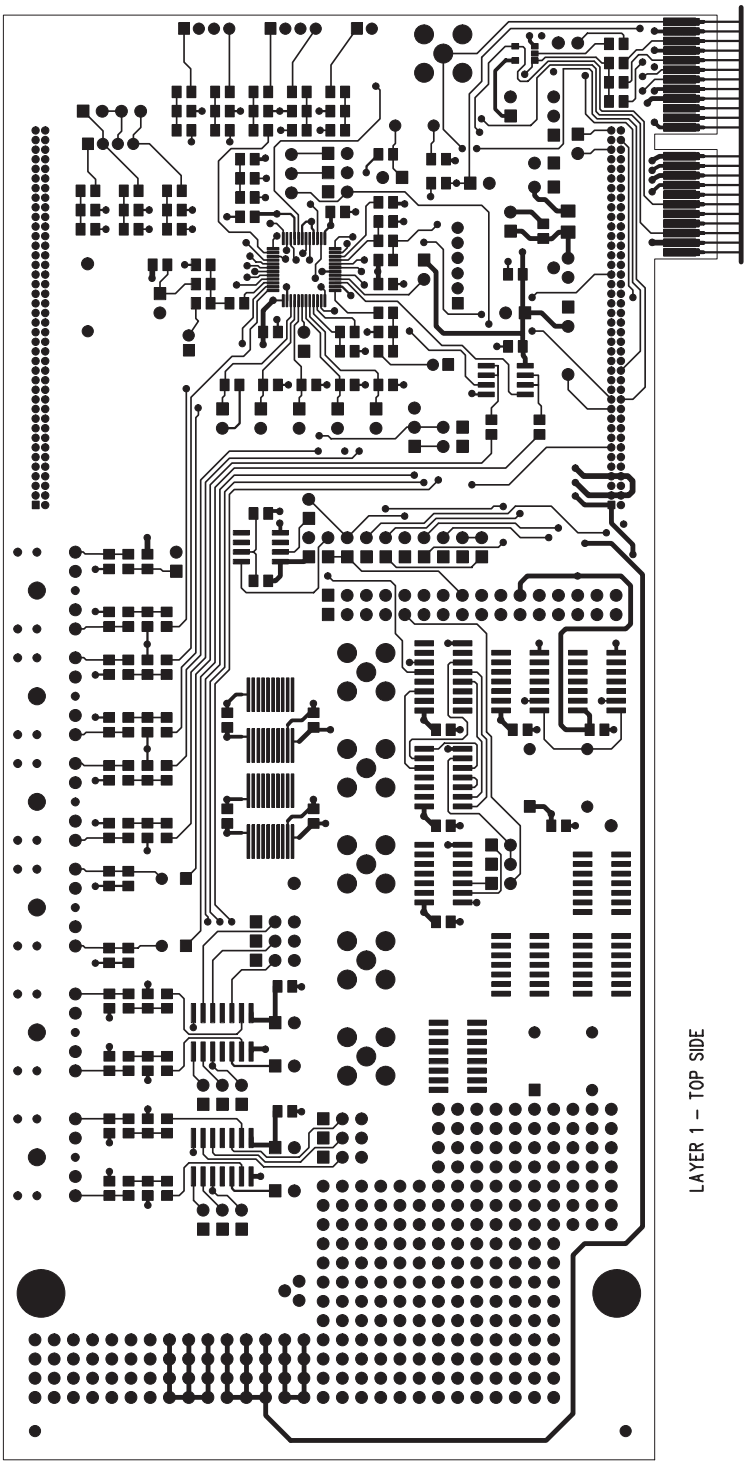
Appendix G

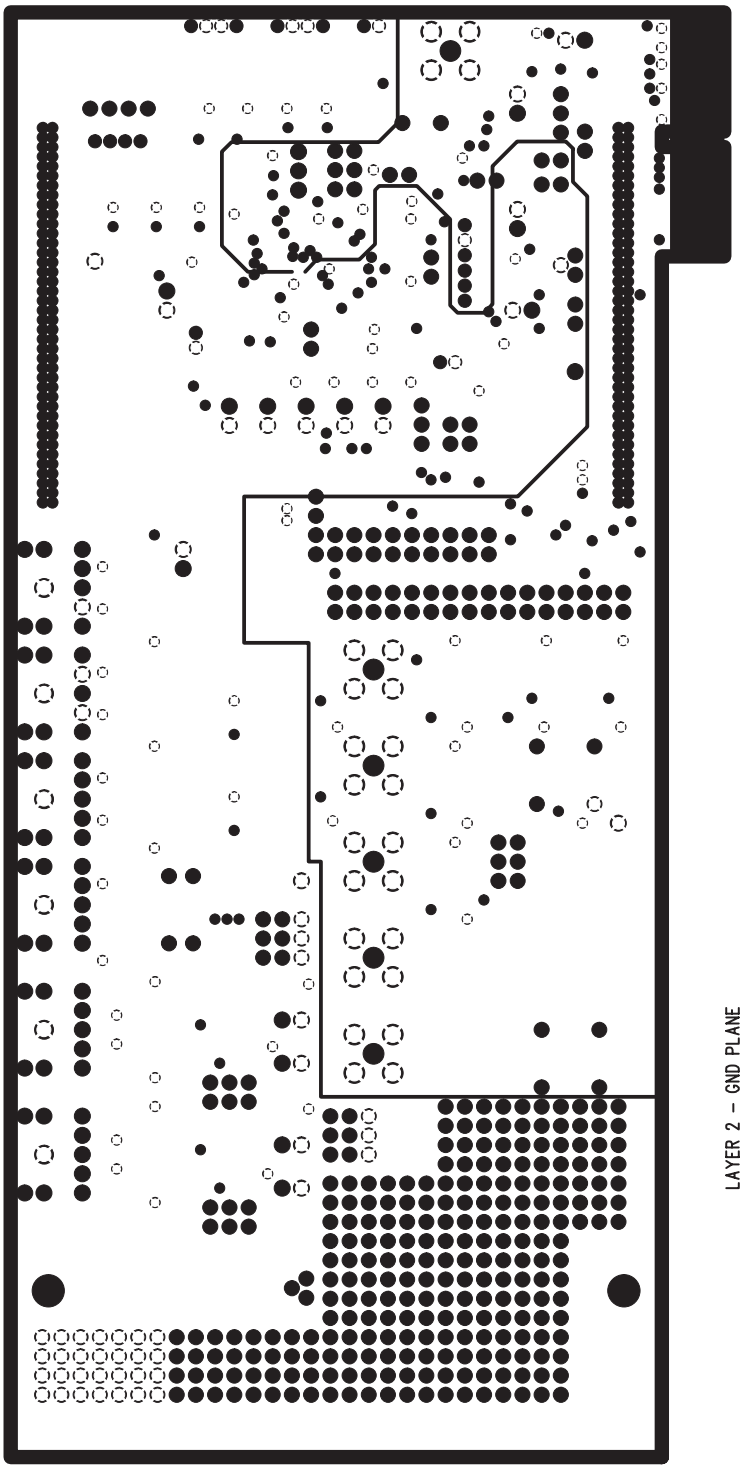
PC Board and Bill of Materials

This appendix contains the pc-board layout and bill of materials for the TLV320AIC27 evaluation module.

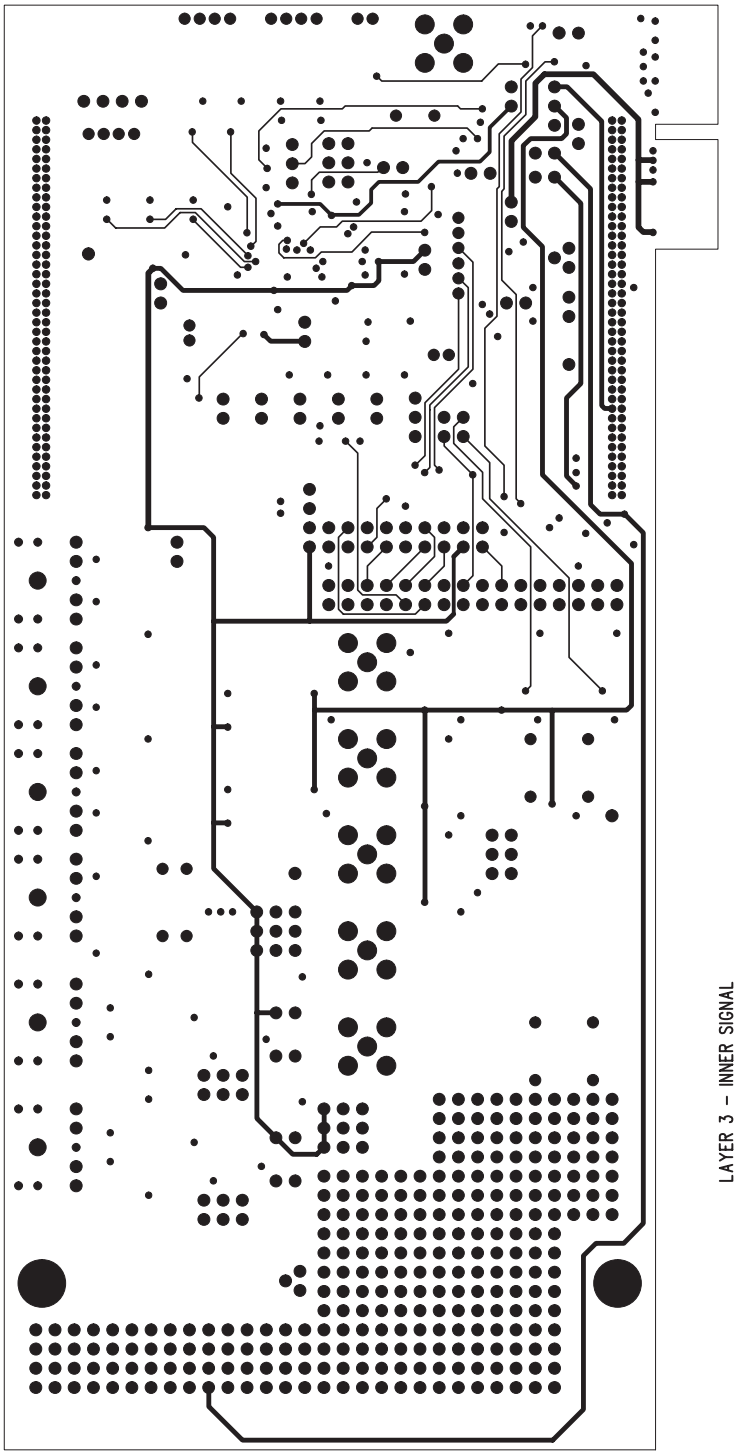
Topic **Page**

G.1 PC Board

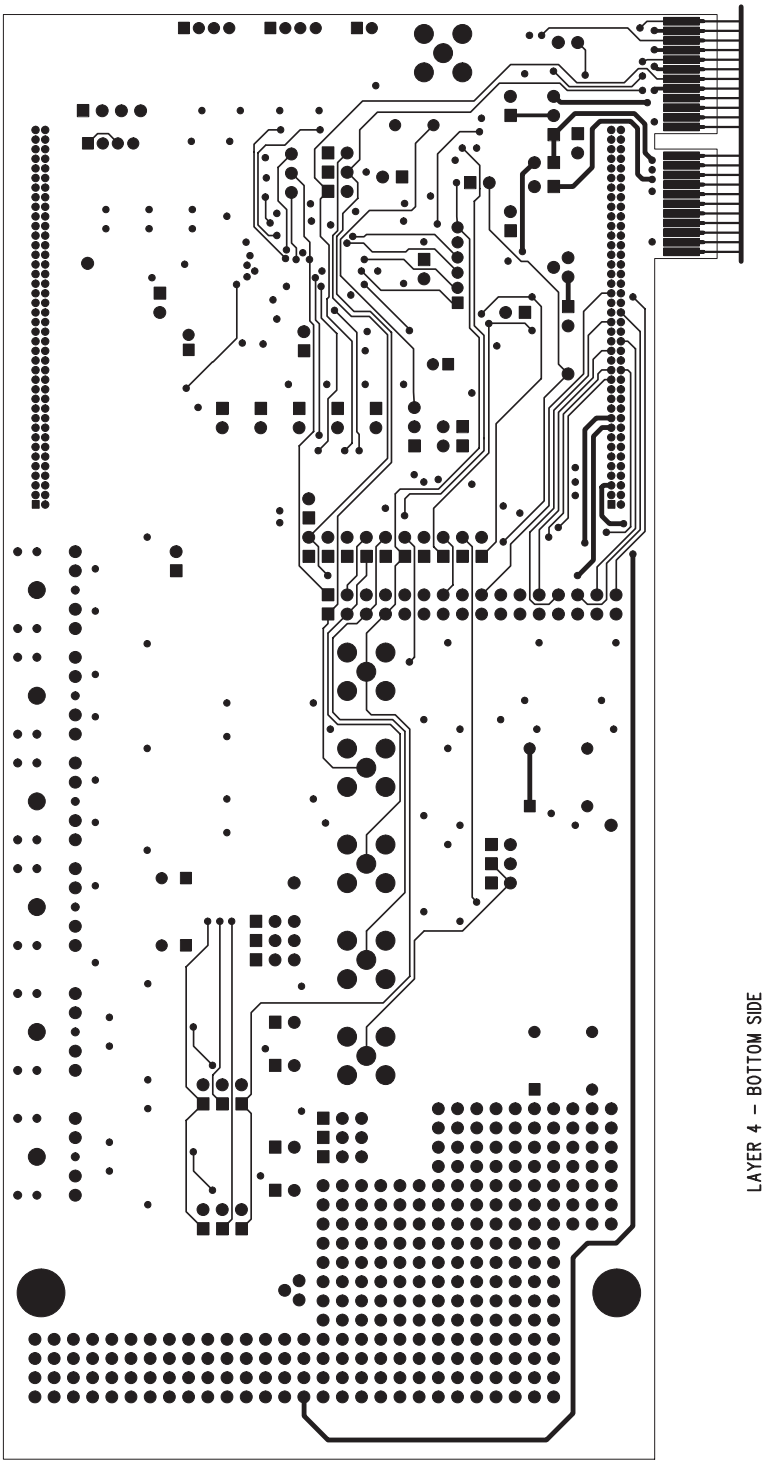




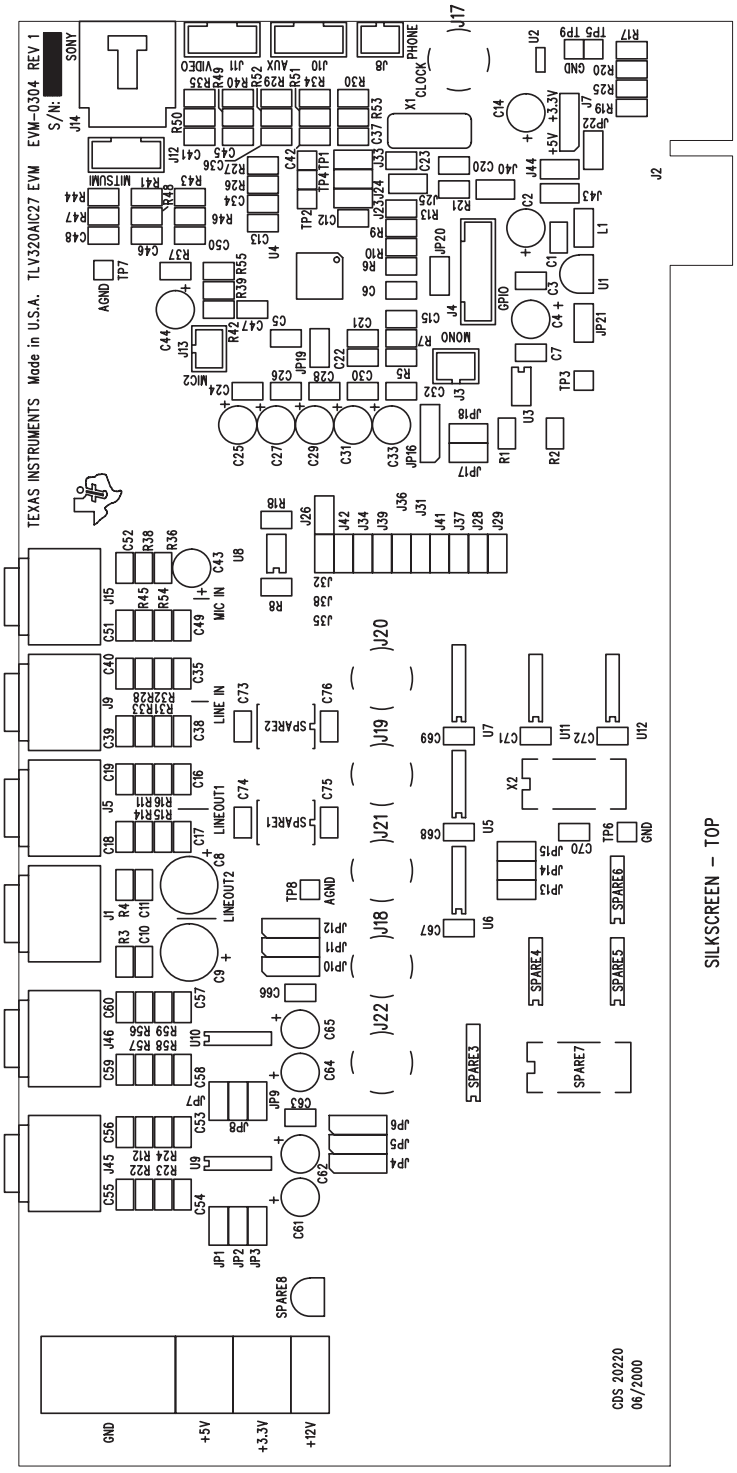
LAYER 2 – GND PLANE

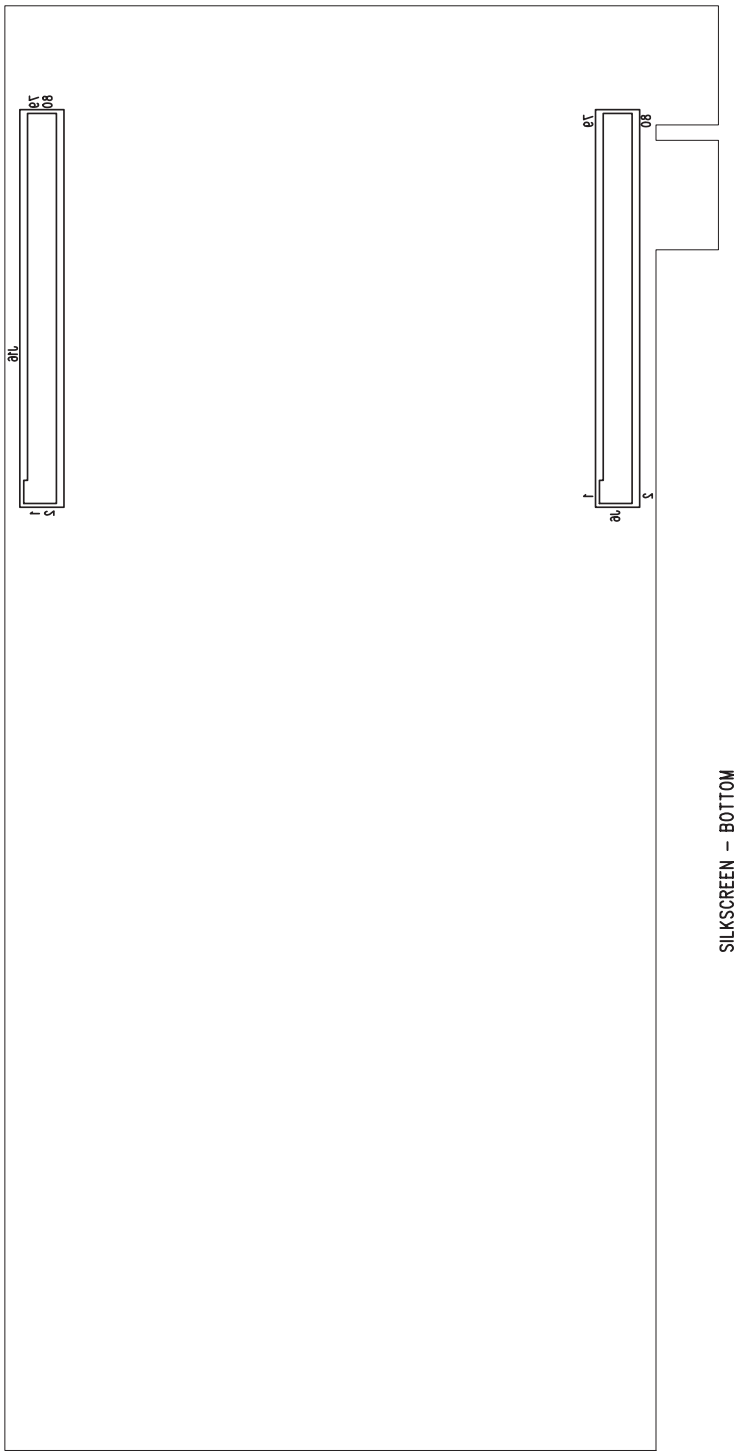


LAYER 3 – INNER SIGNAL



LAYER 4 – BOTTOM SIDE


TEXAS INSTRUMENTS Made in U.S.A. TLV320AIC27 EVM EVM-0304 REV 1
S/N:
SONY
MITSUMI
VIDEO
AUX
PHONE
CLOCK
GPIO
MONO
MIC2
MIC IN
LINE IN
LINEOUT1
LINEOUT2
AGND
GND
+5V
+3.3V
+12V
SPARE1
SPARE2
SPARE3
SPARE4
SPARE5
SPARE6
SPARE7
SPARE8
SILKSCREEN – TOP
CDS 20220
06/2000


SILKSCREEN – BOTTOM

G.2 Bill of Materials

Item	Reference	Qty	Value	Foot Print	Manufacturer	Part Number
1	C1	1	0.33 µF	CAP0805	Panasonic or equivalent	Digi–Key # PCC1817CT–ND
2	C17, C15, C16, C53, C54, C57, C58	7	2.2 µF	CAP0805	Panasonic or equivalent	PCC1923CT–ND
3	C19, C10, C11, C18, C39, C40, C51, C52, C56, C60, C55, C59	12	220 pF	CAP0805	Panasonic or equivalent	PCC221CGCT–ND
4	C2, C4, C14, C25, C27, C29, C31, C33, C43, C44, C61, C62, C64, C65	14	10uFX 16 V	4MM × 7MM	XICON	MOURSER 140–MLRL16V10
5	C20, C23	2	22 pF	CAP0805	Panasonic or equivalent	PCC1973CT–ND
6	C22	1	47 nF	CAP0805	Panasonic or equivalent	PCC1808CT–ND
7	C3, C5, C6, C7, C12, C13, C21, C24, C26, C28, C30, C32, C67, C68, C69, C70, C71, C72	18	0.1 µF	CAP0805	Panasonic or equivalent	PCC1812CT–ND
8	C35, C36, C37, C38, C41, C42, C45, C50, C34	9	0.47 µF	CAP0805	Panasonic or equivalent	PCC1818CT–ND
9	C8, C9	2	330 µF × 16 V	8MM × 11MM	XICON	MOURSER 140XRL16V330
10	J6, J16	2		CON\80P\TFM	SAMTEC	TFM–140–31–S–D
11	J1, J5, J9, J15, J45, J56	6		JACK_35	MOUSER	161–3504
12	J10, J11, J12	4			LEOCO	HDR1X4V–2MM
13	J17, J18, J19, J20, J21, J22	6	RF connector	SMA	Lighthorse Technologies or equivalent	LTI–SASF54GT
14	J2	1			PCB AMR_CONNECTOR	
15	J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J36, J37, J39, J40, J41, J42, J43, J44	20	2 POS JMPR	SIP\2P	SAMTEC	TSW–102–07–L–S.1” spacing

Item	Reference	Qty	Value	Foot Print	Manufacturer	Part Number
16	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22	22	2-POS JMPR	SIP\2P	SAMTEC	TSW–102–07–L–S .1” spacing
17	J3, J8, J13	3	2-Pin HDR	HDR1X2V–2MM	LEOCO	2011P02V000
18	J10, J11, J12	3	4-Pin HDR	HDR1X4V–2MM	LEOCO	2011P04V000
19	J14	1	4-Pin RT HDR	HDR1X4H–2MM	LEOCO	2550P04HU00
20	J4	1	6-PIN HDR	HDR1X6V–2MM	LEOCO	2011P06V000
21	J7	1		HDR1X3	SAMTEC	
22	J35, J38	2		SIP\16	SAMTEC	TSW–116–07–L–D .1” spacing
23	JMP_C1	1		SIP\3P	SAMTEC	SAMTEC TSW–103–07–L–S .1” spacing
24	JMPM0–1	2		JUMPER1		
25	L1	1		Chip 1206	Steward	Digi–Key 240–1019–1–ND
26	R10, R26	2	1KΩ, 1%	RES0805	Panasonic or equivalent	Digi–Key P/N P1.00K CCT– ND
27	R1, R2	2	22R1, 1%	RES0805	Panasonic or equivalent	P22.1CCT–ND
28	R13, R19, R20, R25, R9	5	UNPOP	RES0805	Panasonic or equivalent	N/A
29	R18, R6, R46, R48	4	10KΩ, 1%	RES0805	Panasonic or equivalent	P10KCCT–ND
30	R21, R17	2	51R1Ω, 1%	RES0805	Panasonic or equivalent	P51.1CCT–ND
31	R27	1	2K21, 1%	RES0805	Panasonic or equivalent	P2.21K
32	R3, R4, R7, R15, R16, R54, R55, R23, R24, R58, R59	11	47K5, 1%	RES0805	Panasonic or equivalent	P47.5KCCT–ND
33	R30, R31, R32, R33, R34, R35, R40, R41, R43, R28, R29, R49, R50, R51, R52, R53	16	8K25 1%	RES0805	Panasonic or equivalent	P8.25KCCT–ND
34	R36, R37, R38, R39	4	1K5 1%	RES0805	Panasonic or equivalent	P1.5KCCT–ND
35	R44	1	11KΩ, 1%	RES0805	Panasonic or equivalent	P11KCCT–ND
36	R47	1	13KΩ, 1%	RES0805	Panasonic or equivalent	P13KCCD–ND
37	R5, R11, R42, R45, R14, R12, R22, R56, R57	9	220R, 1%	RES0805	Panasonic or equivalent	P220CCT–ND

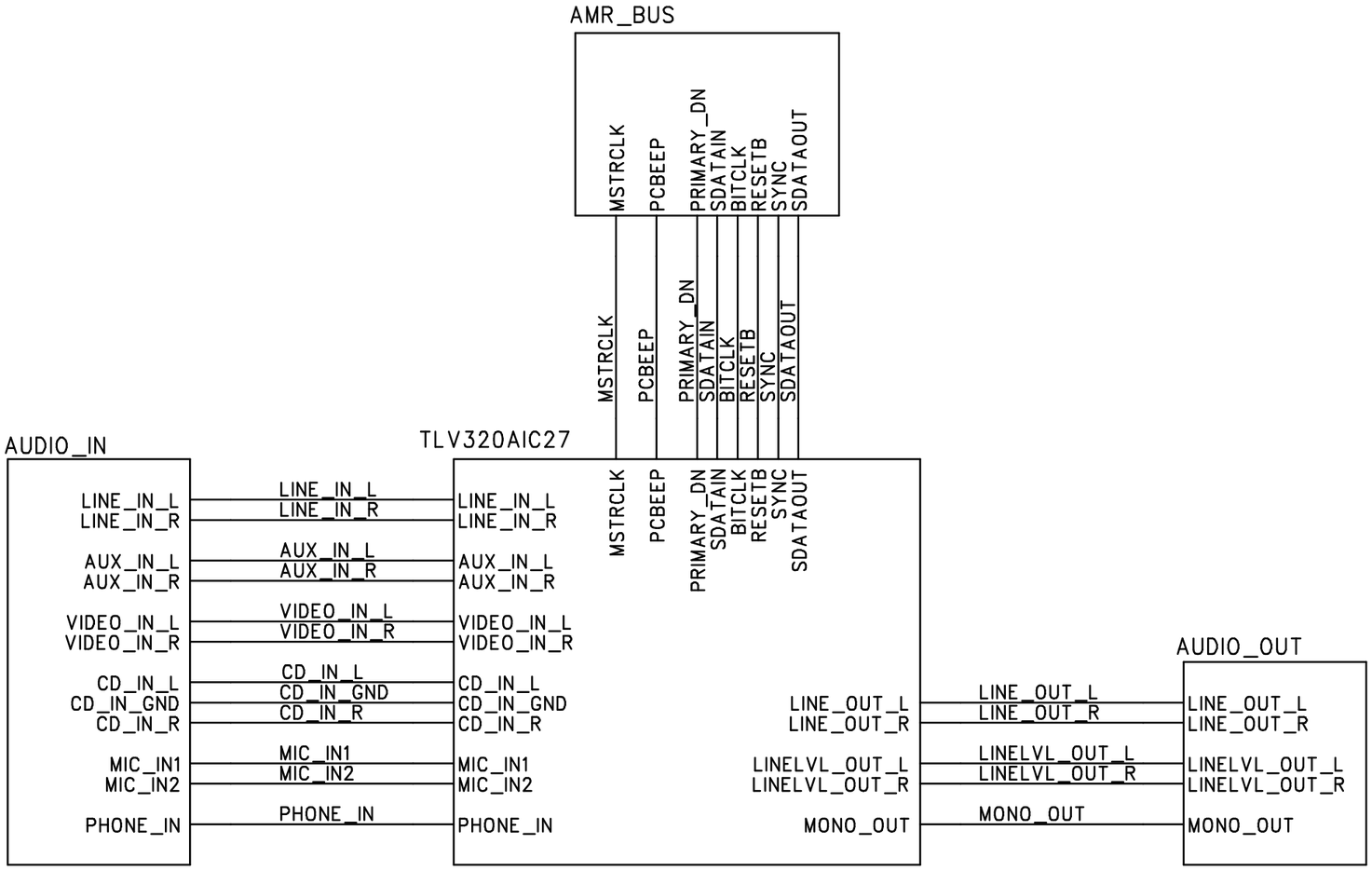
Item	Reference	Qty	Value	Foot Print	Manufacturer	Part Number
38	R8	1	20KΩ, 1%	RES0805	Panasonic or equivalent	P20KCCT–ND
39	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9		Test point	SAMTEC	TWS–101–07–L–S .025” pin
40	U1	1			National	LM78L05ACZ
41	U2	1			National	NC7SZ66
42	U3	1	TPA112D		TI	TPA112D
43	U4	1	TLV320AIC27–PFB		TI	TLV320AIC27
44	U5	1	SN74HC08D		TI	SN74HC08
45	U6	1	SN74HC32D		TI	SN74HC32
46	U7	1	SN74HC4060D		TI	SN74HC4060
47	U8	1	SN65LVDS9637D		TI	SN65LVDS9637
48	U9, U10	2			WOLFSON MICRO.	WM8725
49	U11, U12	2	SN74LVC04AD		TI	SN74LVC04A
50						
51	X1	1	24.576 MHz		CTS or Equv	HC–94
52	X2	1	24.576 MHz		EPSON	SG–8002DC–PCC–24.576 MHz

Appendix H

Schematics

This appendix contains the schematics for the TLV320AIC27 evaluation board.

Topic **Page**



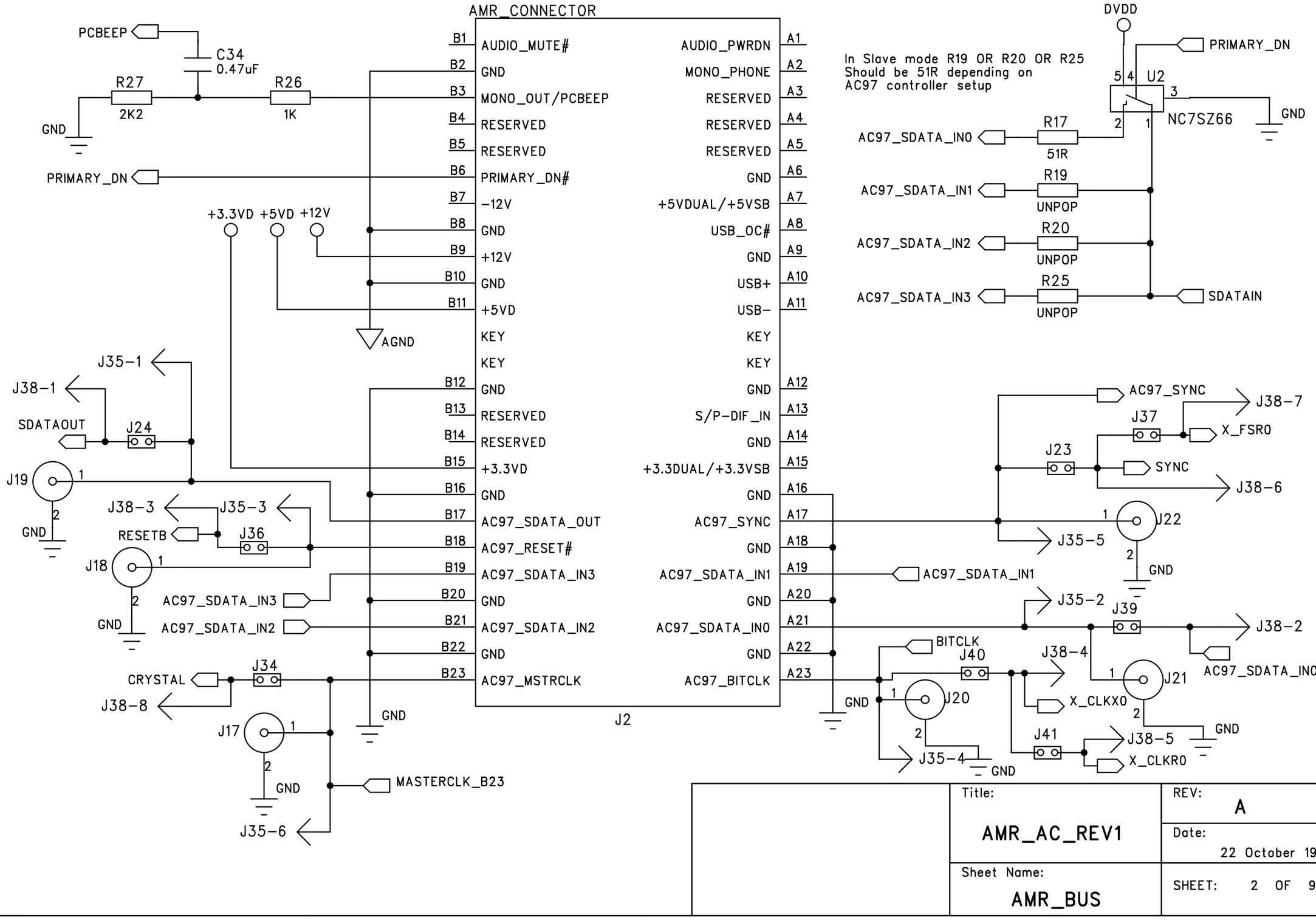
CONNECTOR

POWER

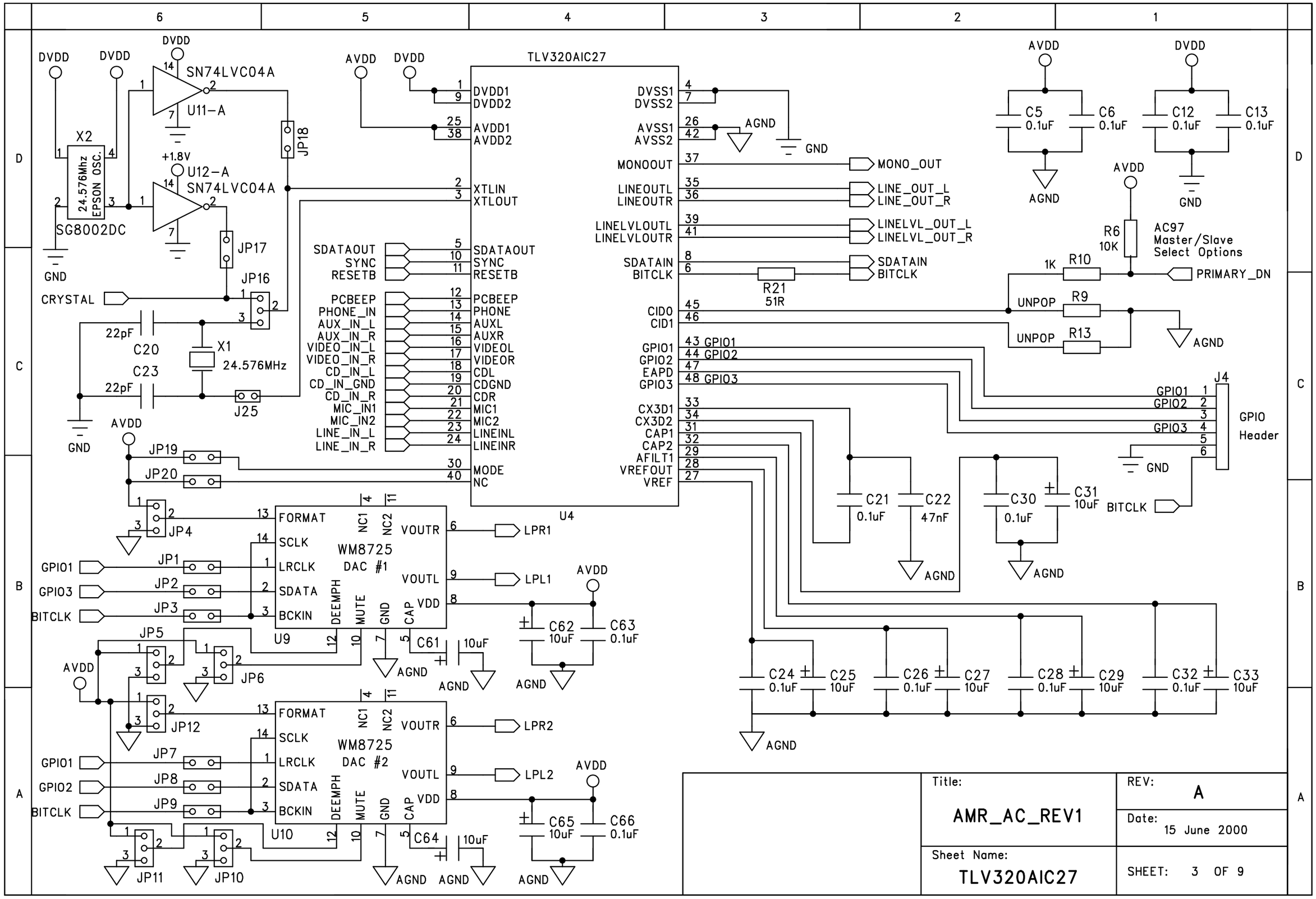
FRAME_SYNC_GENERATOR

LEVEL_SHIFTER

Title: AMR_AC_REV1	REV: A
	Date: 09 June 2000
Sheet Name: Functional Diagram	SHEET: 1 OF 9



Title: AMR_AC_REV1	REV: A
	Date: 22 October 1999
Sheet Name: AMR_BUS	SHEET: 2 OF 9


TLV320AIC27
SN74LVC04A
U11-A
U12-A
SN74LVC04A
X2
24.576Mhz
EPSON OSC.
SG8002DC
+1.8V
DVDD
AVDD
AGND
GND
JP16
JP17
JP18
JP19
JP20
JP1
JP2
JP3
JP4
JP5
JP6
JP7
JP8
JP9
JP10
JP11
JP12
J25
CRYSTAL
X1
24.576MHz
C20
22pF
C23
22pF
DVDD1
DVDD2
AVDD1
AVDD2
XTLIN
XTLOUT
SDATAOUT
SYNC
RESETB
PCBEEP
PHONE_IN
AUX_IN_L
AUX_IN_R
VIDEO_IN_L
VIDEO_IN_R
CD_IN_L
CD_IN_GND
CD_IN_R
MIC_IN1
MIC_IN2
LINE_IN_L
LINE_IN_R
MODE
NC
DVSS1
DVSS2
AVSS1
AVSS2
MONOOUT
LINEOUTL
LINEOUTR
LINELVLOUTL
LINELVLOUTR
SDATAIN
BITCLK
R21
51R
CID0
CID1
GPIO1
GPIO2
EAPD
GPIO3
CX3D1
CX3D2
CAP1
CAP2
AFILT1
VREFOUT
VREF
MONO_OUT
LINE_OUT_L
LINE_OUT_R
LINELVL_OUT_L
LINELVL_OUT_R
C5
0.1uF
C6
0.1uF
C12
0.1uF
C13
0.1uF
R6
10K
AC97
Master/Slave
Select Options
1K
R10
PRIMARY_DN
UNPOP
R9
UNPOP
R13
J4
GPIO
Header
C21
0.1uF
C22
47nF
C30
0.1uF
C31
10uF
BITCLK
C24
0.1uF
C25
10uF
C26
0.1uF
C27
10uF
C28
0.1uF
C29
10uF
C32
0.1uF
C33
10uF
U4
WM8725
DAC #1
U9
WM8725
DAC #2
U10
FORMAT
SCLK
LRCLK
SDATA
BCKIN
NC1
NC2
VOUTR
VOUTL
VDD
DEEMPH
MUTE
GND
CAP
LPR1
LPL1
LPR2
LPL2
C61
10uF
C62
10uF
C63
0.1uF
C64
10uF
C65
10uF
C66
0.1uF
Title:
AMR_AC_REV1
REV:
A
Date:
15 June 2000
Sheet Name:
TLV320AIC27
SHEET: 3 OF 9

PHONE Header
AUX Header
VIDEO Header
MITSUMI Header
CD INPUT
SONY Header
MIC2 Header
MIC_IN
3.5mm Jack
LINE_IN
3.5mm Jack

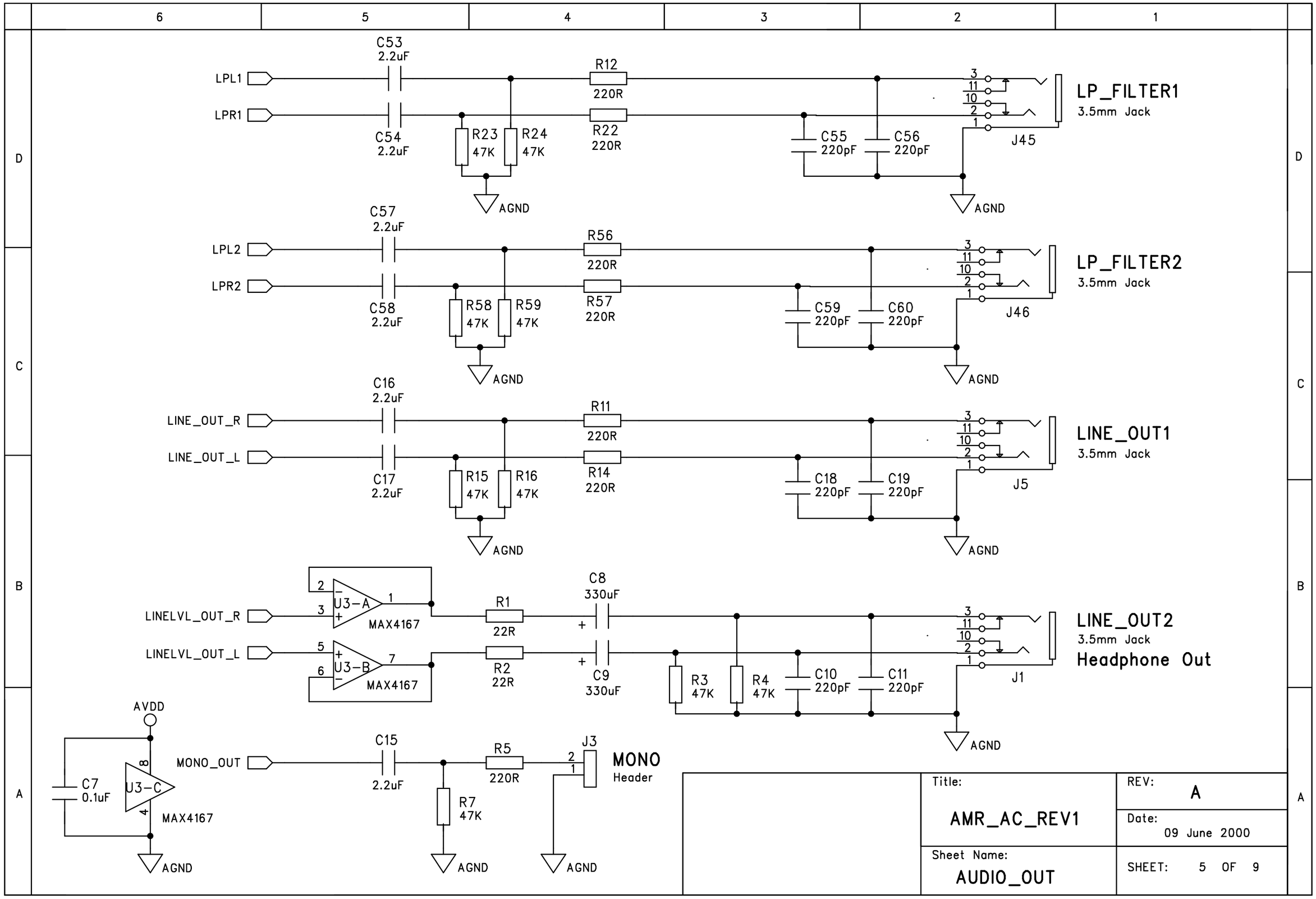
J8 R30 8K2 C37 0.47uF PHONE_IN
J10 R29 8K2 C36 0.47uF AUX_IN_L
J10 R34 8K2 C42 0.47uF AUX_IN_R
J11 R35 8K2 C41 0.47uF VIDEO_IN_L
J11 R40 8K2 C45 0.47uF VIDEO_IN_R
J12 R41 8K2 C46 0.47uF CD_IN_L
J12 R44 11K C48 0.47uF CD_IN_GND
J14 R43 8K2 C50 0.47uF CD_IN_R

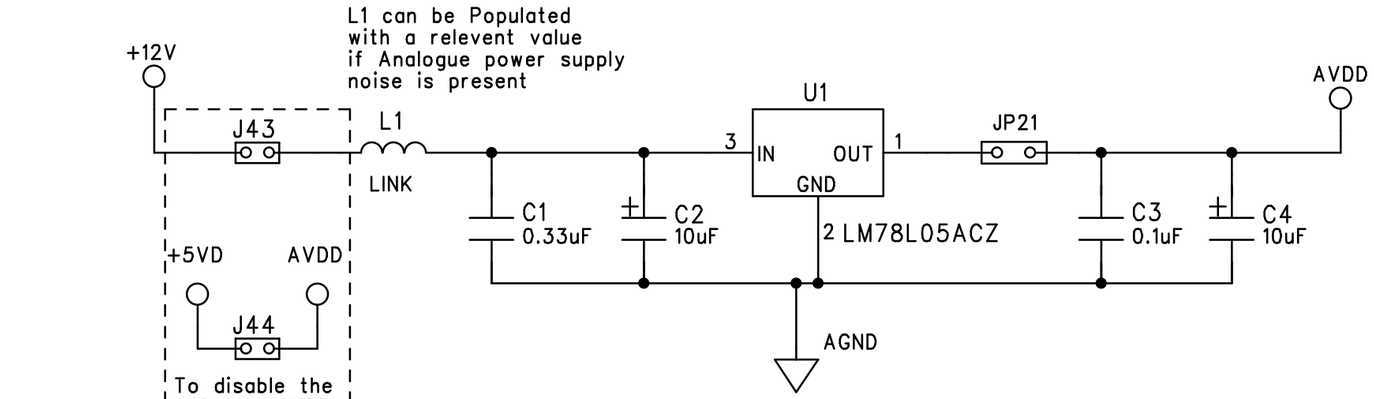
AGND
R46 10K
R47 13K
R48 10K
R49 8K2
R50 8K2
R51 8K2
R52 8K2
R53 8K2

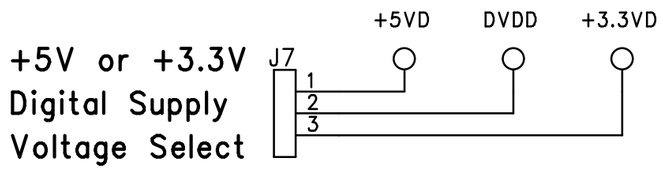
AVDD
R37 1K5
C44 10uF
R39 1K5
R36 1K5
R38 1K5
C43 10uF
J13 R42 220R
C47 0.47uF MIC_IN2
J15 R45 220R
C49 0.47uF MIC_IN1
C51 220pF
C52 220pF
R54 47K
R55 47K

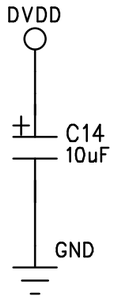
J9 R28 8K2 C35 0.47uF LINE_IN_R
J9 R33 8K2 C38 0.47uF LINE_IN_L
C39 220pF
C40 220pF
R31 8K2
R32 8K2

Title: AMR_AC_REV1	REV: A
	Date: 22 October 1999
Sheet Name: AUDIO_IN	SHEET: 4 OF 9

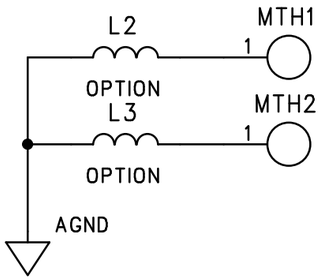

C53
2.2uF
LPL1
LPR1
C54
2.2uF
R23
47K
R24
47K
R12
220R
R22
220R
C55
220pF
C56
220pF
3
11
10
2
1
J45
LP_FILTER1
3.5mm Jack
AGND
C57
2.2uF
LPL2
LPR2
C58
2.2uF
R58
47K
R59
47K
R56
220R
R57
220R
C59
220pF
C60
220pF
J46
LP_FILTER2
3.5mm Jack
C16
2.2uF
LINE_OUT_R
LINE_OUT_L
C17
2.2uF
R15
47K
R16
47K
R11
220R
R14
220R
C18
220pF
C19
220pF
J5
LINE_OUT1
3.5mm Jack
2
3
U3-A
1
MAX4167
5
6
U3-B
7
LINELVL_OUT_R
LINELVL_OUT_L
R1
22R
R2
22R
C8
330uF
C9
330uF
R3
47K
R4
47K
C10
220pF
C11
220pF
J1
LINE_OUT2
3.5mm Jack
Headphone Out
AVDD
C7
0.1uF
U3-C
8
4
MAX4167
MONO_OUT
C15
2.2uF
R5
220R
R7
47K
J3
2
1
MONO
Header
Title:
AMR_AC_REV1
REV:
A
Date:
09 June 2000
Sheet Name:
AUDIO_OUT
SHEET: 5 OF 9





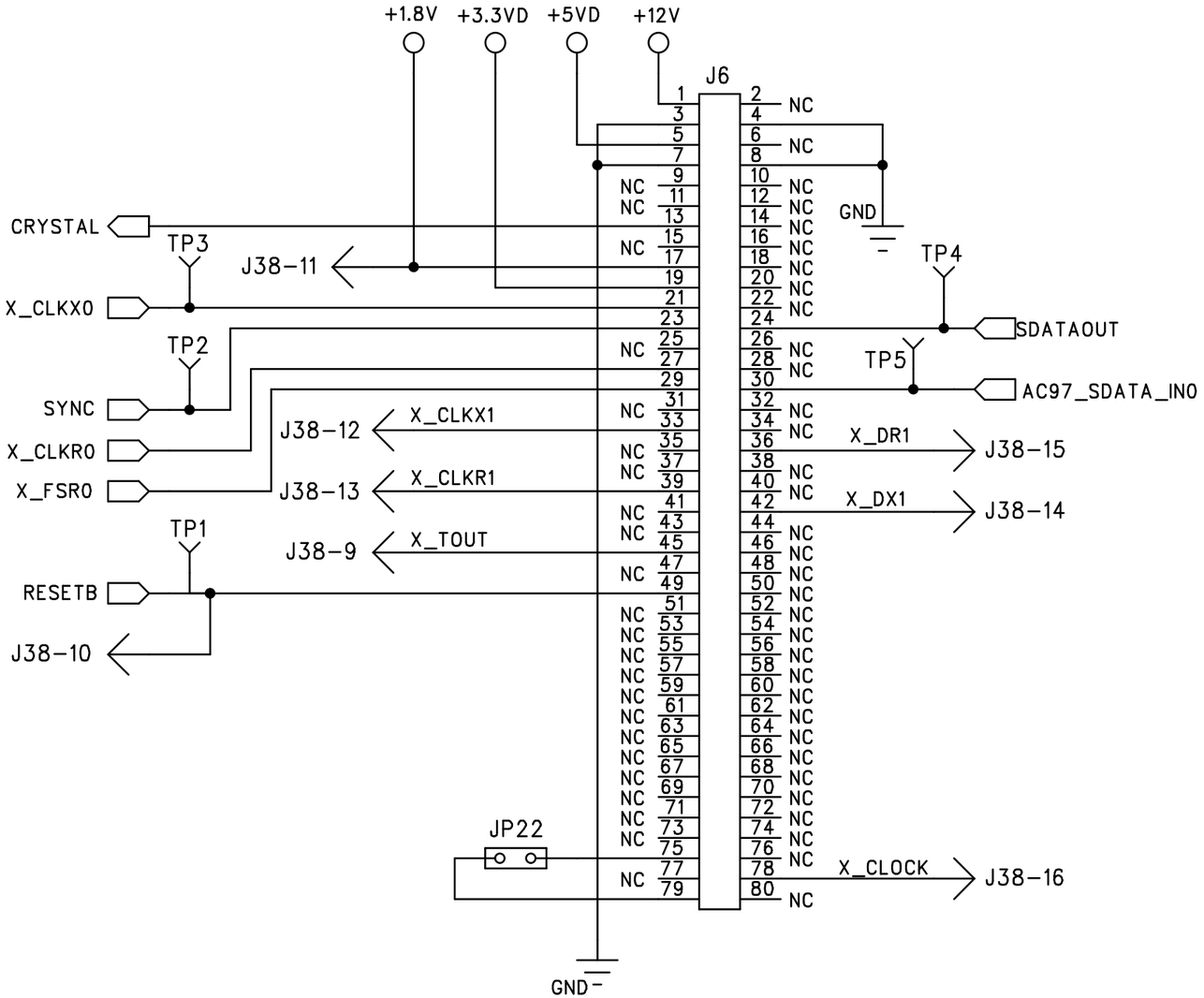


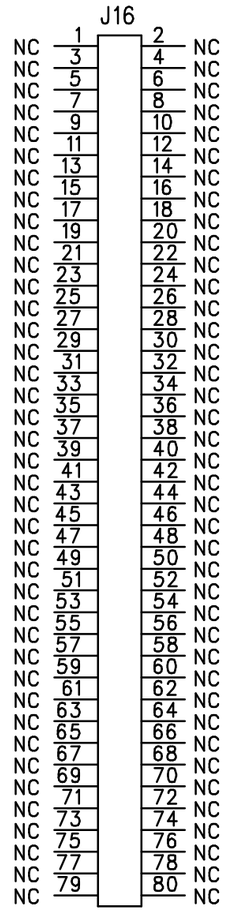
L2 and/or L3 can be populated with relevent values to acheive EMC performance



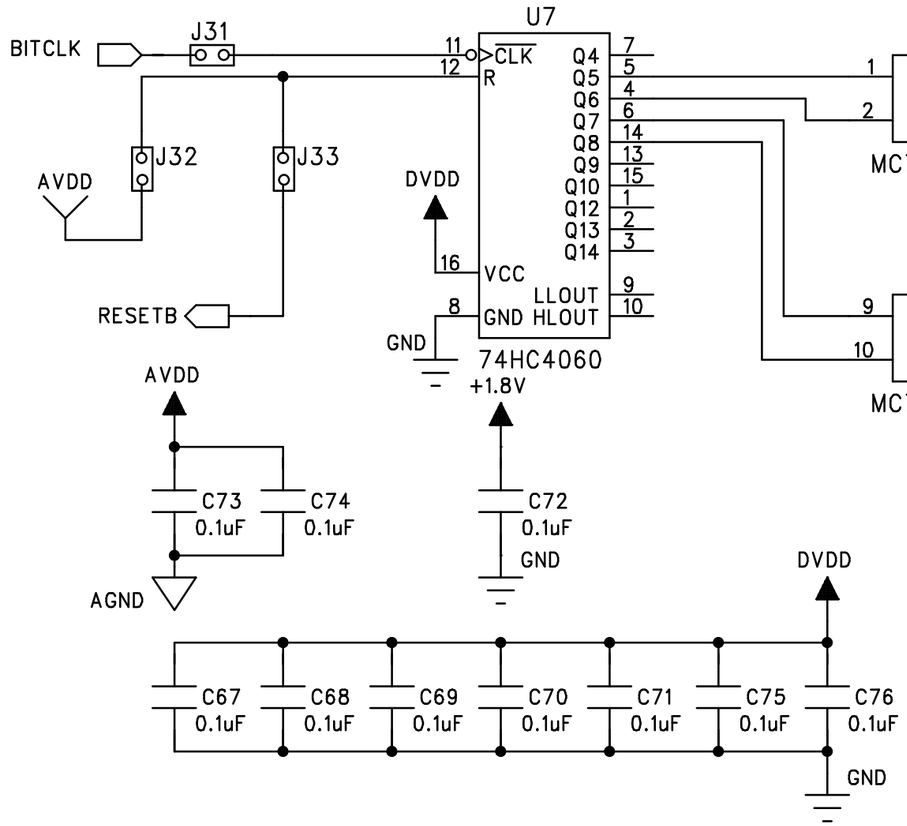
Bracket Mounting Holes

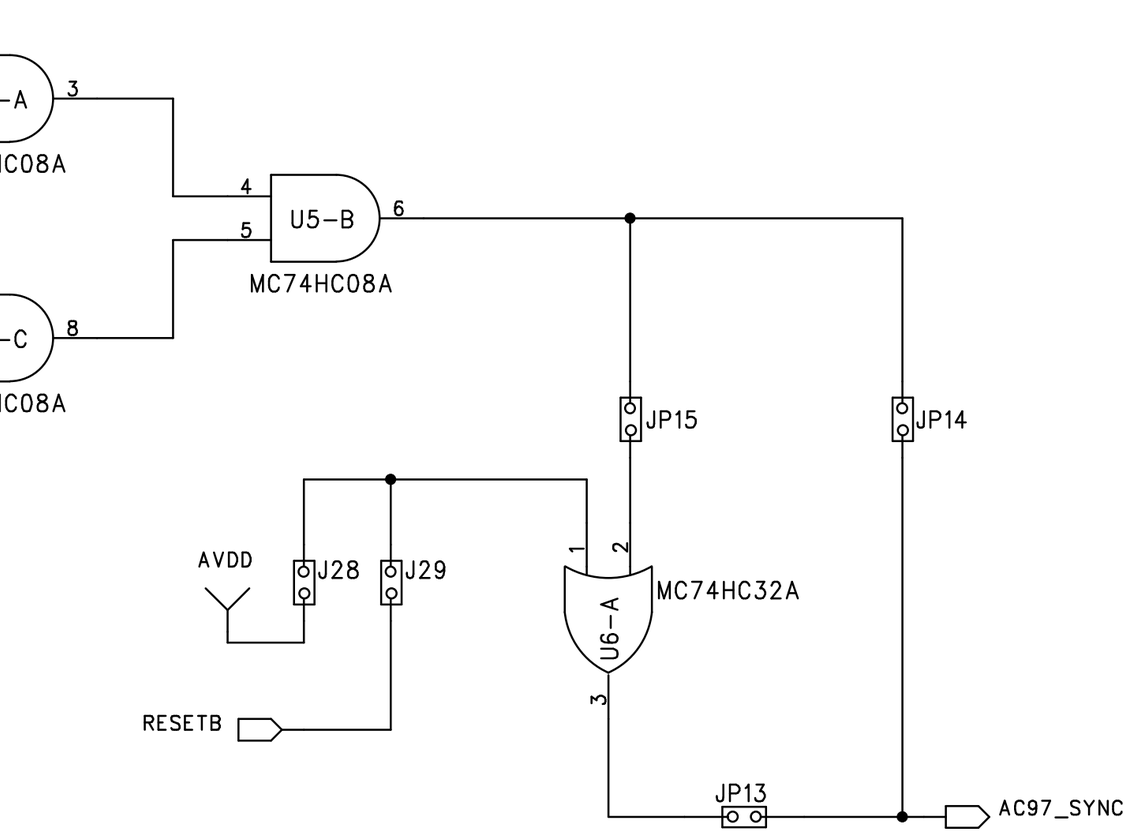
	Title: AMR_AC_REV1	REV: A
		Date: 09 June 2000
	Sheet Name: POWER	SHEET: 6 OF 9

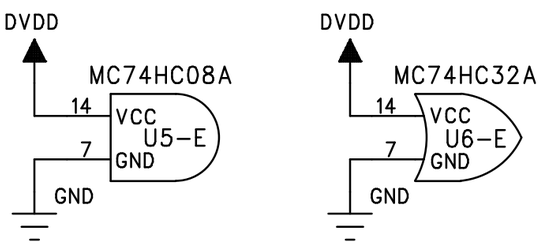




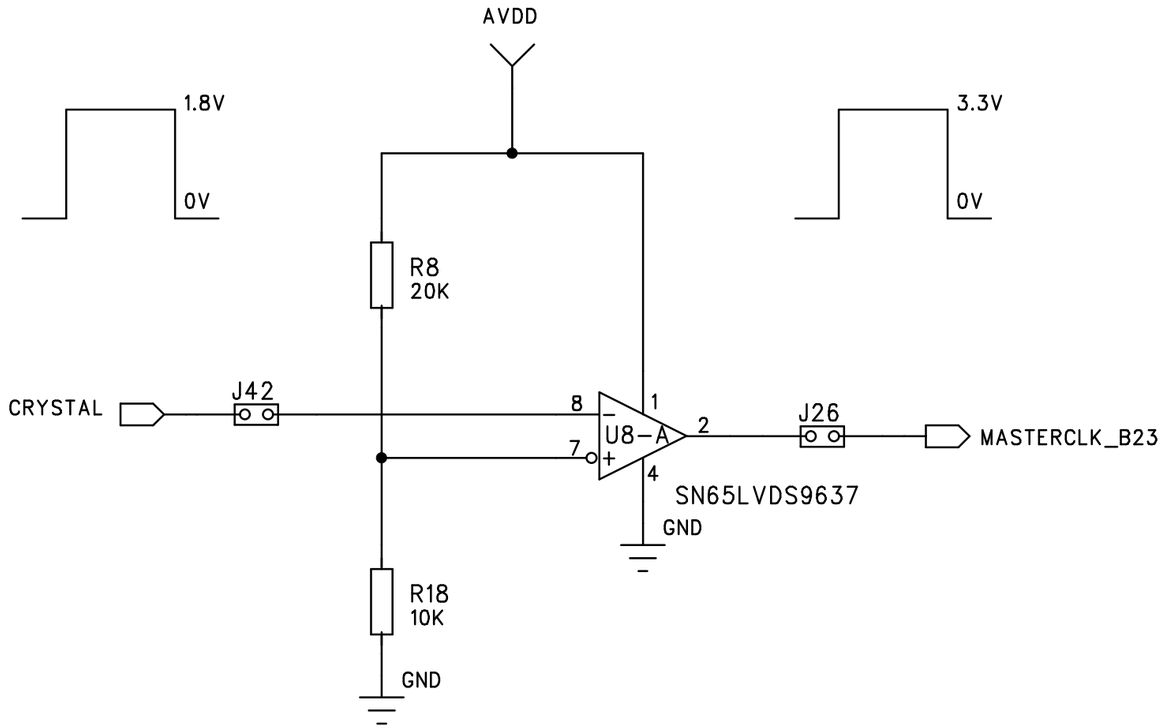
Title: AMR_AC_REV1	REV: A
	Date: 09 June 2000
Sheet Name: CONNECTORS	SHEET: 7 OF 9







	Title: AMR_AC_REV1	REV: A
		Date: 14 June 2000
	Sheet Name: FRAME SYNC GENERATOR	SHEET: 8 OF 9



	Title: AMR_AC_REV1	REV: A
		Date: 14 June 2000
	Sheet Name: LEVEL SHIFTER (1.8V to 3.3V)	SHEET: 9 OF 9