TLV320DAC3203 Applications

Reference Guide

Literature Number: SLAU434A
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The TLV320DAC3203 (sometimes referred to as the DAC3203) is a flexible, low-power, low-voltage stereo audio codec with programmable outputs, PowerTune capabilities, fixed predefined and parameterizable signal processing blocks, integrated PLL, integrated LDO and flexible digital interfaces. Extensive register-based control of power, input/output channel configuration, gains, effects, pin-multiplexing and clocks is included, allowing the device to be precisely targeted to its application.

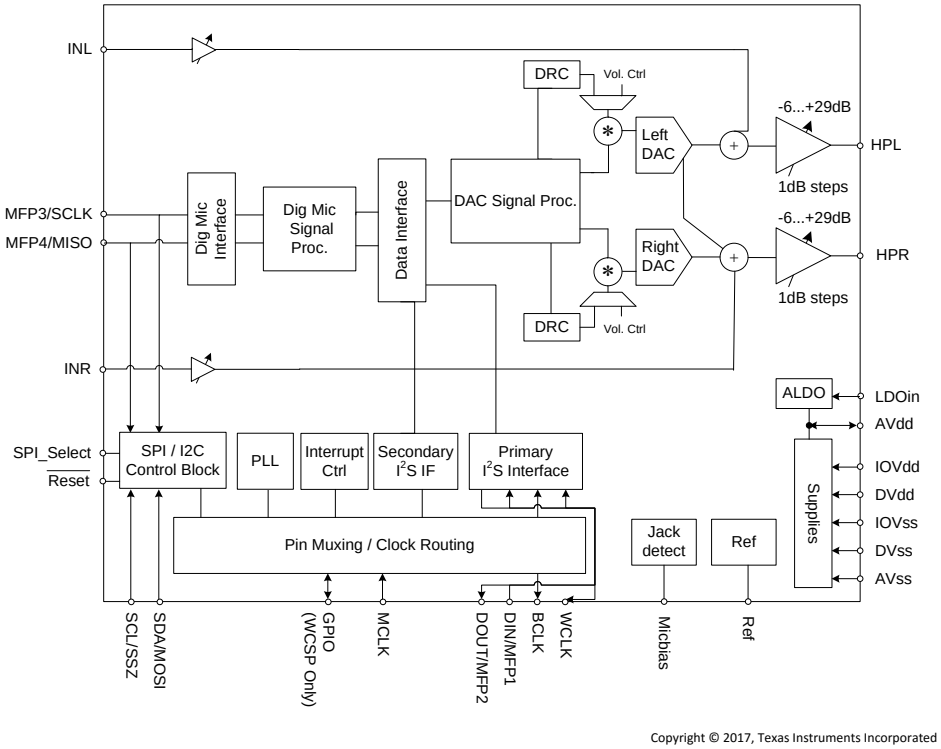

Figure 1-1. Simplified Block Diagram

Combined with the advanced PowerTune technology, the device can cover operations from 8kHz mono voice playback to stereo 192kHz DAC playback, making it ideal for portable battery-powered audio and telephony applications.

The record path of the TLV320DAC3203 consists of a stereo digital microphone PDM interface (not available when using SPI control interface) typically used at 64Fs or 128Fs.

The playback path offers signal processing blocks for filtering and effects, true differential output signal, flexible mixing of DAC and analog input signals as well as programmable volume controls. The TLV320DAC3203 contains two high-power output drivers which can be configured in multiple ways, including stereo, and mono BTL. The integrated PowerTune technology allows the device to be tuned to just the right power-performance trade-off. Mobile applications frequently have multiple use cases requiring very low-power operation while being used in a mobile environment. When used in a docked environment power consumption typically is less of a concern while lowest possible noise is important. With PowerTune the TLV320DAC3203 can address both cases.

The voltage supply range for the TLV320DAC3203 for analog is 1.5V–1.95V, and for digital it is 1.26V–1.95V. To ease system-level design, a low-dropout regulator (LDO) is integrated to generate the appropriate analog supply from input voltages ranging from 1.8V to 3.6V. Digital I/O voltages are supported in the range of 1.1V–3.6V.

The required internal clock of the TLV320DAC3203 can be derived from multiple sources, including the MCLK, BCLK or GPIO pins or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK, BCLK or GPIO pins. Although using the internal, fractional PLL ensures the availability of a suitable clock signal, it is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz.

The device is available in the 4mm × 4mm QFN and 2.7mm × 2.7mm WCSPpackage.

1.2 Typical Circuit Configuration

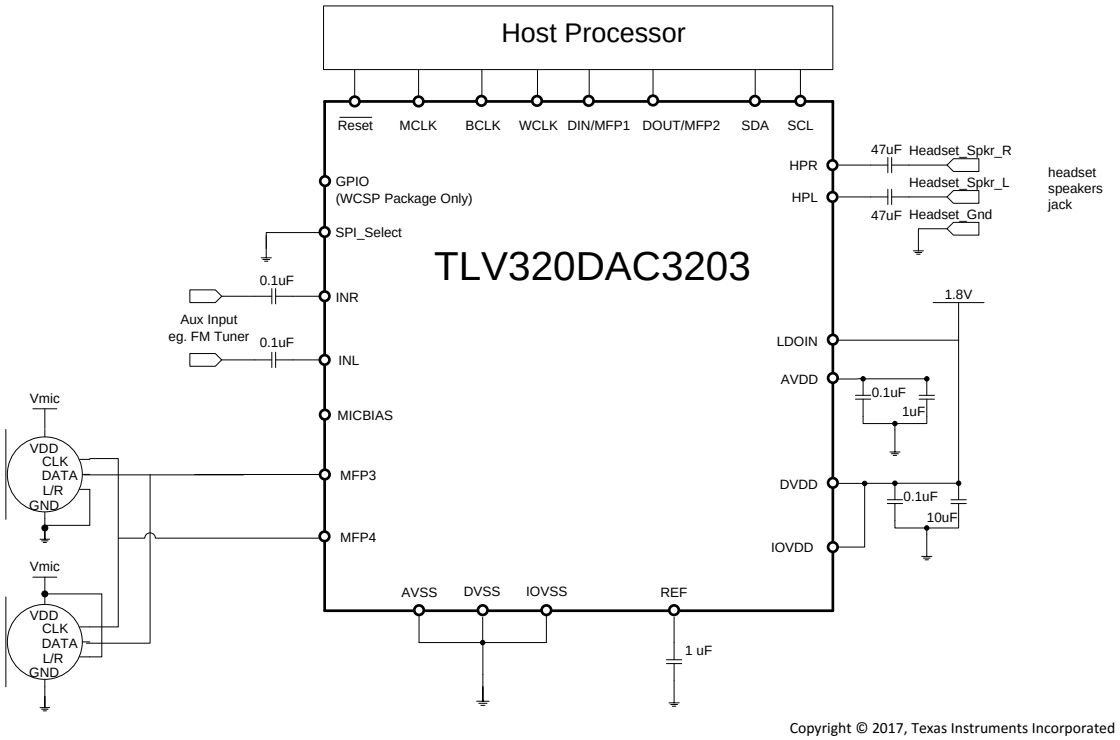

Figure 1-2. Typical Circuit Configuration

2.1 Terminal Descriptions

2.1.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are $\overline{\text{Reset}}$ and the SPI_Select pin, which are HW control pins. Depending on the state of SPI_Select, the two control-bus pins SCL/$\overline{\text{SS}}$ and SDA/MOSI are configured for either I^2C or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in *Section 2.1.1.1*.

2.1.1.1 Multifunction Pins

Table 2-1 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

Table 2-1. Multifunction Pin Assignments

		1	2	3	4	5	6	7	8
	Pin Function	**MCLK**	**BCLK**	**WCLK**	**DIN MFP1**	**DOUT MFP2**	**MFP3/ SCLK**	**MFP4/ MISO**	**GPIO MFP5**
A	PLL Input	S(1)	S(2)		E				S(3)
B	Codec Clock Input	S(1),D(4)	S(2)						S(3)
C	I^2S BCLK input		S,D						
D	I^2S BCLK output		E(5)						
E	I^2S WCLK input			E, D					
F	I^2S WCLK output			E					
G	I^2S ADC word clock input						E		E
H	I^2S ADC WCLK out							E	E
I	I^2S DIN				E, D				
J	I^2S DOUT					E, D			
K	General Purpose Output I					E			
K	General Purpose Output II							E	
K	General Purpose Output III								E
L	General Purpose Input I				E				
L	General Purpose Input II						E		
L	General Purpose Input III								E
M	INT1 output					E		E	E

(1) S(1): The MCLK pin can drive the PLL and Codec Clock inputs **simultaneously**.
(2) S(2): The BCLK pin can drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**.
(3) S(3): The GPIO/MFP5 pin can drive the PLL and Codec Clock inputs simultaneously.
(4) D: Default Function
(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin. (If GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time.)

Table 2-1. Multifunction Pin Assignments (continued)

		1	2	3	4	5	6	7	8
	Pin Function	**MCLK**	**BCLK**	**WCLK**	**DIN MFP1**	**DOUT MFP2**	**MFP3/ SCLK**	**MFP4/ MISO**	**GPIO MFP5**
N	INT2 output					E		E	E
Q	Secondary I^2S BCLK input						E		E
R	Secondary I^2S WCLK in						E		E
S	Secondary I^2S DIN						E		E
T	Secondary I^2S DOUT							E	
U	Secondary I^2S BCLK OUT					E		E	E
V	Secondary I^2S WCLK OUT					E		E	E
X	Aux Clock Output					E		E	E

2.1.2 Analog Pins

Analog functions can also be configured to a large degree. For minimum power consumption, analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.

2.1.3 Register Settings for Multifunction Pins

To configure the settings seen in Table 2-1, please see the letter-number combination in for the appropriate registers to modify. In , the letter/number combination represents the row and the column number from Table 2-1 in bold type.

Please be aware that more settings may be necessary to obtain a full interface definition matching the application requirement (see Page 0, Register 25 to 33).

Table 2-2. Multifunction Pin Register Configuration

	Description	Required Register Setting		Description	Required Register Setting
A1	PLL Input on MCLK	Page 0, Register 4, Bits D3-D2 = 00	N5	INT2 output DOUT/MFP2	Page 0, Register 53,Bits D3-D1 = 101
A2	PLL Input on BCLK	Page 0, Register 4, Bits D3-D2 = 01	N7	INT2 output on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 0101
A4	PLL Input on DIN/MFP1	Page 0, Register 54, Bits D2-D1 = 01 Page 0, Register 4, Bits D3-D2 = 11	N8	INT2 output on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0110
A8	PLL Input on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0001 Page 0, Register 4, Bits D3-D2 = 10	O4	Digital Microphone Data Input on DIN/MFP1	Page 0, Register 54, Bits D2-D1 = 01 Page 0, Register 81, Bits D5-D4 = 10
B1	Codec Clock Input on MCLK	Page 0, Register 4, Bits D1-D0 = 00	O6	Digital Microphone Data Input on SCLK/MFP3	Page 0, Register 56, Bits D2-D1 = 01 Page 0, Register 81, Bits D5-D4 = 01
B2	Codec Clock Input on BCLK	Page 0, Register 4, Bits D1-D0 = 01	O8	Digital Microphone Data Input on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0001 Page 0, Register 81, Bits D5-D4 = 00
B8	Codec Clock Input on GPIO/MPF5	Page 0, Register 52, Bits D5-D2 = 0001 Page 0, Register 4, Bits D1-D0 = 10	P7	Digital Microphone Clock Output on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 0111
C2	I^2S BCLK input on BCLK	Page 0, Register 27, Bit D3 = 0	P8	Digital Microphone Clock Output on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 1010
D2	I^2S BCLK output on BCLK	Page 0, Register 27, Bit D3 = 1	Q6	Secondary I^2S BCLK input on SCLK/MFP3	Page 0, Register 56, Bits D2-D1 = 01 Page 0, Register 31, Bits D6-D5 = 01
E3	I^2S WCLK input on WCLK	Page 0, Register 27, Bit D2 = 0	Q8	Secondary I^2S BCLK input on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0001 Page 0, Register 31, Bits D6-D5 = 00
F3	I^2S WCLK output WCLK	Page 0, Register 27, Bit D2 = 1	R6	Secondary I^2S WCLK in on SCLK/MFP3	Page 0, Register 56, Bits D2-D1 = 01 Page 0, Register 31, Bits D4-D3 = 01
G6	I^2S ADC word clock input on SCLK/MFP3	Page 0, Register 56, Bits D2-D1 = 01 Page 0, Register 31, Bits D2-D1 = 01	R8	Secondary I^2S WCLK in on GPIO/MFP50	Page 0, Register 52, Bits D5-D2 = 0001 Page 0, Register 31, Bits D4-D3 = 0
G8	I^2S ADC word clock input on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0001 Page 0, Register 31, Bits D2-D1 = 00	S6	Secondary I^2S DIN on SCLK/MFP3	Page 0, Register 56, Bits D2-D1 = 01 Page 0, Register 31, Bit D0 = 1
H7	I^2S ADC WCLK out on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 0110	S8	Secondary I^2S DIN on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0001 Page 0, Register 31, Bit D0 = 0
H8	I^2S ADC WCLK out on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0111	T7	Secondary I^2S DOUT on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 1000

Table 2-2. Multifunction Pin Register Configuration (continued)

	Description	Required Register Setting		Description	Required Register Setting
I4	I^2S DIN on DIN/MFP1	Page 0, Register 54, Bits D2-D1 = 01	U5	Secondary I^2S BCLK OUT on DOUT/MFP2	Page 0, Register 53, Bits D3-D1 = 110
J5	I^2S DOUT on DOUT/MFP2	Page 0, Register 53, Bits D3-D1 = 001	U7	Secondary I^2S BCLK OUT on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 1001
K5	General Purpose Out I on DOUT/MFP2	Page 0, Register 53, Bits D3-D1 = 010	U8	Secondary I^2S BCLK OUT on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 1000
K7	General Purpose Out II on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 0010	V5	Secondary I^2S WCLK OUT on SCLK/MFP3	Page 0, Register 53, Bits D3-D1 = 111
K8	General Purpose Out III on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0011	V7	Secondary I^2S WCLK OUT on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 1010
L4	General Purpose In I on DIN/MFP1	Page 0, Register 54, Bits D2-D1 = 10	V8	Secondary I^2S WCLK OUT on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 1001
L6	General Purpose In II on SCLK/MFP3	Page 0, Register 56, Bits D2-D1 = 10	W6	Headset Detect Input on SCLK/MFP3	Page 0, Register 56, Bits D2-D1 = 00 Page 0, Register 67, Bit D7 = 1
L8	General Purpose In III on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0010	X5	Aux Clock Output on DOUT/MFP2	Page 0, Register 53, Bits D3-D1 = 011
M5	INT1 output on DOUT/MFP2	Page 0, Register 53, Bits D3-D1 = 100	X7	Aux Clock Output on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 0011
M7	INT1 output on MISO/MFP4	Page 0, Register 55, Bits D4-D1 = 0100	X8	Aux Clock Output on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0100
M8	INT1 output on GPIO/MFP5	Page 0, Register 52, Bits D5-D2 = 0101			

2.2 Analog Audio I/O

The analog I/O path of the TLV320DAC3203 offers a variety of options for signal conditioning and routing:

- 2 headphone amplifier outputs
- Analog gain setting
- Single ended and differential modes

2.2.1 Analog Low Power Bypass

The TLV320DAC3203 offers an analog-bypass mode. An analog signal can be routed from the analog input pin to the output amplifier. Neither the digital-input processing blocks nor the DAC resources are required for such operation; this supports low-power operation during analog-bypass mode.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs INL to the left headphone amplifier (HPL) and INR to HPR.

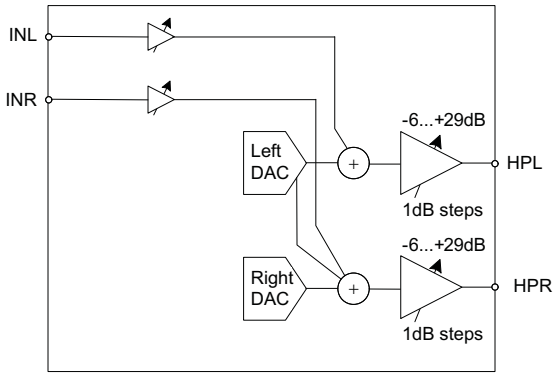

Figure 2-1. Low Power Analog Bypass

2.2.2 Headphone Output

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended AC-coupled headphone configurations, or loads down to 32Ω in differential mode, where a speaker is connected between HPL and HPR. In single-ended drive configuration these drivers can drive up to 15mW power into each headphone channel while operating from 1.8V analog supplies. While running from the AVdd supply, the output common-mode of the headphone driver is set by the common-mode setting of analog inputs to allow maximum utilization of the analog supply range while simultaneously providing a higher output-voltage swing. In cases when higher output-voltage swing is required, the headphone amplifiers can run directly from the higher supply voltage on LDOIN input (up to 3.6V). To use the higher supply voltage for higher output signal swing, the output common-mode can be adjusted to either 1.25V, 1.5V or 1.65V. When the common-mode voltage is configured at 1.65V and LDOIN supply is 3.3V, the headphones can each deliver up to 40mW power into a 16Ω load.

The headphone drivers are capable of driving a mixed combination of DAC signal and bypass from analog input INL and INR. The analog input signals can be attenuated up to 72dB before routing. The level of the DAC signal can be controlled using the digital volume control of the DAC. To control the output-voltage swing of headphone drivers, the digital volume control provides a range of –6.0dB to +29.0dB [(1)] in steps of 1dB. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration. Refer to for recommendations for using headphone volume control for achieving 0dB gain through the DAC channel with various configurations.

2.2.2.1 Stereo Single Ended Configuration

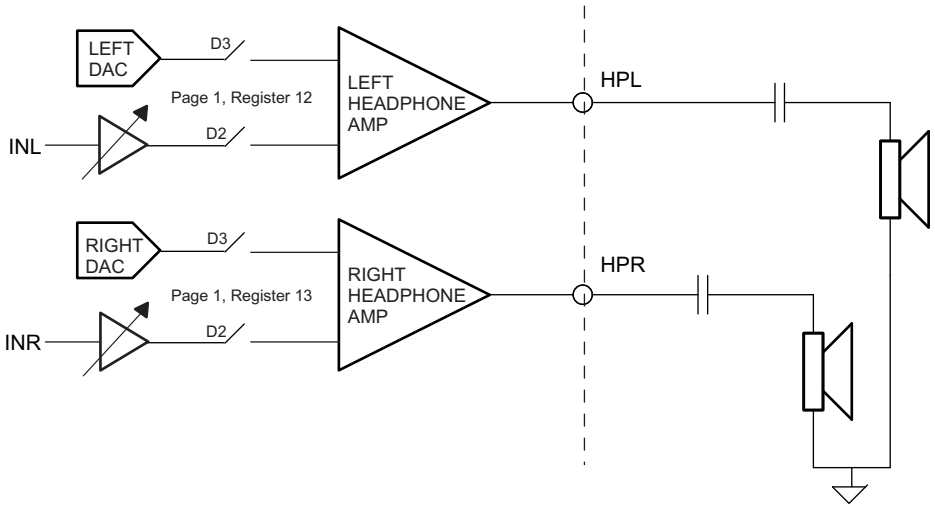

Figure 2-2. Stereo Headphone Configuration

The left and right DAC channels are routed to the corresponding left and right headphone amplifier. This configuration is also used to drive line-level loads.

The TLV320DAC3203 headphone drivers support pop-free operation. Because the HPL and HPR are high-power drivers, pop can result due to sudden transient changes in the output drivers if care is not taken. The most critical care is required while using the drivers as stereo single-ended capacitively-coupled drivers as shown in Figure 2-2. The output drivers achieve pop-free power-up by using slow power-up modes. Conceptually, the circuit during power-up can be visualized as

(1) If the device must be placed into 'mute' from the –6.0dB setting, set the device at a gain of –5.0dB first, then place the device into mute.

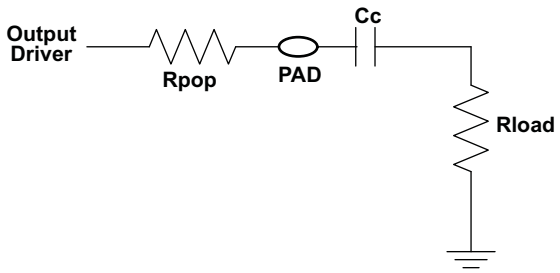

Figure 2-3. Conceptual Circuit for Pop-Free Power-up

The value of R_{pop} can be chosen by setting register Page 1, Register 20, Bits D1-D0).

Table 2-3. R_{pop} Values

Page 1, Register 20, Bits D1-D0)	R_{pop} Value
00	2 kΩ
01	6 kΩ
10	25 kΩ

To minimize audible artifacts, two parameters can be adjusted to match application requirements. The voltage V_{load} across R_{load} at the beginning of slow charging should not be more than a few mV. At that time the voltage across R_{load} can be determined as:

$$V_{load} = \frac{R_{load}}{R_{load} + R_{pop}} \times V_{cm} \quad (1)$$

For a typical R_{load} of 32Ω, R_{pop} of 6 kΩ or 25 kΩ will deliver good results (see Table 2-3 for register settings).

According to the conceptual circuit in Figure 2-3, the voltage on PAD will exponentially settle to the output common-mode voltage based on the value of R_{pop} and C_c. Thus, the output drivers must be in slow power-up mode for time T, such that at the end of the slow power-on period, the voltage on V_{pad} is very close to the common-mode voltage. The TLV320DAC3203 allows the time T to be adjusted to allow for a wide range of R_{load} and C_c by programming Page 1, Register 20, Bits D5-D2). For the time adjustments, the value of C_c is assumed to be 47μF. N=5 is expected to yield good results.

Page 1, Register 20, Bits D5-D2)	Slow Charging Time=N*Time – Constants(for R_{pop} and 47μF)
0000	N=0
0001	N=0.5
0010	N=0.625
0011	N=0.75
0100	N=0.875
0101	N=1.0
0110	N=2.0
0111	N=3.0
1000	N=4.0
1001	N=5.0
1010	N=6.0
1011	N=7.0
1100	N=8.0
1101	N=16 (Not valid for R_{pop}=25kΩ)
1110	N=24 (Not valid for R_{pop}=25kΩ)
1111	N=32 (Not valid for R_{pop}=25kΩ)

Again, for example, for R_{load}=32Ω, C_c=47μF and common mode of 0.9V, the number of time constants required for pop-free operation is 5 or 6. A higher or lower C_c value will require higher or lower value for N.

During the slow-charging period, no signal is routed to the output driver. Therefore, choosing a larger than necessary value of N results in a delay from power-up to signal at output. At the same time, choosing N to be smaller than the optimal value results in poor pop performance at power-up.

The signals being routed to headphone drivers (e.g. DAC and IN) often have DC offsets due to less-than-ideal processing. As a result, when these signals are routed to output drivers, the offset voltage causes a pop. To improve the pop-performance in such situations, a feature is provided to soft-step the DC-offset. At the beginning of the signal routing, a high-value attenuation can be applied which can be progressively reduced in steps until the desired gain in the channel is reached. The time interval between each of these gain changes can be controlled by programming Page 1, Register 20, Bits D7-D6). This gain soft-stepping is applied only during the initial routing of the signal to the output driver and not during subsequent gain changes.

Page 1, Register 20, Bits D7-D6	Soft-stepping Step Time During initial signal routing
00	0 ms (soft-stepping disabled)
01	50ms
10	100ms
11	200ms

It is recommended to use the following sequence for achieving optimal pop performance at power-up:

1. Choose the value of R_{pop}, N (time constants) and soft-stepping step time for slow power-up.
2. Choose the configuration for output drivers, including common modes and output stage power connections
3. Select the signals to be routed to headphones.
4. Power-up the blocks driving signals into HPL and HPR, but keep it muted
5. Unmute HPL and HPR and set the desired gain setting.
6. Power-on the HPL and HPR drivers.
7. Unmute the block driving signals to HPL and HPR after the Driver PGA flags are set to indicate completion of soft-stepping after power-up. These flags can be read from Page 1, Register 63, Bits D7-D6).

It is important to configure the Headphone Output driver depop control registers before powering up the headphone; these register contents should not be changed when the headphone drivers are powered up.

Before powering down the HPL and HPR drivers, it is recommended that user read back the flags in Page 1, Register 63. For example. before powering down the HPL driver, ensure that bit D(7) = 1 and bit D(3) = 1 if INL is routed to HPL and bit D(1) = 1 if the Left Mixer is routed to HPL. The output driver should be powered down only after a steady-state power-up condition has been achieved. This steady state power-up condition also must be satisfied for changing the HPL/R driver mute control in Page 1, Register 16 and 17, Bits D7), i.e. muting and unmuting should be done after the gain and volume controls associated with routing to HPL/R finished soft-stepping.

In the differential configuration of HPL and HPR, when no coupling capacitor is used, the slow charging method for pop-free performance need not be used. In the differential load configuration for HPL and HPR, it is recommended to not use the output driver MUTE feature, because a pop may result.

During the power-down state, the headphone outputs are weakly pulled to ground using an approximately 50kΩ resistor to ground, to maintain the output voltage on HPL and HPR pins.

2.2.2.2 Mono Differential DAC to Mono Differential Headphone Output

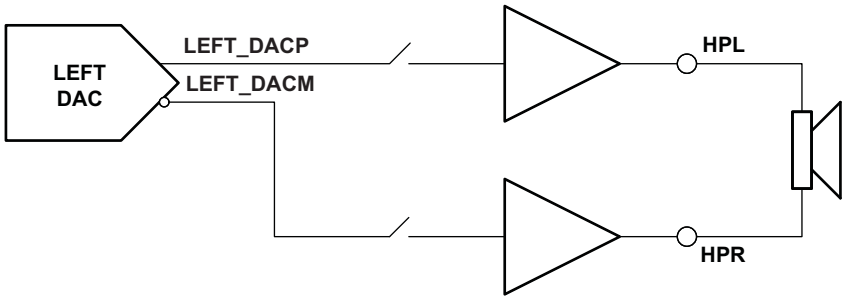

Figure 2-4. Low Power Mono DAC to Differential Headphone

This configuration supports the routing of the two differential outputs of the mono, left channel DAC to the headphone amplifiers in differential mode (Page 1 / Register 12, D3 =1 and Page 1 / Register 13, D4 =1).

2.2.2.2.1 Offset Correction Scheme for Differential DAC to Differential Headphone Output

The TLV320DAC3203 offers an offset correction scheme which is based on calibration during power up. This scheme will minimize differences in DC voltage between the HPL and HPR outputs.

The offset calibration happens after the headphones are powered up in differential mode. All other headphone configurations like signal routings, gain settings and mute removal needs to be configured before the power up of headphones. Any change in these settings while the headphones are powered up may result in additional differential offsets and are best avoided.

The offset calibration block has a few programmable parameters which the user needs to control. The user can either choose to calibrate the offset at each power-up of headphones or do it only for first power up of headphone after system power up and hardware reset.

Programming Page 1 / Register 125, D(1:0) as “01” would cause the offset to be calibrated for each power up of headphone. This is particularly useful when some headphone configurations like gain or signal routings change between power ups.

Programming Page 1 / Register 125, D(1:0) as “10” would cause the offset to be calibrated for only the first power-up of the headphone amplifiers after hardware reset. The calibration data will be stored in internal memory until the next hardware reset or until AVDD power is removed. Since offset calibration is not done every time the headphone amplifiers power up the turn on time is reduced by approximately 3.6 ms for subsequent powerups.

Programming Page 1 / Reg 125, D (1:0) as “00” (default) will disable offset correction block.

While the offset is being calibrated no signal should be applied to the headphone amplifier, i.e. the DAC should be kept muted and analog bypass routing should be kept at highest attenuation setting of 78dB. The user can read Page 1 / Regiseter 2, D2 to poll if calibration is completed (D2=”1” -> calibration is completed).

Please see Section 4.8 for an example setup script enabling offset correction.

2.2.2.3 Headphone Amplifier Class-D Mode

By default the headphone amplifiers in the TLV320DAC3203 work in Class-AB mode. By writing to Page 1, Register 3, Bits D7-D6) for the left headphone amplifier, and Page 1, Register 4, Bits D7-D6) with value 11, the headphone amplifiers enter a Class-D mode of operation.

In this mode a high frequency digital pulse-train representation of the DAC signal is fed to the load connected to HPL and HPR outputs.

Because the output signal is a pulse train switching between Power Supply and Ground, the efficiency of the amplifier is greatly improved. In this mode however, for good noise performance, care should be taken to keep the analog power supply clean.

For using the Class-D mode of operation, the following clock-divider condition should be met:

MDAC = I × 4, where I = 1, 2, ..., 32

When a direct digital pulse train is driven out as a signal, high frequencies as a function of pulse train frequency are also present which lead to power waste. To increase the efficiency and reduce power dissipation in the load due to these high frequencies, an LC filter should be used in series with the output and the load. The cutoff frequency of the LC filter should be adjusted to allow audio signals below 20kHz to pass through, but highly attenuate the high-frequency signal content.

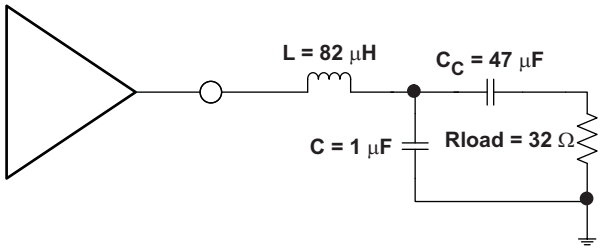

Figure 2-5. Configuration for Using Headphone Amplifier in Class-D Mode

For using the headphones in the Class-D mode of operation, the headphones should first be powered up in default Class-AB mode to charge the AC-coupling capacitor to the set common mode voltage. Once the headphone amplifiers have been so powered up, the DAC should be routed to headphones and unmuted before they can be switched to the Class-D mode. After Class D mode has been turned on, the linear, Class AB mode amplifier must be turned off. For powering down the headphone amplifiers, the DAC should first be muted.

See Section 4.6 for an example setup script enabling Class-D mode.

2.3 Digital Microphone Input/Decimation Filter

The TLV320DAC3203 includes a stereo decimation filter for digital microphone inputs. The stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The digital microphone input path of the TLV320DAC3203 features a large set of options for signal conditioning as well as signal routing:

- Stereo decimation filters (PDM input)
- Fine gain adjustment of digital channels with 0.1dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function

In addition to the standard set of stereo decimation filter features the TLV320DAC3203 also offers the following special functions:

- Channel-to-channel phase adjustment
- Adaptive filter mode

2.3.1 Digital Microphone Interface

The TLV320DAC3203 digital-microphone interface is shown in Figure 2-6.

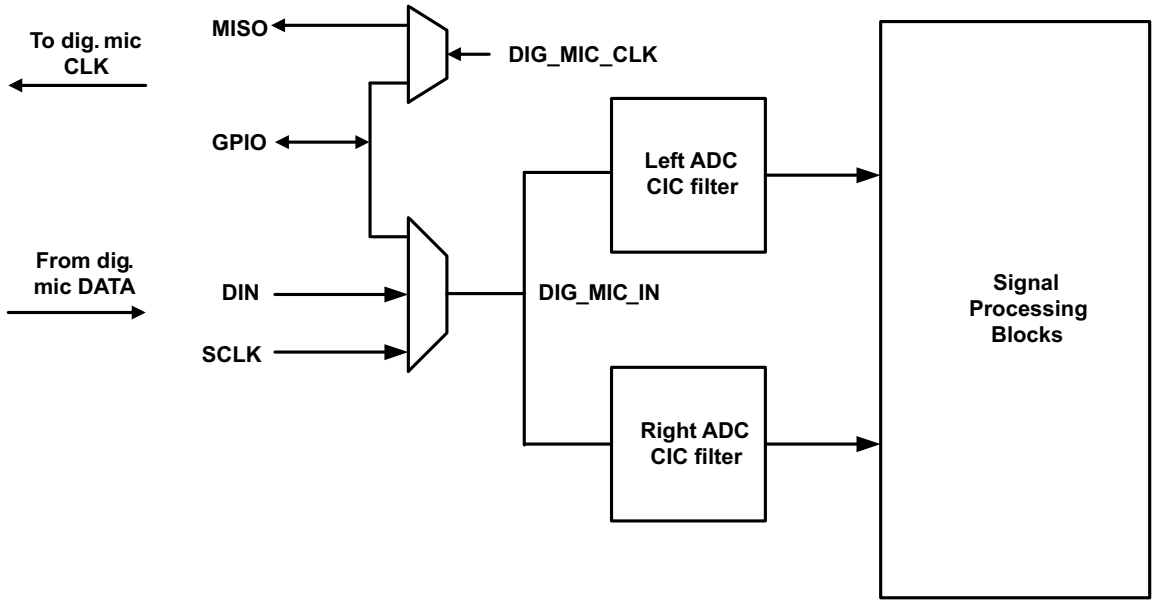

Figure 2-6. Digital Microphone in TLV320DAC3203

The TLV320DAC3203 outputs internal clock DIG_MIC_CLK on GPIO pin (Page 0, Register 51, D(5:2)) or MISO pin (Page 0, Register 55, D(4:1)). This clock can be connected to the external digital microphone device. The single-bit output of the external digital microphone device can be connected to GPIO, DIN or SCLK pins. Internally the TLV320DAC3203 latches the steady value of data on the rising edge of DIG_MIC_CLK for the Left ADC channel, and the steady value of data on falling edge for the Right ADC channel.

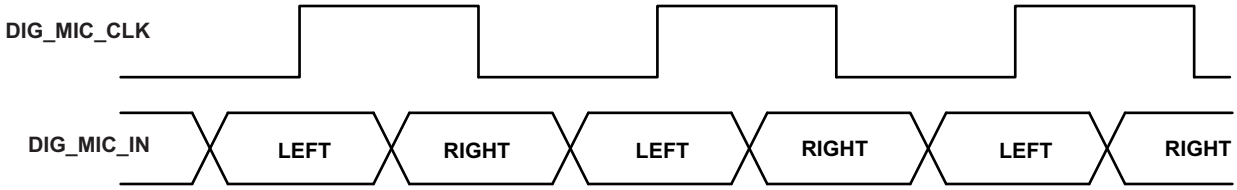

Figure 2-7. Timing Diagram for Digital Microphone Interface

The digital-microphone mode can be selectively enabled for only-left, only-right, or stereo channels. The AOSR value for the ADC channel must be configured to select the desired decimation ratio to be achieved based on the external digital microphone properties.

2.3.2 Digital Volume Control

The TLV320DAC3203 also has a digital volume-control block with a range from -12dB to +20dB in steps of 0.5dB. The system controls the volume by programming Page 0, Register 83 and 84 respectively for left and right channels.

Table 2-4. Digital Volume Control for ADC

Desired Gain dB	Left or Right Channel Page 1, Register 83 or 84 (respectively), D(6:0)
–12.0	110 1000
–11.5	110 1001
–11.0	110 1010
..	
–0.5	111 1111
0.0	000 0000 (Default)
+0.5	000 0001
..	
+19.5	010 0111
+20.0	010 1000

During volume control changes, using the soft-stepping feature avoids audible artifacts. The soft-stepping rate can be set to either 1 or 2 gain steps per sample. Soft-stepping can also be entirely disabled. This soft-stepping is configured via Page 1, Register 81, D(1:0), and is common to the soft-stepping control for the analog PGA. During power-down of an ADC channel, this volume control soft-steps down to –12.0dB before powering down. Due to the soft-stepping control, soon after changing the volume control setting or powering down the ADC channel, the actual applied gain may be different from the one programmed through the control register. The TLV320DAC3203 gives feedback to the user, through read-only flags Page 1, Reg 36, D(7) for Left Channel and Page 1, Reg 36, D(3) for the right channel.

2.3.2.1 Fine Digital Gain Adjustment

Additionally, the gain in each of the channels is finely adjustable in steps of 0.1dB. This granularity is useful when trying to match the gain between channels. By programming Page 0, Register 82 the gain can be adjusted from 0dB to -0.4dB in steps of 0.1dB. This feature, in combination with the regular digital volume control, allows the gains through the left and right channels be matched in the range of -0.5dB to +0.5dB with a resolution of 0.1dB.

2.3.3 Digital Microphone Decimation Filtering and Signal Processing Overview

The TLV320DAC3203 includes a built-in digital decimation filter to process the oversampled data from the PDM input to generate digital data at Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay and sampling rate.

2.3.3.1 Processing Blocks

The TLV320DAC3203 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

Table 2-5 gives an overview of the available processing blocks and their properties.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 2-5. Processing Blocks

Processing Blocks	Channel	Decimation Filter	1st Order IIR Available	Number BiQuads	FIR	Required AOSR Value	Resource Class
PRB_R1[1]	Stereo	A	Yes	0	No	128,64	6
PRB_R2	Stereo	A	Yes	5	No	128,64	8
PRB_R3	Stereo	A	Yes	0	25-Tap	128,64	8
PRB_R4	Right	A	Yes	0	No	128,64	3
PRB_R5	Right	A	Yes	5	No	128,64	4
PRB_R6	Right	A	Yes	0	25-Tap	128,64	4
PRB_R7	Stereo	B	Yes	0	No	64	3
PRB_R8	Stereo	B	Yes	3	No	64	4
PRB_R9	Stereo	B	Yes	0	20-Tap	64	4
PRB_R10	Right	B	Yes	0	No	64	2
PRB_R11	Right	B	Yes	3	No	64	2
PRB_R12	Right	B	Yes	0	20-Tap	64	2
PRB_R13	Stereo	C	Yes	0	No	32	3
PRB_R14	Stereo	C	Yes	5	No	32	4
PRB_R15	Stereo	C	Yes	0	25-Tap	32	4
PRB_R16	Right	C	Yes	0	No	32	2
PRB_R17	Right	C	Yes	5	No	32	2
PRB_R18	Right	C	Yes	0	25-Tap	32	2

(1) Default

2.3.3.2 Signal Processing Details

2.3.3.2.1 Processing Block Descriptions

2.3.3.2.1.1 1st order IIR, Filter A

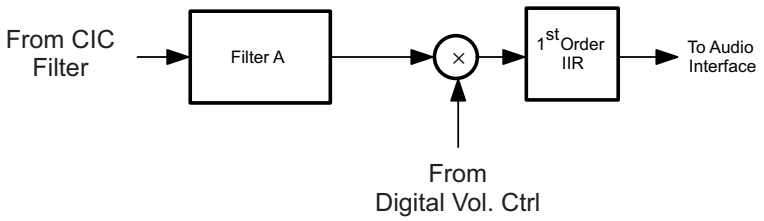

Figure 2-8. Signal Chain for PRB_R1 and PRB_R4

2.3.3.2.1.2 5 Biquads, 1st order IIR, Filter A

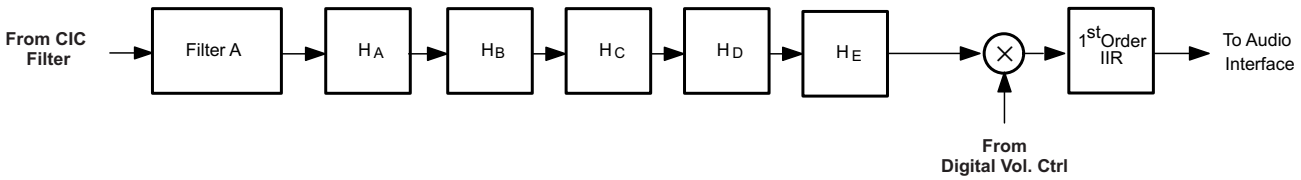

Figure 2-9. Signal Chain PRB_R2 and PRB_R5

2.3.3.2.1.3 25 Tap FIR, 1st order IIR, Filter A

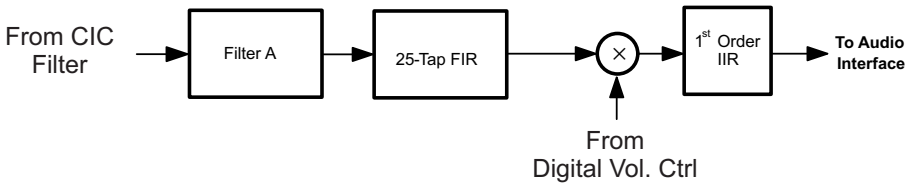

Figure 2-10. Signal Chain for PRB_R3 and PRB_R6

2.3.3.2.1.4 1st order IIR, Filter B

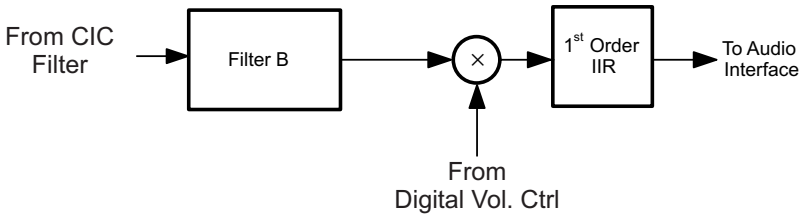

Figure 2-11. Signal Chain for PRB_R7 and PRB_R10

2.3.3.2.1.5 3 Biquads, 1st order IIR, Filter B

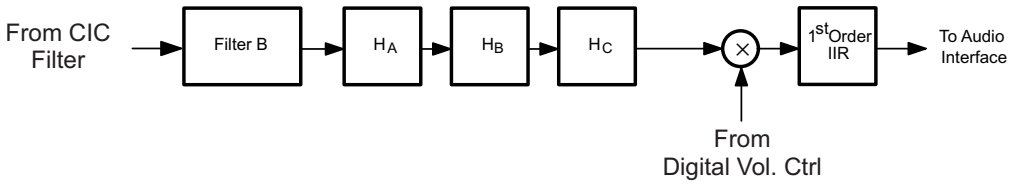

Figure 2-12. Signal Chain for PRB_R8 and PRB_R11

2.3.3.2.1.6 20 Tap FIR, 1st order IIR, Filter B

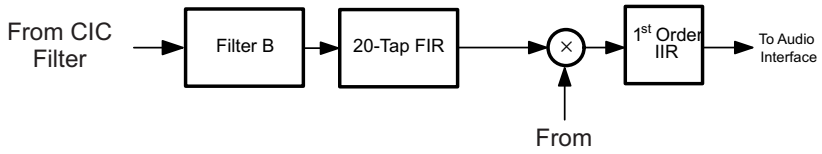

Figure 2-13. Signal Chain for PRB_R9 and PRB_R12

2.3.3.2.1.7 1st order IIR, Filter C

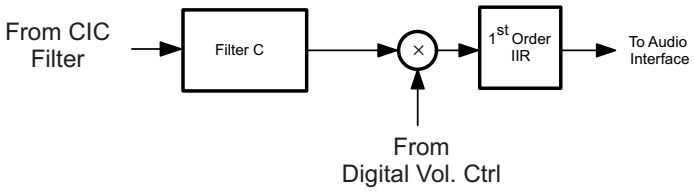

Figure 2-14. Signal Chain for PRB_R13 and PRB_R16

2.3.3.2.1.8 5 Biquads, 1st order IIR, Filter C

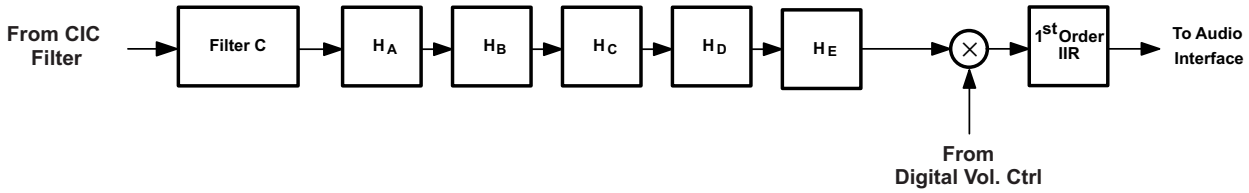

Figure 2-15. Signal Chain for PRB_R14 and PRB_R17

2.3.3.2.1.9 25 Tap FIR, 1st order IIR, Filter C

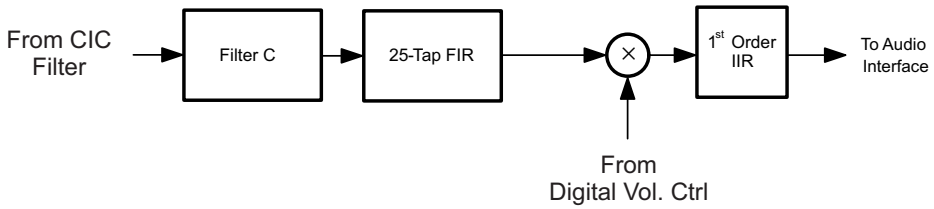

Figure 2-16. Signal for PRB_R15 and PRB_R18

2.3.3.2.2 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. A 1st-order IIR filter is always available, and is useful to efficiently filter out possible DC components of the signal. Up to 5 biquad section or alternatively up to 25-tap FIR filters are available for specific processing blocks. The coefficients of the available filters are arranged as sequentially indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched on-the-fly. For more details on adaptive filtering see Section 2.3.3.3.3 below.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see Section 5.17.

2.3.3.2.2.1 1st Order IIR Section

The transfer function for the first order IIR Filter is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (2)$$

The frequency response for the 1st order IIR Section with default coefficients is flat at a gain of 0dB. Details on coefficient default values are given in Section 5.17.

Table 2-6. First-Order IIR Filter Coefficients

Filter	FIlter Coefficient	Coefficient Left Channel	Coefficient Right Channel
1st Order IIR	N0	C4 (Pg 8,Reg 24,25,26)	C36 (Pg 9,Reg 32,33,34)
	N1	C5 (Pg 8,Reg 28,29,30)	C37 (Pg 9,Reg 36,37,38)
	D1	C6 (Pg 8,Reg 32,33,34)	C39 (Pg 9,Reg 40,41,42)

2.3.3.2.2.2 Biquad Section

The transfer function of each of the Biquad Filters is given by

$$H(z) = \frac{N_0 + 2 * N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2 * D_1 z^{-1} - D_2 z^{-2}} \quad (3)$$

The frequency response for each of the biquad section with default coefficients is flat at a gain of 0dB. Details on coefficient default values are given in Section 5.17.

Table 2-7. Biquad Filter Coefficients

Filter	FIlter Coefficient	Coefficient Left Channel	Coefficient Right Channel
BIQUAD A	N0	C7 (Pg 8, Reg 36,37,38)	C39 (Pg 9, Reg 44,45,46)
	N1	C8 (Pg 8, Reg 40,41,42)	C40 (Pg 9, Reg 48,49,50)
	N2	C9 (Pg 8, Reg 44,45,46)	C41 (Pg 9, Reg 52,53,54)
	D1	C10 (Pg 8, Reg 48,49,50)	C42 (Pg 9, Reg 56,57,58)
	D2	C11 (Pg 8, Reg 52,53,54)	C43 (Pg 9, Reg 60,61,62)
BIQUAD B	N0	C12 (Pg 8, Reg 56,57,58)	C44 (Pg 9, Reg 64,65,66)
	N1	C13 (Pg 8, Reg 60,61,62)	C45 (Pg 9, Reg 68,69,70)
	N2	C14 (Pg 8, Reg 64,65,66)	C46 (Pg 9, Reg 72,73,74)
	D1	C15 (Pg 8, Reg 68,69,70)	C47 (Pg 9, Reg 76,77,78)
	D2	C16 (Pg 8, Reg 72,73,74)	C48 (Pg 9, Reg 80,81,82)
BIQUAD C	N0	C17 (Pg 8, Reg 76,77,78)	C49 (Pg 9, Reg 84,85,86)
	N1	C18 (Pg 8, Reg 80,81,82)	C50 (Pg 9, Reg 88,89,90)
	N2	C19 (Pg 8, Reg 84,85,86)	C51 (Pg 9, Reg 92,93,94)
	D1	C20 (Pg 8, Reg 88,89,90)	C52 (Pg 9, Reg 96,97,98)
	D2	C21 (Pg 8, Reg 92,93,94)	C53 (Pg 9, Reg 100,101,102)
BIQUAD D	N0	C22 (Pg 8, Reg 96,97,98)	C54 (Pg 9, Reg 104,105,106)
	N1	C23 (Pg 8, Reg 100,101,102)	C55 (Pg 9, Reg 108,109,110)
	N2	C24 (Pg 8, Reg 104,105,106)	C56 (Pg 9, Reg 112,113,114)
	D1	C25 (Pg 8, Reg 108,109,110)	C57 (Pg 9, Reg 116,117,118)
	D2	C26 (Pg 8, Reg 112,113,114)	C58 (Pg 9, Reg 120,121,122)
BIQUAD E	N0	C27 (Pg 8, Reg 116,117,118)	C59 (Pg 9, Reg 124,125,126)
	N1	C28 (Pg 8, Reg 120,121,122)	C60 (Pg 10, Reg 8,9,10)
	N2	C29 (Pg 8, Reg 124,125,126)	C61 (Pg 10, Reg 12,13,14)
	D1	C30 (Pg 9, Reg 8,9,10)	C62 (Pg 10, Reg 16,17,18)
	D2	C31 (Pg 9, Reg 12,13,14)	C63 (Pg 10, Reg 20,21,22)

2.3.3.2.2.3 FIR Section

Six of the available processing blocks offer FIR filters for signal processing. PRB_R9 and PRB_R12 feature a 20-tap FIR filter while the processing blocks PRB_R3, PRB_R6, PRB_R15 and PRB_R18 feature a 25-tap FIR filter

$$H(z) = \sum_{n=0}^{M} Fir_n z^{-n}$$

$$M = 24, \text{for PRB\_R3, PRB\_R6, PRB\_R15 and PRB\_R18}$$

$$M = 19, \text{for PRB\_R9 and PRB\_R12} \quad (4)$$

The coefficients of the FIR filters are 24-bit 2's complement format and correspond to the coefficient space as listed below. There is no default transfer function for the FIR filter. When the FIR filter gets used all applicable coefficients must be programmed.

Table 2-8. FIR Filter Coefficients

Filter	FIlter Coefficient Left Channel	Filter Coefficient Right Channel
Fir0	C7 (Pg 8, Reg 36,37,38)	C39 (Pg 9, Reg 44,45,46)
Fir1	C8 (Pg 8, Reg 40,41,42)	C40 (Pg 9, Reg 48,49,50)
Fir2	C9 (Pg 8, Reg 44,45,46)	C41 (Pg 9, Reg 52,53,54)
Fir3	C10 (Pg 8, Reg 48,49,50)	C42 (Pg 9, Reg 56,57,58)
Fir4	C11 (Pg 8, Reg 52,53,54)	C43 (Pg 9, Reg 60,61,62)
Fir5	C12 (Pg 8, Reg 56,57,58)	C44 (Pg 9, Reg 64,65,66)
Fir6	C13 (Pg 8, Reg 60,61,62)	C45 (Pg 9, Reg 68,69,70)
Fir7	C14 (Pg 8, Reg 64,65,66)	C46 (Pg 9, Reg 72,73,74)
Fir8	C15 (Pg 8, Reg 68,69,70)	C47 (Pg 9, Reg 76,77,78)
Fir9	C16 (Pg 8, Reg 72,73,74)	C48 (Pg 9, Reg 80,81,82)
Fir10	C17 (Pg 8, Reg 76,77,78)	C49 (Pg 9, Reg 84,85,86)
Fir11	C18 (Pg 8, Reg 80,81,82)	C50 (Pg 9, Reg 88,89,90)
Fir12	C19 (Pg 8, Reg 84,85,86)	C51 (Pg 9, Reg 92,93,94)
Fir13	C20 (Pg 8, Reg 88,89,90)	C52 (Pg 9, Reg 96,97,98)
Fir14	C21 (Pg 8, Reg 92,93,94)	C53 (Pg 9, Reg 100,101,102)
Fir15	C22 (Pg 8, Reg 96,97,98)	C54 (Pg 9, Reg 104,105,106)
Fir16	C23 (Pg 8, Reg 100,101,102)	C55 (Pg 9, Reg 108,109,110)
Fir17	C24 (Pg 8, Reg 104,105,106)	C56 (Pg 9, Reg 112,113,114)
Fir18	C25 (Pg 8, Reg 108,109,110)	C57 (Pg 9, Reg 116,117,118)
Fir19	C26 (Pg 8, Reg 112,113,114)	C58 (Pg 9, Reg 120,121,122)
Fir20	C27 (Pg 8, Reg 116,117,118)	C59 (Pg 9, Reg 124,125,126)
Fir21	C28 (Pg 8, Reg 120,121,122)	C60 (Pg 10, Reg 8,9,10)
Fir22	C29 (Pg 8, Reg 124,125,126)	C61 (Pg 10, Reg 12,13,14)
Fir23	C30 (Pg 9, Reg 8,9,10)	C62 (Pg 10, Reg 16,17,18)
Fir24	C31 (Pg 9, Reg 12,13,14)	C63 (Pg 10, Reg 20,21,22)

2.3.3.2.3 Decimation Filter

The TLV320DAC3203 offers 3 different types of decimation filters. The integrated digital decimation filter removes high-frequency content and down samples the audio data from an initial sampling rate of AOSR*Fs to the final output sampling rate of Fs. The decimation filtering is achieved using a higher-order CIC filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself, it is implicitly set through the chosen processing block.

The following subsections describe the properties of the available filters A, B and C.

2.3.3.2.3.1 Decimation Filter A

This filter is intended for use at sampling rates up to 48kHz. When configuring this filter, the oversampling ratio of the can either be 128 or 64. For highest performance the oversampling ratio must be set to 128. Please also see the PowerTune chapter for details on performance and power in dependency of AOSR.

Filter A can also be used for 96kHz at an AOSR of 64.

Table 2-9. Decimation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
AOSR = 128			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…64Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
AOSR = 64			
Filter Gain Pass Band	0…0.39 Fs	0.062	dB
Filter Gain Stop Band	0.55…32Fs	–73	dB
Filter Group Delay		17/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39 Fs	0.062	dB
Pass Band Ripple, 44.1 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 48 ksps	0…0.39 Fs	0.05	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.1	dB

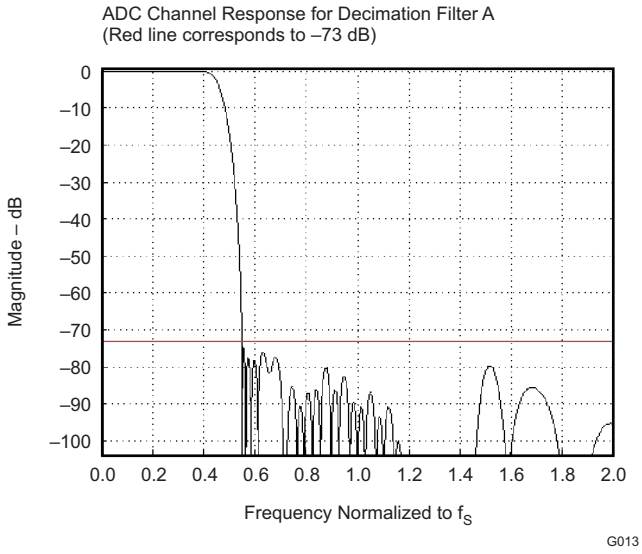

Figure 2-17. Decimation Filter A, Frequency Response

2.3.3.2.3.2 Decimation Filter B

Filter B is intended to support sampling rates up to 96kHz at a oversampling ratio of 64.

Table 2-10. Decimation Filter B, Specifications

Parameter	Condition	Value (Typical)	Units
AOSR = 64			
Filter Gain Pass Band	0…0.39Fs	±0.077	dB
Filter Gain Stop Band	0.60Fs…32Fs	–46	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.39Fs	0.076	dB
Pass Band Ripple, 44.1 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 48 ksps	0…0.39Fs	0.06	dB
Pass Band Ripple, 96 ksps	0…20kHz	0.11	dB

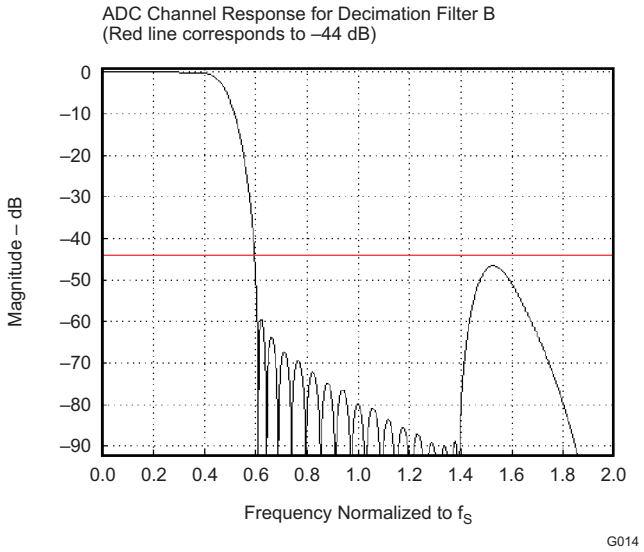

Figure 2-18. Decimation Filter B, Frequency Response

2.3.3.2.3.3 Decimation Filter C

Filter type C along with AOSR of 32 is specially designed for 192ksps operation for the ADC. The pass band which extends up to 0.11*Fs (corresponds to 21kHz), is suited for audio applications.

Table 2-11. Decimation Filter C, Specifications

Parameter	Condition	Value (Typical)	Units
Filter Gain from 0 to 0.11Fs	0…0.11Fs	±0.033	dB
Filter Gain from 0.28Fs to 16Fs	0.28Fs…16Fs	–60	dB
Filter Group Delay		11/Fs	Sec.
Pass Band Ripple, 8 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 44.1 ksps	0…0.11Fs	0.033	dB
Pass Band Ripple, 48 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 96 ksps	0…0.11Fs	0.032	dB
Pass Band Ripple, 192 ksps	0…20kHz	0.086	dB

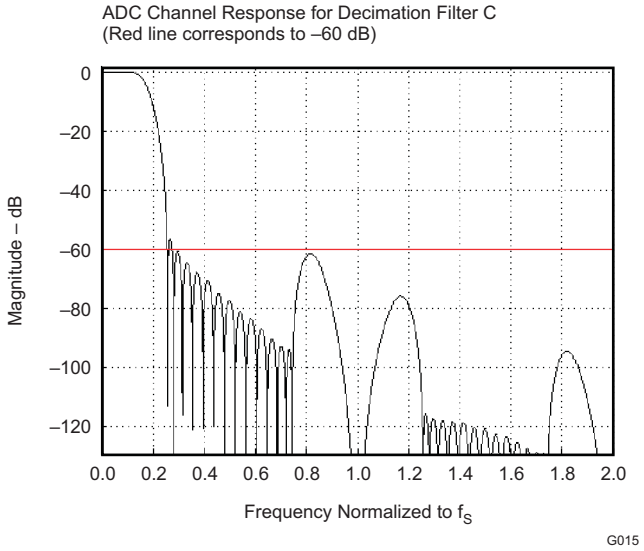

Figure 2-19. Decimation Filter C, Frequency Response

2.3.3.2.4 ADC Data Interface

The decimation filter and signal processing block in the ADC channel passes 32-bit data words to the audio serial interface once every cycle of Fs,ADC. During each cycle of Fs,ADC, a pair of data words (for left and right channel) are passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data as per the different modes for audio serial interface.

2.3.3.3 Special Functions

2.3.3.3.1 Microphone Bias

The TLV320DAC3203 has a built-in low noise Microphone Bias support for electret-condenser microphones. The Bias amplifier can support up to 3mA of load current to support multiple microphones. The Bias amplifier has been designed to provide a combination of high PSRR, low noise and programmable bias voltages to allow the user to fine tune the biasing to specific microphone combinations. To support a wide range of bias voltages, the bias amplifier can work of either a low analog supply or high LDOIN supply.

Table 2-12. MICBIAS Voltage Control

Page 1, Reg 51, D(5:4)	Page 1, Reg 10, D(6)	Page 1, Reg 51, D(3)	MICBIAS Voltage (without load)
00	0	X	1.25V
00	1	X	1.0V
01	0	X	1.7V
01	1	X	1.4V
10	0	1	2.5V
10	1	1	2.1V
11	X	0	AVdd
11	X	1	LDOIN

2.3.3.3.2 Channel-to-Channel Phase Adjustment

The TLV320DAC3203 has a built-in feature to fine-adjust the phase between the stereo ADC record signals. The phase compensation is particularly helpful to adjust delays when using dual microphones for noise cancellation etc.

This delay can be controlled in fine amounts in the following fashion.

Delay(7:0) = Page 0/Register 85/D(7:0)

Where

$$RIGHT\_ADC\_PHASE\_COMP(t) = RIGHT\_ADC\_OUT(t - t_{pr}) \quad (5)$$

where

$$t_{pr} = \frac{(Delay(4:0) + Delay(6:5) * AOSR * k_f)}{AOSR * ADC\_FS} \quad (6)$$

Where k_f is a function of the decimation filter:

Decimation Filter Type	k_f
A	0.25
B	0.5
C	1

and

$$LEFT\_ADC\_PHASE\_COMP(t) = LEFT\_ADC\_OUT(t - t_{pl}) \quad (7)$$

Where

$$t_{pl} = \frac{Delay(7)}{ADC\_FS} \quad (8)$$

2.3.3.3.3 Adaptive Filtering

After the ADC is running, the filter coefficients are locked and cannot be accessed for read or write. However the TLV320DAC3203 offers an adaptive filter mode as well. Setting Register Page 8,Reg 1, D(2)=1 turns on double buffering of the coefficients. In this mode filter coefficients can be updated through the host and activated without stopping and restarting the ADC, enabling advanced adaptive filtering applications.

To support double buffering, all coefficients are stored in two buffers (Buffer A and B). When the ADC is running and adaptive filtering mode is turned on, setting the control bit Page 8, Reg 1,D(0)=1 switches the coefficient buffers at the next start of a sampling period. The bit reverts to 0 after the switch occurs. At the same time, the flag Page 8, Reg 1, D(1) toggles.

The flag in Page 8, Reg 1, D(1) indicates which of the two buffers is actually in use.

Page 8, Reg 1, D(1)=0: Buffer A is in use by the ADC engine, D(1)=1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the ADC, regardless to which buffer the coefficients have been written

ADC running	Flag, Page 8, Reg 1, D(1)	Coefficient Buffer in use	Writing to	Will update
No	0	None	C4, Buffer A	C4, Buffer A
No	0	None	C4, Buffer B	C4, Buffer B
Yes	0	Buffer A	C4, Buffer A	C4, Buffer B
Yes	0	Buffer A	C4, Buffer B	C4, Buffer B
Yes	1	Buffer B	C4, Buffer A	C4, Buffer A
Yes	1	Buffer B	C4, Buffer B	C4, Buffer A

2.3.3.4 Setup

The following discussion is intended to guide a system designer through the steps necessary to configure the TLV320DAC3203 ADC.

Step 1

The system clock source (master clock) and the targeted ADC sampling frequency must be identified.

The oversampling ratio (OSR) of the TLV320DAC3203 must be configured to match the properties of the digital microphone.

Based on the identified filter type and the required signal processing capabilities the appropriate processing block can be determined from the list of available processing blocks (PRB_R1 to PRB_R18) (See Table 2-5).

Based on the available master clock, the chosen OSR and the targeted sampling rate, the clock divider values NADC and MADC can be determined. If necessary the internal PLL will add a large degree of flexibility.

In summary, Codec_Clkin which is either derived directly from the system clock source or from the internal PLL, divided by MADC, NADC and AOSR, must be equal to the ADC sampling rate ADC_FS. The codec_clkin clock signal is shared with the DAC clock generation block.

CODEC_CLKIN = NADC*MADC*AOSR*ADC_FS

To a large degree NADC and MADC can be chosen independently in the range of 1 to 128. In general NADC should be as large as possible as long as the following condition can still be met:

MADC*AOSR/32 ≥ RC

RC is a function of the chosen processing block, and is listed in Table 2-5.

The common mode setting of the device is determined by the available analog power supply and the desired PowerTune mode, this common mode setting is shared across DAC (input common mode) and analog bypass path.

At this point the following device specific parameters are known:

PRB_Rx, AOSR, NADC, MADC, common mode setting

Additionally if the PLL is used the PLL parameters P, J, D and R are determined as well.

Step 2

Setting up the device via register programming:

The following list gives a sequence of items that must be executed between powering the device up and reading data from the device:

Define starting point:	Set register page to 0 Initiate SW Reset
Program Clock Settings	Program PLL clock dividers P,J,D,R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NADC Program and power up MADC Program OSR value Program the processing block to be used

At this point, at the latest, analog power supply must be applied to the device (via internal LDO or external)

Program Analog Blocks	Set register Page to 1 Disable coarse AVdd generation Enable Master Analog Power Control

A detailed example can be found in Chapter 4.

2.4 DAC

The TLV320DAC3203 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize performance, the TLV320DAC3203 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320DAC3203 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the TLV320DAC3203 features many options for signal conditioning and signal routing:

- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the TLV320DAC3203 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

The TLV320DAC3203 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

Table 2-13 gives an overview over all available processing blocks of the DAC channel and their properties.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for typical cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

Table 2-13. Overview – DAC Predefined Processing Blocks

Processing Block No.	Interpolation Filter	Channel	1st Order IIR Available	Num. of Biquads	DRC	3D	Beep Generator	Resource Class
PRB_P1[1]	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

(1) Default

2.4.1 Processing Blocks – Details

2.4.1.1 Three Biquads, Interpolation Filter A

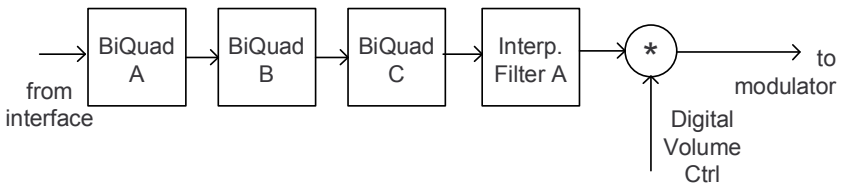

Figure 2-20. Signal Chain for PRB_P1 and PRB_P4

2.4.1.2 Six Biquads, First Order IIR, DRC, Interpolation Filter A or B

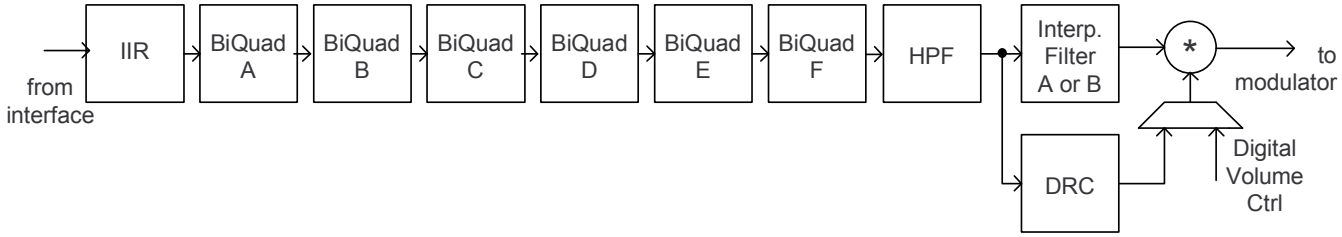

Figure 2-21. Signal Chain for PRB_P2, PRB_P5, PRB_P10 and PRB_P15

2.4.1.3 Six Biquads, First Order IIR, Interpolation Filter A or B

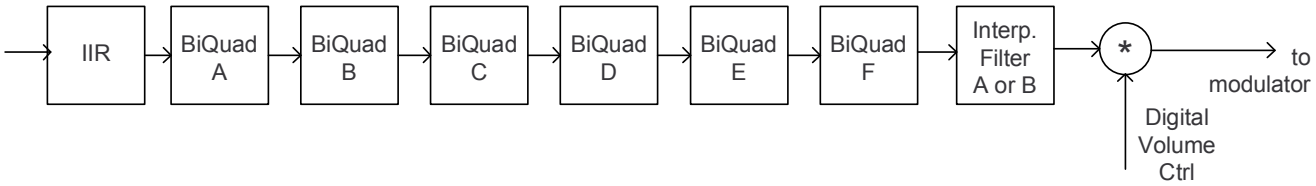

Figure 2-22. Signal Chain for PRB_P3, PRB_P6, PRB_P11 and PRB_P16

2.4.1.4 IIR, Interpolation Filter B or C

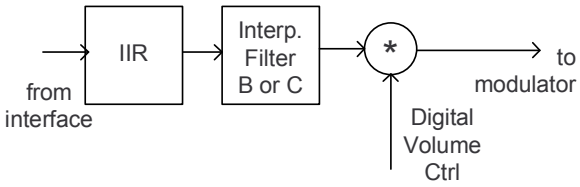

Figure 2-23. Signal Chain for PRB_P7, PRB_P12, PRB_P17 and PRB_P20

2.4.1.5 Four Biquads, DRC, Interpolation Filter B

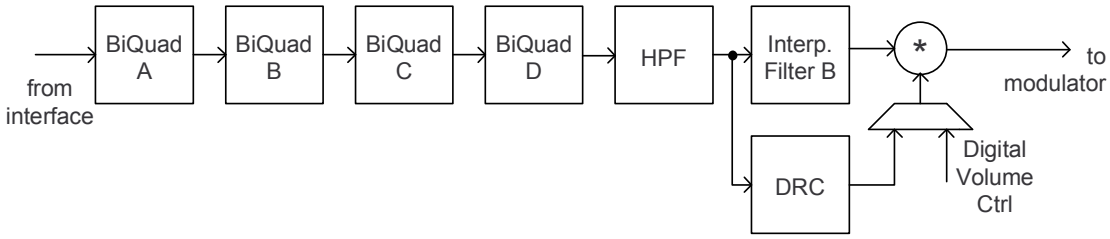

Figure 2-24. Signal Chain for PRB_P8 and PRB_P13

2.4.1.6 Four Biquads, Interpolation Filter B

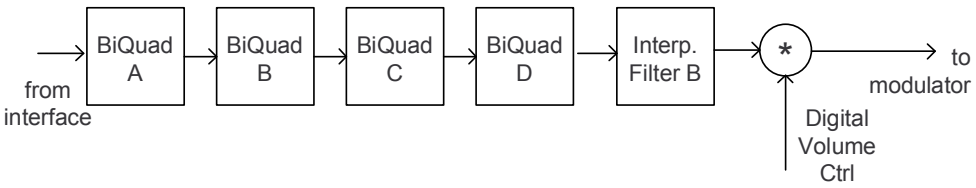

Figure 2-25. Signal Chain for PRB_P9 and PRB_P14

2.4.1.7 Four Biquads, First Order IIR, DRC, Interpolation Filter C

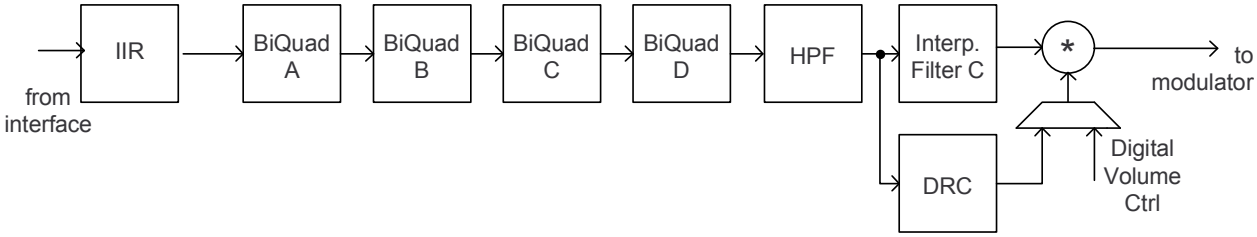

Figure 2-26. Signal Chain for PRB_P18 and PRB_P21

2.4.1.8 Four Biquads, First Order IIR, Interpolation Filter C

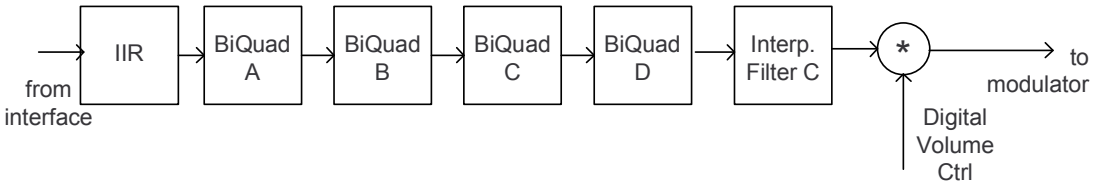

Figure 2-27. Signal Chain for PRB_P19 and PRB_P22

2.4.1.9 Two Biquads, 3D, Interpolation Filter A

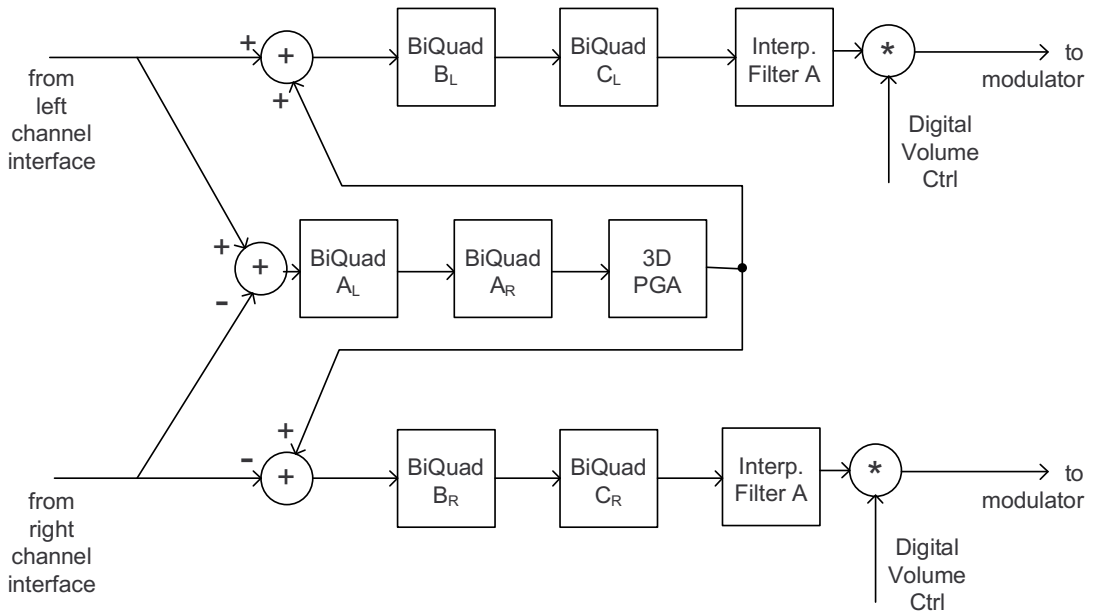

Figure 2-28. Signal Chain for PRB_P23

2.4.1.10 Five Biquads, DRC, 3D, Interpolation Filter A

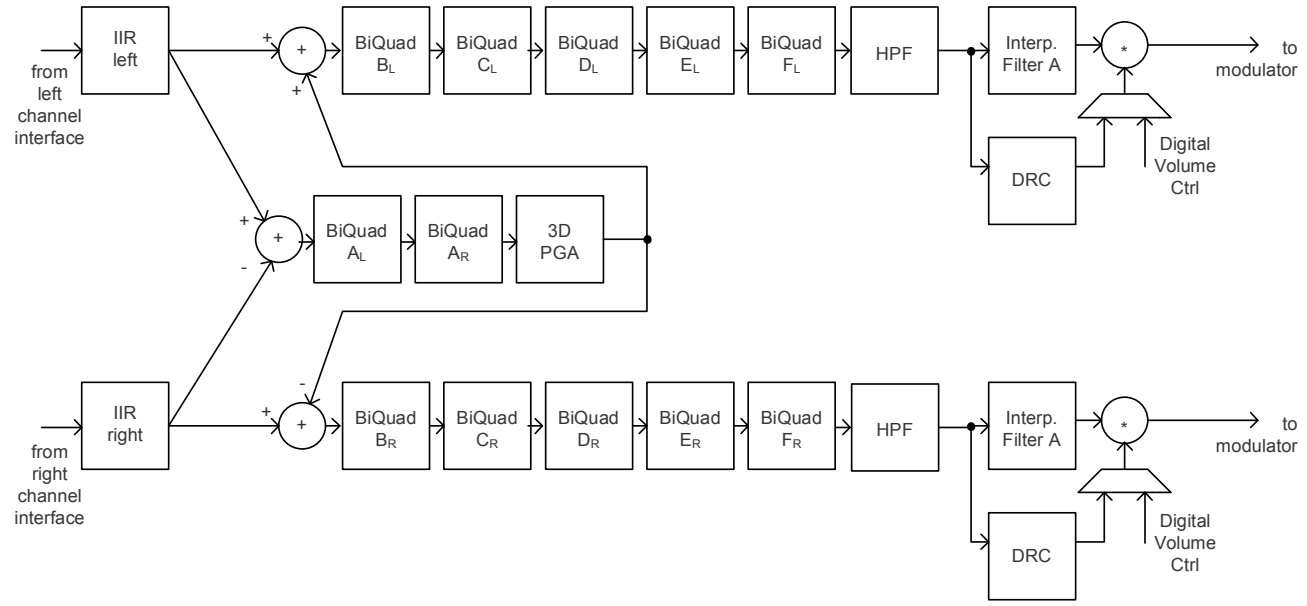

Figure 2-29. Signal Chain for PRB_P24

2.4.1.11 Five Biquads, DRC, 3D, Beep Generator, Interpolation Filter A

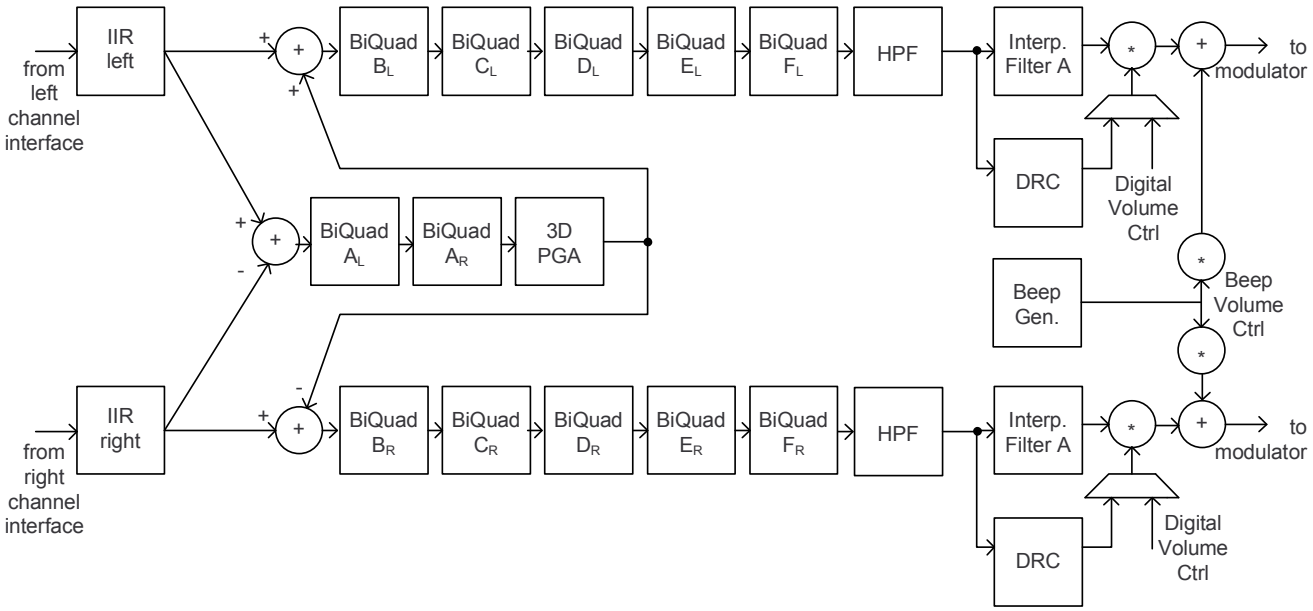

Figure 2-30. Signal Chain for PRB_P25

2.4.2 User Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. Up to 6 biquad sections are available for specific processing blocks.

The coefficients of the available filters are arranged as sequentially-indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched in real time. For more details on adaptive filtering please see Section 2.4.5.3.

The coefficients of these filters are each 24-bits wide, in two's-complement and occupy 3 consecutive 8-bit registers in the register space. For default values please see the default values tables in the Register Map section.

2.4.2.1 First Order IIR Section

The IIR is of first-order and its transfer function is given by

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \tag{9}$$

The frequency response for the first order IIR Section with default coefficients is flat. Details on DAC coefficient default values are given in Section 5.19.

Table 2-14. DAC IIR Filter Coefficients

Filter	Filter Coefficient	ADC Coefficient Left Channel	ADC Coefficient Right Channel
First order IIR	N0	C65 (Page 46, Registers 28,29,30)	C68 (Page 46, Registers 40,41,42)
	N1	C66 (Page 46, Registers 32,33,34)	C69 (Page 46, Registers 44,45,46)
	D1	C67 (Page 46, Registers 36,37,38)	V70 (Page 46, Registers 48,49,50)

2.4.2.2 Biquad Section

The transfer function of each of the Biquad Filters is given by

$$H(z) = \frac{N_0 + 2 * N_1 z^{-1} + N_2 z^{-2}}{2^{23} - 2 * D_1 z^{-1} - D_2 z^{-2}} \tag{10}$$

The frequency response for each biquad section with default coefficients is flat at a gain of 0dB. Details on DAC coefficient default values are given in Section 5.19.

Table 2-15. DAC Biquad Filter Coefficients

Filter	Coefficient	Left DAC Channel	Right DAC Channel
BIQUAD A	N0	C1 (Page 44, Registers 12,13,14)	C33 (Page 45, Registers 20,21,22)
	N1	C2 (Page 44, Registers 16,17,18)	C34 (Page 45, Registers 24,25,26)
	N2	C3 (Page 44, Registers 20,21,22)	C35 (Page 45, Registers 28,29,30)
	D1	C4 (Page 44, Registers 24,25,26)	C36 (Page 45, Registers 32,33,34)
	D2	C5 (Page 44, Registers 28,29,30)	C37 (Page 45, Registers 36,37,38)
BIQUAD B	N0	C6 (Page 44, Registers 32,33,34)	C38 (Page 45, Registers 40,41,42)
	N1	C7 (Page 44, Registers 36,37,38)	C39 (Page 45, Registers 44,45,46)
	N2	C8 (Page 44, Registers 40,41,42)	C40 (Page 45, Registers 48,49,50)
	D1	C9 (Page 44, Registers 44,45,46)	C41 (Page 45, Registers 52,53,54)
	D2	C10 (Page 44, Registers 48,49,50)	C42 (Page 45, Registers 56,57,58)
BIQUAD C	N0	C11 (Page 44, Registers 52,53,54)	C43 (Page 45, Registers 60,61,62)
	N1	C12 (Page 44, Registers 56,57,58)	C44 (Page 45, Registers 64,65,66)
	N2	C13 (Page 44, Registers 60,61,62)	C45 (Page 45, Registers 68,69,70)
	D1	C14 (Page 44, Registers 64,65,66)	C46 (Page 45, Registers 72,73,74)
	D2	C15 (Page 44, Registers 68,69,70)	C47 (Page 45, Registers 76,77,78)
BIQUAD D	N0	C16 (Page 44, Registers 72,73,74)	C48 (Page 45, Registers 80,81,82)
	N1	C17 (Page 44, Registers 76,77,78)	C49 (Page 45, Registers 84,85,86)
	N2	C18 (Page 44, Registers 80,81,82)	C50 (Page 45, Registers 88,89,90)
	D1	C19 (Page 44, Registers 84,85,86)	C51 (Page 45, Registers 92,93,94)

Table 2-15. DAC Biquad Filter Coefficients (continued)

Filter	Coefficient	Left DAC Channel	Right DAC Channel
	D2	C20 (Page 44, Registers 88,89,90)	C52 (Page 45, Registers 96,97,98)
BIQUAD E	N0	C21 (Page 44, Registers 92,93,94)	C53 (Page 45, Registers 100,101,102)
	N1	C22 (Page 44, Registers 96,97,98)	C54 (Page 45, Registers 104,105,106)
	N2	C23 (Page 44, Registers 100,101,102)	C55 (Page 45, Registers 108,109,110)
	D1	C24 (Page 44, Registers 104,105,106)	C56 (Page 45, Registers 112,113,114)
	D2	C25 (Page 44, Registers 108,109,110)	C57 (Page 45, Registers 116,117,118)
BIQUAD F	N0	C26 (Page 44, Registers 112,113,114)	C58 (Page 45, Registers 120,121,122)
	N1	C27 (Page 44, Registers 116,117,118)	C59 (Page 45, Registers 124,125,126)
	N2	C28 (Page 44, Registers 120,121,122)	C60 (Page 46, Registers 8,9,10)
	D1	C29 (Page 44, Registers 124,125,126)	C61 (Page 46, Registers 12,13,14)
	D2	C30 (Page 45, Registers 8,9,10)	C62 (Page 46, Registers 16,17,18)

2.4.2.2.1 3D-PGA

The 3D-PGA attenuation block as used in the processing blocks PRB_P23, PRB_P24 and PRB_P25 can be programmed in the range of -1.0 to +1.0. A value of -1.0 corresponds to 0x7FFFFF in DAC coefficient C32 (Page 45, Register 16,17 and 18). A value of 1.0 corresponds to 0x800000 in coefficient C32.

2.4.3 Interpolation Filter Characteristics

2.4.3.1 Interpolation Filter A

Filter A is designed for an f_S up to 48ksps with a flat passband of 0kHz–20kHz.

Table 2-16. DAC Interpolation Filter A, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45f_S	±0.015	dB
Filter Gain Stop Band	0.55… 7.455f_S	–65	dB
Filter Group Delay		21 / f_S	s

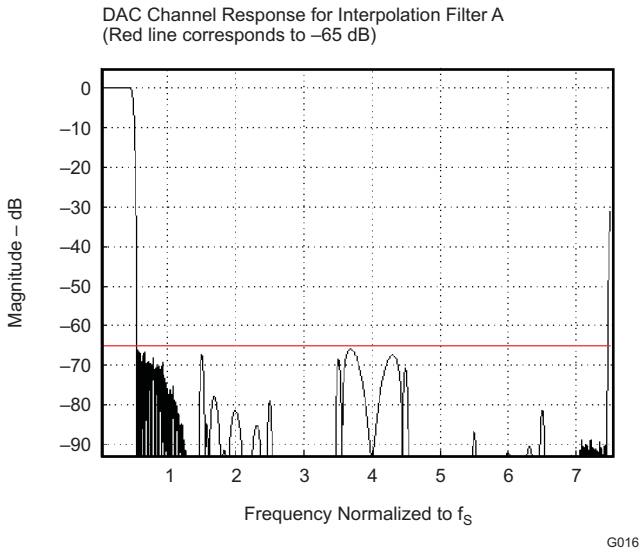

Figure 2-31. DAC Interpolation Filter A, Frequency Response

2.4.3.2 Interpolation Filter B

Filter B is specifically designed for an f_S of above 96ksps. Thus, the flat pass-band region easily covers the required audio band of 0-20kHz.

Table 2-17. DAC Interpolation Filter B, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.45f_S	±0.015	dB
Filter Gain Stop Band	0.55… 3.45f_S	–58	dB
Filter Group Delay		18 / f_S	s

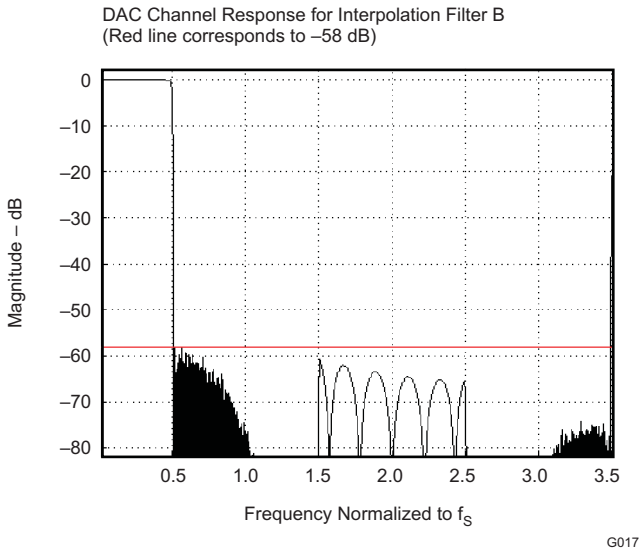

Figure 2-32. Channel Interpolation Filter B, Frequency Response

2.4.3.3 Interpolation Filter C

Filter C is specifically designed for the 192ksps mode. The pass band extends up to 0.40 * f_S (corresponds to 80kHz), more than sufficient for audio applications.

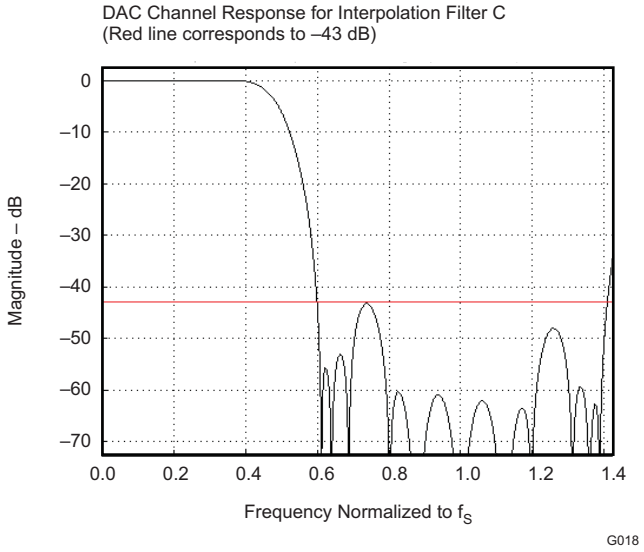

Figure 2-33. DAC Interpolation Filter C, Frequency Response

Table 2-18. DAC Interpolation Filter C, Specification

Parameter	Condition	Value (Typical)	Units
Filter Gain Pass Band	0 … 0.35f_S	±0.03	dB
Filter Gain Stop Band	0.60… 1.4f_S	–43	dB
Filter Group Delay		13 / f_S	s

2.4.4 DAC Gain Setting

2.4.4.1 Digital Volume Control

The TLV320DAC3203 signal processing blocks incorporate a digital volume control block that can control the volume of the playback signal from +24dB to –63.5dB in steps of 0.5dB. These can be controlled by writing to Page 0, Register 65 and 66. The volume control of left and right channels by default can be controlled independently, however by programming Page 0, Reg 64, D(1:0), they can be made interdependent. The volume changes are soft-stepped in steps of 0.5dB to avoid audible artifacts during gain change. The rate of soft-stepping can be controlled by programming Page 0, Reg 63, D(1:0) to either one step per frame (DAC_FS) or one step per 2 frames. The soft-stepping feature can also be entirely disabled. During soft-stepping the value of the actual applied gain would differ from the programmed gain in register. The TLV320DAC3203 gives a feedback to the user in form of register readable flag to indicate that soft-stepping is currently in progress. The flags for left and right channels can be read back by reading Page 0, Reg 38, Bits D4 and D0 respectively. A value of 0 in these flags indicates a soft-stepping operation in progress, and a value of 1 indicates that soft-stepping has completed. A soft-stepping operation comes into effect during

a. power-up, when the volume control soft-steps from –63.5dB to programmed gain value,
b. volume change by user when DAC is powered up, and
c. power-down, when the volume control block soft-steps to –63.5dB before powering down the channel.

2.4.4.2 Dynamic Range Compression

Typical music signals are characterized by crest factors, the ratio of peak signal power to average signal power, of 12dB or more. To avoid audible distortion due to clipping of peak signals, the gain of the DAC channel must be adjusted to prevent hard clipping of peak signals. As a result, during nominal periods, the applied gain is low, causing the perception that the signal is not loud enough. To overcome this problem, the DRC in the TLV320DAC3203 continuously monitors the output of the DAC Digital Volume control to detect its power level w.r.t. 0dBFS. When the power level is low, it increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. The resulting sound can be more pleasing to the ear as well as sounding louder during nominal periods.

The DRC functionality in the TLV320DAC3203 is implemented by a combination of Processing Blocks in the DAC channel as described in Section 2.4.1.

The DRC can be disabled by writing into Page 0, Reg 68, D(6:5).

The DRC works on the filtered version of the input signal. The input signals have no audio information at DC and extremely low frequencies; however they can significantly influence the energy estimation function in DRC. To remove the DC content, the signal is passed through a first-order IIR filter configured as high-pass filter. The frequency response of this high-pass filter is given by

$$H_{HPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \tag{11}$$

The default values of the coefficients implement a cut-off at 0.000083*DAC_FS (or 3.9Hz at 48ksps sampling rate).

Most of the information about signal energy is concentrated in the low frequency region of the input signal. To calculate the energy in audio signal the output of high-pass filter above is low-pass filtered by a first-order IIR filter configured for a low-pass frequency response. The frequency response of the low-pass filter is given by

$$H_{LPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{23} - D_1 z^{-1}} \quad (12)$$

The default values of the coefficients implement a cut-off at 0.000164*DAC_FS (or 7.9Hz at 48ksps sampling rate).

The coefficients for these filters are 24-bits wide in two's-complement and are user programmable through register write as given in Table 2-19, and coefficient default values are summarized in Section 5.19.

Table 2-19. DRC HPF and LPF Coefficients

Coefficient	Location
HPF N0	C71 Page 46, Register 52 to 55
HPF N1	C72 Page 46, Register 56 to 59
HPF D1	C73 Page 46, Register 60 to 63
LPF N0	C74 Page 46, Register 64 to 67
LPF N1	C75 Page 46, Register 68 to 71
LPF D1	C76 Page 46, Register 72 to 75

The gain in the DAC Digital Volume Control is controlled by Page 0, Register 65 and 66. When the DRC is enabled, the applied gain is a function of the Digital Volume Control register setting and the output of the DRC.

The DRC parameters are described in sections that follow.

2.4.4.2.1 DRC Threshold

The DRC Threshold represents the level of the DAC playback signal at which the gain compression becomes active. The output of the digital volume control in the DAC is compared with the set threshold. The threshold value is programmable by writing to register Page 0, Register 68, D(4:2). The Threshold value can be adjusted between –3dBFS to –24dBFS in steps of 3dB. Keeping the DRC Threshold value too high may not leave enough time for the DRC block to detect peaking signals, and can cause excessive distortion at the outputs. Keeping the DRC Threshold value too low can limit the perceived loudness of the output signal.

The recommended DRC-Threshold value is –24dB.

When the output signal exceeds the set DRC Threshold, the interrupt flag bits at Page 0, Register 44, D(3:2) are updated. These flag bits are 'sticky' in nature, and are reset only after they are read back by the user. The non-sticky versions of the interrupt flags are also available at Page 0, Register 46, D(3:2).

2.4.4.2.2 DRC Hysteresis

DRC Hysteresis is programmable by writing to Page 0, Register 68, D(1:0) with values between 0dB and 3dB in steps of 1dB. DRC Hysteresis is a programmable window around the programmed DRC Threshold that must be exceeded for a disabled DRC to become enabled, or an enabled DRC to become disabled. For example, if the DRC Threshold is set to –12dBFS and DRC Hysteresis is set to 3dB, then if the gain compressions in the DRC is inactive, the output of the DAC Digital Volume Control must exceed –9dBFS before gain compression due to the DRC is activated. Similarly, when the gain compression in the DRC is active, the output of the DAC Digital Volume Control must fall below –15dBFS for gain compression in the DRC to be deactivated. The DRC Hysteresis feature prevents the rapid activation and de-activation of gain compression in the DRC in cases when the output of DAC Digital Volume Control rapidly fluctuates in a narrow region around the programmed DRC Threshold. Programming the DRC Hysteresis as 0dB disables the hysteresis action.

Recommended Value of DRC Hysteresis is 3dB.

2.4.4.2.3 DRC Hold

The DRC Hold function slows the start of decay for a specified period of time in response to a decrease in energy level. To minimize audible artifacts, it is recommended to set the DRC Hold time to 0 through programming Page 0, Register 69, D(6:3) = 0000.

2.4.4.2.4 DRC Attack Rate

When the output of the DAC Digital Volume Control exceeds the programmed DRC Threshold, the gain applied in the DAC Digital Volume Control is progressively reduced to avoid the signal from saturating the channel. This process of reducing the applied gain is called Attack. To avoid audible artifacts, the gain is reduced slowly with a rate equaling the Attack Rate programmable via Page 0, Register 70, D(7:4). Attack Rates can be programmed from 4dB gain change per sample period (1 / DAC_FS) to 1.2207e-5dB gain change per sample period.

Attack Rates should be programmed such that before the output of the DAC Digital Volume control can clip, the input signal should be sufficiently attenuated. High Attack Rates can cause audible artifacts, and too-slow Attack Rates may not prevent the input signal from clipping.

The recommended DRC Attack Rate value is 1.9531e-4 dB per sample period.

2.4.4.2.5 DRC Decay Rate

When the DRC detects a reduction in output signal swing beyond the programmed DRC Threshold, the DRC enters a Decay state, where the applied gain in Digital Volume Control is gradually increased to programmed values. To avoid audible artifacts, the gain is slowly increased with a rate equal to the Decay Rate programmed through Page 0, Register 70, D(3:0). The Decay Rates can be programmed from 1.5625e-3dB per sample period to 4.7683e-7dB per sample period. If the Decay Rates are programmed too high, then sudden gain changes can cause audible artifacts. However, if it is programmed too slow, then the output may be perceived as too low for a long time after the peak signal has passed.

The recommended Value of DRC Decay Rate is 2.4414e-5 dB per sample period.

2.4.4.2.6 Example Setup for DRC

- PGA Gain = 12dB
- Threshold = -24dB
- Hysteresis = 3dB
- Hold time = 0ms
- Attack Rate = 1.9531e-4 dB per sample period
- Decay Rate = 2.4414e-5 dB per sample period

Script

```
w 30 00 00    #Go to Page 0
w 30 41 18    #DAC => 12 db gain left
w 30 42 18    #DAC => 12 db gain right
w 30 44 7F    #DAC => DRC Enabled for both channels, Threshold = -24 db, Hysteresis = 3 dB
w 30 45 00    #DRC Hold = 0 ms, Rate of Changes of Gain = 0.5 dB/Fs'
w 30 46 B6    #Attack Rate = 1.9531e-4 dB/Frame , DRC Decay Rate =2.4414e-5 dB/Frame
w 30 00 2E    #Go to Page 46
w 30 34 7F AB 00 00 80 55 00 00 7F 56 00 00    #DRC HPF
w 30 40 00 11 00 00 00 11 00 00 7F DE 00 00    #DRC LPF
```

2.4.5 DAC Special Functions

2.4.5.1 Beep Generation

A special function has also been included in the processing block PRB_P25 for generating a digital sine-wave signal that is sent to the DAC. This signal is intended for generating key-click sounds for user feedback. A default value for the sine-wave frequency, sine burst length, and signal magnitude is kept in the Tone Generator Registers Page 0, Registers 71 through 79. The sine wave generator is very flexible, and is completely register programmable via 9 registers of 8 bits each to provide many different sounds.

Two registers are used for programming the 16-bit, two's-complement, sine-wave coefficient (Page 0, Registers 76 and 77). Two other registers program the 16-bit, two's-complement, cosine-wave coefficient (Page 0, Registers 78 and 79). This coefficient resolution allows virtually any frequency of sine wave in the audio band to be generated up to DAC_FS / 2.

The sine-wave coefficient can be calculated by sine = round(sin(2*pi*Fin/Fs)*2^15); Fin is the beep frequency. The sine should not be zero.

The cosine-wave coefficient can be calculated by cosine = round(cos(2*pi*Fin/Fs)*2^15); Fin is the beep frequency. The cosine should not be zero.

Three registers are used to control the length of the sine burst waveform which are located on Page 0, Registers 73, 74, and 75. The resolution (bit) in the registers of the sine burst length is one sample time, so this allows great control on the overall time of the sine burst waveform. This 24-bit length timer supports 16,777,215 sample times. (For example if DAC_FS is set at 48kHz, and the registers combined value equals 96000d (01770h), then the sine burst would last exactly two seconds.)

The length of beep in seconds is given by Beep Length = floor(Cycles * Fs / Fin) ; Fin is the beep frequency and Cycles is the value of 24-bit timer (Page-0, Register 73, 74 and 75).

Separate registers independently control the Left sine-wave volume and the Right sine-wave volume. The 6-bit digital volume control allows level control of 0dB to –63dB in one-dB steps. The left-channel volume is controlled by writing to Page 0, Register 71, D(5:0). The right-channel volume is controlled by Page 0, Register 72, D(5:0). A master volume control for the left and right channel of the beep generator can be set up using Page 0, Register 72, D(7:6). The default volume control setting is 0dB, the tone generator maximum-output level.

To play back the sine wave, the DAC must be configured with regards to clock setup and routing. The sine wave starts by setting the Beep Generator Enable Bit (Page 1, Register 71, D(7) = 1). After the sine wave has played for its predefined time period this bit automatically resets back to 0. While the sine wave is playing, the parameters of the beep generator cannot be changed. To stop the sine wave before the predefined time period expires, set the Beep Generator Enable Bit to 0.

To insert a beep in the middle of an already playing signal over DAC, the following sequence is recommended. Before the beep is desired, the user should program the desired beep frequency, volume and length in the configuration registers. When a beep is desired, the example configuration script should be used.

```
w 30 00 00          # change to Page 0
w 30 40 0C          # mute DAC's
f  30 26 xxx1xxx1            # wait for DAC gain flag to be set
w 30 0B 02          # power down NDAC divider
w 30 47 80          # enable beep generator with left channel volume = 0dB, volume level could
be different as per requirement
w 30 0B 82          # power up NDAC divider, in this specific example NDAC=2, could be different
value as per overall setup
w 30 40 00          # un-mute DAC to resume playing audio
```

NOTE: In this scheme, the audio signal on the DAC is temporarily muted to enable beep generation. Because this requires powering down of NDAC clock divider, the DAC_CLK or DAC_MOD_CLK should not be used for generation of I^2S clocks.

2.4.5.2 Digital Auto Mute

The TLV320DAC3203 also incorporates a special feature where the DAC channel is auto-muted when a continuous stream of DC-input is detected. By default, this feature is disabled, and is enabled by writing a non-zero value into Page 0, Register 64, D(6:4). This non-zero value controls the duration of the continuous stream of DC-input before the auto-mute feature takes effect. This feature is especially helpful for eliminating high-frequency noise power from being delivered into the load during silent periods of speech or music.

2.4.5.3 Adaptive Filtering

When the DAC is running, the user-programmable filter coefficients are locked and cannot be accessed for either read or write.

However the TLV320DAC3203 offers an adaptive filter mode as well. Setting Register Page 44, Reg 1, Bit D(2) = 1 turns on double buffering of the coefficients. In this mode, filter coefficients can be updated through the host, and activated without stopping and restarting the DAC. This enables advanced adaptive filtering applications.

In the double-buffering scheme, all coefficients are stored in two buffers (Buffers A and B). When the DAC is running and adaptive filtering mode is turned on, setting the control bit Page 44, Register 1, D(0) = 1 switches the coefficient buffers at the next start of a sampling period. This bit resets back to 0 after the switch occurs. At the same time, the flag (Page 44, Reg 1, D(1)) toggles.

The flag in Page 44, Register 1, D(1) indicates which of the two buffers is actually in use.

Page 44, Register 1, D(1) = 0: Buffer A is in use by the DAC engine, Bit D(1) = 1: Buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the DAC, regardless to which buffer the coefficients have been written.

DAC running	Page 44, Reg 1, Bit D1	Coefficient Buffer in use	Writing to	Will update
No	0	None	C1, Buffer A	C1, Buffer A
No	0	None	C1, Buffer B	C1, Buffer B
Yes	0	Buffer A	C1, Buffer A	C1, Buffer B
Yes	0	Buffer A	C1, Buffer B	C1, Buffer B
Yes	1	Buffer B	C1, Buffer A	C1, Buffer A
Yes	1	Buffer B	C1, Buffer B	C1, Buffer A

The user programmable coefficients C1 to C70 are defined on Pages 44, 45 and 46 for Buffer A and Pages 62, 63 and 64 for Buffer B.

2.4.6 DAC Setup

This section lists the steps necessary to configure the TLV320DAC3203 DAC.

Step 1

Determine the system clock source (master clock) and the targeted DAC sampling frequency.

Choose the targeted performance. This drives the choice of the decimation filter type (A, B or C) and DOSR value.

Use Filter A for 48kHz high-performance operation; DOSR must be a multiple of 8.

Use Filter B for up to 96kHz operations; DOSR must be a multiple of 4.

Use Filter C for up to 192kHz operations; DOSR must be a multiple of 2.

In all cases the DOSR range is limited by the following condition:

2.8MHz < DOSR * DAC_FS < 6.2MHz

Based on the identified filter type and the required signal processing capabilities, the appropriate processing block is determined from the list of available processing blocks (PRB_P1 to PRB_P25).

Based on the available master clock, the chosen DOSR and the targeted sampling rate, the clock divider values NDAC and MDAC are calculated. If necessary, the internal PLL can add a large degree of flexibility.

In summary, codec_clkin (derived directly from the system clock source or from the internal PLL) divided by MDAC, NDAC and DOSR must be equal to the DAC sampling rate DAC_FS. The codec_clkin clock signal is shared with the ADC clock generation block.

CODEC_CLKIN = NDAC * MDAC * DOSR * DAC_FS

To a large degree, NDAC and MDAC can be chosen independently in the range of 1 to 128. In general, NDAC should be as large as possible as long as the following condition can still be met:

MDAC * DOSR / 32 ≥ RC

RC is a function of the chosen processing block and is listed in Table 2-13.

The common-mode voltage setting of the device is determined by the available analog power supply. This common-mode (input common-mode) value is common across the ADC, DAC and analog bypass path. The output common-mode setting is determined by the available analog power supplies (AV_{DD} and) and the desired output-signal swing.

At this point the following device specific parameters are known:

PRB_Px, DOSR, NDAC, MDAC, input and output common-mode values

If the PLL is used, the PLL parameters P, J, D and R are determined as well.

Step 2

Setting up the device via register programming:

The following list gives a sequence of items that must be executed in the time between powering the device up and reading data from the device:

Define starting point:	Set register page to 0 Initiate SW Reset
Program Clock Settings	Program PLL clock dividers P,J,D,R (if PLL is necessary) Power up PLL (if PLL is necessary) Program and power up NDAC Program and power up MDAC Program OSR value Program I^2S word length if required (for example, 20bit) Program the processing block to be used

At this point, at the latest, the analog power supply must be applied to the device

Program Analog Blocks	Set register Page to 1 Disable coarse AV_{DD} generation Enable Master Analog Power Control Program Common Mode voltage Program Reference fast charging Program Headphone specific depop settings (in case of headphone driver used) Program routing of DAC output to the output amplifier (headphone) Unmute and set gain of output driver Power up output driver

Apply waiting time determined by the de-pop settings and the soft-stepping settings of the driver gain or poll Page 1 , Register 63

Power Up DAC	Set register Page to 0 Power up DAC Channels Unmute digital volume control

2.5 PowerTune

The TLV320DAC3203 features PowerTune, a mechanism to balance power-versus-performance trade-offs at the time of device configuration. The device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application.

2.5.1 PowerTune Modes

2.5.1.1 DAC - Programming PTM_P1 to PTM_P4

On the playback side, the performance is determined by a combination of register settings and the audio data word length applied. For the highest performance setting (PTM_P4), an audio-data word length of 20 bits is required, while for the modes PTM_P1 to PTM_P3 a word length of 16 bits is sufficient.

	PTM_P1	PTM_P2	PTM_P3	PTM_P4
Pg 1, Reg 3, D(4:2)	0x2	0x1	0x0	0x0
Pg 1, Reg 4, D(4:2)	0x2	0x1	0x0	0x0
Audio Data word length	16 bits	16 bits	16 bits	20 or more bits
Pg 0, Reg 27, D(5:4)	0x0	0x0	0x0	0x1, 0x2, 0x3

2.5.1.2 Processing Blocks

The choice of processing blocks, PRB_P1 to PRB_P25 for playback and PRB_R1 to PRB_R18 for recording, also influences the power consumption. In fact, the numerous processing blocks have been implemented to offer a choice between power-optimization and configurations with more signal-processing resources.

2.5.2 DAC Power Consumption

The tables in this section give recommendations for various DAC PowerTune modes. Typical performance and power-consumption numbers are listed.

All measurements were taken with the PLL turned off, no signal is present, and the DAC modulator is fully running.

2.5.2.1 DAC, Stereo, 48kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 128, Processing Block = PRB_P8 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		75	211	375	375	100	281	500	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.4	93.4	97.0	96.7	90.7	95.3	99.2	100.1	dB
	Power consumption[2]	9.7	10.6	11.3	11.3	9.7	10.6	11.3	11.3	mW
	Power consumption[3]	8.1	9.0	9.7	9.7	8.1	9.0	9.7	9.7	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .
(2) Measured data using PRB_P8.
(3) Calculated data for PRB_P7.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	0
PRB_P2	A	+3.1
PRB_P3	A	+1.6
PRB_P7	B	–1.6
PRB_P9	B	0
PRB_P10	B	+1.6
PRB_P11	B	–0.8
PRB_P23	A	0
PRB_P24	A	+3.1
PRB_P25	A	+3.1

2.5.2.2 DAC, Stereo, 48kHz, Lowest Power Consumption

Using its full potential, the device can be used with even lower power consumption than shown in the tabulated PowerTune information. 94dB SNR, 48kHz stereo playback to the headphone amplifier outputs can be achieved with a measured power consumption of 4.1mW. For more information on the setup of such modes please see the product folder of the device at www.ti.com.

DOSR = 64, Interpolation Filter B, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V PRB_P8 PTM_P1	CM = 0.9V AVdd=1.8V PRB_P8 PTM_P1	CM = 0.75V AVdd=1.5V PRB_P7 PTM_P4	UNIT
0dB full scale[1]		75	100	375	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	87.8	90.4	97.8	dB
	Power consumption[2]	5.3	6.0	5.9	mW
	Power consumption[3]	4.5	5.2	5.1	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .
(2) Measured data using PRB_P8.
(3) Calculated data for PRB_P7.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)[1]
PRB_P1	A	0
PRB_P2	A	+1.5
PRB_P3	A	+0.8
PRB_P7	B	–0.8
PRB_P9	B	0
PRB_P10	B	+0.8
PRB_P11	B	0
PRB_P23	A	0
PRB_P24	A	+1.5
PRB_P25	A	+1.5

(1) Estimated power change is w.r.t. PRB_P8.

2.5.2.3 DAC, Mono, 48kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 128, Processing Block = PRB_P13 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		75	211	375	375	100	281	500	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.6	93.1	97.1	97.0	91.1	95.3	99.9	99.8	dB
	Power consumption[2]	6.1	6.5	6.9	6.9	6.1	6.5	6.9	6.9	mW
	Power consumption[3]	5.3	5.7	6.1	6.1	5.3	5.7	6.1	6.1	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .
(2) Measured data using PRB_P13.
(3) Calculated data for PRB_P12.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change(mW)
PRB_P4	A	0
PRB_P5	A	+1.6
PRB_P6	A	+1.6
PRB_P12	B	–0.8
PRB_P14	B	0
PRB_P15	B	+1.6
PRB_P16	B	0

2.5.2.4 DAC, Mono, 48kHz, Lowest Power Consumption

DOSR = 64, Processing Block = PRB_P13 (Interpolation Filter B), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		75	100	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.7	91.5	dB
	Power consumption[2]	3.3	3.7	mW
	Power consumption[3]	2.9	3.3	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .
(2) Measured data using PRB_P13.
(3) Calculated data for PRB_P12.

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P4	A	0
PRB_P5	A	+0.8
PRB_P6	A	+0.8
PRB_P12	B	–0.4
PRB_P14	B	0
PRB_P15	B	+0.8
PRB_P16	B	0

2.5.2.5 DAC, Stereo, 8kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 768, Processing Block = PRB_P7 (Interpolation Filter B)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale		75	211	375	375	100	281	500	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale[1]	88.3	93.3	97.7	98.0	90.5	95.3	99.2	99.7	dB
	Power consumption	6.8	7.8	8.5	8.5	6.8	7.8	8.5	8.5	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	+0.3
PRB_P2	A	+0.8
PRB_P3	A	+0.5

Processing Block	Filter	Est. Power Change (mW)
PRB_P8	B	+0.3
PRB_P9	B	+0.3
PRB_P10	B	+0.5
PRB_P11	B	+0.3
PRB_P23	A	+0.3
PRB_P24	A	+0.8
PRB_P25	A	+0.8

2.5.2.6 DAC, Stereo, 8kHz, Lowest Power Consumption

DOSR = 384, Processing Block = PRB_P7 (Interpolation Filter B), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		75	100	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.4	90.7	dB
	Power consumption	3.9	4.6	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P1	A	+0.1
PRB_P2	A	+0.4
PRB_P3	A	+0.3
PRB_P8	B	+0.1
PRB_P9	B	+0.1
PRB_P10	B	+0.3
PRB_P11	B	+0.1
PRB_P23	A	+0.1
PRB_P24	A	+0.4
PRB_P25	A	+0.4

2.5.2.7 DAC, Mono, 8kHz, Highest Performance, DVdd = 1.8V, AVdd = 1.8V

DOSR = 768, Processing Block = PRB_P4 (Interpolation Filter A)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		75	211	375	375	100	281	500	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	89.1	92.6	97.0	96.8	91.0	95.0	99.4	100.5	dB
	Power consumption	4.7	5.2	5.5	5.5	4.7	5.2	5.5	5.5	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P5	A	+0.3
PRB_P6	A	+0.3
PRB_P12	B	–0.1

Processing Block	Filter	Est. Power Change (mW)
PRB_P13	B	0
PRB_P14	B	0
PRB_P15	B	+0.3
PRB_P16	B	0

2.5.2.8 DAC, Mono, 8kHz, Lowest Power Consumption

DOSR = 384, Processing Block = PRB_P4 (Interpolation Filter A), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		75	100	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.4	91.1	dB
	Power consumption	2.5	2.9	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P5	A	+0.1
PRB_P6	A	+0.1
PRB_P12	B	–0.1
PRB_P13	B	0
PRB_P14	B	0
PRB_P15	B	+0.1
PRB_P16	B	0

2.5.2.9 DAC, Stereo, 192kHz, DVdd = 1.8V, AVdd = 1.8V

DOSR = 32, Processing Block = PRB_P17 (Interpolation Filter C)

		Device Common Mode Setting = 0.75V				Device Common Mode Setting = 0.9V				
		PTM_P1	PTM_P2	PTM_P3	PTM_P4	PTM_P1	PTM_P2	PTM_P3	PTM_P4	UNIT
0dB full scale[1]		75	211	375	375	100	281	500	500	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.3	92.1	96.4	97.2	90.7	94.6	99.3	99.7	dB
	Power consumption	11.3	12.3	13.0	13.1	11.3	12.3	13.0	13.1	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P18	C	+9.3
PRB_P19	C	+3.1

2.5.2.10 DAC, Stereo, 192kHz, Lowest Power Consumption

DOSR = 16, Processing Block = PRB_P17 (Interpolation Filter C), PowerTune Mode = PTM_P1, DVdd = 1.26V

		CM = 0.75V AVdd=1.5V	CM = 0.9V AVdd=1.8V	UNIT
0dB full scale[1]		75	100	mV_{RMS}
HP out (32Ω load)	Effective SNR w.r.t. 0dB full scale	88.3	90.6	dB
	Power consumption	6.0	6.7	mW

(1) Reduced 0dB full-scale swing can be compensated by applying appropriate gain in the output drivers see .

Alternative processing blocks:

Processing Block	Filter	Est. Power Change (mW)
PRB_P18	C	+4.5
PRB_P19	C	+1.5

2.6 Audio Digital I/O Interface

Audio data flows between the host processor and the TLV320DAC3203 on the digital audio data serial interface, or audio bus. This very flexible bus includes left or right-justified data options, support for I^2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master-slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320DAC3203 can be configured for left or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30. The number of bit-clock pulses in a frame may need adjustment to accommodate various word lengths, and to support the case when multiple TLV320DAC3203s may share the same audio bus.

The TLV320DAC3203 also includes a feature to offset the position of start of data transfer with respect to the word-clock. Control the offset in terms of number of bit-clocks by programming Page 0, Register 28.

The TLV320DAC3203 also has the feature to invert the polarity of the bit-clock used to transfer the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. Page 0, Register 29, D(3) configures bit clock polarity.

The TLV320DAC3203 further includes programmability (Page 0, Register 27, D(0)) to place the DOUT line into a hi-Z (3-state) condition during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the TLV320DAC3203, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This intermittent clock operation reduces power consumption. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This continuous clock feature is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

2.6.1 Right Justified Mode

The Audio Interface of the TLV320DAC3203 can be put into Right Justified Mode by programming Page 0, Register 27, D(7:6) = 10b. In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

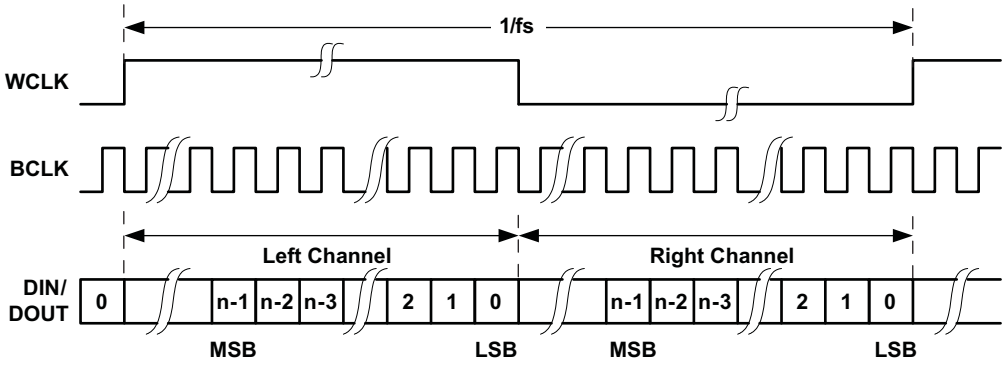

Figure 2-34. Timing Diagram for Right-Justified Mode

For Right-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data.

2.6.2 Left Justified Mode

The Audio Interface of the TLV320DAC3203 can be put into Left Justified Mode by programming Page 0, Register 27, D(7:6) = 11b. In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

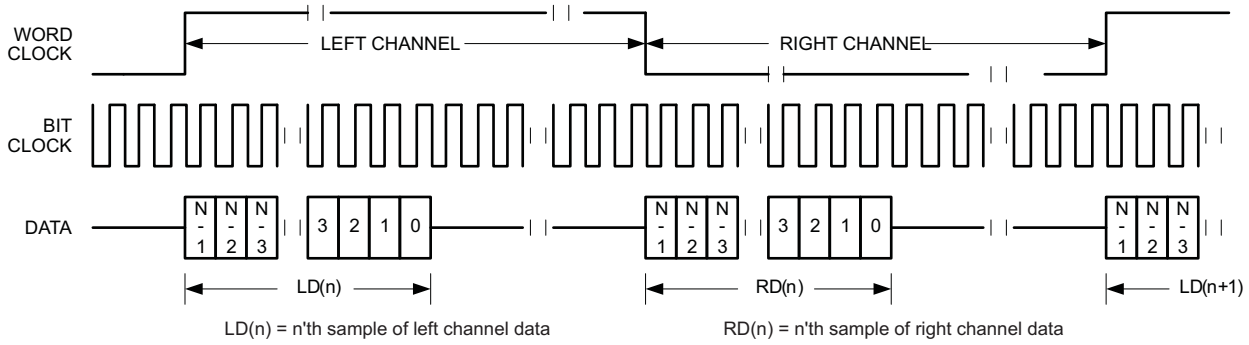

Figure 2-35. Timing Diagram for Left-Justified Mode

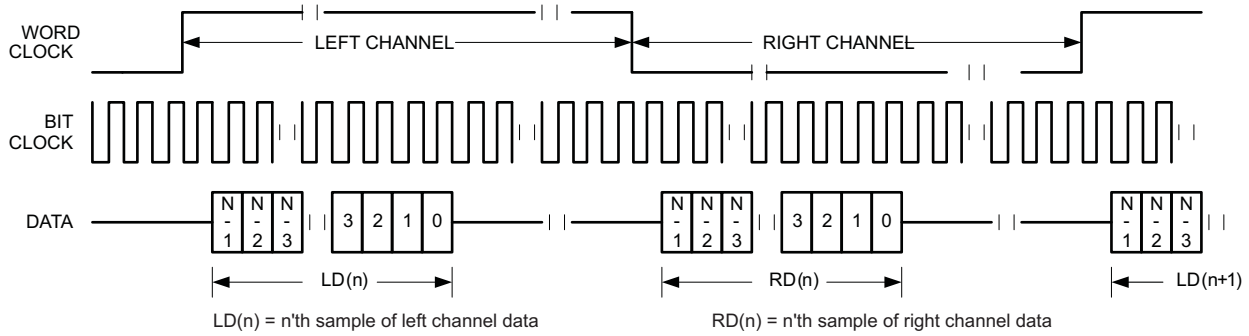

Figure 2-36. Timing Diagram for Left-Justified Mode with Offset = 1

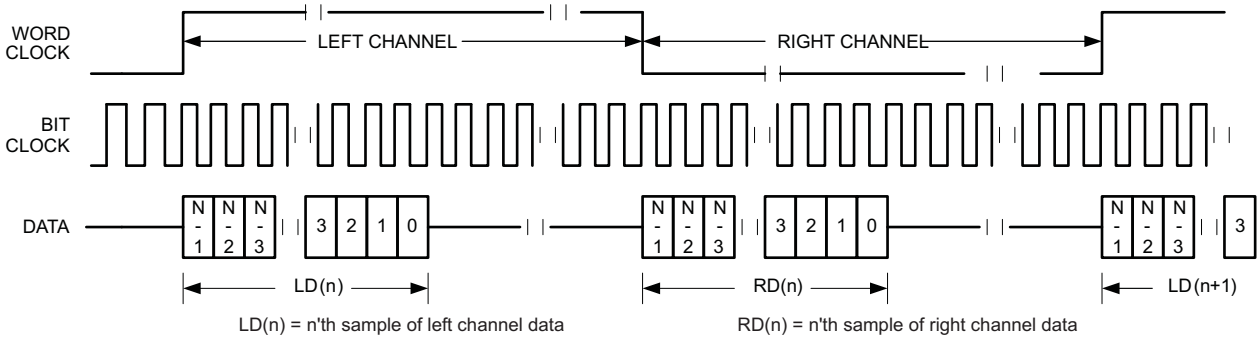

Figure 2-37. Timing Diagram for Left-Justified Mode with Offset = 0 and inverted bit clock

For Left-Justified mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also, the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

2.6.3 I²S Mode

The Audio Interface of the TLV320DAC3203 can be put into I²S Mode by programming Page 0, Register 27, D(7:6) = to 00b. In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

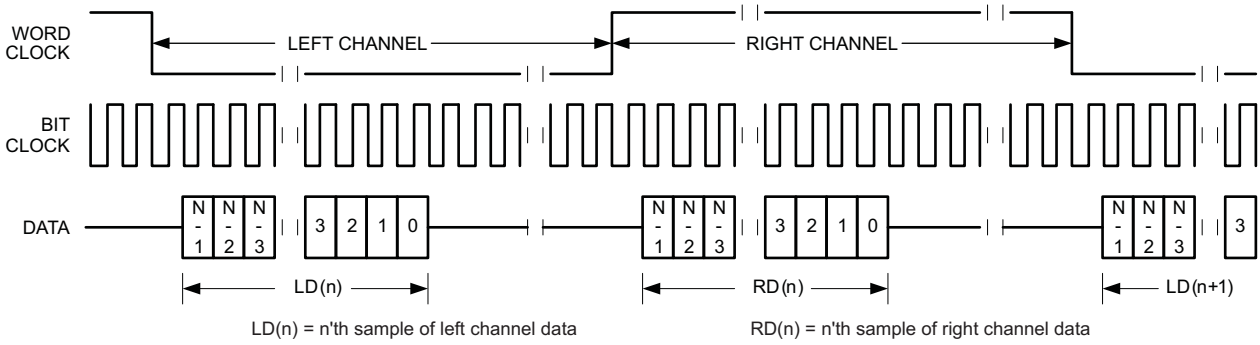

Figure 2-38. Timing Diagram for I²S Mode

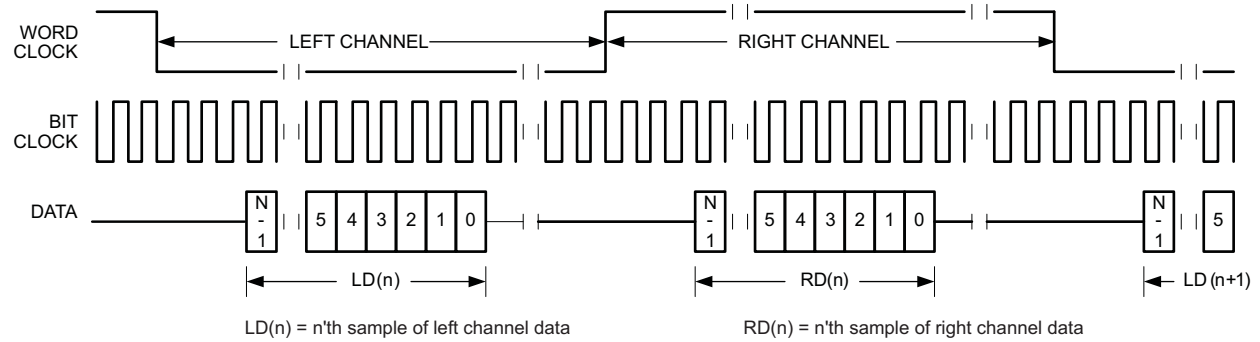

Figure 2-39. Timing Diagram for I²S Mode with offset = 2

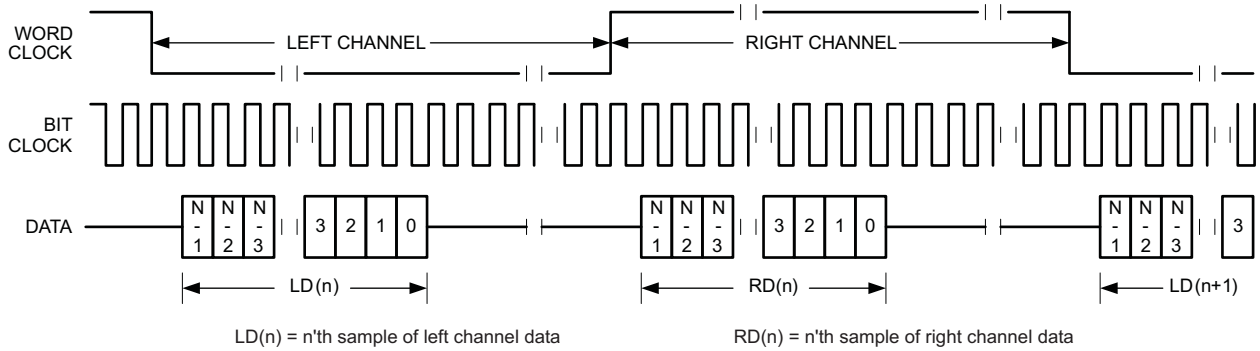

Figure 2-40. Timing Diagram for I²S Mode with offset = 0 and bit clock invert

For I²S mode, the number of bit-clocks per channel should be greater than or equal to the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

2.6.4 DSP Mode

The Audio Interface of the TLV320DAC3203 can be put into DSP Mode by programming Page 0, Register 27, D(7:6) = 01b. In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

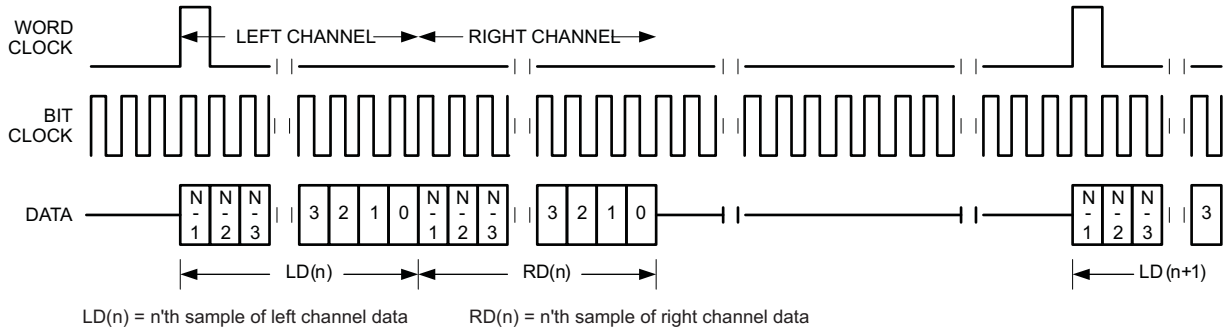

Figure 2-41. Timing Diagram for DSP Mode

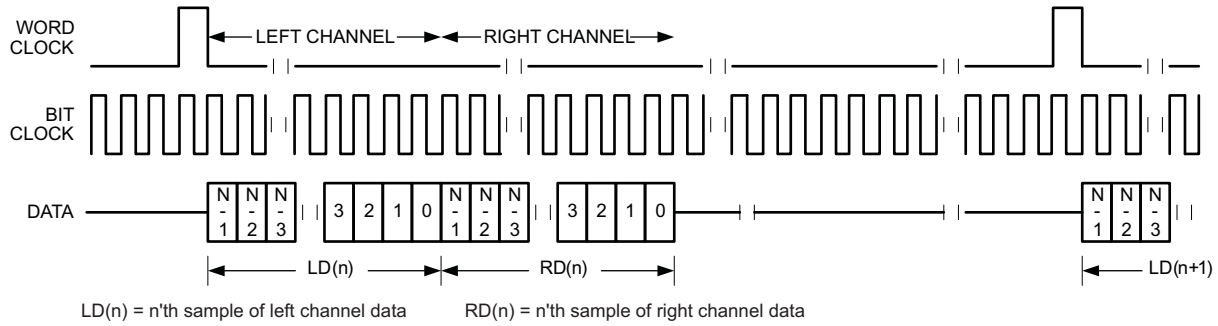

Figure 2-42. Timing Diagram for DSP Mode with offset = 1

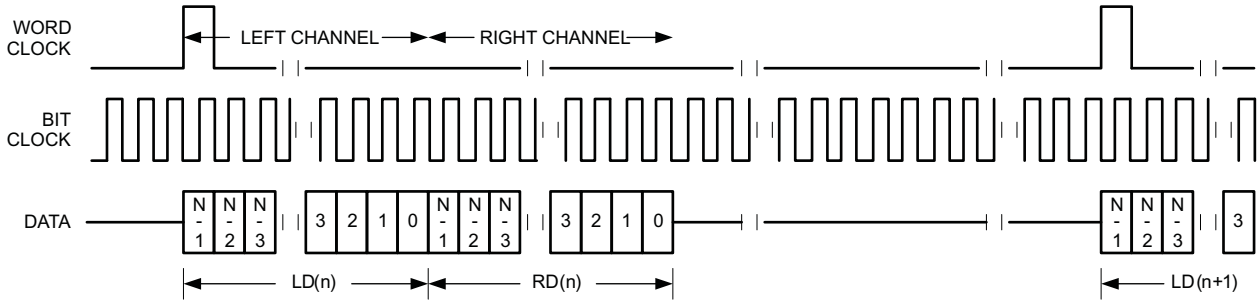

Figure 2-43. Timing Diagram for DSP Mode with offset = 0 and bit clock inverted

For DSP mode, the number of bit-clocks per frame should be greater than twice the programmed word-length of the data. Also the programmed offset value should be less than the number of bit-clocks per frame by at least the programmed word-length of the data.

2.6.5 Secondary I²S

The audio serial interface on the TLV320DAC3203 has an extensive IO control to allow communication with two independent processors for audio data. Each processor can communicate with the device one at a time. This feature is enabled by register programming of the various pin selections.

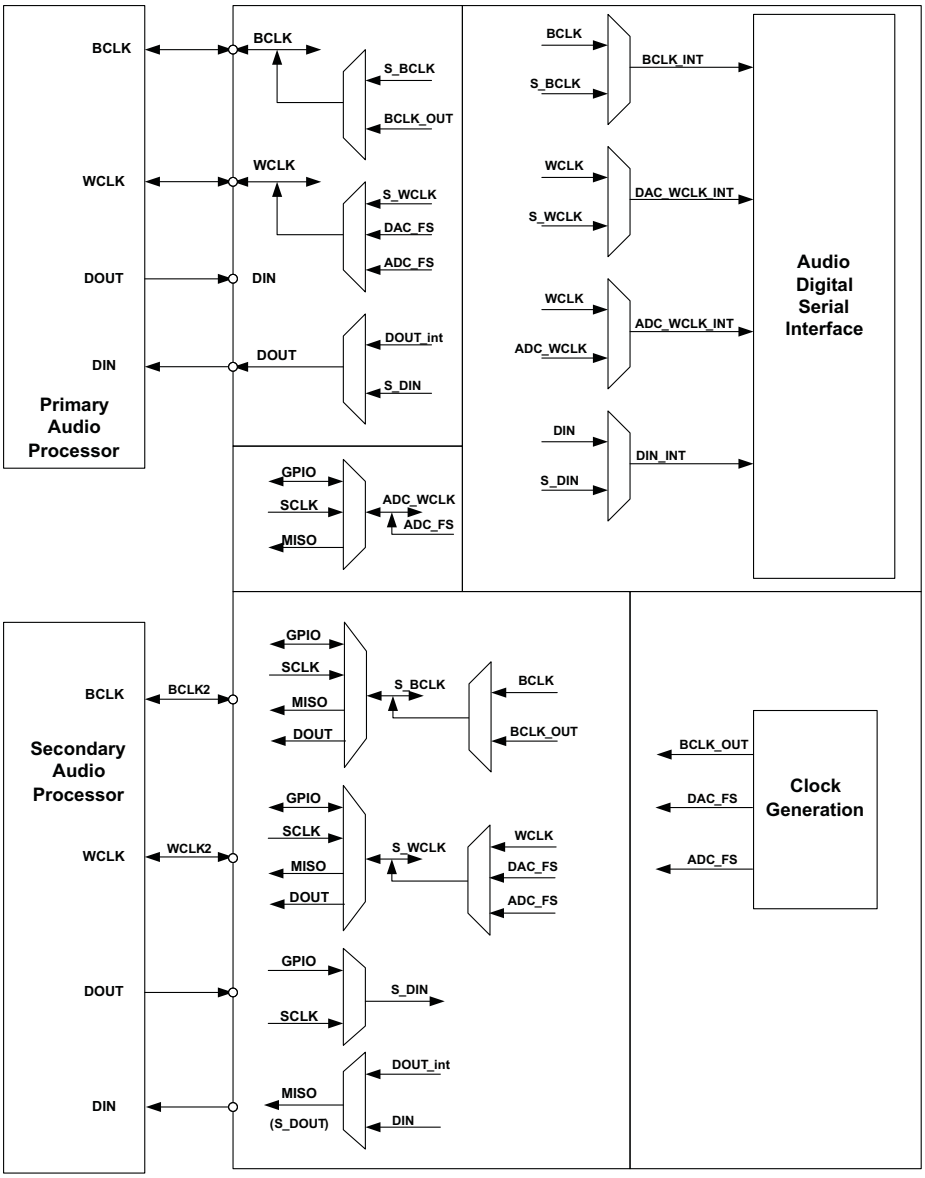

Figure 2-44. Audio Serial Interface Multiplexing

The secondary audio interface uses multifunction pins. For an overview on multifunction pins please see Section 2.1.1.1. Figure 2-44 illustrates possible audio interface routing. The multifunction pins SCLK and MISO are only available in I²C communication mode.

This multiplexing capability allows the TLV320DAC3203 to communicate with two separate devices with independent I²S or PCM busses, one at a time.

2.7 Clock Generation and PLL

The TLV320DAC3203 supports a wide range of options for generating clocks for the DAC as well as interface and other control blocks. The clocks for the DAC require a source reference clock. This clock can be provided on a variety of device pins such as MCLK, BCLK, or GPIO pins. The CODEC_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for the DAC sections. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK, or GPIO, the TLV320DAC3203 also provides the option of using the on-chip PLL, which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN the TLV320DAC3203 provides several programmable clock dividers to help achieve a variety of sampling rates for the DAC.

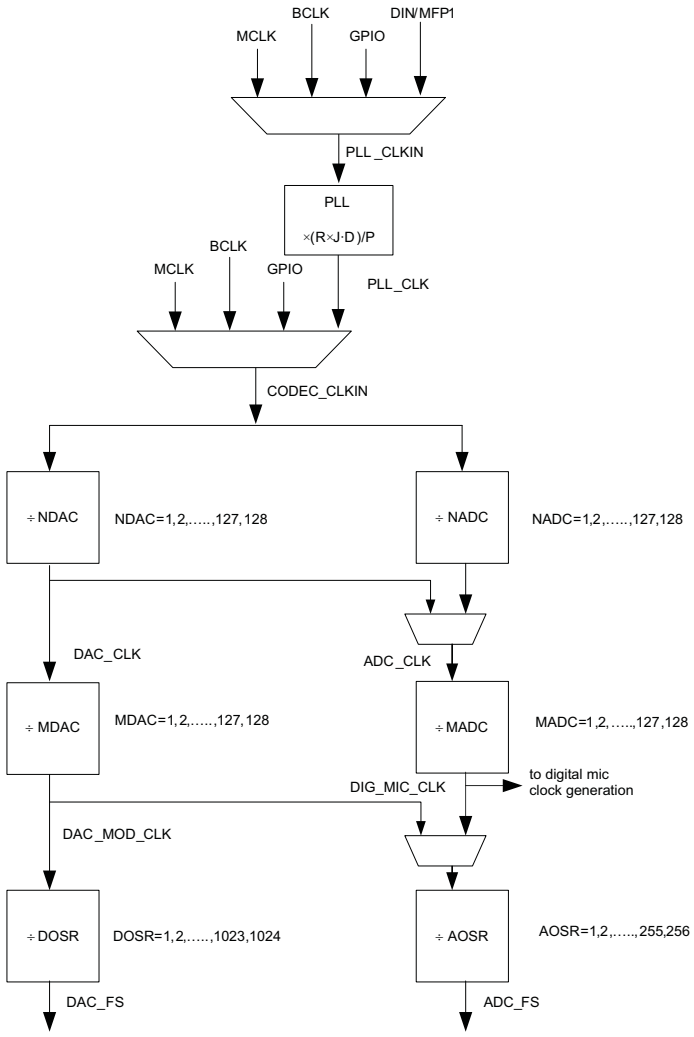

Figure 2-45. Clock Distribution Tree

$$ADC\_f_S = \frac{CODEC\_CLKIN}{NADC \times MADC \times AOSR} \quad (13)$$

$$DIG\_MIC\_CLK = \frac{CODEC\_CLKIN}{NADC \times MADC} \quad (14)$$

$$DAC\_f_S = \frac{CODEC\_CLKIN}{NDAC \times MDAC \times DOSR} \quad (15)$$

$$DAC\_MOD\_CLK = \frac{CODEC\_CLKIN}{NDAC \times MDAC} \quad (16)$$

Table 2-20. CODEC CLKIN Clock Dividers

Divider	Bits
NDAC	Page 0, Register 11, D(6:0)
MDAC	Page 0, Register 12, D(6:0)
DOSR	Page 0, Register 13, D(1:0) + Page 0, Register 14, D(7:0)
NADC	Page 0, Register 18, D(6:0)
MADC	Page 0, Register 19, D(6:0)
AOSR	Page 0, Register 20, D(7:0)

The DAC Modulator is clocked by DAC_MOD_CLK. For proper power-up of the DAC Channel, these clocks must be enabled by configuring the NDAC and MDAC clock dividers (Page 0,Register 11, D(7) = 1 and Page 0, Register 12, D(7) = 1). When the DAC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NDAC and MDAC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read the power-status flag in Page 0, Register 37, D(7) and Page 0, Register 37, D(3). When both flags indicate power-down, the MDAC divider may be powered down, followed by the NDAC divider.

The is clocked by DIG_MIC_CLK. For proper power-up of the ADC Channel, these clocks are enabled by the NADC and MADC clock dividers (Page 0,Register 18, D(7) = 1 and Page 0, Register 19, D(7) = 1). When the ADC channel is powered down, the device internally initiates a power-down sequence for proper shut-down. During this shut-down sequence, the NADC and MADC dividers must not be powered down, or else a proper low power shut-down may not take place. The user can read the power-status flag in Page 0, Register 36, D(6) and Page 0, Register 36, D(2). When both flags indicate power-down, the MADC divider may be powered down, followed by NADC divider.

When ADC_CLK is derived from the NDAC divider output, the NDAC must be kept powered up till the power-down status flags for ADC do not indicate power-down. When the input to the AOSR clock divider is derived from DAC_MOD_CLK, then MDAC must be powered up when ADC_FS is needed (such as when WCLK is generated by TLV320DAC3203) and can be powered down only after the ADC power-down flags indicate power-down status.

In general, all the root clock dividers should be powered down only after the child clock dividers have been powered down for proper operation.

The TLV320DAC3203 also has options for routing some of the internal clocks to the output pins of the device to be used as general purpose clocks in the system. The feature is shown in Figure 2-46.

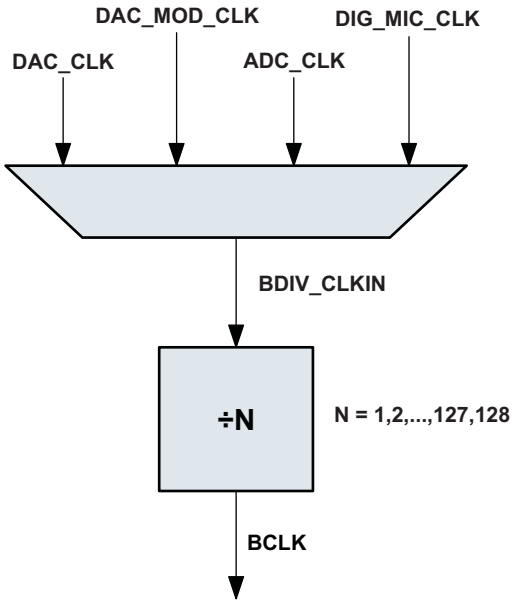

Figure 2-46. BCLK Output Options

In the mode when TLV320DAC3203 is configured to drive the BCLK pin (Page 0, Register 27, D(3) = '1') it can be driven as divided value of BDIV_CLKIN. The division value can be programmed in Page 0, Register 30, D(6:0) from 1 to 128. The BDIV_CLKIN can itself be configured to be one of DAC_CLK, DAC_MOD_CLK, ADC_CLK or DIG_MIC_CLK by configuring the BDIV_CLKIN mux in Page 0, Register 29, D(1:0). Additionally a general purpose clock can be driven out on either GPIO, DOUT or MISO pin. This clock can be a divided-down version of CDIV_CLKIN. The value of this clock divider can be programmed from 1 to 128 by writing to Page 0, Register 26, D(6:0). The CDIV_CLKIN can itself be programmed as one of the clocks among the list shown in Figure 2-47. This configuration is available by programming the mux in Page 0, Register 25, D(2:0).

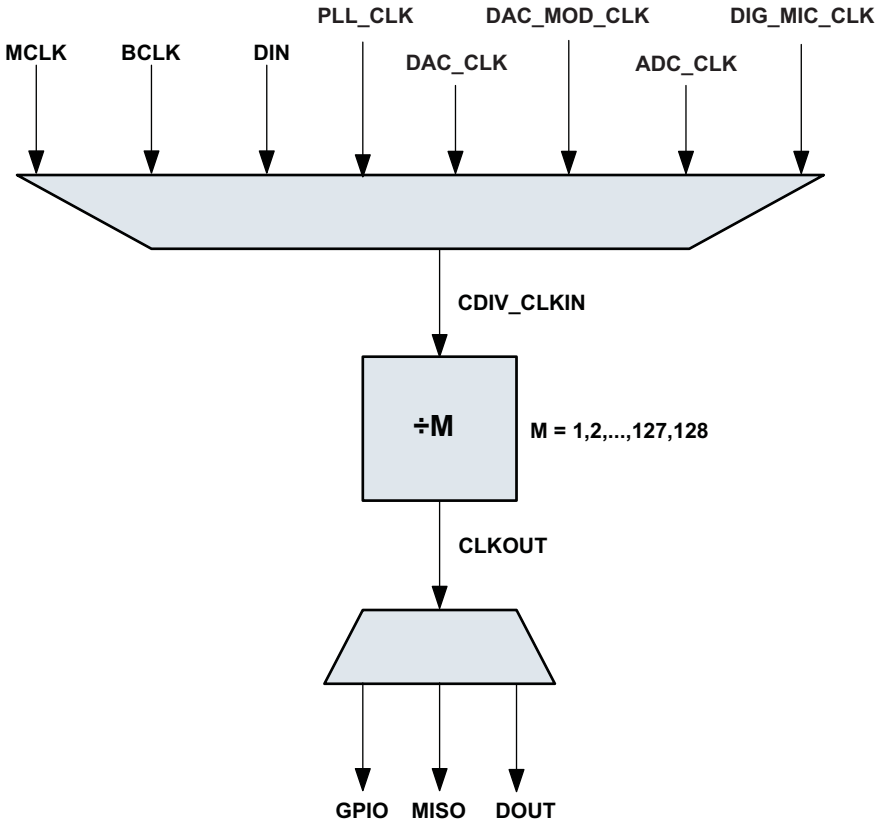

Figure 2-47. General Purpose Clock Output Options

Table 2-21. Maximum TLV320DAC3203 Clock Frequencies

	DVdd ≥ 1.26V	DVdd ≥ 1.65V
CODEC_CLKIN	50MHz	137MHz when NDAC is even, NADC is even 112MHz when NDAC is even, NADC is odd 110MHz when NDAC is odd, NADC is even 110MHz when NDAC is odd, NADC is odd
ADC_CLK	25MHz	55.296MHz
DIG_MIC_CLK	6.758MHz	6.758MHz
ADC_FS	0.192MHz	0.192MHz
DAC_CLK	25MHz	55.296MHz
DAC_MOD_CLK	6.758MHz 4.2MHz when Class-D Mode Headphone is used	6.758MHz
DAC_FS	0.192MHz	0.192MHz
BDIV_CLKIN	25MHz	55.296MHz
CDIV_CLKIN	50MHz	112MHz when M is odd 137MHz when M is even

2.7.1 PLL

The TLV320DAC3203 has an on-chip PLL to generate the clock frequency for the audio ADC, DAC, and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system.

The PLL input supports clocks varying from 512kHz to 20MHz and is register programmable to enable generation of required sampling rates with fine resolution. The PLL can be turned on by writing to Page 0, Register 5, D(7). When the PLL is enabled, the PLL output clock PLL_CLK is given by the following equation:

$$PLL\_CLK = \frac{PLL\_CLKIN \times R \times J.D}{P} \quad (17)$$

R = 1, 2, 3, 4

J = 1, 2, 3, 4,… 63, and D = 0, 1, 2, 3, 4, … 9999

P = 1, 2, 3, 4, … 8

R, J, D, and P are register programmable.

The PLL can be programmed via Page 0, Registers 5-8. The PLL can be turned on via Page 0, Register 5, D(7). The variable P can be programmed via Page 0, Register 5, D(6:4). The default register value for P is 1, and for J is 4. The variable R can be programmed via Page 0, Register 5, D(3:0). The default register value for R is 1. The variable J can be programmed via Page 0, Register 6, D(5:0). The variable D is 12-bits, programmed into two registers. The MSB portion can be programmed via Page 0, Register 7, D(5:0), and the LSB portion is programmed via Page 0, Register 8, D(7:0). The default register value for D is 0.

When the PLL is enabled the following conditions must be satisfied

- When the PLL is enabled and D = 0, the following conditions must be satisfied for PLL_CLKIN:

$$512kHz \le \frac{PLL\_CLKIN}{P} \le 20MHz \quad (18)$$

- When the PLL is enabled and D ≠ 0, the following conditions must be satisfied for PLL_CLKIN:

$$10MHz \le \frac{PLL\_CLKIN}{P} \le 20MHz \quad (19)$$

In the TLV320DAC3203 the PLL_CLK supports a wide range of output clock, based on register settings and power-supply conditions.

Table 2-22. PLL_CLK Frequency Range

AVdd	PLL Mode Page 0, Reg 4, D6	Min PLL_CLK frequency (MHz)	Max PLL_CLK frequency (MHz)
≥1.5V	0	80	103
	1	95	110
≥1.65V	0	80	118
	1	92	123
≥1.80V	0	80	132
	1	92	137

The PLL can be powered up independently from the ADC and DAC blocks, and can also be used as a general purpose PLL by routing its output to the GPIO output. After powering up the PLL, PLL_CLK is available typically after 10ms. The PLL output frequency is controlled by J.D and R dividers

PLL Divider	Bits
J	Page 0, Register 6, D(5:0)
D	Page 0, Register 7, D(5:0) and Page 0, Register 8, D(7:0)
R	Page 0, Register 5, D(3:0)

The D-divider value is 14-bits wide and is controlled by 2 registers. For proper update of the D-divider value, Page 0, Register 7 must be programmed first followed immediately by Page 0, Register 8. Unless the write to Page 0, Register 8 is completed, the new value of D will not take effect.

The clocks for codec and various signal processing blocks, CODEC_CLKIN can be generated from MCLK input, BCLK input, GPIO input or PLL_CLK (Page 0, Register 4, D(1:0)).

If the CODEC_CLKIN is derived from the PLL, then the PLL must be powered up first and powered down last.

Table 2-23 lists several example cases of typical MCLK rates and how to program the PLL to achieve a sample rate f_S of either 44.1kHz or 48kHz.

Table 2-23. PLL Example Configurations

f_S = 44.1kHz										
MCLK (MHz)	**PLLP**	**PLLR**	**PLLJ**	**PLLD**	**MADC**	**NADC**	**AOSR**	**MDAC**	**NDAC**	**DOSR**
2.8224	1	3	10	0	3	5	128	3	5	128
5.6448	1	3	5	0	3	5	128	3	5	128
12	1	1	7	560	3	5	128	3	5	128
13	1	2	4	2336	13	3	64	4	6	104
16	1	1	5	2920	3	5	128	3	5	128
19.2	1	1	4	4100	3	5	128	3	5	128
48	4	1	7	560	3	5	128	3	5	128
f_S = 48kHz										
2.048	1	3	14	0	2	7	128	7	2	128
3.072	1	4	7	0	2	7	128	7	2	128
4.096	1	3	7	0	2	7	128	7	2	128
6.144	1	2	7	0	2	7	128	7	2	128
8.192	1	4	3	0	2	8	128	4	4	128
12	1	1	7	1680	2	7	128	7	2	128
16	1	1	5	3760	2	7	128	7	2	128
19.2	1	1	4	4800	2	7	128	7	2	128
48	4	1	7	1680	2	7	128	7	2	128

2.8 Control Interfaces

The TLV320DAC3203 control interface supports SPI or I^{2}C communication protocols, with the protocol selectable using the SPI_SELECT pin. For SPI, SPI_SELECT should be tied high; for I^{2}C, SPI_SELECT should be tied low. Changing the state of SPI_SELECT during device operation is not recommended.

2.8.1 I^{2}C Control Mode

The TLV320DAC3203 supports the I^{2}C control protocol, and will respond to the I^{2}C address of 0011000. I^{2}C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^{2}C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This circuit prevents two devices from conflicting; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^{2}C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^{2}C devices can act as masters or slaves, but the TLV320DAC3203 can only act as a slave device.

An I^{2}C bus consists of two lines, SDA and SCL. SDA carries data, and the SCL signal provides the clock. All data is transmitted across the I^{2}C bus in groups of eight bits. To send a bit on the I^{2}C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero, while a HIGH indicates the bit is one).

Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on the SCL line clocks the SDA bit into the receiver's shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start communication on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that selects the slave device for communication. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. The master then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not−acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320DAC3203 can also respond to and acknowledge a General Call, which consists of the master issuing a command with a slave address byte of 00H. This feature is disabled by default, but can be enabled via Page 0, Register 34, Bit D(5).

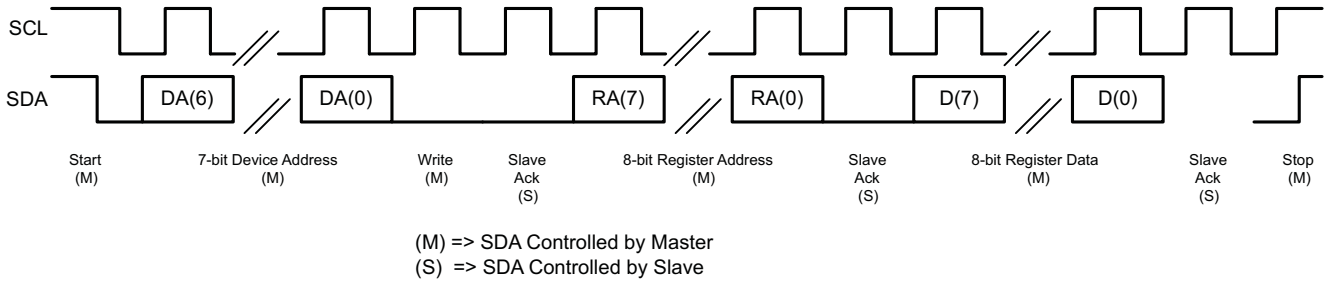

Figure 2-48. I^2C Write

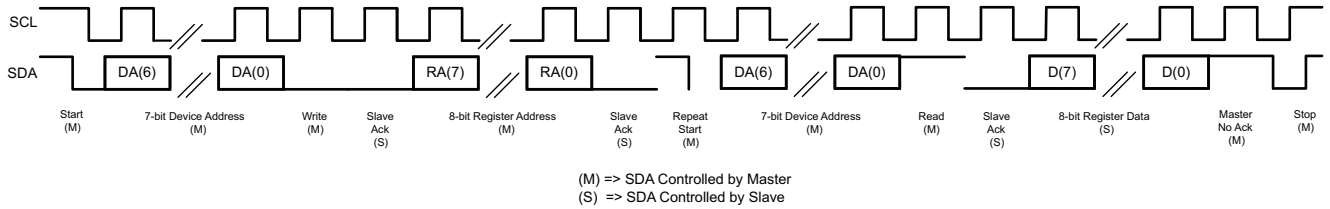

Figure 2-49. I^2C Read

In the case of an I^2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I^2C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next 8 clocks the data of the next incremental register.

2.8.2 SPI Digital Interface

In the SPI control mode, the TLV320DAC3203 uses the pins SCL/$\overline{SS}$ as $\overline{SS}$, SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the TLV320DAC3203) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

The TLV320DAC3203 interface is designed so that with a clock-phase bit setting of 1 (typical microprocessor SPI control bit CPHA = 1), the master begins driving its MOSI pin and the slave begins driving its MISO pin on the first serial clock edge. The SSZ pin can remain low between transmissions; however, the TLV320DAC3203 only interprets the first 8 bits transmitted after the falling edge of SSZ as a command byte, and the next 8 bits as a data byte only if writing to a register. Reserved register bits should be written to their default values. The TLV320DAC3203 is entirely controlled by registers. Reading and writing these registers is accomplished by an 8-bit command sent to the MOSI pin of the part prior to the data for that register. The command is structured as shown in Table 2-24. The first 7 bits specify the register address which is being written or read, from 0 to 127 (decimal). The command word ends with an R/W bit, which specifies the direction of data flow on the serial bus. In the case of a register write, the R/W bit should be set to 0. A second byte of data is sent to the MOSI pin and contains the data to be written to the register. Reading of registers is accomplished in similar fashion. The 8-bit command word sends the 7-bit register address, followed by R/W bit = 1 to signify a register read is occurring. The 8-bit register data is then clocked out of the part on the MISO pin during the second 8 SCLK clocks in the frame.

Table 2-24. SPI Command Word

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR(6)	ADDR(5)	ADDR(4)	ADDR(3)	ADDR(2)	ADDR(1)	ADDR(0)	R/WZ

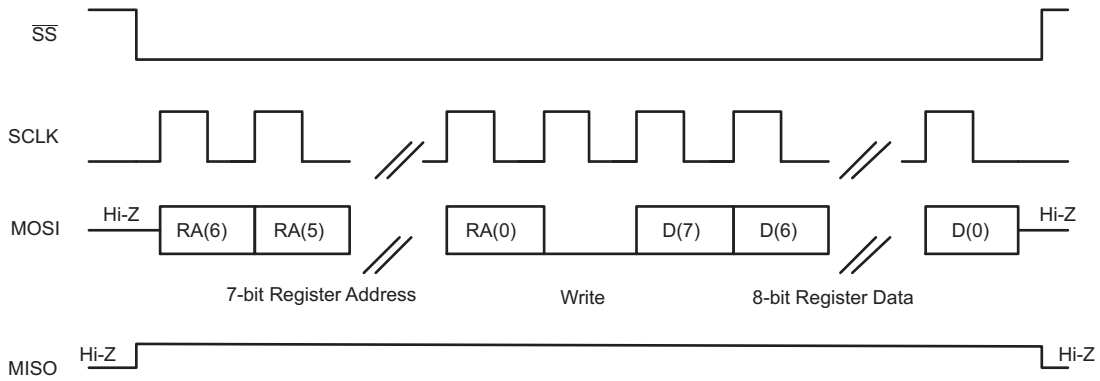

Figure 2-50. SPI Timing Diagram for Register Write

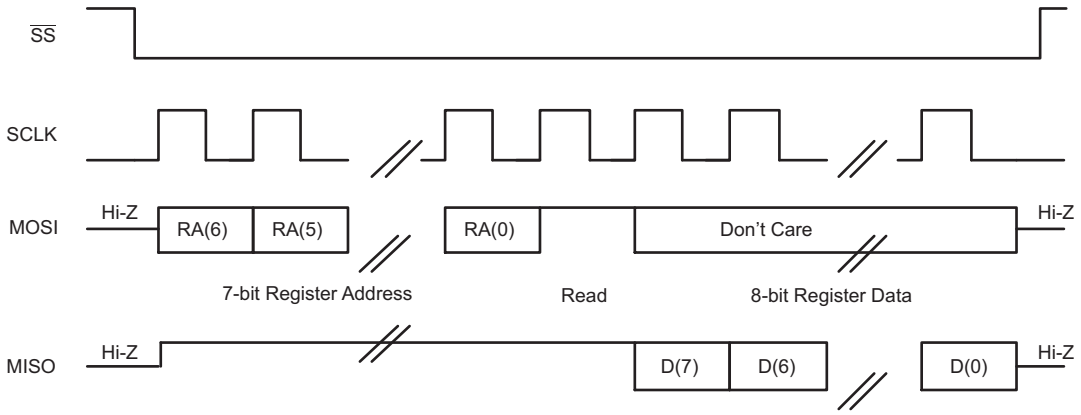

Figure 2-51. SPI Timing Diagram for Register Read

2.9 Power Supply

The four supply pins are LDOin, DVdd, AVdd and IOVDD.

- **IOVdd** - The IOVdd pin supplies the digital IO cells of the device. The voltage of IOVdd can range from 1.1 to 3.6V and is determined by the digital IO voltage of the rest of the system.
- **DVdd** - This pin supplies the digital core of the device. Lower DVdd voltages cause lower power dissipation. If efficient switched-mode power supplies are used in the system, system power can be optimized using low DVdd voltages. the full clock range is only supported with DVdd in the range of 1.65 to 1.95V. Also, operation with DVdd down to 1.26V is possible. (See Table 2-21)
- **AVdd** - This pin is either a supply input to the device, or if the internal LDO is used it is used to connect an external capacitor. It supplies the analog core of the device. The analog core voltage (AVdd) should be in the range of 1.5 to 1.95V for specified performance. For AVdd voltages above 1.8V, the internal common mode voltage can be set to 0.9V (Pg 1, Reg 10, D(6)=0, default) resulting in 500mVrms full-scale voltage internally. For AVdd voltages below 1.8V, the internal common mode voltage should be set to 0.75V (Pg 1, Reg 10, D(6)=1), resulting in 375mVrms internal full scale voltage.

NOTE: At powerup, AVdd is weakly connected to DVdd. This coarse AVdd generation must be turned off by writing Pg 1, Reg 1, D(3) = 1 at the time AVdd is applied, either from internal LDO or through external LDO.

- **LDOin** - The LDOin pin serves two main functions. It serves as supply to the internal LDO as well as to the analog-output amplifiers of the device. The LDOin voltage can range from 1.9V to 3.6V.

2.9.1 System Level Considerations

While there is flexibility in supplying the device through multiple options of power supplies, care must be taken to stay within safe areas when going to standby and shutdown modes.

In summary, the lowest shutdown current is achieved when all supplies to the device are turned off, implying that all settings must be reapplied to the device after bringing the power back up. In order to retain settings in the device, the DVdd voltage and either internally or externally the AVdd voltage also must be maintained. In this case the TLV320DAC3203 exhibits shutdown currents of below 1.5μA.

2.9.1.1 Supply from single voltage rail (1.8V).

If a single 1.8V rail is used, generating the 1.8V from a higher battery voltage via a DC-DC converter results in good system-level efficiency. In this setup, the headphone output voltage is limited to 500mV$_{rms}$, and the maximum headphone output power is 15mW into 16Ω.

The 1.8V rail connected to the DVdd pincan also be connected to the AVdd pin. This connection will make the device function, but the achievable performance is a function of the voltage ripple typically found on DC-DC converter outputs. To achieve specified performance, an external low-input-voltage 1.6V LDO must be connected between the 1.8V rail and the AVdd input.

During operation, the AVdd LDO is deactivated via control register Page 1 / Register 2, D(0)=0. In this case the LDOin pin should be connected to DVdd.

2.9.1.1.1 Standby Mode (1.8V operation)

To put the device in standby mode, both external voltages (AVdd and DVdd) and the reference block inside the TLV320DAC3203 must stay on (Page 1 / Register 123, D(2:0) = 101), all other blocks should be powered down. This results in standby current of approximately 100μA from the AVdd supply.

In standby mode the device responds very quickly to playback requests.

2.9.1.1.2 Sleep Mode (1.8V operation)

In this mode, all settings and memory content of the device is retained. To put the device into sleep mode, the external DVdd must remain powered up, the external AVdd LDO must be powered down, the crude AVdd generation must be turned on (Pg 1, Reg 1, D(3)=0) and the analog blocks must be powered down (Pg 1, Reg 2, D(3)=1). The device's sleep mode power consumption in this case is < 1.5μA

2.9.1.1.3 Shutdown Mode

To shut down the device, the external supplies can be turned off completely. If the 1.8V rail cannot be turned off, the crude AVdd generation must be turned on (Pg 1, Reg 1, D(3)=0) and the analog blocks must be powered down (Pg 1, Reg 2, D(3)=1). This results in a device shutdown current < 1.5μA.

2.9.1.2 Other Supply Options

There are other options to power the device. Apply the following rules:

- During normal operation all supply pins must be connected to a supply (via internal LDO or external)
- Whenever the LDOin supply is present,
  - DVdd supply must be present as well
  - If AVdd supply is not present, then the crude internal AVdd generation must be turned on (Pg 1, Reg 1, D(3)=0)
- Whenever the DVdd supply is on, and either AVdd or LDOin or both supplies are off, the analog blocks must be powered down (Pg 1, Reg 2, D(3)=1)

2.10 Reference Voltage

All data converters require a DC reference voltage. The TLV320DAC3203 achieves its low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with a good PSRR performance. This reference voltage must be filtered externally using a minimum 1μF capacitor connected from the REF pin to analog ground (AV_{SS}).

This reference block is powered down when all analog blocks inside the device are powered down. In this condition, the REF pin is 3-stated. On powerup of any analog block, the reference block also powers up and the REF pin settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the REF pin). This time is approximately 1 second when using a 1μF decoupling capacitor. In the event that a faster power-up is required, the reference block can be kept powered up (even when no other analog block is powered up) by programming Page 1, Register 123, D(2) = 1. However, in this case, an additional 125μA of current from AV_{DD} is consumed. Additionally, to achieve a faster powerup, a fast-charge option is also provided where the charging time can be controlled between 40ms and 120ms by programming Page 1, Register 123, D(1:0). By default, the fast charge option is disabled.

2.11 Device Special Functions

2.11.1 Interrupts

Some specific events in the TLV320DAC3203 which may require host processor intervention, can be used to trigger interrupts to the host processor. INterrupt use avoids polling the status-flag registers continuously. The TLV320DAC3203 has two defined interrupts; INT1 and INT2 that can be configured by programming Page 0, Register 48 and 49. A user can configure the interrupts INT1 and INT2 to be triggered by one or many events such as

- DAC DRC Signal exceeding Threshold
- Over-current condition in headphones
- Data Overflow in ADC and DAC Processing Blocks and Filters

Each of these INT1 and INT2 interrupts can be routed to output pins like GPIO, DOUT and MISO by configuring the respective output control registers in Page 0, Register 52, 53 and 55. These interrupt signals can either be configured as a single pulse or a series of pulses by programming Page 0, Register 48, D(0) and Page 0, Register 49, D(0). If the user configures the interrupts as a series of pulses, the events will trigger the start of pulses that will stop when the flag registers in Page 0, Register 42, 44 and 45 are read by the user to determine the cause of the interrupt.

Device Initialization

The requirements of the application circuit determine device setup details such as clock generation, power sources, references voltage,and special functions that may add value to the end application. Example device setups are described in the final section.

Topic **Page**

3.1 Reset

The TLV320DAC3203 internal logic must be initialized to a known condition for proper device function. To initialize the device to the default operation condition, the hardware reset pin ($\overline{RESET}$) must be pulled low for at least 10ns. For this initialization to work, both the IOV_{DD} and DV_{DD} supplies must be powered up. While the TLV320DAC3203 supplies are powering up, pull the $\overline{RESET}$ pin low. To allow hardware reset control independent of system power supply, drive the $\overline{RESET}$ pin through a GPIO terminal from the host processor. While the device requires a hardware reset after the power supplies are powered up, subsequently the device can be reset via software reset. Writing '1' into Page 0, Register 1, D(0) resets the device. After a device reset, all registers are initialized with default values as listed in the Register Map section.

3.2 Device Startup Lockout Times

After the TLV320DAC3203 initializes through hardware reset at power-up or software reset, the internal registers initialize to default values. This initialization takes place within 1ms after pulling the $\overline{RESET}$ signal high. During this initialization phase, no register-read or register-write operation should be performed on ADC or DAC coefficient buffers. Also, no block within the codec should be powered up during the initialization phase.

3.3 Analog and Reference Startup

The TLV320DAC3203 uses an external REF pin for decoupling the reference voltage used for the data converters and other analog blocks. The REF pin requires a minimum 1µF decoupling capacitor from REF to AV_{SS}. In order for any analog block to be powered up, the Analog Reference block must be powered up. By default, the Analog Reference block is implicitly powered up when any analog block is powered up, or it can be powered up independently. Detailed descriptions of Analog Reference including fast power-up options are provided in Section 2.10. During the time that the reference block is not completely powered up, subsequent requests for powering up analog blocks (such as the PLL) are queued, and executed after the reference power up is complete.

3.4 PLL Startup

When the PLL is powered up, a startup delay of approximately 10ms is involved after the power up command of the PLL and before the clocks are available to the codec. This delay provides stable operation of PLL and clock-divider logic.

3.5 Setting Device Common Mode Voltage

The TLV320DAC3203 allows the user to set the common mode voltage for analog inputs to 0.75V or 0.9V by programming Page 1, Register 10, D(6). The input common-mode voltage of 0.9V works best when the analog supply voltage is centered around 1.8V or above, and offers the highest possible performance. For analog supply voltages below 1.8V, a common mode voltage of 0.75V must be used.

Table 3-1. Input Common Mode voltage and Input Signal Swing

Input Common Mode Voltage (V)	AVdd (V)	Channel Gain (dB)	Single-Ended Input Swing for 0dBFS output signal (V_{RMS})	Differential Input Swing for 0dBFS output signal (V_{RMS})
0.75	>1.5	–2	0.375	0.75
0.90	1.8 … 1.95	0	0.5	1.0

NOTE: The input common mode setting is common for DAC playback and Analog Bypass path

Example Setups

The following example setups can be taken directly for the TLV320DAC3203 EVM setup.

The # marks a comment line, w marks an I^2C write command followed by the device address, the I^2C register address and the value.

4.1 Fast Startup

For the fastest startup time, the device will be initialized to most of its default settings. The minimum necessary configurations are mentioned and explained in this section. Using the TLV320DAC3203EVM board and the script provided at the end of this section provides a startup time of about 18-mS from the last I^2C command to the output being able to play audio. Special care must be taken as this sequence is not focused in eliminating pop-noise; this specific topic will be covered in another section.

NOTE: The Fast Startup sequence is meant to be used in systems where there is an external amplifier that can be muted during the initialization sequence.

4.1.1 Clock Settings

The system used to develop this configuration has a MCLK input of 12.288-MHz, the device is configured as slave for the I2S interface and the sampling frequency is 48-kHz. So the device would only need to divide MCLK by 256 to obtain the desired sampling frequency, thus there is no need to power up and configure the PLL. As a side note, keep in mind that it is always recommended to set DOSR to 128 for best audio quality

4.1.2 Signal Processing

The processing blocks are the path that the signal will follow inside the device; it includes several processing stages as explained in TLV320DAC3203 Data Sheet. The default processing block is the number 1, as this sequence is only focused on a fast startup it can be left as default.

4.1.3 Power Supply Settings

The most important things to do in terms of supply settings is to set the reference power up time, which minimum is 40-mS, and also power up the analog blocks.

4.1.4 DAC & Output Driver Settings

The recommendation for both DAC and output drivers is to route the input/output, set the gain and power up and unmute at the very end. The first step is to route the output of each DAC channel to the correspondent output driver. Then set the DAC gain and power up the DACs, while these are still muted. The next steps are to power up the output drivers, set the gain and at last unmute them. The DAC must be unmuted at the final step.

4.1.5 Example Script Code

```
################################################
# Audio is routed to headphone outputs.
################################################

################################################
# Software Reset
################################################
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
################################################

################################################
# Clock Settings
# ---------------------------------------------
# Codec receives: MCLK = 12.288 MHz,
# BLCK = 3.072 MHz, WCLK = 48 kHz
################################################
# Select Page 0
w 30 00 00
# NDAC = 1, MDAC = 2
w 30 0b 81 82
################################################

################################################
# Configure Power Supplies
################################################
# Select Page 1
w 30 00 01
# Disable weak AVDD to DVDD connection
w 30 01 08
# Enable Master Analog Power Control
w 30 02 00
# Set the REF charging time to 40ms (FASTEST)
w 30 7b 01
################################################



################################################
# Configure DAC Channel
################################################
# Select Page 1
w 30 00 01
# Route LDAC/RDAC to HPL/HPR
w 30 0c 08 08
# Select Page 0
w 30 00 00
# DAC => 0dB
w 30 41 00 00
# Power up LDAC/RDAC
w 30 3f d6
# Select Page 1
w 30 00 01
# Power up HPL/HPR
w 30 09 30
# Unmute HPL/HPR driver, 0dB Gain
w 30 10 00 00
# Select Page 0
w 30 00 00
# Unmute LDAC/RDAC
w 30 40 00
################################################
```

4.2 Fast Startup without Pop-Noise

The outputs of this device are biased to the common-mode voltage, so a DC-coupling capacitor at each output is required. The fast charging of these capacitors may cause pop-noise; however, the pop-noise can be reduced and even eliminated, if the output drivers are powered with a ramp-up time.

The same procedure as the previous section is followed for this example. The only difference will be at the output driver power up time to remove the pop-noise.

4.2.1 DAC & Output Driver Settings

The Register 0x14 on Page 1 is used to configure the Headphone Driver Startup. The key things that are used to reduce or eliminate the pop-noise are the resistance reference (Rpop) for the power up time determination, and also the time constants that set the startup time. The startup time is set in reference to the time constant of the selected resistance (2-kΩ, 6-kΩ or 25-kΩ) and the coupling capacitor at the outputs. Please follow the recommendations explained in *Section 2.2.2.1*.

4.2.2 2.2 Example Script Code

```
################################################
# Audio is routed to headphone outputs.
################################################

################################################
# Software Reset
################################################
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
################################################

################################################
# Clock Settings
# ---------------------------------------
# Codec receives: MCLK = 12.288 MHz,
# BLCK = 3.072 MHz, WCLK = 48 kHz
################################################
# Select Page 0
w 30 00 00
# NDAC = 1, MDAC = 2
w 30 0b 81 82
################################################




################################################
# Configure Power Supplies
################################################
# Select Page 1
w 30 00 01
# Disable weak AVDD to DVDD connection
w 30 01 08
# Enable Master Analog Power Control
w 30 02 00
# Set the REF charging time to 40ms (FASTEST)
w 30 7b 01
# Set HP power up time for NO POP
w 30 14 04
################################################

################################################
# Configure DAC Channel
################################################
# Select Page 1
```

```
w 30 00 01
# Route LDAC/RDAC to HPL/HPR
w 30 0c 08 08
# Select Page 0
w 30 00 00
# DAC => 0dB
w 30 41 00 00
# Power up LDAC/RDAC
w 30 3f d6
# Select Page 1
w 30 00 01
# Unmute HPL/HPR driver, 0dB Gain
w 30 10 00 00
# Power up HPL/HPR
w 30 09 30
# Select Page 0
w 30 00 00
# Unmute LDAC/RDAC
w 30 40 00
################################################
```

4.3 Analog Bypass

The digital interface and the DAC are not needed on this operation mode. This mode only configures the signal path from the analog inputs INL and INR to the headphone outputs. Digital interface and clock settings are not needed.

4.3.1 Example Script Code

```
################################################
# Direct Analog Bypass
# ----------------------------------------
# This script routes INL/R inputs to HPL/R outputs. Connect a portable media player
# to J4 (LINE_IN) and headphones to J2.
# Ensure the input signal does not exceed the maximum rated input voltage.
################################################

################################################
# Software Reset
################################################
# Select Page 0
w 30 00 00
# Initialize the device through software reset
w 30 01 01
################################################
# Configure Power Supplies
################################################
# Select Page 1
w 30 00 01
# Disable weak AVDD to DVDD connection
w 30 01 08
# Enable Master Analog Power Control
w 30 02 00
# Set the input power-up time to 3.1ms
w 30 47 32
# Set the REF charging time to 40ms
w 30 7b 01
################################################
# Playback Setup
################################################
# Select Page 1
w 30 00 01
# De-pop: 5 time constants, 6k resistance
w 30 14 25
# Direct Bypass Gain = 0dB
w 30 16 00 00
```

```
# Route INL/R to HPL/R
w 30 0C 04 04
# Unmute HPL/HPR driver, 0dB Gain
w 30 10 00 00
# Power up HPL/HPR drivers
w 30 09 30
################################################
```

4.4 Stereo DAC Playback with 48 ksps Sample Rate and High Performance

```
Assumption: MCLK = 12.288MHz, Slave I2S

#----------- Initialize to page 0
w 30 00 00
#----------- Initialize the device through software reset
w 30 01 01
#----------- Power up the NDAC divider with value 1
w 30 0b 81
#----------- Power up the MDAC divider with value 2
w 30 0c 82
#----------- Program the OSR of DAC to 128
w 30 0d 00
w 30 0e 80
#----------- Set the word length of audio interface to 20 bits PTM_P4
w 30 1b 10
#----------- Set the DAC mode to PRB_P8
w 30 3c 08
#----------- Select page 1
w 30 00 01
#----------- Disable internal crude AVdd in presence of external AVdd supply
#----------- or before powering up internal AVdd LDO
w 30 01 08
#----------- Enable master analog power control
w 30 02 00
#----------- Set the REF charging time to 40ms
w 30 7b 01
#----------- Set the input common mode to 0.9V and output common mode for headphone
#----------- to input common mode
w 30 0a 00
#----------- Route left DAC to HPL
w 30 0c 08
#----------- Route right DAC to HPR
w 30 0d 08
#----------- Set the DAC PTM mode to PTM_P3/4
w 30 03 00
w 30 04 00
#----------- Set the HPL gain to 0dB
w 30 10 00
#----------- Set the HPR gain to 0dB
w 30 11 00
#----------- HP soft stepping settings for optimal pop performance at power up
#----------- Rpop used is 6k with N = 6 & soft step = 20usec.
w 30 14 29
#----------- Power up HPL and HPR drivers
w 30 09 30
#----------- Wait for 2.5 sec for soft stepping to take effect
#----------- else read page 1, register 63d, D(7:6). When = “11” soft-stepping is complete
#----------- Select page 0
w 30 00 00
#----------- Power up the left and right DAC channels and route the left channel I2S data
#----------- to left channel DAC and right channel I2S data to right channel DAC
w 30 3f d6
#----------- Unmute the DAC digital volume control
w 30 40 00
```

4.5 Stereo DAC Playback with 48ksps Sample Rate and Low Power Mode

```
Assumption: MCLK = 12.288MHz, Slave I2S

#----------- Initialize to page 0
w 30 00 00
#----------- Initialize the device through software reset
w 30 01 01
#----------- Power up the NDAC divide with value 1
w 30 0b 81
#----------- Power up the MDAC divider with value 4
w 30 0c 84
#----------- Program the OSR of DAC to 64
w 30 0d 00
w 30 0e 40
#----------- Set the DAC mode to PRB_P8
w 30 3c 08
#----------- Select page 1
w 30 00 01
#----------- Disable internal crude AVdd in presence of external AVdd supply
#----------- or before powering up internal AVdd LDO
w 30 01 08
#----------- Enable master analog power control
w 30 02 00
#----------- Set the REF charging time to 40ms
w 30 7b 01
#----------- Set the input common mode to 0.9V and output common mode for headphone
#----------- to input common mode
w 30 0a 00
#----------- Route left DAC to HPL
w 30 0c 08
#----------- Route right DAC to HPR
w 30 0d 08
#----------- Set the DAC PTM mode to PTM_P1
w 30 03 08
w 30 04 08
#----------- Set the HPL gain to 0dB
w 30 10 00
#----------- Set the HPR gain to 0dB
w 30 11 00
#----------- HP soft stepping settings for optimal pop performance at power up
#----------- Rpop used is 6k with N = 6 & soft step = 20usec.
w 30 14 29
#----------- Power up HPL and HPR drivers
w 30 09 30
#----------- Wait for 2.5 sec for soft stepping to take effect
#----------- Else read Page 1, Register 63d, D(7:6). When = “11” soft-stepping is complete
#----------- Select page 0
w 30 00 00
#----------- Power up the left and right DAC channels and route the left channel I2S data
#----------- to left channel DAC and right channel I2S data to right channel DAC
w 30 3f d4
#----------- Unmute the DAC digital volume control
w 30 40 00
```

4.6 DAC Playback with 48 ksps Sample Rate through Class-D Headphone Amplifiers

```
Assumption: MCLK = 24.576MHz, Slave I2S

#----------- Power-up
#----------- Initialize to page 0
w 30 00 00
#----------- Initialize the device through software reset
w 30 01 01
#----------- Power up the NDAC divider with value 1
w 30 0b 81
```

```
#----------- Power up the MDAC divider with value 4
#----------- For class-D mode, MDAC = I*4
w 30 0c 84
#----------- Program the OSR of DAC to 128
w 30 0d 00
w 30 0e 80
#----------- Set the DAC Mode to PRB_P1v
w 30 3c 01
#----------- Select page 1
w 30 00 01
#----------- Disable internal crude AVdd in presence of external AVdd supply
#----------- or before powering up internal AVdd LDO
w 30 01 08
#----------- Enable master analog power control
w 30 02 00
#----------- Set the REF charging time to 40ms
w 30 7b 01
#----------- Set the input common mode to 0.9V and output common mode for headphone
#----------- to input common mode
w 30 0a 00
#----------- Enable class-D mode for HPL output
w 30 03 c0
#----------- Enable class-D mode for HPR output
w 30 04 c0
#----------- Route left DAC to HPL
w 30 0c 08
#----------- Route right DAC to HPR
w 30 0d 08
#----------- Unmute HPL driver
w 30 10 00
#----------- Unmute HPR driver
w 30 11 00
#----------- HP soft stepping settings for optimal pop performance at power up
#----------- Rpop used is 6k with N = 6 & soft step = 20usec.
w 30 14 29
#----------- Power up HPL and HPR drivers
w 30 09 30
#----------- Wait for 2.5 sec for soft stepping to take effect
#----------- Else read Page 1, Register 63d, D(7:6). When = “11” soft-stepping is complete
#----------- Switch to page 0
w 30 00 00
#----------- Power up the left and right DAC channels and route the left channel I2S data
#----------- to left channel DAC and right channel I2S data to right channel DAC
w 30 3f d4
#----------- Unmute the DAC digital volume control
w 30 40 00
#----------- Breakpoint
b
#----------- Power-down
#----------- Select page 1
w 30 00 01
#----------- Power down HPL and HPR drivers
w 30 09 00
#----------- Select page 0
w 30 00 00
#----------- Mute the DAC digital volume control
w 30 40 0d
#----------- Power down the DAC
w 30 3f c0
#----------- Disable class-D mode for HPL output
w 30 03 00
#----------- Disable class-D mode for HPL output
w 30 04 00
```

4.7 ADC Record through Digital Microphone with 44.1 ksps Sample Rate

Assumption: MCLK = 11.2896 MHz

```
#----------- Initialize to page 0
w 30 00 00
#----------- Initialize the device through software reset
w 30 01 01
#----------- Set PLL_CLKIN as MCLK and CODEC_CLKIN as PLL_CLK,
w 30 04 03
#----------- Power up pll, set pll divider P=1 and pll divider R=1,
w 30 05 91
#----------- Set pll divider J=8
w 30 06 08
#----------- Set pll divider D=0000
w 30 07 00
w 30 08 00
#----------- Power up and set NADC divider = 2,
w 30 12 82
#----------- Power up and set MDAC divider = 16
w 30 13 90
#----------- Set AOSR = 64
w 30 14 40
#----------- Select page 1
w 30 00 01
#----------- Disable internal crude AVdd in presence of external AVdd supply
#----------- or before powering up internal AVdd LDO
w 30 01 08
#----------- Enable master analog power control
w 30 02 00
#----------- Set the REF charging time to 40ms
w 30 7b 01
#----------- Select page 0
w 30 00 00
#----------- Select PRB_R2
w 30 3d 02
#----------- Configure MISO as clock output for digital microphone
w 30 37 0e
#----------- Power up left ADC and right ADC. Enable digital microphone mode for left ADC
#----------- and right ADC. Treat data on SCLK as digital microphone data
w 30 51 dc
#----------- Unmute left ADC and right ADC
w 30 52 00
```

4.8 Mono Differential Output

TLV320DAC3203 also has the ability to configure its outputs in a mono differential mode. However a special procedure must be followed to ensure the correct device operation; not doing so could cause clipping and distortion at the output signal.

4.8.1 Offset Correction

TLV320DAC3203 features an offset correction based on calibration during power up. Further information of this feature can be found in *Section 2.2.2.2.1*.

This feature must be enabled before powering up the headphone outputs. The suggested initialization procedure is listed below. An example script is provided as well.

The process to write this into the device is as follows:

- Open TLV320DAC3203 GUI.
- Connect EVM
- Open Command-Line Interface from GUI.
- Copy the script into the Command Buffer.
- Click on Execute Command Buffer. At this point, the device is configured, so playback is available.
- Configure other device features if needed such as BQ filters.

4.8.2 Example Script Code

```
#----------- Initialize to page 0
w 30 00 00
#----------- Software RESET
w 30 01 01
#----------- Power up and set NDAC divider = 1
w 30 0b 81
#----------- Power up and set MDAC divider = 2
w 30 0c 82
#----------- Select page 1
w 30 00 01
#----------- Disable internal crude AVdd in presence of external AVdd supply
#----------- or before powering up internal AVdd LDO
w 30 01 08
#----------- Enable master analog power control
w 30 02 00
#----------- Set the REF charging time to 40ms
w 30 7b 05
#----------- Left DAC reconstruction filter +ve terminal to HPL
w 30 0c 08
#----------- Left DAC reconstruction filter -ve terminal to HPR
w 30 0d 10
#----------- Unmute HPL, gain set to 0dB
w 30 10 00
#----------- Unmute HPR, gain set to 0dB
w 30 11 00
#----------- Offset calibration mode “01”
w 30 7d 21
#----------- Device common mode=0.75V, headphone output common mode = 1.5V
#----------- Headphone powered by LDOIN supply and LDONIN > 1.8V
w 30 0a 63
#----------- Select page 0
w 30 00 00
#----------- Select PRB_P1 for DAC playback
w 30 3c 01
#----------- Power up left DAC
w 30 3f 94
#----------- Select page 1
w 30 00 01
#----------- Power up HPL and HPR
```

```
w 30 09 30
#----------- Poll page 1, register 2, D2. If the bit is '1' go to next step, else wait
#----------- If not polling wait for 8ms
d 10
#----------- Select page 0
w 30 00 00
#----------- Unmute left DAC digital volume control
w 30 40 04
```

Register Map

The TLV320DAC3203 contains 108 pages of 8-bit registers, each page can contain up to 128 registers. The register pages are divided up based on functional blocks for this device. Page 0 is the default home page after hardware reset.

5.1 Register Map Summary

Table 5-1. Summary of Register Map

PAGE NO.	DESCRIPTION
0	Configuration for Serial Interface, Digital IO, Clocking, ADC and DAC configuration etc.
1	Configuration for Analog PGAs, ADC, DAC, Output.Drivers, Volume controls etc.
2-7	Reserved
8	ADC adaptive filtering control and ADC Coefficient Buffer-A (0:29). See Table 5-2.
9-10	ADC Coefficient Buffer-A (30:63). See Table 5-2 and Table 5-4.
11-25	Reserved
26-28	ADC Coefficient Buffer-B (0:63). See Table 5-3 and Table 5-4.
29-43	Reserved
44	DAC adaptive filtering control and DAC Coefficient Buffer-A (0:29). See Table 5-5.
45-46	DAC Coefficient BufferA (30:76). See Table 5-5 and Table 5-7.
47-61	Reserved
62-64	DAC Coefficient BufferB C(0:76). See Table 5-6 and Table 5-7.
65-255	Reserved

5.2 Page 0 Registers

5.2.1 Page 0 / Register 0: Page Select Register - 0x00 / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.2.2 Page 0 / Register 1: Software Reset Register - 0x00 / 0x01

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	R	0000 000	Reserved, Write only default values
D0	W	0	Self clearing software reset bit 0: Don't care 1: Self clearing software reset

5.2.3 Page 0 / Register 2: Reserved Register - 0x00 / 0x02

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0XXX 0XXX	Reserved, Write only default values

5.2.4 Page 0 / Register 3: Reserved Register - 0x00 / 0x03

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved, Write only default values to this register

5.2.5 Page 0 / Register 4: Clock Setting Register 1, Multiplexers - 0x00 / 0x04

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved, Write only default values
D6	R/W	0	Select PLL Range 0: Low PLL Clock Range 1: High PLL Clock Range
D5-D4	R	00	Reserved, Write only default values any other value than reset value.
D3-D2	R/W	00	Select PLL Input Clock 00: MCLK pin is input to PLL 01: BCLK pin is input to PLL 10: GPIO pin is input to PLL (** Availble only for WCSP Package) 11: DIN pin is input to PLL
D1-D0	R/W	00	Select CODEC_CLKIN 00: MCLK pin is CODEC_CLKIN 01: BCLK pin is CODEC_CLKIN 10: GPIO pin is CODEC_CLKIN (** Availble only for WCSP Package) 11: PLL Clock is CODEC_CLKIN

5.2.6 Page 0 / Register 5: Clock Setting Register 2, PLL P&R Values - 0x00 / 0x05

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Power Up 0: PLL is powered down 1: PLL is powered up
D6-D4	R/W	001	PLL divider P Value 000: P=8 001: P=1 010: P=2 … 110: P=6 111: P=7
D3-D0	R/W	0001	PLL divider R Value 000: Reserved, do not use 001: R=1 010: R=2 011: R=3 100: R=4 101…111: Reserved, do not use

5.2.7 Page 0 / Register 6: Clock Setting Register 3, PLL J Values - 0x00 / 0x06

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values any value other than default
D5-D0	R/W	00 0100	PLL divider J value 00 0000…00 0011: Do not use 00 0100: J=4 00 0101: J=5 … 11 1110: J=62 11 1111: J=63

5.2.8 Page 0 / Register 7: Clock Setting Register 4, PLL D Values (MSB) - 0x00 / 0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values any value other than default

Page 0 / Register 7: Clock Setting Register 4, PLL D Values (MSB) - 0x00 / 0x07 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	00 0000	PLL divider D value (MSB) PLL divider D value(MSB) & PLL divider D value(LSB) 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 … 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000…11 1111 1111 1111: Do not use Note: This register will be updated only when the Page-0, Reg-8 is written immediately after Page-0, Reg-7

5.2.9 Page 0 / Register 8: Clock Setting Register 5, PLL D Values (LSB) - 0x00 / 0x08

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	PLL divider D value (LSB) PLL divider D value(MSB) & PLL divider D value(LSB) 00 0000 0000 0000: D=0000 00 0000 0000 0001: D=0001 … 10 0111 0000 1110: D=9998 10 0111 0000 1111: D=9999 10 0111 0001 0000…11 1111 1111 1111: Do not use Note: Page-0, Reg-8 should be written immediately after Page-0, Reg-7

5.2.10 Page 0 / Register 9-10: Reserved Register - 0x00 / 0x09-0x0A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved, Write only default values.

5.2.11 Page 0 / Register 11: Clock Setting Register 6, NDAC Values - 0x00 / 0x0B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	NDAC Divider Power Control 0: NDAC divider powered down 1: NDAC divider powered up
D6-D0	R/W	000 0001	NDAC Value 000 0000: NDAC=128 000 0001: NDAC=1 000 0010: NDAC=2 … 111 1110: NDAC=126 111 1111: NDAC=127 Note: Please check the clock frequency requirements in the Overview section

5.2.12 Page 0 / Register 12: Clock Setting Register 7, MDAC Values - 0x00 / 0x0C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	MDAC Divider Power Control 0: MDAC divider powered down 1: MDAC divider powered up
D6-D0	R/W	000 0001	MDAC Value 000 0000: MDAC=128 000 0001: MDAC=1 000 0010: MDAC=2 … 111 1110: MDAC=126 111 1111: MDAC=127 Note: Please check the clock frequency requirements in the Overview section

5.2.13 Page 0 / Register 13: DAC OSR Setting Register 1, MSB Value - 0x00 / 0x0D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	0000 00	Reserved. Write only default values
D1-D0	R/W	00	DAC OSR (DOSR) Setting DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: Reserved. Do not use 00 0000 0010: DOSR=2 … 11 1111 1110: DOSR=1022 11 1111 1111: Reserved. Do not use Note: This register is updated when Page-0, Reg-14 is written to immediately after Page-0, Reg-13 Note: DOSR should be a multiple of 2 while using DAC Filter Type A, Multiple of 4 while using DAC Filter Type B and Multiple of 8 while using DAC Filter Type C

5.2.14 Page 0 / Register 14: DAC OSR Setting Register 2, LSB Value - 0x00 / 0x0E

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1000 0000	DAC OSR (DOSR) Setting DAC OSR(MSB) & DAC OSR(LSB) 00 0000 0000: DOSR=1024 00 0000 0001: Reserved. Do not use 00 0000 0010: DOSR=2 … 11 1111 1110: DOSR=1022 11 1111 1111: Reserved. Do not use Note: This register should be written immediately after Page-0, Reg-13 Note: DOSR should be a multiple of 2 while using DAC Filter Type A, Multiple of 4 while using DAC Filter Type B and Multiple of 8 while using DAC Filter Type C

5.2.15 Page 0 / Register 15: Reserved Register - 0x00 / 0x0F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0010	Reserved. Write only default value

5.2.16 Page 0 / Register 16: Reserved Register - 0x00 / 0x10

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Write only default value

5.2.17 Page 0 / Register 17: Reserved Register - 0x00 / 0x11

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 1000	Reserved. Write only default values

5.2.18 Page 0 / Register 18: Reserved Register - 0x00 / 0x12

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0001	Reserved. Write only default values

5.2.19 Page 0 / Register 19: Reserved Register - 0x00 / 0x13

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0001	

5.2.20 Page 0 / Register 20: ADC Oversampling (AOSR) Register - 0x00 / 0x14

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	1000 0000	ADC Oversampling Value 0000 0000: ADC AOSR = 256 0000 0001-0001 1111: Reserved. Do not use 0010 0000: ADC AOSR=32 (Use with PRB_R13 to PRB_R18, ADC Filter Type C) 0010 0001-0011 1111: Reserved.Do not use 0100 0000: AOSR=64 (Use with PRB_R1 to PRB_R12, ADC Filter Type A or B) 0100 0001-0111 1111: Reserved. Do not use 1000 0000: AOSR=128(Use with PRB_R1 to PRB_R6, ADC Filter Type A) 1000 0001-1111 1111: Reserved. Do not use

5.2.21 Page 0 / Register 21: Reserved Register - 0x00 / 0x15

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0001	Reserved. Write only default values

5.2.22 Page 0 / Register 22: Reserved Register - 0x00 / 0x16

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.2.23 Page 0 / Register 23: Reserved Register - 0x00 / 0x17

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0100	Reserved. Write only default values

5.2.24 Page 0 / Register 24: Reserved Register - 0x00 / 0x18

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.2.25 Page 0 / Register 25: Clock Setting Register 8, Multiplexers - 0x00 / 0x19

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values
D2-D0	R/W	000	CDIV_CLKIN Clock Selection 000: CDIV_CLKIN= MCLK 001: CDIV_CLKIN= BCLK 010: CDIV_CLKIN=DIN 011: CDIV_CLKIN=PLL_CLK 100: CDIV_CLKIN=DAC_CLK 101: CDIV_CLKIN=DAC_MOD_CLK 110-111: Reserved

5.2.26 Page 0 / Register 26: Clock Setting Register 9, CLKOUT M divider value - 0x00 / 0x1A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	CLKOUT M divider power control 0: CLKOUT M divider powered down 1: CLKOUT M divider powered up
D6-D0	R/W	000 0001	CLKOUT M divider value 000 0000: CLKOUT M divider = 128 000 0001: CLKOUT M divider = 1 000 0010: CLKOUT M divider = 2 … 111 1110: CLKOUT M divider = 126 111 1111: CLKOUT M divider = 127 Note: Please check the clock frequency requirements in the application overview section

5.2.27 Page 0 / Register 27: Audio Interface Setting Register 1 - 0x00 / 0x1B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Audio Interface Selection 00: Audio Interface = I2S 01: Audio Interface = DSP 10: Audio Interface = RJF 11: Audio Interface = LJF
D5-D4	R/W	00	Audio Data Word length 00: Data Word length = 16 bits 01: Data Word length = 20 bits 10: Data Word length = 24 bits 11: Data Word length = 32 bits
D3	R/W	0	BCLK Direction Control 0: BCLK is input to the device 1: BCLK is output from the device
D2	R/W	0	WCLK Direction Control 0: WCLK is input to the device 1: WCLK is output from the device
D1	R	0	Reserved. Write only default value
D0	R/W	0	MFP2 (DOUT of loopback data) High Impendance Output Control 0: MFP2 will not be high impedance while Audio Interface is active 1: MFP2 will be high impedance after data has been transferred

5.2.28 Page 0 / Register 28: Audio Interface Setting Register 2, Data offset setting - 0x00 / 0x1C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Data Offset Value 0000 0000: Data Offset = 0 BCLK's 0000 0001: Data Offset = 1 BCLK's … 1111 1110: Data Offset = 254 BCLK's 1111 1111: Data Offset = 255 BCLK's

5.2.29 Page 0 / Register 29: Audio Interface Setting Register 3 - 0x00 / 0x1D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Reserved. Write only default values
D5	R/W	0	Loopback control 0: No Loopback 1: Audio Data in is routed to Audio Data out (DOUT signal on MFP2)
D4	R/W	0	Reserved. Write only default values
D3	R/W	0	Audio Bit Clock Polarity Control 0: Default Bit Clock polarity 1: Bit Clock is inverted w.r.t. default polarity
D2	R/W	0	Primary BCLK and Primary WCLK Power control 0: Priamry BCLK and Primary WCLK buffers are powered down when the codec is powered down 1: Primary BCLK and Primary WCLK buffers are powered up when they are used in clock generation even when the codec is powered down
D1-D0	R/W	00	BDIV_CLKIN Multiplexer Control 00: BDIV_CLKIN = DAC_CLK 01: BDIV_CLKIN = DAC_MOD_CLK 10-11: Reserved

5.2.30 Page 0 / Register 30: Clock Setting Register 10, BCLK N Divider - 0x00 / 0x1E

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	BCLK N Divider Power Control 0: BCLK N divider powered down 1: BCLK N divider powered up

Page 0 / Register 30: Clock Setting Register 10, BCLK N Divider - 0x00 / 0x1E (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0001	BCLK N Divider value 0000 0000: BCLK N divider = 128 0000 0001: BCLK N divider = 1 … 1111 1110: BCLK N divider = 126 1111 1111: BCLK N divider = 127

5.2.31 Page 0 / Register 31: Audio Interface Setting Register 4, Secondary Audio Interface - 0x00 / 0x1F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6-D5	R/W	00	Secondary Bit Clock Multiplexer 00: Secondary Bit Clock = GPIO (** Availble only for WCSP Package) 01: Secondary Bit Clock = SCLK 10: Secondary Bit Clock = MISO 11: Secondary Bit Clock = DOUT
D4-D3	R/W	00	Secondary Word Clock Multiplexer 00: Secondary Word Clock = GPIO (** Availble only for WCSP Package) 01: Secondary Word Clock = SCLK 10: Secondary Word Clock = MISO 11: Secondary Word Clock = DOUT
D2-D1	R/W	00	ADC Word Clock Multiplexer 00: ADC Word Clock = GPIO (** Availble only for WCSP Package) 01: ADC Word Clock = SCLK 10: ADC Word Clock = MISO 11: Do not use
D0	R/W	0	Secondary Data Input Multiplexer 0: Secondary Data Input = GPIO (** Availble only for WCSP Package) 1: Secondary Data Input = SCLK

5.2.32 Page 0 / Register 32: Audio Interface Setting Register 5 - 0x00 / 0x20

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only default values
D3	R/W	0	Primary / Secondary Bit Clock Control 0: Primary Bit Clock(BCLK) is used for Audio Interface and Clocking 1: Secondary Bit Clock is used for Audio Interface and Clocking
D2	R/W	0	Primary / Secondary Word Clock Control 0: Primary Word Clock(WCLK) is used for Audio Interface 1: Secondary Word Clock is used for Audio Interface
D1	R/W	0	Reserved. Write only default value
D0	R/W	0	Audio Data In Control 0: DIN is used for Audio Data In 1: Secondary Data In is used for Audio Data In

5.2.33 Page 0 / Register 33: Audio Interface Setting Register 6 - 0x00 / 0x21

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	BCLK Output Control 0: BCLK Output = Generated Primary Bit Clock 1: BCLK Output = Secondary Bit Clock Input
D6	R/W	0	Secondary Bit Clock Output Control 0: Secondary Bit Clock = BCLK input 1: Secondary Bit Clock = Generated Primary Bit Clock

Page 0 / Register 33: Audio Interface Setting Register 6 - 0x00 / 0x21 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R/W	00	WCLK Output Control 00: WCLK Output = Generated DAC_FS 01: Reserved. Do not use 10: WCLK Output = Secondary Word Clock Input 11: Reserved. Do not use
D3-D2	R/W	00	Secondary Word Clock Output Control 00: Secondary Word Clock output = WCLK input 01: Secondary Word Clock output = Generated DAC_FS 10-11: Reserved Do not use
D1	R/W	0	Primary Data Out output control (MFP2) 0: no Data output 1: Primary Data Output = Secondary Data Input (Loopback)
D0	R/W	0	Secondary Data Out output control (MFP4) 0: Secondary Data Output = DIN input (Loopback) 1: no Data output

5.2.34 Page 0 / Register 34: Digital Interface Misc. Setting Register - 0x00 / 0x22

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6	R	0	Reserved. Write only default value
D5	R/W	0	I2C General Call Address Configuration 0: I2C General Call Address will be ignored 1: I2C General Call Address accepted
D4-D0	R	0 0000	Reserved. Write only default values

5.2.35 Page 0 / Register 35-36: Reserved Register - 0x00 / 0x23-0x24

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default value

5.2.36 Page 0 / Register 37: DAC Flag Register 1 - 0x00 / 0x25

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Power Status Flag 0: Left DAC Powered Down 1: Left DAC Powered Up
D6	R	0	Reserved.
D5	R	0	Left Headphone Driver (HPL) Power Status Flag 0: HPL Powered Down 1: HPL Powered Up
D4	R	0	Reserved.
D3	R	0	Right DAC Power Status Flag 0: Right DAC Powered Down 1: Right DAC Powered Up
D2	R	0	Reserved.
D1	R	0	Right Headphone Driver (HPR) Power Status Flag 0: HPR Powered Down 1: HPR Powered Up
D0	R	0	Reserved.

5.2.37 Page 0 / Register 38: DAC Flag Register 2 - 0x00 / 0x26

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved.

Page 0 / Register 38: DAC Flag Register 2 - 0x00 / 0x26 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4	R	0	Left DAC PGA Status Flag 0: Gain applied in Left DAC PGA is not equal to Gain programmed in Control Register 1: Gain applied in Left DAC PGA is equal to Gain programmed in Control Register
D3-D1	R	000	Reserved.
D0	R	0	Right DAC PGA Status Flag 0: Gain applied in Right DAC PGA is not equal to Gain programmed in Control Register 1: Gain applied in Right DAC PGA is equal to Gain programmed in Control Register

5.2.38 Page 0 / Register 39-41: Reserved Register - 0x00 / 0x27-0x29

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.2.39 Page 0 / Register 42: Sticky Flag Register 1 - 0x00 / 0x2A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Left DAC 1: Overflow has happened in Left DAC since last read of this register
D6	R	0	Right DAC Overflow Status. This sticky flag will self clear on read 0: No overflow in Right DAC 1: Overflow has happened in Right DAC since last read of this register
D5-D0	R	0 0000	Reserved.

5.2.40 Page 0 / Register 43: Interrupt Flag Register 1 - 0x00 / 0x2B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Overflow Status. 0: No overflow in Left DAC 1: Overflow condition is present in Left ADC at the time of reading the register
D6	R	0	Right DAC Overflow Status. 0: No overflow in Right DAC 1: Overflow condition is present in Right DAC at the time of reading the register
D5-D4	R	00	Reserved.
D3	R	0	Left ADC Overflow Status. 0: No overflow in Left ADC 1: Overflow condition is present in Left ADC at the time of reading the register
D2	R	0	Right ADC Overflow Status. 0: No overflow in Right ADC 1: Overflow condition is present in Right ADC at the time of reading the register

5.2.41 Page 0 / Register 44: Sticky Flag Register 2 - 0x00 / 0x2C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Over Current Detect Flag 0: Over Current not detected on HPL 1: Over Current detected on HPL (will be cleared when the register is read)
D6	R	0	HPR Over Current Detect Flag 0: Over Current not detected on HPR 1: Over Current detected on HPR (will be cleared when the register is read)
D5	R	0	Headset Button Press 0: Button Press not detected 1: Button Press detected (will be cleared when the register is read)
D4	R	0	Headset Insertion/Removal Detect Flag 0: Insertion/Removal event not detected 1: Insertion/Removal event detected (will be cleared when the register is read)

Page 0 / Register 44: Sticky Flag Register 2 - 0x00 / 0x2C (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)
D2	R	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold (will be cleared when the register is read)
D1-D0	R	00	Reserved.

5.2.42 Page 0 / Register 45: Reserved Register - 0x00 / 0x2D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.2.43 Page 0 / Register 46: Interrupt Flag Register 2 - 0x00 / 0x2E

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Over Current Detect Flag 0: Over Current not detected on HPL 1: Over Current detected on HPL
D6	R	0	HPR Over Current Detect Flag 0: Over Current not detected on HPR 1: Over Current detected on HPR
D5	R	0	Headset Button Press 0: Button Press not detected 1: Button Press detected
D4	R	0	Headset Insertion/Removal Detect Flag 0: Headset removal detected 1: Headset insertion detected
D3	R	0	Left Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D2	R	0	Right Channel DRC, Signal Threshold Flag 0: Signal Power is below Signal Threshold 1: Signal Power exceeded Signal Threshold
D1-D0	R	00	Reserved.

5.2.44 Page 0 / Register 47: Reserved Register - 0x00 / 0x2F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	0000 0000	Reserved. Write only default values

5.2.45 Page 0 / Register 48: INT1 Interrupt Control Register - 0x00 / 0x30

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT1 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT1 interrupt 1: Headset Insertion even will generate a INT1 interrupt
D6	R/W	0	INT1 Interrupt for Button Press Event 0: Button Press event will not generate a INT1 interrupt 1: Button Press event will generate a INT1 interrupt
D5	R/W	0	INT1 Interrupt for DAC DRC Signal Threshold 0: DAC DRC Signal Power exceeding Signal Threshold will not generate a INT1 interrupt 1: DAC DRC Signal Power exceeding Signal Threshold for either of Left or Right Channel will generate a INT1 interrupt. Read Page-0, Register-44 to distinguish between Left or Right Channel
D4	R	0	Reserved. Write only default value

Page 0 / Register 48: INT1 Interrupt Control Register - 0x00 / 0x30 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R/W	0	INT1 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT1 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT1 interrupt. Read Page-0, Register-44 to distinguish between HPL and HPR
D2	R/W	0	INT1 Interrupt for overflow event 0: ADC or DAC data overflows does not result in a INT1 interrupt 1: ADC or DAC data overflow will result in a INT1 interrupt. Read Page-0, Register-42 to distinguish between ADC or DAC data overflow
D1	R	0	Reserved. Write only default value
D0	R/W	0	INT1 pulse control 0: INT1 is active high interrupt of 1 pulse of approx. 2ms duration 1: INT1 is active high interrupt of multiple pulses, each of duration 2ms. To stop the pulse train, read Page-0, Reg-42d, 44d or 45d

5.2.46 Page 0 / Register 49: INT2 Interrupt Control Register - 0x00 / 0x31

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	INT2 Interrupt for Headset Insertion Event 0: Headset Insertion event will not generate a INT2 interrupt 1: Headset Insertion even will generate a INT2 interrupt
D6	R/W	0	INT2 Interrupt for Button Press Event 0: Button Press event will not generate a INT2 interrupt 1: Button Press event will generate a INT2 interrupt
D5	R/W	0	INT2 Interrupt for DAC DRC Signal Threshold 0: DAC DRC Signal Power exceeding Signal Threshold will not generate a INT2 interrupt 1: DAC DRC Signal Power exceeding Signal Threshold for either of Left or Right Channel will generate a INT2 interrupt. Read Page-0, Register-44 to distinguish between Left or Right Channel
D4	R	0	Reserved. Write only default value
D3	R/W	0	INT2 Interrupt for Over Current Condition 0: Headphone Over Current condition will not generate a INT2 interrupt. 1: Headphone Over Current condition on either off Left or Right Channels will generate a INT2 interrupt. Read Page-0, Register-44 to distinguish between HPL and HPR
D2	R/W	0	INT2 Interrupt for overflow event 0: DAC data overflow will not result in a INT2 interrupt 1: DAC data overflow will result in a INT2 interrupt. Read Page-0, Register-42 on DAC data overflow details
D1	R	0	Reserved. Write only default value
D0	R/W	0	INT2 pulse control 0: INT2 is active high interrupt of 1 pulse of approx. 2ms duration 1: INT2 is active high interrupt of multiple pulses, each of duration 2ms. To stop the pulse train, read Page-0, Reg-42d, 44d and 45d

5.2.47 Page 0 / Register 50-51: Reserved Register - 0x00 / 0x32-0x33

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.2.48 Page 0 / Register 52: GPIO/MFP5 Control Register (** Availble only for WCSP Package) - 0x00 / 0x34

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values

Page 0 / Register 52: GPIO/MFP5 Control Register (Availble only for WCSP Package) - 0x00 / 0x34 (continued)**

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D2	R/W	0000	GPIO Control 0000: GPIO input/output disabled. 0001: GPIO input is used for secondary audio interface, digital microphone input or clock input. Configure other registers to choose the functionality of GPIO input 0010: GPIO is general purpose input 0011: GPIO is general purpose output 0100: GPIO output is CLKOUT 0101: GPIO output is INT1 0110: GPIO output is INT2 0111: GPIO output is ADC_WCLK for Audio Interface 1000: GPIO output is secondary bit-clock for Audio Interface 1001: GPIO output is secondary word-clock for Audio Interface 1010: GPIO output is clock for digital microphone 1011-1111: Reserved. Do not use.
D1	R	X	GPIO Input Pin state, used along with GPIO as general purpose input
D0	R/W	0	GPIO as general purpose output control 0: GPIO pin is driven to '0' in general purpose output mode 1: GPIO pin is driven to '1' in general purpose output mode

5.2.49 Page 0 / Register 53: MFP2 Function Control Register - 0x00 / 0x35

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values
D4	R/W	1	MFP2 Bus Keeper Control 0: MFP2 Bus Keeper Enabled 1: MFP2 Bus Keeper Disabled
D3-D1	R/W	001	MFP2 MUX Control 000: MFP2 disabled 001: MFP2 is Primary DOUT (Loopback data) 010: MFP2 is General Purpose Output 011: MFP2 is CLKOUT 100: MFP2 is INT1 101: MFP2 is INT2 110: MFP2 is Secondary BCLK 111: MFP2 is Secondary WCLK
D0	R/W	0	MFP2 as General Purpose Output 0: MFP2 General Purpose Output is '0' 1: MFP2 General Purpose Output is '1'

5.2.50 Page 0 / Register 54: DIN/MFP1 Function Control Register - 0x00 / 0x36

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0 0000	Reserved. Write only reserved values
D2-D1	R/W	01	DIN function control 00: DIN pin is disabled 01: DIN is enabled for Primary Data Input or Digital Microphone Input or General Purpose Clock input 10: DIN is used as General Purpose Input 11: Reserved. Do not use
D0	R	X	Value of DIN input pin. To be used when for General Purpose Input

5.2.51 Page 0 / Register 55: MISO/MFP4 Function Control Register - 0x00 / 0x37

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values

Page 0 / Register 55: MISO/MFP4 Function Control Register - 0x00 / 0x37 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D1	R/W	0001	MISO function control 0000: MISO buffer disabled 0001: MISO is used for data output in SPI interface, is disabled for I2C interface 0010: MISO is General Purpose Output 0011: MISO is CLKOUT output 0100: MISO is INT1 output 0101: MISO is INT2 output 0110: MISO is ADC Word Clock output 0111: MISO is clock output for Digital Microphone 1000: MISO is Secondary Data Output for Audio Interface 1001: MISO is Secondary Bit Clock for Audio Interface 1010: MISO is Secondary Word Clock for Audio Interface 1011-1111: Reserved. Do not use
D0	R/W	0	Value to be driven on MISO pin when used as General Purpose Output

5.2.52 Page 0 / Register 56: SCLK/MFP3 Function Control Register - 0x00 / 0x38

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0 0000	Reserved. Write only default values
D2-D1	R/W	01	SCLK function control 00: SCLK pin is disabled 01: SCLK pin is enabled for SPI clock in SPI Interface mode or when in I2C Interface enabled for Secondary Data Input or Secondary Bit Clock Input or Secondary Word Clock or Digital Microphone Input 10: SCLK is enabled as General Purpose Input 11: Reserved. Do not use
D0	R	X	Value of SCLK input pin when used as General Purpose Input

5.2.53 Page 0 / Register 57-59: Reserved Registers - 0x00 / 0x39-0x3B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.2.54 Page 0 / Register 60: DAC Signal Processing Block Control Register - 0x00 / 0x3C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values
D4-D0	R/W	0 0001	Selects the DAC (playback) signal processing block 0 0000: Reserved. Do not use 0 0001: DAC Signal Processing Block PRB_P1 0 0010: DAC Signal Processing Block PRB_P2 0 0011: DAC Signal Processing Block PRB_P3 0 0100: DAC Signal Processing Block PRB_P4 … 1 1000: DAC Signal Processing Block PRB_P24 1 1001: DAC Signal Processing Block PRB_P25 1 1010-1 1111: Reserved. Do not use Note; Please check the overview section for description of the Signal Processing Blocks

5.2.55 Page 0 / Register 61: Reserved Register - 0x00 / 0x3D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values

Page 0 / Register 61: Reserved Register - 0x00 / 0x3D (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4-D0	R/W	0 0001	0 0000: Reserved. Do not use 0 0001: ADC Singal Processing Block PRB_R1 0 0010: ADC Signal Processing Block PRB_R2 0 0011: ADC Signal Processing Block PRB_R3 0 0100: ADC Signal Processing Block PRB_R4 … 1 0001: ADC Signal Processing Block PRB_R17 1 0010: ADC Signal Processing Block PRB_R18 1 0010-1 1111: Reserved. Do not use Note: Please check the overview section for description of the Signal Processing Modes

5.2.56 Page 0 / Register 62: Reserved Register - 0x00 / 0x3E

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.2.57 Page 0 / Register 63: DAC Channel Setup Register 1 - 0x00 / 0x3F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Channel Power Control 0: Left DAC Channel Powered Down 1: Left DAC Channel Powered Up
D6	R/W	0	Right DAC Channel Power Control 0: Right DAC Channel Powered Down 1: Right DAC Channel Powered Up
D5-D4	R/W	01	Left DAC Data path Control 00: Left DAC data is disabled 01: Left DAC data Left Channel Audio Interface Data 10: Left DAC data is Right Channel Audio Interface Data 11: Left DAC data is Mono Mix of Left and Right Channel Audio Interface Data
D3-D2	R/W	01	Right DAC Data path Control 00: Right DAC data is disabled 01: Right DAC data Right Channel Audio Interface Data 10: Right DAC data is Left Channel Audio Interface Data 11: Right DAC data is Mono Mix of Left and Right Channel Audio Interface Data
D1-D0	R/W	00	DAC Channel Volume Control's Soft-Step control 00: Soft-Stepping is 1 step per 1 DAC Word Clock 01: Soft-Stepping is 1 step per 2 DAC Word Clocks 10: Soft-Stepping is disabled 11: Reserved. Do not use

5.2.58 Page 0 / Register 64: DAC Channel Setup Register 2 - 0x00 / 0x40

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right Modulator Output Control 0: When Right DAC Channel is powered down, the data is zero. 1: When Right DAC Channel is powered down, the data is inverted version of Left DAC Modulator Output. Can be used when differential mono output is used
D6-D4	R/W	000	DAC Auto Mute Control 000: Auto Mute disabled 001: DAC is auto muted if input data is DC for more than 100 consecutive inputs 010: DAC is auto muted if input data is DC for more than 200 consecutive inputs 011: DAC is auto muted if input data is DC for more than 400 consecutive inputs 100: DAC is auto muted if input data is DC for more than 800 consecutive inputs 101: DAC is auto muted if input data is DC for more than 1600 consecutive inputs 110: DAC is auto muted if input data is DC for more than 3200 consecutive inputs 111: DAC is auto muted if input data is DC for more than 6400 consecutive inputs
D3	R/W	1	Left DAC Channel Mute Control 0: Left DAC Channel not muted 1: Left DAC Channel muted

Page 0 / Register 64: DAC Channel Setup Register 2 - 0x00 / 0x40 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2	R/W	1	Right DAC Channel Mute Control 0: Right DAC Channel not muted 1: Right DAC Channel muted
D1-D0	R/W	00	DAC Master Volume Control 00: Left and Right Channel have independent volume control 01: Left Channel Volume is controlled by Right Channel Volume Control setting 10: Right Channel Volume is controlled by Left Channel Volume Control setting 11: Reserved. Do not use

5.2.59 Page 0 / Register 65: Left DAC Channel Digital Volume Control Register - 0x00 / 0x41

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Left DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB … 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use

5.2.60 Page 0 / Register 66: Right DAC Channel Digital Volume Control Register - 0x00 / 0x42

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Right DAC Channel Digital Volume Control Setting 0111 1111-0011 0001: Reserved. Do not use 0011 0000: Digital Volume Control = +24dB 0010 1111: Digital Volume Control = +23.5dB … 0000 0001: Digital Volume Control = +0.5dB 0000 0000: Digital Volume Control = 0.0dB 1111 1111: Digital Volume Control = -0.5dB ... 1000 0010: Digital Volume Control = -63dB 1000 0001: Digital Volume Control = -63.5dB 1000 0000: Reserved. Do not use

5.2.61 Page 0 / Register 67: Headset Detection Configuration Register - 0x00 / 0x43

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset Detection Disabled 1: Headset Detection Enabled
D6-D5	R	00	Headset Type Flag 00: Headset not detected 01: Stereo Headset detected 10: Reserved 11: Stereo + Cellular Headset detected
D4-D2	R/W	000	Headset Detection Debounce Programmability 000: Debounce Time = 16ms 001: Debounce Time = 32ms 010: Debounce Time = 64ms 011: Debounce Time = 128ms 100: Debounce Time = 256ms 101: Debounce Time = 512ms 110-111: Reserved. Do not use Note: All times are typical values

Page 0 / Register 67: Headset Detection Configuration Register - 0x00 / 0x43 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1-D0	R/W	00	Headset Button Press Debounce Programmability 00: Debounce disabled 01: Debounce Time = 8ms 10: Debounce Time = 16ms 11: Debounce Time = 32ms Note: All times are typical values

5.2.62 Page 0 / Register 68: DRC Control Register 1 - 0x00 / 0x44

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value
D6	R/W	1	DRC Enable Control 0: Left Channel DRC disabled 1: Left Channel DRC enabled
D5	R/W	1	DRC Enable Control 0: Right Channel DRC disabled 1: Right Channel DRC enabled
D4-D2	R/W	011	DRC Threshold control 000: DRC Threshold = -3dBFS 001: DRC Threshold = -6dBFS 010: DRC Threshold = -9dBFS 011: DRC Threshold = -12dBFS 100: DRC Threshold = -15dBFS 101: DRC Threshold = -18dBFS 110: DRC Threshold = -21dBFS 111: DRC Threshold = -24dBFS
D1-D0	R/W	11	DRC Hysteresis Control 00: DRC Hysteresis = 0dB 01: DRC Hysteresis = 1dB 10: DRC Hysteresis = 2dB 11: DRC Hysteresis = 3dB

5.2.63 Page 0 / Register 69: DRC Control Register 2 - 0x00 / 0x45

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6-D3	R/W	0111	DRC Hold Programmability 0000: DRC Hold Disabled 0001: DRC Hold Time = 32 DAC Word Clocks 0010: DRC Hold Time = 64 DAC Word Clocks 0011: DRC Hold Time = 128 DAC Word Clocks 0100: DRC Hold Time = 256 DAC Word Clocks 0101: DRC Hold Time = 512 DAC Word Clocks ... 1110: DRC Hold Time = 4*32768 DAC Word Clocks 1111: DRC Hold Time = 5*32768 DAC Word Clocks
D2-D0	R/W	000	Reserved. Write only default values

5.2.64 Page 0 / Register 70: DRC Control Register 3 - 0x00 / 0x46

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	DRC Attack Rate control 0000: DRC Attack Rate = 4.0dB per DAC Word Clock 0001: DRC Attack Rate = 2.0dB per DAC Word Clock 0010: DRC Attack Rae = 1.0dB per DAC Word Clock … 1110: DRC Attack Rate = 2.4414e-4dB per DAC Word Clock 1111: DRC Attack Rate = 1.2207e-4dB per DAC Word Clock

Page 0 / Register 70: DRC Control Register 3 - 0x00 / 0x46 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3-D0	R/W	0000	DRC Decay Rate control 0000: DRC Decay Rate = 1.5625e-2dB per DAC Word Clock 0001: DRC Decay Rate = 7.8125e-3dB per DAC Word Clock 0010: DRC Decay Rae = 3.9062e-3dB per DAC Word Clock … 1110: DRC Decay Rate = 9.5367e-7dB per DAC Word Clock 1111: DRC Decay Rate = 4.7683e-7dB per DAC Word Clock

5.2.65 Page 0 / Register 71: Beep Generator Register 1 - 0x00 / 0x47

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Beep Generator Disabled 1: Beep Generator Enabled. This bit will self clear after the beep has been generated.
D6	R	0	Reserved. Write only default value
D5-D0	R/W	00 0000	Left Channel Beep Volume Control 00 0000: Left Channel Beep Volume = 0dB 00 0001: Left Channel Beep Volume = -1dB … 11 1110: Left Channel Beep Volume = -62dB 11 1111: Left Channel Beep Volume = -63dB

5.2.66 Page 0 / Register 72: Beep Generator Register 2 - 0x00 / 0x48

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	Beep Generator Master Volume Control Setting 00: Left and Right Channels have independent Volume Settings 01: Left Channel Beep Volume is the same as programmed for Right Channel 10: Right Channel Beep Volume is the same as programmed for Left Channel 11: Reserved. Do not use
D5-D0	R	00 0000	Right Channel Beep Volume Control 00 0000: Right Channel Beep Volume = 0dB 00 0001: Right Channel Beep Volume = -1dB … 11 1110: Right Channel Beep Volume = -62dB 11 1111: Right Channel Beep Volume = -63dB

5.2.67 Page 0 / Register 73: Beep Generator Register 3 - 0x00 / 0x49

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Programmed value is Beep Sample Length(23:16)

5.2.68 Page 0 / Register 74: Beep Generator Register 4 - 0x00 / 0x4A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Programmed value is Beep Sample Length(15:8)

5.2.69 Page 0 / Register 75: Beep Generator Register 5 - 0x00 / 0x4B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1110 1110	Programmed value is Beep Sample Length(7:0)

5.2.70 Page 0 / Register 76: Beep Generator Register 6 - 0x00 / 0x4C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0001 0000	Programmed Value is Beep Sin(x)(15:8), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.71 Page 0 / Register 77: Beep Generator Register 7 - 0x00 / 0x4D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1101 1000	Programmed Value is Beep Sin(x)(7:0), where Sin(x) = sin(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.72 Page 0 / Register 78: Beep Generator Register 8 - 0x00 / 0x4E

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0111 1110	Programmed Value is Beep Cos(x)(15:8), where Cos(x) = cos(2*pi*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.73 Page 0 / Register 79: Beep Generator Register 9 - 0x00 / 0x4F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	1110 0011	Programmed Value is Beep Cos(x)(7:0), where Cos(x) = cos(2*π*Fin/Fs), where Fin is desired beep frequency and Fs is DAC sample rate

5.2.74 Page 0 / Register 80: Reserved Register - 0x00 / 0x50

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
x	0	81	Reserved Register
D7	R/W	0	Left Channel ADC Power Control 0: Left Channel ADC is powered down 1: Left Channel ADC is powered up
D6	R/W	0	Right Channel ADC Power Control 0: Right Channel ADC is powered down 1: Right Channel ADC is powered up
D5-D4	R/W	00	Digital Microphone Input Configuration 00: GPIO serves as Digital Microphone Input (** Availble only for WCSP Package) 01: SCLK serves as Digital Microphone Input 10: DIN serves as Digital Microphone Input 11: Reserved. Do not use
D3	R/W	0	Left Channel Digital Microphone Power Control 0: Left Channel ADC not configured for Digital Microphone 1: Left Channel ADC configured for Digital Microphone
D2	R/W	0	Right Channel Digital Microphone Power Control 0: Right Channel ADC not configured for Digital Microphone 1: Right Channel ADC configured for Digital Microphone
D1-D0	R/W	00	ADC Volume Control Soft-Stepping Control 00: ADC Volume Control changes by 1 gain step per ADC Word Clock 01: ADC Volume Control changes by 1 gain step per two ADC Word Clocks 10: ADC Volume Control Soft-Stepping disabled 11: Reserved. Do not use

5.2.75 Page 0 / Register 82: Reserved Register - 0x00 / 0x52

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left ADC Channel Mute Control 0: Left ADC Channel Un-muted 1: Left ADC Channel Muted
D6-D4	R/W	000	Left ADC Channel Fine Gain Adjust 000: Left ADC Channel Fine Gain = 0dB 111: Left ADC Channel Fine Gain = -0.1dB 110: Left ADC Channel Fine Gain = -0.2dB 101: Left ADC Channel Fine Gain = -0.3dB 100: Left ADC Channel Fine Gain = -0.4dB 001-011: Reserved. Do not use
D3	R/W	1	Right ADC Channel Mute Control 0: Right ADC Channel Un-muted 1: Right ADC Channel Muted
D2-D0	R/W	000	Right ADC Channel Fine Gain Adjust 000: Right ADC Channel Fine Gain = 0dB 111: Right ADC Channel Fine Gain = -0.1dB 110: Right ADC Channel Fine Gain = -0.2dB 101: Right ADC Channel Fine Gain = -0.3dB 100: Right ADC Channel Fine Gain = -0.4dB 001-011: Reserved. Do not use

5.2.76 Page 0 / Register 83: Left ADC Channel Volume Control Register - 0x00 / 0x53

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6-D0	R/W	000 0000	Left ADC Channel Volume Control 000 0000-110 0111: Reserved. Do not use 110 1000: Left ADC Channel Volume = -12dB 110 1001: Left ADC Channel Volume = -11.5dB 110 1010: Left ADC Channel Volume = -11.0dB … 111 1111: Left ADC Channel Volume = -0.5dB 000 0000: Left ADC Channel Volume = 0.0dB 000 0001: Left ADC Channel Volume = 0.5dB ... 010 0110: Left ADC Channel Volume = 19.0dB 010 0111: Left ADC Channel Volume = 19.5dB 010 1000: Left ADC Channel Volume = 20.0dB 010 1001-111 1111: Reserved. Do not use

5.2.77 Page 0 / Register 84: Right ADC Channel Volume Control Register - 0x00 / 0x54

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default values
D6-D0	R/W	000 0000	Right ADC Channel Volume Control 000 0000-110 0111: Reserved. Do not use 110 1000: Left ADC Channel Volume = -12dB 110 1001: Left ADC Channel Volume = -11.5dB 110 1010: Left ADC Channel Volume = -11.0dB … 111 1111: Left ADC Channel Volume = -0.5dB 000 0000: Left ADC Channel Volume = 0.0dB 000 0001: Left ADC Channel Volume = 0.5dB ... 010 0110: Left ADC Channel Volume = 19.0dB 010 0111: Left ADC Channel Volume = 19.5dB 010 1000: Left ADC Channel Volume = 20.0dB 010 1001-111 1111: Reserved. Do not use

5.2.78 Page 0 / Register 85: ADC Phase Adjust Register - 0x00 / 0x55

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	ADC Phase Compensation Control 1000 0000-1111 1111: Left ADC Channel Data is delayed with respect to Right ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section. 0000 0000: Left and Right ADC Channel data are not delayed with respect to each other 0000 0001-0111 1111: Right ADC Channel Data is delayed with respect to Left ADC Channel Data. For details of delayed amount please refer to the description of Phase Compensation in the Overview section.

5.2.79 Page 0 / Register 80-127: Reserved Register - 0x00 / 0x50-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Do not use

5.3 Page 1 Registers

5.3.1 Page 1 / Register 0: Page Select Register - 0x01 / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.3.2 Page 1 / Register 1: Power Configuration Register - 0x01 / 0x01

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only default values
D3	R/W	0	0: AVDD will be weakly connected to DVDD. Use when DVDD is powered, but AVDD LDO is powered down and AVDD is not externally powered 1: Disabled weak connection of AVDD with DVDD
D2-D0	R	000	Reserved. Write only default values

5.3.3 Page 1 / Register 2: LDO Control Register - 0x01 / 0x02

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values
D5-D4	R/W	00	AVDD LDO Control 00: AVDD LDO output is nominally 1.72V 01: AVDD LDO output is nominally 1.67V 10: AVDD LDO output is nominally 1.77V 11: Do not use
D3	R/W	1	Analog Block Power Control 0: Analog Blocks Enabled 1: Analog Blocks Disabled
D2	R	0	Offset Correction Flag 0: Offset Correction not completed 1: Offset Correction completed
D1	R	0	AVDD LDO Over Current Detect 0: Over Current not detected for AVDD LDO 1: Over Current detected for AVDD LDO
D0	R/W	0	AVDD LDO Power Control 0: AVDD LDO Powered down 1: AVDD LDO Powered up

5.3.4 Page 1 / Register 3: Playback Configuration Register 1 - 0x01 / 0x03

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	00: Left DAC routing to HPL uses Class-AB driver 01-10: Reserved. Do not use 11: Left DAC routing to HPL uses Class-D driver
D5	R	0	Reserved. Write only default value
D4-D2	R/W	000	Left DAC PTM Control 000: Left DAC in mode PTM_P3, PTM_P4 001: Left DAC in mode PTM_P2 010: Left DAC in mode PTM_P1 011-111: Reserved. Do not use
D1-D0	R	00	Reserved. Write only default value

5.3.5 Page 1 / Register 4: Playback Configuration Register 2 - 0x01 / 0x04

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	00: Right DAC routing to HPL uses Class-AB driver 01-10: Reserved. Do not use 11: Right DAC routing to HPL uses Class-D driver
D5	R	0	Reserved. Write only default value
D4-D2	R/W	000	Right DAC PTM Control 000: Right DAC in mode PTM_P3, PTM_P4 001: Right DAC in mode PTM_P2 010: Right DAC in mode PTM_P1 011-111: Reserved. Do not use
D1-D0	R	00	Reserved. Write only default value

5.3.6 Page 1 / Register 5-8: Reserved Register - 0x01 / 0x05-0x08

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.7 Page 1 / Register 9: Output Driver Power Control Register - 0x01 / 0x09

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default value
D5	R/W	0	0: HPL is powered down 1: HPL is powered up
D4	R/W	0	0: HPR is powered down 1: HPR is powered up
D3-D0	R	000	Reserved. Write only default value

5.3.8 Page 1 / Register 10: Common Mode Control Register - 0x01 / 0x0A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	0	0: Full Chip Common Mode is 0.9V 1: Full Chip Common Mode is 0.75V
D5-D4	R/W	00	00: Output Common Mode for HPL & HPR is same as full-chip common mode 01: Output Common Mode for HPL & HPR is 1.25V 10: Output Common Mode for HPL & HPR is 1.5V 11: Output Common Mode for HPL & HPR is 1.65V if D6=0, 1.5V if D6=1
D3-D2	R	00	Reserved. Write only default value
D1	R/W	0	0: Output of HPL & HPR is powered with AVDD supply 1: Output of HPL & HPR is powered with LDOIN supply
D0	R/W	0	0: When Page-1, Reg-10, D1=1, then LDOIN input range is 1.5V to 1.95V 1: When Page-1, Reg-10, D1=1, then LDOIN input range is 1.8V to 3.6V

5.3.9 Page 1 / Register 11: Over Current Protection Configuration Register - 0x01 / 0x0B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values
D4	R/W	1	0: Over Current detection is disabled for HPL & HPR 1: Over Current detection is enabled for HPL & HPR
D3-D1	R/W	000	000: No debounce is used for Over Current detection 001: Over Current detection is debounced by 8ms 010: Over Current detection is debounce by 16ms 011: Over Current detection is debounced by 32ms 100: Over Current detection is debounced by 64ms 101: Over Current detection is debounced by 128ms 110: Over Current detection is debounced by 256ms 111: Over Current detection is debounced by 512ms
D0	R/W	0	0: Output current will be limited if over current condition is detected 1: Output driver will be powered down if over current condition is detected

5.3.10 Page 1 / Register 12: HPL Routing Selection Register - 0x01 / 0x0C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R	0000	Reserved. Write only default values
D3	R/W	0	0: Left Channel DAC reconstruction filter's positive terminal is not routed to HPL 1: Left Channel DAC reconstruction filter's positive terminal is routed to HPL
D2	R/W	0	0: IN1L is not routed to HPL 1: IN1L is routed to HPL
D1-D0	R/W	00	Reserved. Write only default values

5.3.11 Page 1 / Register 13: HPR Routing Selection Register - 0x01 / 0x0D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Reserved. Write only default values
D4	R/W	0	0: Left Channel DAC reconstruction filter's negative terminal is not routed to HPR 1: Left Channel DAC reconstruction filter's negative terminal is routed to HPR
D3	R/W	0	0: Right Channel DAC reconstruction filter's positive terminal is not routed to HPR 1: Right Channel DAC reconstruction filter's positive terminal is routed to HPR
D2	R/W	0	0: IN1R is not routed to HPR 1: IN1R is routed to HPR
D1-D0	R/W	00	Reserved. Write only default values

5.3.12 Page 1 / Register 14-15: Reserved Register - 0x01 / 0x0E-0x0F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.13 Page 1 / Register 16: HPL Driver Gain Setting Register - 0x01 / 0x10

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	1	0: HPL driver is not muted 1: HPL driver is muted

Page 1 / Register 16: HPL Driver Gain Setting Register - 0x01 / 0x10 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D0	R/W	00 0000	10 0000-11 1001: Reserved. Do not use 11 1010: HPL driver gain is -6dB (Note: It is not possible to mute HPR while programmed to -6dB) 11 1011: HPL driver gain is -5dB 11 1100: HPL driver gain is -4dB … 00 0000: HPL driver gain is 0dB ... 01 1011: HPL driver gain is 27dB 01 1100: HPL driver gain is 28dB 01 1101: HPL driver gain is 29dB 01 1110-01 1111: Reserved. Do not use Note: These gains are not valid while using the driver in Class-D mode

5.3.14 Page 1 / Register 17: HPR Driver Gain Setting Register - 0x01 / 0x11

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	1	0: HPR driver is not muted 1: HPR driver is muted
D5-D0	R/W	00 0000	10 0000-11 1001: Reserved. Do not use 11 1010: HPR driver gain is -6dB (Note: It is not possible to mute HPR while programmed to -6dB) 11 1011: HPR driver gain is -5dB 11 1100: HPR driver gain is -4dB … 00 0000: HPR driver gain is 0dB ... 01 1011: HPR driver gain is 27dB 01 1100: HPR driver gain is 28dB 01 1101: HPR driver gain is 29dB 01 1110-01 1111: Reserved. Do not use Note: These gains are not valid while using the driver in Class-D mode

5.3.15 Page 1 / Register 18-19: Reserved Register - 0x01 / 0x12-0x13

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0100 0000	Reserved. Write only default value.

5.3.16 Page 1 / Register 20: Headphone Driver Startup Control Register - 0x01 / 0x14

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	00: Soft routing step time is 0ms 01: Soft routing step time is 50ms 10: Soft routing step time is 100ms 11: Soft routing step time is 200ms

Page 1 / Register 20: Headphone Driver Startup Control Register - 0x01 / 0x14 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D2	R/W	0000	0000: Slow power up of headphone amp's is disabled 0001: Headphone amps power up slowly in 0.5 time constants 0010: Headphone amps power up slowly in 0.625 time constants 0011; Headphone amps power up slowly in 0.725 time constants 0100: Headphone amps power up slowly in 0.875 time constants 0101: Headphone amps power up slowly in 1.0 time constants 0110: Headphone amps power up slowly in 2.0 time constants 0111: Headphone amps power up slowly in 3.0 time constants 1000: Headphone amps power up slowly in 4.0 time constants 1001: Headphone amps power up slowly in 5.0 time constants 1010: Headphone amps power up slowly in 6.0 time constants 1011: Headphone amps power up slowly in 7.0 time constants 1100: Headphone amps power up slowly in 8.0 time constants 1101: Headphone amps power up slowly in 16.0 time constants (do not use for Rchg=25K) 1110: Headphone amps power up slowly in 24.0 time constants (do not use for Rchg=25K) 1111: Headphone amps power up slowly in 32.0 time constants (do not use for Rchg=25K) Note: Time constants assume 47uF decoupling cap
D1-D0	R/W	00	00: Headphone amps power up time is determined with 25K resistance 01: Headphone amps power up time is determined with 6K resistance 10: Headphone amps power up time is determined with 2K resistance 11: Reserved. Do not use

5.3.17 Page 1 / Register 21: Reserved Register - 0x01 / 0x15

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.18 Page 1 / Register 22: INL to HPL Volume Control Register - 0x01 / 0x16

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.

Page 1 / Register 22: INL to HPL Volume Control Register - 0x01 / 0x16 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0000	IN1L to HPL Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = -0.5dB 000 0010: Volume Control = -1.0dB 000 0011: Volume Control = -1.5dB 000 0100: Volume Control = -2.0dB 000 0101: Volume Control = -2.5dB 000 0110: Volume Control = -3.0dB 000 0111: Volume Control = -3.5dB 000 1000: Volume Control = -4.0dB 000 1001: Volume Control = -4.5dB 000 1010: Volume Control = -5.0dB 000 1011: Volume Control = -5.5dB 000 1100: Volume Control = -6.0dB 000 1101: Volume Control = -7.0dB 000 1110: Volume Control = -8.0dB 000 1111: Volume Control = -8.5dB 001 0000: Volume Control = -9.0dB 001 0001: Volume Control = -9.5dB 001 0010: Volume Control = -10.0dB 001 0011: Volume Control = -10.5dB 001 0100: Volume Control = -11.0dB 001 0101: Volume Control = -11.5dB 001 0110: Volume Control = -12.0dB 001 0111: Volume Control = -12.5dB 001 1000: Volume Control = -13.0dB 001 1001: Volume Control = -13.5dB 001 1010: Volume Control = -14.0dB 001 1011: Volume Control = -14.5dB 001 1100: Volume Control = -15.0dB 001 1101: Volume Control = -15.5dB 001 1110: Volume Control = -16.0dB 001 1111: Volume Control = -16.5dB 010 0000: Volume Control = -17.1dB 010 0001: Volume Control = -17.5dB 010 0010: Volume Control = -18.1dB 010 0011: Volume Control = -18.6dB 010 0100: Volume Control = -19.1dB 010 0101: Volume Control = -19.6dB 010 0110: Volume Control = -20.1dB 010 0111: Volume Control = -20.6dB 010 1000: Volume Control = -21.1dB 010 1001: Volume Control = -21.6dB 010 1010: Volume Control = -22.1dB 010 1011: Volume Control = -22.6dB 010 1100: Volume Control = -23.1dB 010 1101: Volume Control = -23.6dB 010 1110: Volume Control = -24.1dB 010 1111: Volume Control = -24.6dB 011 0000: Volume Control = -25.1dB 011 0001: Volume Control = -25.6dB 011 0010: Volume Control = -26.1dB 011 0011: Volume Control = -26.6dB 011 0100: Volume Control = -27.1dB 011 0101: Volume Control = -27.6dB 011 0110: Volume Control = -28.1dB 011 0111: Volume Control = -28.6dB 011 1000: Volume Control = -29.1dB 011 1001: Volume Control = -29.6dB 011 1010: Volume Control = -30.1dB 011 1011: Volume Control = -30.6dB 011 1100: Volume Control = -31.1dB 011 1100: Volume Control = -31.6dB 011 1101: Volume Control = -32.1dB 011 1110: Volume Control = -32.6dB 011 1111: Volume Control = -33.1dB 100 0000: Volume Control = -33.6dB 100 0001: Volume Control = -34.1dB

Page 1 / Register 22: INL to HPL Volume Control Register - 0x01 / 0x16 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -34.6dB 100 0011: Volume Control = -35.2dB 100 0100: Volume Control = -35.7dB 100 0101: Volume Control = -36.2dB 100 0110: Volume Control = -36.7dB 100 0111: Volume Control = -37.2dB 100 1000: Volume Control = -37.7dB 100 1001: Volume Control = -38.2dB 100 1010: Volume Control = -38.7dB 100 1011: Volume Control = -39.2dB 100 1100: Volume Control = -39.7dB 100 1101: Volume Control = -40.2dB 100 1110: Volume Control = -40.7dB 100 1111: Volume Control = -41.2dB 101 0000: Volume Control = -41.7dB 101 0001: Volume Control = -42.1dB 101 0010: Volume Control = -42.7dB 101 0011: Volume Control = -43.2dB 101 0100: Volume Control = -43.8dB 101 0101: Volume Control = -44.3dB 101 0110: Volume Control = -44.8dB 101 0111: Volume Control = -45.2dB 101 1000: Volume Control = -45.8dB 101 1001: Volume Control = -46.2dB 101 1010: Volume Control = -46.7dB 101 1011: Volume Control = -47.4dB 101 1100: Volume Control = -47.9dB 101 1101: Volume Control = -48.2dB 101 1110: Volume Control = -48.7dB 101 1111: Volume Control = -49.3dB 110 0000: Volume Control = -50.0dB 110 0001: Volume Control = -50.3dB 110 0010: Volume Control = -51.0dB 110 0011: Volume Control = -51.42dB 110 0100: Volume Control = -51.82dB 110 0101: Volume Control = -52.3dB 110 0110: Volume Control = -52.7dB 110 0111: Volume Control = -53.7dB 110 1000: Volume Control = -54.2dB 110 1001: Volume Control = -55.4dB 110 1010: Volume Control = -56.7dB 110 1011: Volume Control = -58.3dB 110 1100: Volume Control = -60.2dB 110 1101: Volume Control = -62.7dB 110 1110: Volume Control = -64.3dB 110 1111: Volume Control = -66.2dB 111 0000: Volume Control = -68.7dB 111 0001: Volume Control = -72.3dB 111 0010: Volume Control = MUTE 111 0011-111 1111: Reserved. Do not use

5.3.19 Page 1 / Register 23: INR to HPR Volume Control Register - 0x01 / 0x17

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value

Page 1 / Register 23: INR to HPR Volume Control Register - 0x01 / 0x17 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	000 0000	INR to HPR Volume Control 000 0000: Volume Control = 0.0dB 000 0001: Volume Control = -0.5dB 000 0010: Volume Control = -1.0dB 000 0011: Volume Control = -1.5dB 000 0100: Volume Control = -2.0dB 000 0101: Volume Control = -2.5dB 000 0110: Volume Control = -3.0dB 000 0111: Volume Control = -3.5dB 000 1000: Volume Control = -4.0dB 000 1001: Volume Control = -4.5dB 000 1010: Volume Control = -5.0dB 000 1011: Volume Control = -5.5dB 000 1100: Volume Control = -6.0dB 000 1101: Volume Control = -7.0dB 000 1110: Volume Control = -8.0dB 000 1111: Volume Control = -8.5dB 001 0000: Volume Control = -9.0dB 001 0001: Volume Control = -9.5dB 001 0010: Volume Control = -10.0dB 001 0011: Volume Control = -10.5dB 001 0100: Volume Control = -11.0dB 001 0101: Volume Control = -11.5dB 001 0110: Volume Control = -12.0dB 001 0111: Volume Control = -12.5dB 001 1000: Volume Control = -13.0dB 001 1001: Volume Control = -13.5dB 001 1010: Volume Control = -14.0dB 001 1011: Volume Control = -14.5dB 001 1100: Volume Control = -15.0dB 001 1101: Volume Control = -15.5dB 001 1110: Volume Control = -16.0dB 001 1111: Volume Control = -16.5dB 010 0000: Volume Control = -17.1dB 010 0001: Volume Control = -17.5dB 010 0010: Volume Control = -18.1dB 010 0011: Volume Control = -18.6dB 010 0100: Volume Control = -19.1dB 010 0101: Volume Control = -19.6dB 010 0110: Volume Control = -20.1dB 010 0111: Volume Control = -20.6dB 010 1000: Volume Control = -21.1dB 010 1001: Volume Control = -21.6dB 010 1010: Volume Control = -22.1dB 010 1011: Volume Control = -22.6dB 010 1100: Volume Control = -23.1dB 010 1101: Volume Control = -23.6dB 010 1110: Volume Control = -24.1dB 010 1111: Volume Control = -24.6dB 011 0000: Volume Control = -25.1dB 011 0001: Volume Control = -25.6dB 011 0010: Volume Control = -26.1dB 011 0011: Volume Control = -26.6dB 011 0100: Volume Control = -27.1dB 011 0101: Volume Control = -27.6dB 011 0110: Volume Control = -28.1dB 011 0111: Volume Control = -28.6dB 011 1000: Volume Control = -29.1dB 011 1001: Volume Control = -29.6dB 011 1010: Volume Control = -30.1dB 011 1011: Volume Control = -30.6dB 011 1100: Volume Control = -31.1dB 011 1100: Volume Control = -31.6dB 011 1101: Volume Control = -32.1dB 011 1110: Volume Control = -32.6dB 011 1111: Volume Control = -33.1dB 100 0000: Volume Control = -33.6dB 100 0001: Volume Control = -34.1dB

Page 1 / Register 23: INR to HPR Volume Control Register - 0x01 / 0x17 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
			100 0010: Volume Control = -34.6dB 100 0011: Volume Control = -35.2dB 100 0100: Volume Control = -35.7dB 100 0101: Volume Control = -36.2dB 100 0110: Volume Control = -36.7dB 100 0111: Volume Control = -37.2dB 100 1000: Volume Control = -37.7dB 100 1001: Volume Control = -38.2dB 100 1010: Volume Control = -38.7dB 100 1011: Volume Control = -39.2dB 100 1100: Volume Control = -39.7dB 100 1101: Volume Control = -40.2dB 100 1110: Volume Control = -40.7dB 100 1111: Volume Control = -41.2dB 101 0000: Volume Control = -41.7dB 101 0001: Volume Control = -42.1dB 101 0010: Volume Control = -42.7dB 101 0011: Volume Control = -43.2dB 101 0100: Volume Control = -43.8dB 101 0101: Volume Control = -44.3dB 101 0110: Volume Control = -44.8dB 101 0111: Volume Control = -45.2dB 101 1000: Volume Control = -45.8dB 101 1001: Volume Control = -46.2dB 101 1010: Volume Control = -46.7dB 101 1011: Volume Control = -47.4dB 101 1100: Volume Control = -47.9dB 101 1101: Volume Control = -48.2dB 101 1110: Volume Control = -48.7dB 101 1111: Volume Control = -49.3dB 110 0000: Volume Control = -50.0dB 110 0001: Volume Control = -50.3dB 110 0010: Volume Control = -51.0dB 110 0011: Volume Control = -51.42dB 110 0100: Volume Control = -51.82dB 110 0101: Volume Control = -52.3dB 110 0110: Volume Control = -52.7dB 110 0111: Volume Control = -53.7dB 110 1000: Volume Control = -54.2dB 110 1001: Volume Control = -55.4dB 110 1010: Volume Control = -56.7dB 110 1011: Volume Control = -58.3dB 110 1100: Volume Control = -60.2dB 110 1101: Volume Control = -62.7dB 110 1110: Volume Control = -64.3dB 110 1111: Volume Control = -66.2dB 111 0000: Volume Control = -68.7dB 111 0001: Volume Control = -72.3dB 111 0010: Volume Control = MUTE 111 0011-111 1111: Reserved. Do not use

5.3.20 Page 1 / Register 24-50: Reserved Register - 0x01 / 0x18-0x32

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.21 Page 1 / Register 51: MICBIAS Configuration Register - 0x01 / 0x33

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Reserved. Write only default value.
D6	R/W	0	0: MICBIAS powered down 1: MICBIAS powered up

Page 1 / Register 51: MICBIAS Configuration Register - 0x01 / 0x33 (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D5-D4	R/W	00	MICBIAS Output Voltage Configuration 00: MICBIAS = 1.04V (CM=0.75V) or MICBIAS = 1.25V(CM=0.9V) 01: MICBIAS = 1.425V(CM=0.75V) or MICBIAS = 1.7V(CM=0.9V) 10: MICBIAS = 2.075V(CM=0.75V) or MICBIAS = 2.5V(CM=0.9V) 11: MICBIAS is switch to power supply
D3	R/W	0	0: MICBIAS voltage is generated from AVDD 1: MICBIAS voltage is generated from LDOIN
D2-D0	R	000	Reserved. Write only default value.

5.3.22 Page 1 / Register 52-57: Reserved Register - 0x01 / 0x34-0x39

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.23 Page 1 / Register 58: Analog Input Settings - 0x01 / 0x3A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Not routed INL settings 0: INL is floated if not routed to HPL 1: INL is connected to CM if not routed to HPL
D6	R/W	0	Not routed INR settings 0: INR is floated if not routed to HPR 1: INR is connected to CM if not routed to HPR
D5-D0	R	00 0000	Reserved. Write only default value.

5.3.24 Page 1 / Register 59-62: Reserved Register - 0x01 / 0x3B-0x3E

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	1000 0000	Reserved. Write only default values

5.3.25 Page 1 / Register 63: DAC Analog Gain Control Flag Register - 0x01 / 0x3F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPL Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D6	R	0	HPR Gain Flag 0: Applied Gain is not equal to Programmed Gain 1: Applied Gain is equal to Programmed Gain
D5-D4	R	00	Reserved. Write only default values
D3	R	0	IN1L to HPL Bypass Volume Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D2	R	0	IN1R to HPR Bypass Volume Flag 0: Applied Volume is not equal to Programmed Volume 1: Applied Volume is equal to Programmed Volume
D1-D0	R	00	Reserved. Write only default values

5.3.26 Page 1 / Register 64-70: Reserved Register - 0x01 / 0x40-0x46

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.27 Page 1 / Register 71: Analog Input Quick Charging Configuration Register - 0x01 / 0x47

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only default values
D5-D0	R/W	00 0000	Analog inputs power up time 00 0000: Default. Use one of the values give below 11 0001: Analog inputs power up time is 3.1 ms 11 0010: Analog inputs power up time is 6.4 ms 11 0011: Analog inputs power up time is 1.6 ms Others: Do not use

5.3.28 Page 1 / Register 72-122: Reserved Register - 0x01 / 0x48-0x7A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.29 Page 1 / Register 123: Reference Power-up Configuration Register - 0x01 / 0x7B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0 0000	Reserved. Write only default values
D2-D0	R/W	000	Reference Power Up configuration 000: Reference will power up slowly when analog blocks are powered up 001: Reference will power up in 40ms when analog blocks are powered up 010: Reference will power up in 80ms when analog blocks are powered up 011: Reference will power up in 120ms when analog blocks are powered up 100: Force power up of reference. Power up will be slow 101: Force power up of reference. Power up time will be 40ms 110: Force power up of reference. Power up time will be 80ms 111: Force power up of reference. Power up time will be 120ms

5.3.30 Page 1 / Register 124: Reserved Register - 0x01 / 0x7C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.3.31 Page 1 / Register 125: Offset Callibration Register - 0x01 / 0x7D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D5	R	000	Offset correction Clock Divider 000: Offset correction takes 190*197 oscillator clock cycles 001: Offset correction takes 38*197 oscillator clock cycles 010: Offset correction takes 76*197 oscillator clock cycles 011: Offset correction takes 114*197 oscillator clock cycles 100: Offset correction takes 142*197 oscillator clock cycles 101: Offset correction takes 190*197 oscillator clock cycles 110: Offset correction takes 228*197 oscillator clock cycles 111: Offset correction takes 266*197 oscillator clock cycles
D4-D2	R	0 00	Reserved. Write only default values
D1-D0	R/W	00	Offset correction settings 00: Offset correction disabled 01: Force calibrate for offset at Headphone Power-up for routings selected 10: Callibrate for offset at headphone power-up for selected routings only for first power-up of headphone 11: Do not use

5.3.32 Page 1 / Register 126-127: Reserved Register - 0x01 / 0x7E-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.4 Page 8 Registers

5.4.1 Page 8 / Register 0: Page Select Register - 0x08 / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.4.2 Page 8 / Register 1: ADC Adaptive Filter Configuration Register - 0x08 / 0x01

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values
D2	R/W	0	ADC Adaptive Filtering Control 0: Adaptive Filtering disabled for ADC 1: Adaptive Filtering enabled for ADC
D1	R	0	ADC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, ADC accesses ADC Coefficient Buffer-A and control interface accesses ADC Coefficient Buffer-B 1: In adaptive filter mode, ADC accesses ADC Coefficient Buffer-B and control interface accesses ADC Coefficient Buffer-A
D0	R/W	0	ADC Adaptive Filter Buffer Switch control 0: ADC Coefficient Buffers will not be switched at next frame boundary 1: ADC Coefficient Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

5.4.3 Page 8 / Register 2-7: Reserved - 0x08 / 0x02-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.4.4 Page 8 / Register 8-127: ADC Coefficients Buffer-A C(0:29) - 0x08 / 0x08-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients C0 through C29 of ADC Coefficient Buffer-A. Refer to Table "ADC Coefficient Buffer A Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.5 Page 9 Registers

5.5.1 Page 9 / Register 0: Page Select Register - 0x09 / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.5.2 Page 9 / Register 1-7: Reserved - 0x09 / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.5.3 Page 9 / Register 8-15: ADC Coefficients Buffer-A C(30:31) - 0x09 / 0x08-0x0F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients ADC Coefficient Buffer-A. Refer to Table "ADC Coefficient Buffer A Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.5.4 Page 9 / Register 16-31: Reserved - 0x09 / 0x10-0x1F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.5.5 Page 9 / Register 32-127: ADC Coefficients Buffer-A C(36:59) - 0x09 / 0x20-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients ADC Coefficient Buffer-A. Refer to Table "ADC Coefficient Buffer A Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.6 Page 10 Registers

5.6.1 Page 10 / Register 0: Page Select Register - 0x0A / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.6.2 Page 10 / Register 1-7: Reserved - 0x0A / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.6.3 Page 10 / Register 8-23: ADC Coefficients Buffer-A C(60:63) - 0x0A / 0x08-0x17

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients ADC Coefficient Buffer-A. Refer to Table "ADC Coefficient Buffer A Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.6.4 Page 10 / Register 24-127: Reserved - 0x0A / 0x18-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Write only default values

5.7 Page 26 Registers

5.7.1 Page 26 / Register 0: Page Select Register - 0x1A / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.7.2 Page 26 / Register 1-7: Reserved. - 0x1A / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.7.3 Page 26 / Register 8-127: ADC Coefficients Buffer-B C(0:29) - 0x1A / 0x08-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficient Buffer-B. Refer to Table "ADC Coefficient Buffer B Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.8 Page 27 Registers

5.8.1 Page 27 / Register 0: Page Select Register - 0x1B / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.8.2 Page 27 / Register 1-7: Reserved. - 0x1B / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.8.3 Page 27 / Register 8-15: ADC Coefficients Buffer-B C(30:31) - 0x1B / 0x08-0x0F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficient Buffer-B. Refer to Table "ADC Coefficient Buffer B Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.8.4 Page 27 / Register 16-31: Reserved. - 0x1B / 0x10-0x1F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.8.5 Page 27 / Register 32-127: ADC Coefficients Buffer-B C(36:59) - 0x1B / 0x20-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	xxxx xxxx	24-bit coefficients of ADC Coefficient Buffer-B. Refer to Table "ADC Coefficient Buffer B Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.9 Page 28 Registers

5.9.1 Page 28 / Register 0: Page Select Register - 0x1C / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.9.2 Page 28 / Register 1-7: Reserved. - 0x1C / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.9.3 Page 28 / Register 8-23: ADC Coefficients Buffer-B C(60:63) - 0x1C / 0x08-0x17

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of ADC Coefficient Buffer-B. Refer to Table "ADC Coefficient Buffer B Map" for details When Page-8, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when ADC channel is powered down

5.9.4 Page 28 / Register 24-127: Reserved. - 0x1C / 0x18-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.10 Page 44 Registers

5.10.1 Page 44 / Register 0: Page Select Register - 0x2C / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.10.2 Page 44 / Register 1: DAC Adaptive Filter Configuration Register - 0x2C / 0x01

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D3	R	0000 0	Reserved. Write only default values
D2	R/W	0	DAC Adaptive Filtering Control 0: Adaptive Filtering disabled for DAC 1: Adaptive Filtering enabled for DAC
D1	R	0	DAC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, DAC accesses DAC Coefficient Buffer-A and control interface accesses DAC Coefficient Buffer-B 1: In adaptive filter mode, DAC accesses DAC Coefficient Buffer-B and control interface accesses DAC Coefficient Buffer-A
D0	R/W	0	DAC Adaptive Filter Buffer Switch control 0: DAC Coefficient Buffers will not be switched at next frame boundary 1: DAC Coefficient Buffers will be switched at next frame boundary, if in adaptive filtering mode. This will self clear on switching.

5.10.3 Page 44 / Register 2-7: Reserved - 0x2C / 0x02-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.10.4 Page 44 / Register 8-11: DAC Coefficients Buffer-A C(0:29) - 0x2C / 0x08-0x0B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients C0 through C29 of DAC Coefficient Buffer-A. Refer to Table "DAC Coefficient Buffer A Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.11 Page 45 Registers

5.11.1 Page 45 / Register 0: Page Select Register - 0x2D / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.11.2 Page 45 / Register 1-7: Reserved - 0x2D / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.11.3 Page 45 / Register 8-11: DAC Coefficients Buffer-A C(30) - 0x2D / 0x08-0x0B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients DAC Coefficient Buffer-A. Refer to Table "DAC Coefficient Buffer A Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.11.4 Page 45 / Register 12-15: Reserved - 0x2D / 0x0C-0x0F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.11.5 Page 45 / Register 16-127: DAC Coefficients Buffer-A C(32:59) - 0x2D / 0x10-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients DAC Coefficient Buffer-A. Refer to Table "DAC Coefficient Buffer A Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.12 Page 46 Registers

5.12.1 Page 46 / Register 0: Page Select Register - 0x2E / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.12.2 Page 46 / Register 1-7: Reserved - 0x2E / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.12.3 Page 46 / Register 8-19: DAC Coefficients Buffer-A C(60:62) - 0x2E / 0x08-0x13

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients DAC Coefficient Buffer-A. Refer to Table "DAC Coefficient Buffer A Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.12.4 Page 46 / Register 20-27: Reserved - 0x2E / 0x14-0x1B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.12.5 Page 46 / Register 28-75: DAC Coefficients Buffer-A C(65:76) - 0x2E / 0x1C-0x4B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	24-bit coefficients DAC Coefficient Buffer-A. Refer to Table "DAC Coefficient Buffer A Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.12.6 Page 46 / Register 76-127: Reserved - 0x2E / 0x4C-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.13 Page 62 Registers

5.13.1 Page 62 / Register 0: Page Select Register - 0x3E / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.13.2 Page 62 / Register 1-7: Reserved. - 0x3E / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.13.3 Page 62 / Register 8-127: DAC Coefficients Buffer-B C(0:29) - 0x3E / 0x08-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Coefficient Buffer-B. Refer Table "DAC Coefficient Buffer B Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.14 Page 63 Registers

5.14.1 Page 63 / Register 0: Page Select Register - 0x3F / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.14.2 Page 63 / Register 1-7: Reserved. - 0x3F / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.14.3 Page 63 / Register 8-11: DAC Coefficients Buffer-B C(30) - 0x3F / 0x08-0x0B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Coefficient Buffer-B. Refer Table "DAC Coefficient Buffer B Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.14.4 Page 63 / Register 12-15: Reserved. - 0x3F / 0x0C-0x0F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.14.5 Page 63 / Register 16-127: DAC Coefficients Buffer-B C(32:59) - 0x3F / 0x10-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	24-bit coefficients of DAC Coefficient Buffer-B. Refer Table "DAC Coefficient Buffer B Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.15 Page 63 Registers

5.15.1 Page 63 / Register 0: Page Select Register - 0x3F / 0x00

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Page Select Register 0-255: Selects the Register Page for next read or write command. Refer Table "Summary of Memory Map" for details.

5.15.2 Page 63 / Register 1-7: Reserved - 0x3F / 0x01-0x07

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.15.3 Page 63 / Register 8-19: DAC Coefficients Buffer-B C(60:62) - 0x3F / 0x08-0x13

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	xxxx xxxx	24-bit coefficients of DAC Coefficient Buffer-B. Refer Table "DAC Coefficient Buffer B Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.15.4 Page 63 / Register 20-27: Reserved - 0x3F / 0x14-0x1B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.15.5 Page 63 / Register 28-75: DAC Coefficients Buffer-B C(65:76) - 0x3F / 0x1C-0x4B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	24-bit coefficients of DAC Coefficient Buffer-B. Refer Table "DAC Coefficient Buffer B Map" for details When Page-44, Reg-01d, D2='0' (Adaptive filtering disabled) the read write access to these registers is allowed only when DAC channel is powered down

5.15.6 Page 63 / Register 76-127: Reserved - 0x3F / 0x4C-0x7F

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	0000 0000	Reserved. Write only default values

5.16 ADC Coefficients A+B

Table 5-2. ADC Coefficient Buffer-A Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	8	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	8	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C29	8	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	9	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C59	9	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	10	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C63	10	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-3. ADC Coefficient Buffer-B Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	26	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	26	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C29	26	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	27	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C59	27	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	28	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C63	28	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

5.17 ADC Coefficient Default Values

Table 5-4. Default values of ADC Coefficients in Buffers A and B

ADC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	01170000H
C2	01170000H
C3	7DD30000H
C4	7FFFFF00H
C5,C6	00000000H
C7	7FFFFF00H

Table 5-4. Default values of ADC Coefficients in Buffers A and B (continued)

ADC Buffer-A,B Coefficients	Default Value at reset
C8,..,C11	00000000H
C12	7FFFFF00H
C13,..,C16	00000000H
C17	7FFFFF00H
C18,..,C21	00000000H
C22	7FFFFF00H
C23,..,C26	00000000H
C27	7FFFFF00H
C28,..,C35	00000000H
C36	7FFFFF00H
C37,C38	00000000H
C39	7FFFFF00H
C40,..,C43	00000000H
C44	7FFFFF00H
C45,..,C48	00000000H
C49	7FFFFF00H
C50,..,C53	00000000H
C54	7FFFFF00H
C55,..,C58	00000000H
C59	7FFFFF00H
C60,..,C63	00000000H

5.18 DAC Coefficients A+B

Table 5-5. DAC Coefficient Buffer-A Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	44	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	44	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C29	44	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C30	45	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C59	45	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	46	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C76	46	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-6. DAC Coefficient Buffer-B Map

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C0	62	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C1	62	12	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C29	62	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

Table 5-6. DAC Coefficient Buffer-B Map (continued)

Coef No	Page No	Base Register	Base Register + 0	Base Register + 1	Base Register + 2	Base Register + 3
C30	63	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C59	63	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
C60	64	8	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.
	..	..	..	..	..	..
C76	64	124	Coef(23:16)	Coef(15:8)	Coef(7:0)	Reserved.

5.19 DAC Coefficient Default Values

Table 5-7. Default values of DAC Coefficients in Buffers A and B

DAC Buffer-A,B Coefficients	Default Value at reset
C0	00000000H
C1	7FFFFF00H
C2,..,C5	00000000H
C6	7FFFFF00H
C7,..,C10	00000000H
C11	7FFFFF00H
C12,..,C15	00000000H
C16	7FFFFF00H
C17,..,C20	00000000H
C21	7FFFFF00H
C22,..,C25	00000000H
C26	7FFFFF00H
C27,..,C30	00000000H
C31,C32	00000000H
C33	7FFFFF00H
C34,..,C37	00000000H
C38	7FFFFF00H
C39,..,C42	00000000H
C43	7FFFFF00H
C44,..,C47	00000000H
C48	7FFFFF00H
C49,..,C52	00000000H
C53	7FFFFF00H
C54,..,C57	00000000H
C58	7FFFFF00H
C59,..,C64	00000000H
C65	7FFFFF00H
C66,C67	00000000H
C68	7FFFFF00H
C69,C70	00000000H
C71	7FF70000H
C72	80090000H
C73	7FEF0000H
C74,C75	00110000H
C76	7FDE0000H

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2012) to A Revision	Page
• Added the *Fast Startup* section	74
• Added the *Fast Startup without Pop-Noise* section	76
• Added the *Analog Bypass* section	77
• Changed Register Script for Mono DAC playback with 48 ksps... To: *Mono Differential Output*	82

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