Arthur Kay

TI Precision Designs: Verified Design
Low Level (5 µA) V-to-I Converter

TEXAS INSTRUMENTS

TI Precision Designs

TI Precision Designs are analog solutions created by TI's analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

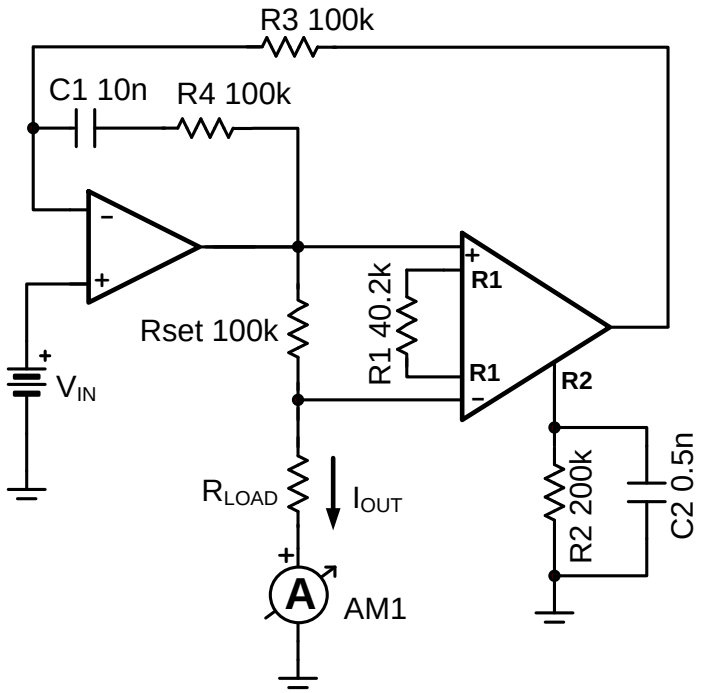
Design Archive	All Design files
TINA-TI™	SPICE Simulator
INA326	Product Folder
OPA333	Product Folder

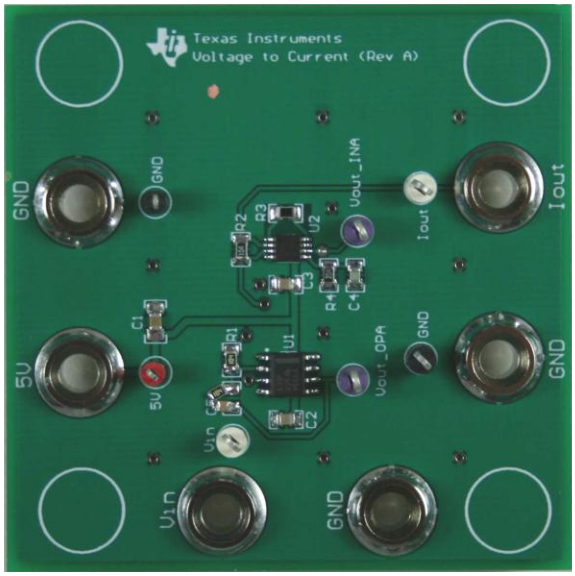
Circuit Description

This micro-amp voltage-to-current (V-I) converter delivers a precise low level current to a load. The design operates on a single 5 V supply and uses a precision low drift op amp and instrumentation amplifier. Simple modifications can change the range and accuracy of the V-I converter.

TI E2E™ Community

Ask The Analog Experts
WEBENCH® Design Center
TI Precision Designs Library





An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

TINA-TI is a trademark of Texas Instruments
WEBENCH is a registered trademark of Texas Instruments

Copyright © 2013, Texas Instruments Incorporated

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V dc
- Input: 0 V – 5 V dc
- Output: 0 µA – 5 µA dc

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Uncalibrated Accuracy (%FSR)	0.2%	0.3%	0.18%
Calibrated Accuracy (%FSR)	0.01%	na	0.001%
Load Compliance 0<R<500k Max Linear Output (µA)	4.0 µA	4.9 µA	4.9 µA
Load Compliance 0<R<500k Min Linear Output (µA)	1.0 µA	0 µA	0.6 µA

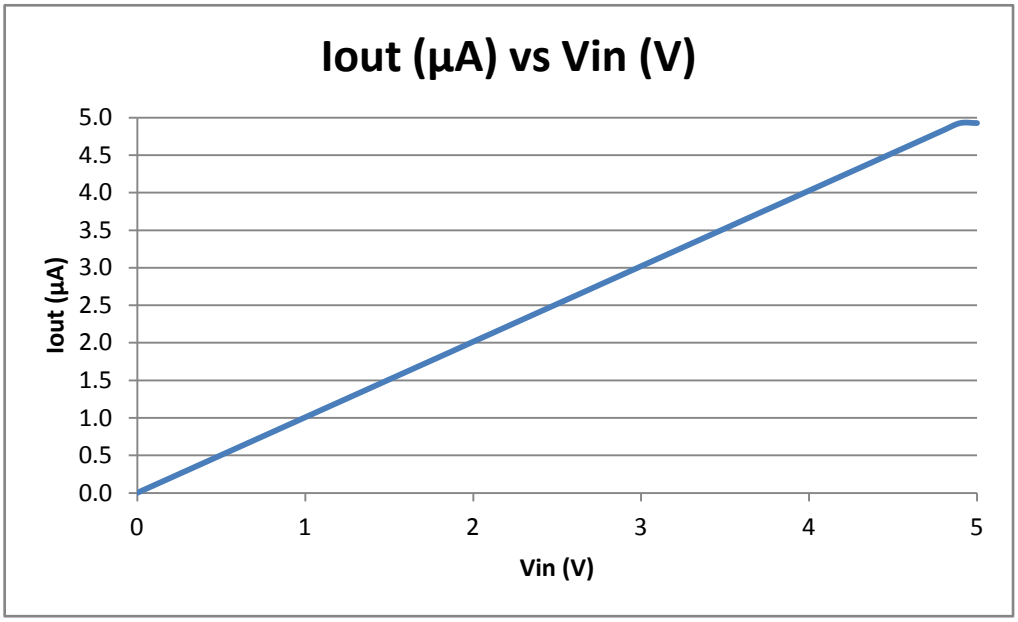


Figure 1: Measured Transfer Function

Copyright © 2013, Texas Instruments Incorporated

2 Theory of Operation

A more complete schematic for this design is shown in Figure 2. The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, R_{SET}, and the instrumentation amplifier (INA) gain. During operation, the input voltage divided by the INA gain will appear across the set resistor ($V_{SET}=V_{IN}/G_{INA}$). The current through R_{SET} must flow through the load, so I_{OUT} is V_{SET} / R_{SET}. I_{OUT} will remain a well regulated current as long as the total voltage across R_{SET} and R_{LOAD} doesn't violate the output limits of the op amp or the input common mode limits of the INA.

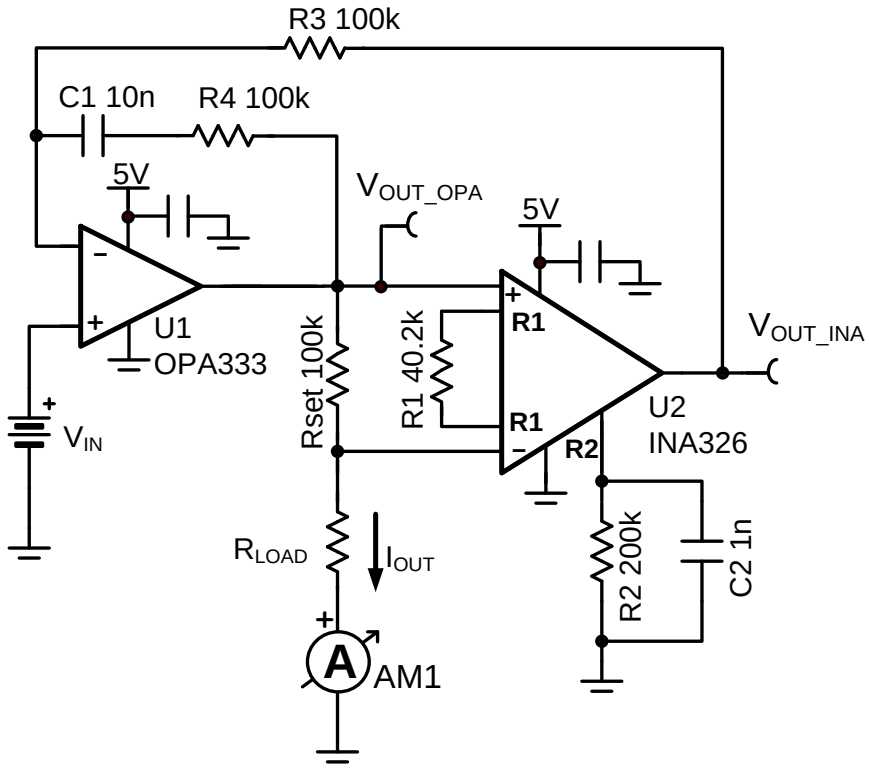


Figure 2: Complete Circuit Schematic

The transfer function for this design is defined as:

$$I_{OUT} = \frac{V_{IN}}{G_{INA} \times R_{SET}} \quad (1)$$

$$G_{INA} = \frac{2 \times R2}{R1} \quad (2)$$

Copyright © 2013, Texas Instruments Incorporated

2.1 Simplified Composite Amplifier

Thinking of the current source as a composite amplifier can help to explain its operation. The INA, U2, is a fixed gain block inside the feedback of op amp U1. The op amp U1 is configured as a unity gain voltage follower, so the voltage applied to the input (V_{IN}) will be amplified by a gain of one and appear at the output of the composite amplifier ($V_{OUT\_INA} = V_{IN}$ x 1). The input of the INA needs to be its output divided by the gain ($V_{INA\_IN} = V_{OUT\_INA} / G_{INA}$ or by substitution $V_{INA\_IN} = V_{IN} / G_{INA}$). The example shown in Figure 4 demonstrates this concept with a 1 V input signal.

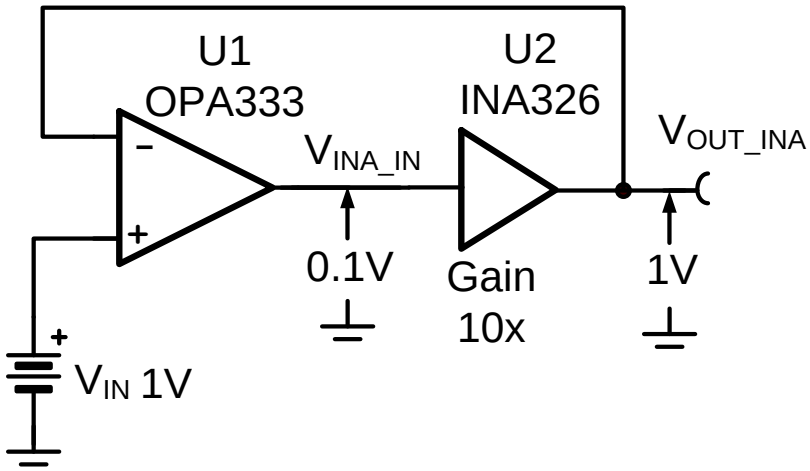


Figure 3: Simplified Composite Amplifier

2.2 Current output function

Figure 4 shows the fundamental building blocks of the I-to-V converter. The voltage across the set resistor (V_{SET}) is the input voltage divided by the INA gain (e.g. V_{SET} = 1 V / 10 = 0.1 V). The current is determined by V_{SET} and R_{SET} ($I_{OUT} = V_{SET} / R_{SET}$ = 0.1 V / 100 kΩ = 1 µA).

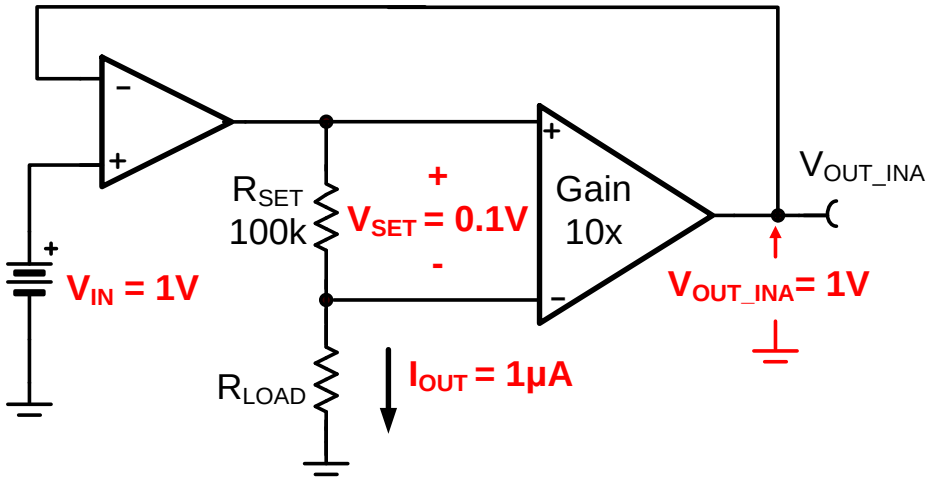


Figure 4: Simplified I-to-V

Copyright © 2013, Texas Instruments Incorporated

2.3 Setting the INA Gain

External components (R1, R2, and C2) are used to set the INA gain. The INA gain will determine the maximum voltage across the current setting resistor (R_{SET}). For example, if the gain is 10 V/V, the maximum voltage across R_{SET} is 0.5 V ($V_{SET\_MAX} = V_S / G_{INA} = 5\ V / 10 = 0.5\ V$). Minimizing the voltage across R_{SET} allows for a wider voltage range across the load. In this example, the load voltage can be as high as 4.5 V (Max Load voltage = $V_S - V_{SET} = 5\ V - 0.5\ V = 4.5\ V$). Using a larger gain could further minimize the drop across R_{SET} but introduces other issues. Section 6.5 covers the compliance issues in detail. Section 7.2 also covers trade-offs in selecting different INA gain settings. In this example, the gain is set to 10 V/V. Table 2 shows an excerpt from the INA326 data sheet that was used to select the gain set components (G_{INA} = 10 V/V, R1 = 40.2 kΩ, R2 = 200 kΩ, C2 = 0.5 nF). Note that 40.2 kΩ is the closest standard value to 40 kΩ, so the gain is actually set to 9.95 V/V. This is not really an issue as this circuit is calibrated for highest accuracy.

Table 2: Gain for INA326 in Single Supply Configuration

Desired Gain (V/V)	R1 (Ω)	R2 || C2 (Ω || nF)
1	400k	200k || 0.5
10	40k	200k || 0.5
20	20k	200k || 0.5

2.4 Setting the output current range

The output current range is determined by the maximum set voltage (V_{SET_MAX}) and the set resistance R_{SET}. As Section 2.3 indicated, V_{SET_MAX} depends on the supply voltage and the gain. R_{SET} is selected to set the output current range ($R_{SET} = V_{SET\_MAX} / I_{OUT\_RANGE} = 0.5\ V / 5\ \mu A = 100\ k\Omega$).

$$R_{SET} = \frac{V_{SET\_MAX}}{I_{OUT\_RANGE}} = \frac{0.5V}{1\mu A} = 100k\Omega \quad (3)$$

2.5 Compensation Components

External components (C1, R3, and R4) are required to make the V-to-I circuit stable. The value of these components will change for different op amps and instrumentation amplifiers. These components form an ac feedback path for the op amp which prevents peaking in the closed loop response. Because of both the stability compensation components and inherent bandwidth limitations of the INA326 and OPA333 the closed loop frequency response of the system is very low. The procedure for selecting the stability network is beyond the scope of this design note; see reference [1] for a detailed explanation of stability.

Copyright © 2013, Texas Instruments Incorporated

3 Component Selection

3.1 Op Amp Selection

This design is a high dc precision low level (micro-amp) current source. The key op amp (U1) characteristics needed to get a stable dc output current are input offset voltage (Vos) and offset drift (ΔVos/ΔT). Since the desired input range is 0 V to 5 V a rail-to-rail input amplifier is needed. Also, to avoid error across the common mode range, good CMRR (110db or better) is desirable.

3.2 INA Selection

Low offset, low offset drift, and low bias current are key characteristics of the instrumentation amplifier selection. Low gain error and low gain error drift are secondary characteristics to consider. Since this circuit is calibrated at 25 °C, the drift characteristics are more important than the absolute accuracy. Another important characteristic of the INA is its common mode input range and output swing range. The INA326 amplifier has common mode range beyond the power supply rails (i.e. -0.02 V < Vcm < 5.1 V). Furthermore, the common mode range is not dependent on gain or the reference voltage as is common for many instrumentation amplifiers. The output can swing very close to the power supply rails (5 mV) with a 25 µA load). This excellent common mode and output swing allows for good load compliance (e.g. load voltages can range from nearly 0 V to 5 V).

3.3 Passive Component Selection

The critical passive components for this design are the three resistors that are part of the transfer function, R1, R2, and R_{SET}. To minimize gain error, 0.1%, 20 ppm/°C resistors were used. The low temperature drift (20 ppm/°C) of the resistors is important to get stable results even when the circuit is operated at room temperature. Remember, room temperature can change +/-2 °C over the course of a few minutes even in a well-controlled environment. To get optimal performance the circuit should be calibrated.

Other passive components in this design may be selected for 1% or greater as they will not directly affect the transfer function of this design.

Copyright © 2013, Texas Instruments Incorporated

4 Simulation

The TINA-TI™ schematic shown in Figure 5 includes the circuit values obtained in the design process.

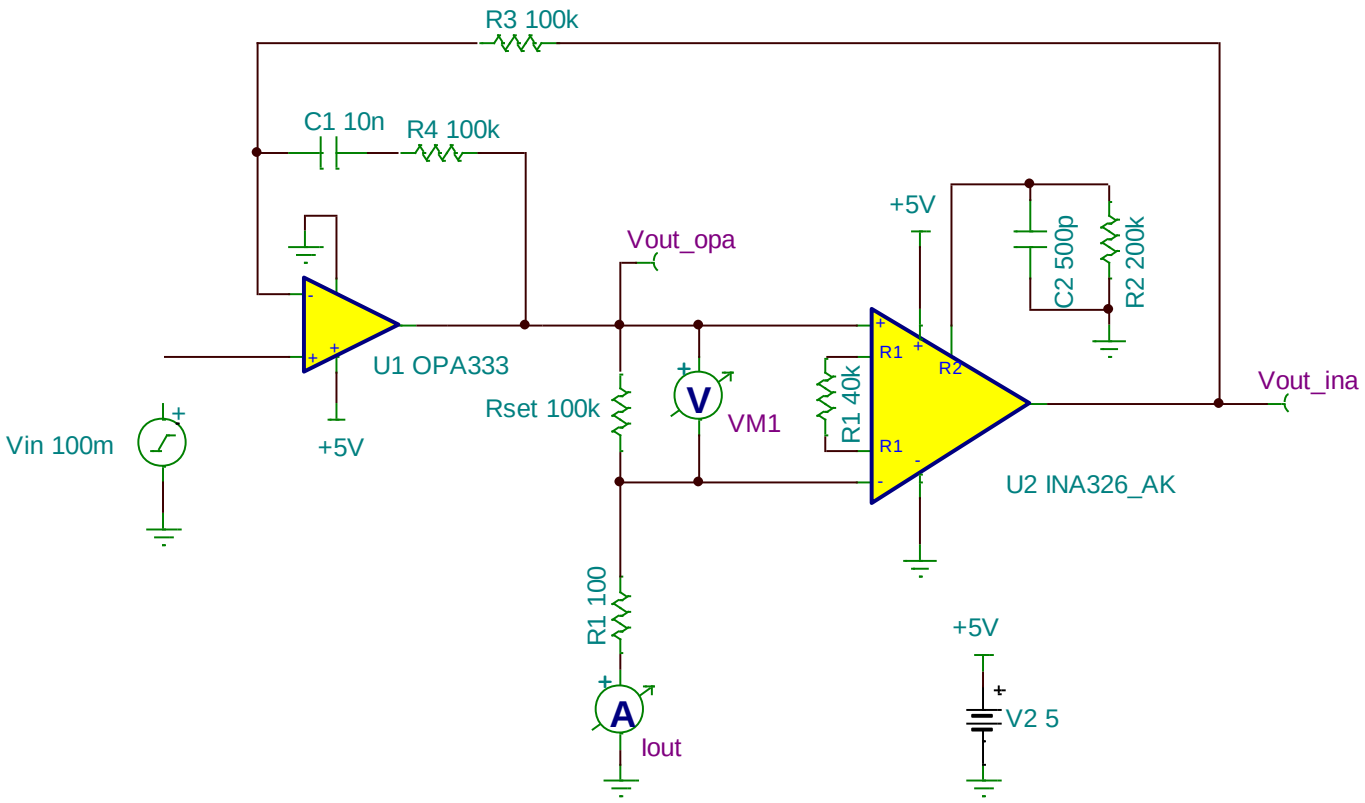


Figure 5: TINA-TI™ Spice Schematic

Copyright © 2013, Texas Instruments Incorporated

4.1 DC Transfer Function

The dc transfer function simulation results of the circuit are shown in Figure 6. The results can be used to reference the voltage or current at a given node as a function of the input voltage.

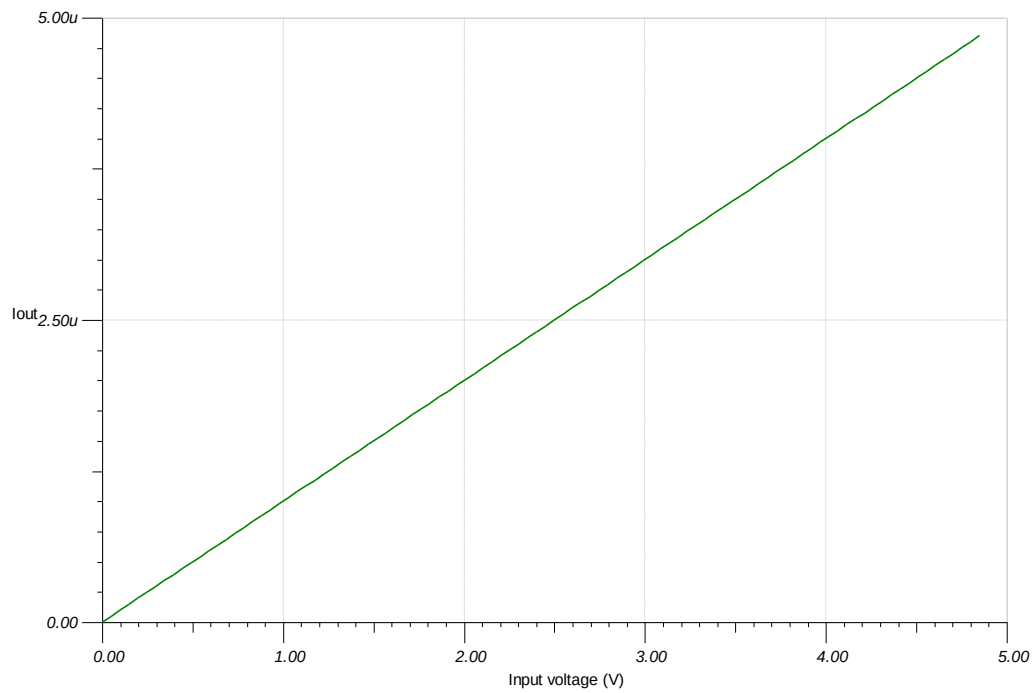


Figure 6: Simulation DC Transfer Results (RL = 500 kΩ)

Figure 7 shows detail on other nodes in the design. For example, the instrumentation amplifier output and op amp output can be observed in Figure 7.

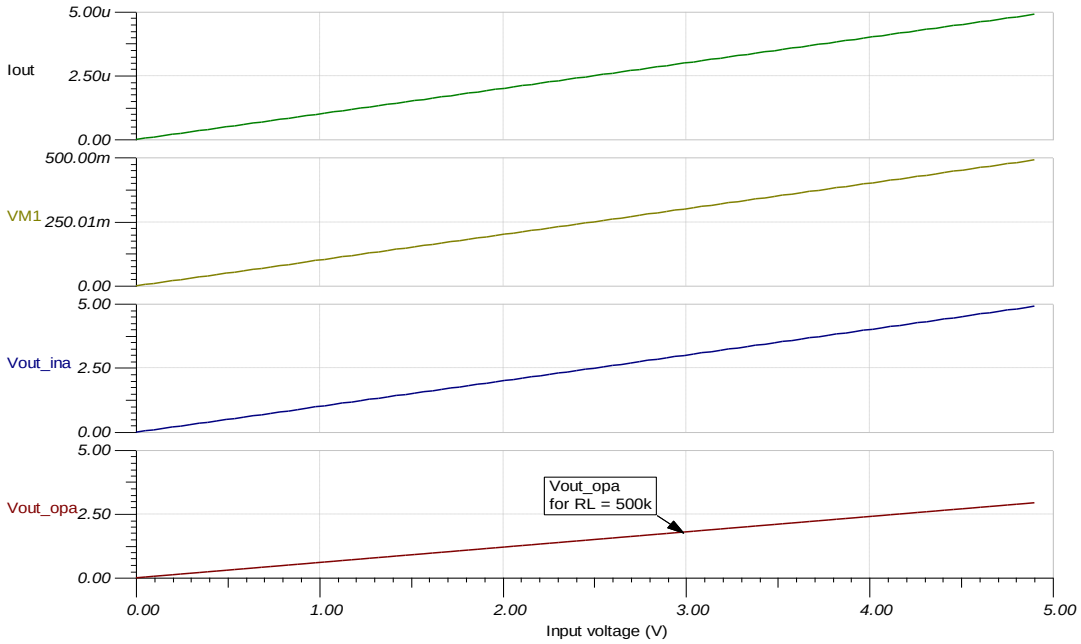


Figure 7: Simulation DC Transfer Results (RL=500 kΩ)

Copyright © 2013, Texas Instruments Incorporated

4.2 Step Response

The step response of the design can be seen in Figure 8. The results show that the output of the op amp, INA, and current output settle to the proper values with little overshoot and ringing. This indicates that the design is stable.

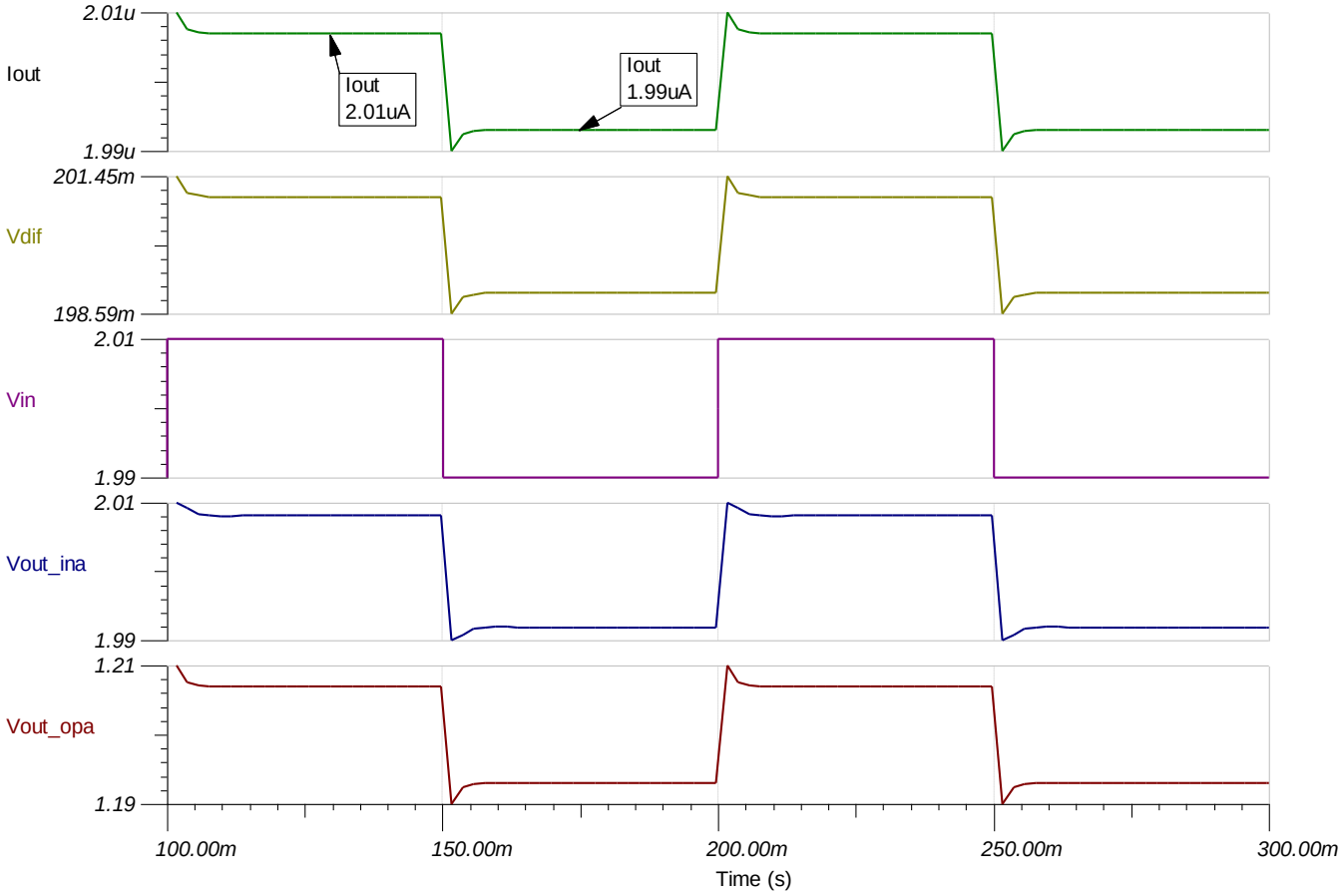


Figure 8: Step-Response Simulation

Copyright © 2013, Texas Instruments Incorporated

4.3 Compliance Voltage

To test the maximum and minimum compliance voltage the input voltage was swept across the full range (0 V to 5 V) for different load resistors. Simulation shows that the maximum compliance is limited by the supply voltage (i.e. $V_{OUT\_OPA\_MAX} = V_{SUPPLY}/(R_{LOAD} + R_{SET})$). More detail on compliance voltage is given in Section 6.5.

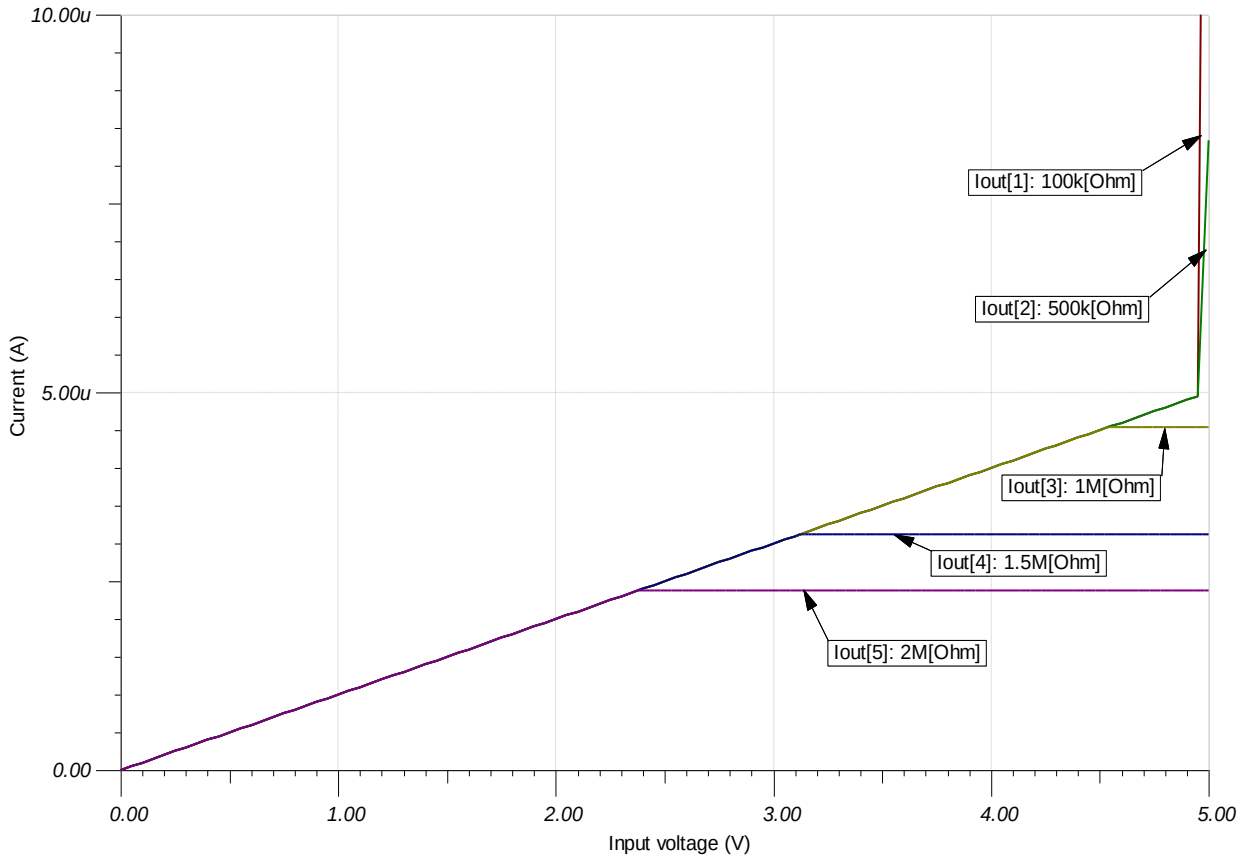


Figure 9: Compliance Voltage vs. Load Resistance Simulation

Copyright © 2013, Texas Instruments Incorporated

Figure 10 shows a Monte Carlo analysis for the uncalibrated output error for this design. This error is dominated by resistor tolerance. In this analysis 0.1% resistors were used. The different current errors curves shown in Figure 10 are the result of resistor variation during the Monte Carlo Analysis. Equation 4 was used to convert the Monte Carlo results to a percentage. Note that R1, R2, and R_{SET} all affect the error.

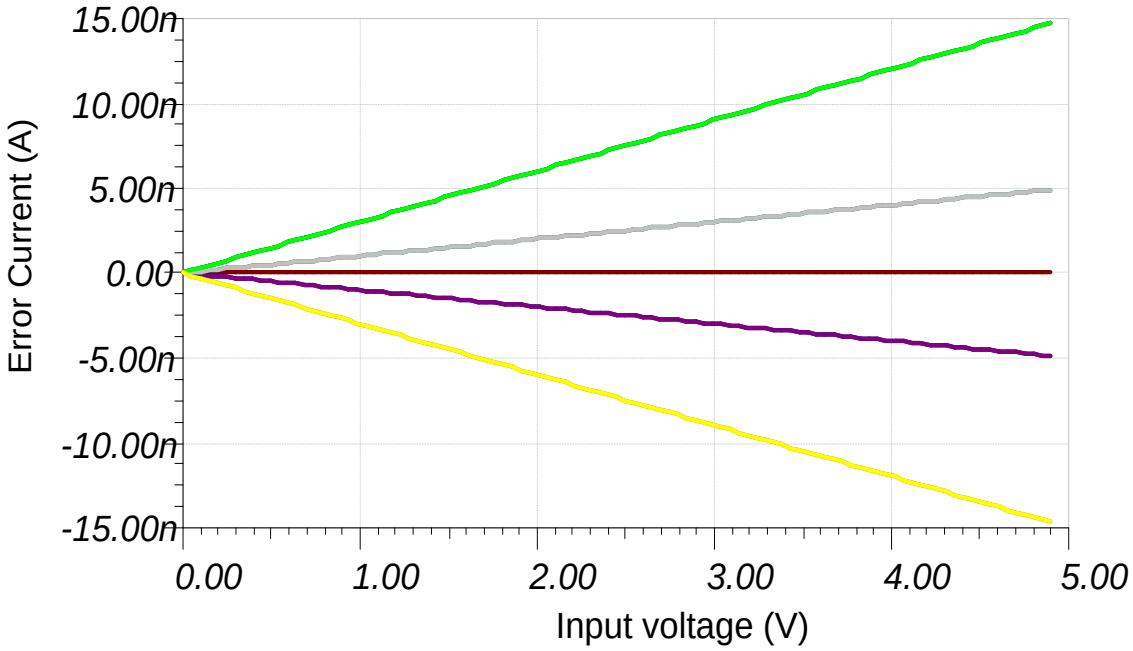


Figure 10: Monte Carlo Analysis for Resistor Tolerance

$$\text{Uncalibrated\_Accuracy} = \frac{I_{ERROR\_MAX}}{I_{OUT\_RANGE}} \times 100\% = \frac{15nA}{5\mu A} \times 100\% = 0.3\% \quad (4)$$

Copyright © 2013, Texas Instruments Incorporated

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The general guidelines for precision PCB layout were used on this design. For example, trace lengths are kept to minimum length especially for decoupling and inverting amplifier inputs. This minimizes EMI pickup and reduces parasitic capacitance. The gain set resistor, R1, on the INA326 is especially sensitive to parasitic capacitance, so the ground plane was removed near and under this resistor.

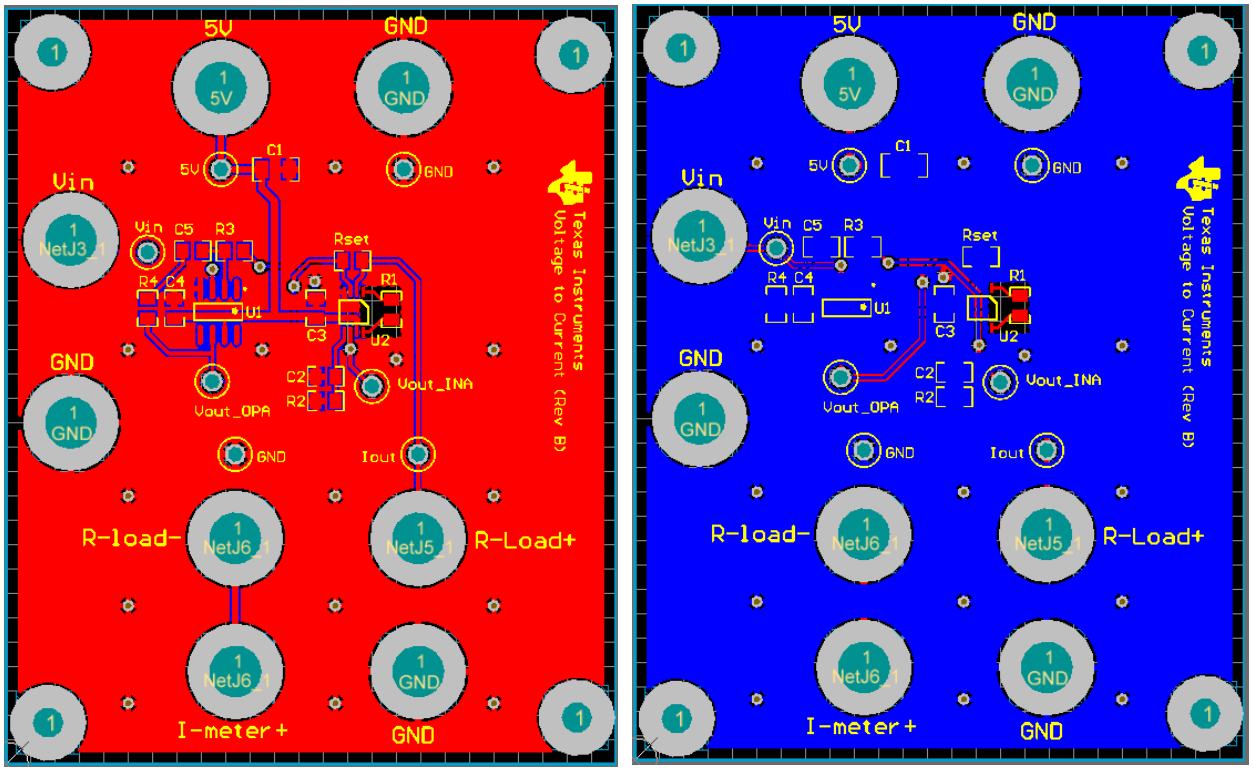


Figure 11: PCB Layout (Top on Left, Bottom on Right)

5.2 Cleaning the PCB

Because this V-to-I circuit delivers very low current levels it is important to properly clean the PCB to avoid parasitic leakage paths from residual solder flux. Use a professional ultrasonic cleaner for initial cleaning followed by a second cleaning using isopropyl alcohol. Avoid handling and breathing on the boards. Be sure to store them in a clean and dry environment. Greater detail on this subject is given in [2].

Copyright © 2013, Texas Instruments Incorporated

6 Verification & Measured Performance

6.1 General precautions used in measuring low level V-to-I circuit

The objective of this circuit is to generate micro-amp level currents with accuracy and stability into the nano-amps. A high precision voltage source and ammeter has to be used to generate the input voltage and measure the output current of this circuit. Also, the V-to-I circuit board should be in a shielded environment to minimize noise pickup. Shielded cables (e.g. coax or shielded twisted pair) should be used to connect the test equipment to the V-to-I board. Figure 12 shows the test equipment setup used to measure the low current output.

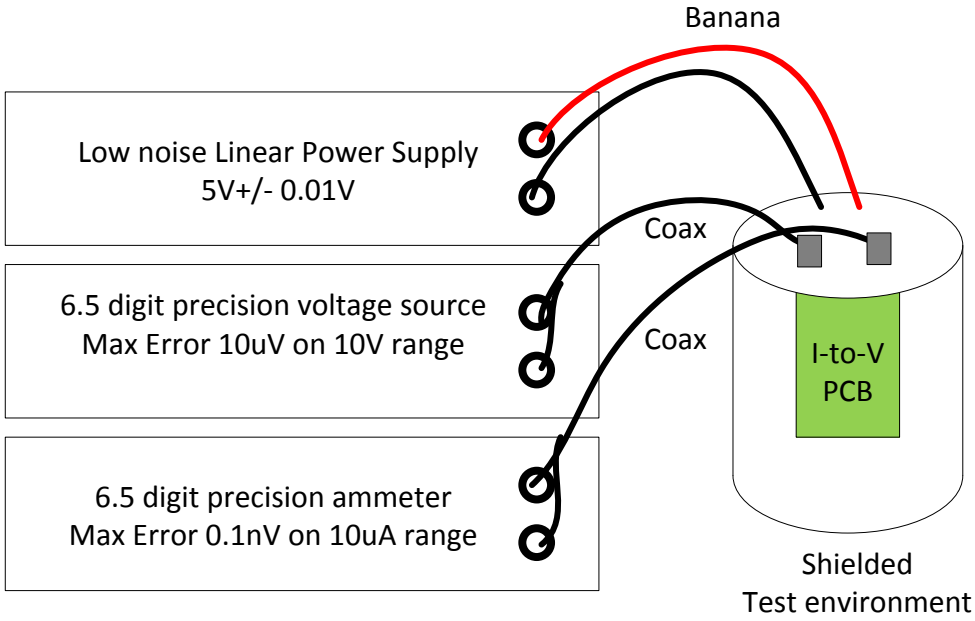


Figure 12: Test Setup for V-to-I Board

Copyright © 2013, Texas Instruments Incorporated

6.2 Transfer Function

Data was collected by sweeping the dc input, $V_{IN,}$ from 0 V to 5 V with a 0.1 V increment while measuring the load current, I_{OUT}. Figure 13 displays a plot of I_{OUT} vs. V_{IN}. The measured error as a percent of full scale is given in Figure 14. Note that the error becomes large at the ends of the output range because the amplifiers are nonlinear in this range. The output range limitations are covered in detail in Section 6.5.

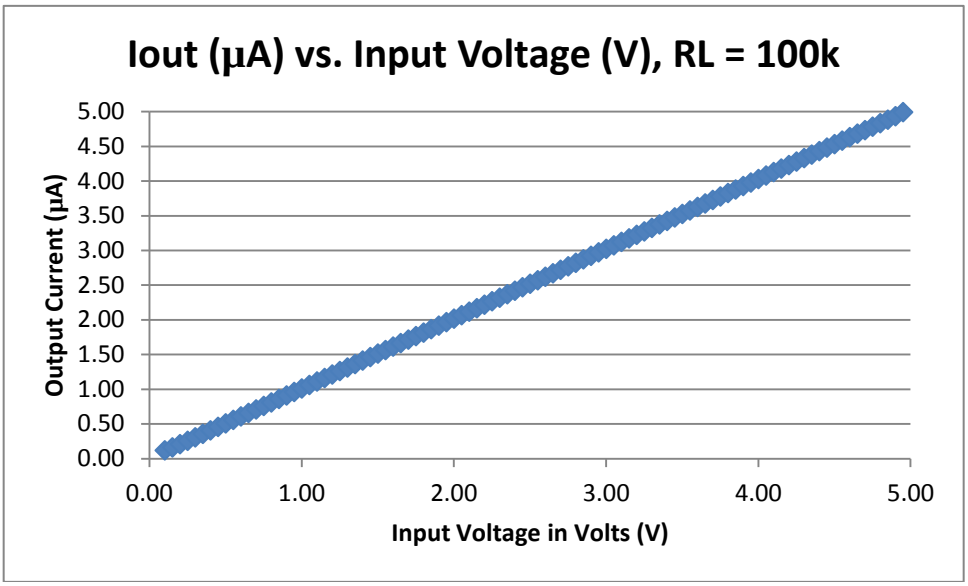


Figure 13: I_{OUT} vs. V_{IN} for 100 kΩ Load

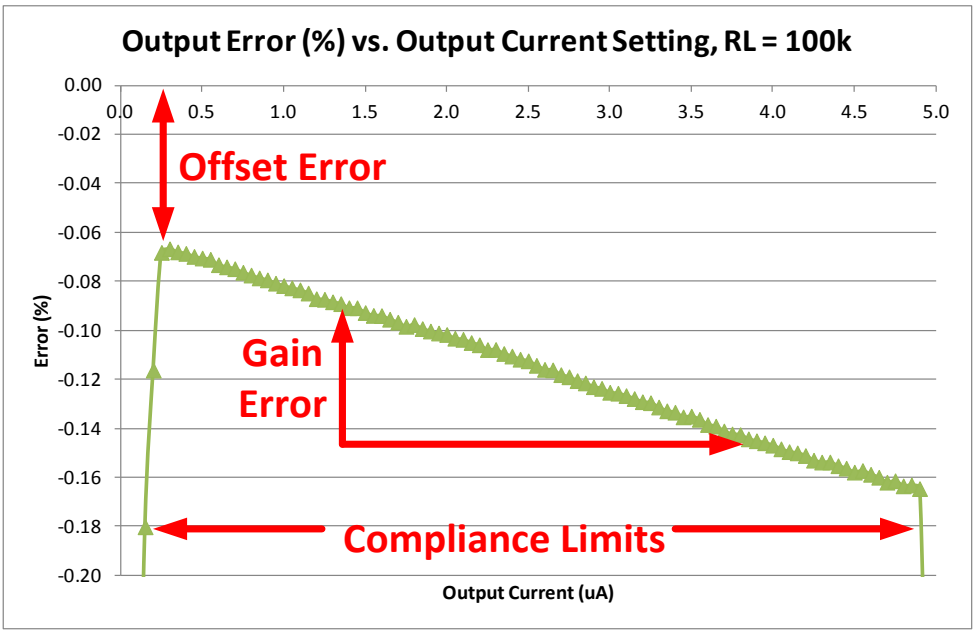


Figure 14: Uncalibrated Output Error in Percent of Full Scale

Copyright © 2013, Texas Instruments Incorporated

6.3 Calibration

The goal of this design is to obtain very accurate, stable, and repeatable output current vs. input voltage characteristics. The accuracy of this design is limited by resistor tolerance, INA gain accuracy, offset voltage and drift. A two point linear calibration can be used to obtain a highly accurate V-to-I converter. A two point linear calibration measures the slope and offset error on the transfer function. Using the equation for a straight line, we compute the slope (m) and the offset (b) using two points on the linear portion of the transfer function. Avoid using the end points of the function as the linearity becomes poor in these regions.

$$y = m \times x + b \tag{5}$$

$$m = \frac{(y_2 - y_1)}{(x_2 - x_1)} \tag{6}$$

$$b = y_2 - m \times x_2 \tag{7}$$

$$x = \frac{y - b}{m} \tag{8}$$

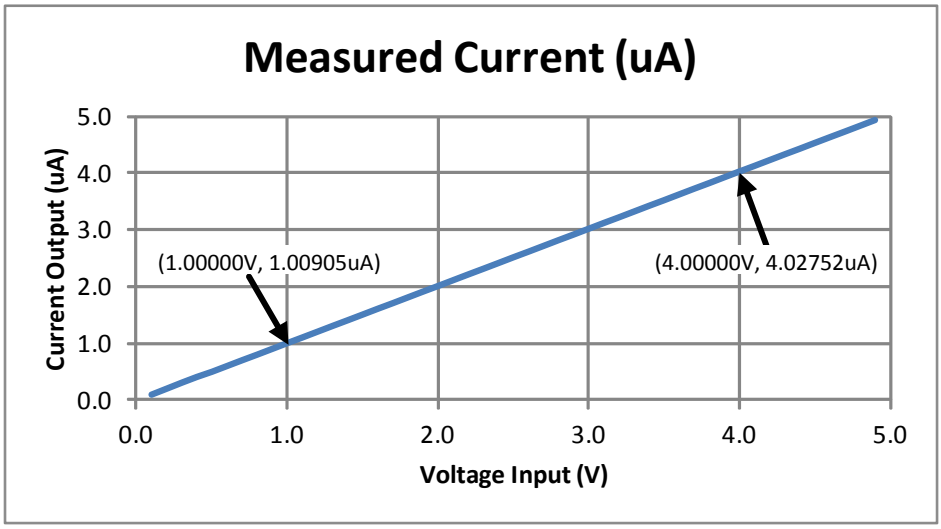


Figure 15: Measured current showing two points used in calibration

Copyright © 2013, Texas Instruments Incorporated

The equation below show an example calculation for finding the slope and offset of the measured transfer function.

$$m = \frac{(4.02752\mu A - 1.00905\mu A)}{(4.00000V - 1.00000V)} = 1.00616\mu A/V \quad (9)$$

$$b = 4.02752 - (1.00616\mu A/V) * 4.00000V = 2.89467nA \quad (10)$$

Using the slope and offset calculated above it is possible to compute the input voltage required to set the output to a precise current value within the compliance range of the circuit. Below is an example showing how the input voltage required to get an accurate 3.0000 µA output can be calculated. In this case, the required input voltage to get a precise 3.0000 µA output is calculated to be 2.97877 V. Measuring the actual output after this calibration will yield very accurate results. Typical maximum post-calibration error is +/-50 pA or less (0.001% of full scale). The components used in this circuit are very stable so the calibration coefficients (*m* and *b*) can be measured once and re-used for all calibrated current settings.

$$x = \frac{y - b}{m} \quad (11)$$

$$V_{in\_required} = \frac{I_{out\_desired} - b}{m} = \frac{3.0000\mu A - 2.89467nA}{1.00616\mu A} = 2.97877V \quad (12)$$

Post-calibration error is calculated as shown below. The post-calibration error is across the entire output current range (0 µA to 5 µA) as shown in Figure 16.

$$Error = \frac{(I_{out\_measured} - I_{out\_ideal})}{Iout\_range} \times 100 = \frac{3.000033\mu A - 3.0\mu A}{5\mu A - 0\mu A} \times 100 = 0.00066\% \quad (13)$$

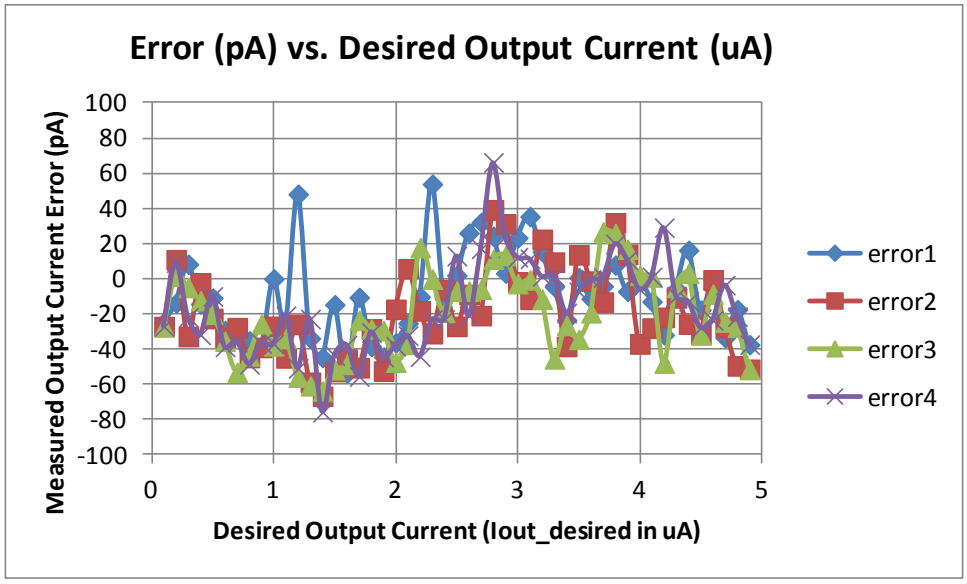


Figure 16: Measured output error post calibration for 0.1 µA < I_{out} < 4.9 µA

Copyright © 2013, Texas Instruments Incorporated

6.4 Transient Response

Figure 17 shows the large-scale step response to a 2 Vp-p, 5 Hz input signal with a 1 MΩ load. Note that the signal is offset so that the output range is from 0.05 µA to 2 µA (or 50 mV to 2.05 V).

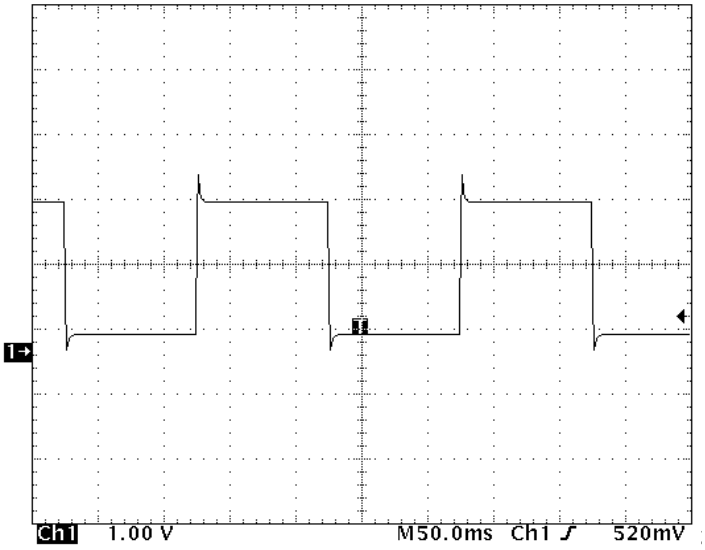


Figure 17: Large-Scale Step Response

Figure 18 is the same circuit arrangement as in Figure 17 except that the frequency was increased to 100 Hz. This is the extreme limit of the bandwidth of this V-to-I converter. This circuit is not intended to be an ac current source. The goal of this implementation is to create a programmable dc current source. Based on the figure below, at least 10 ms is required for settling (100 ms for highest accuracy).

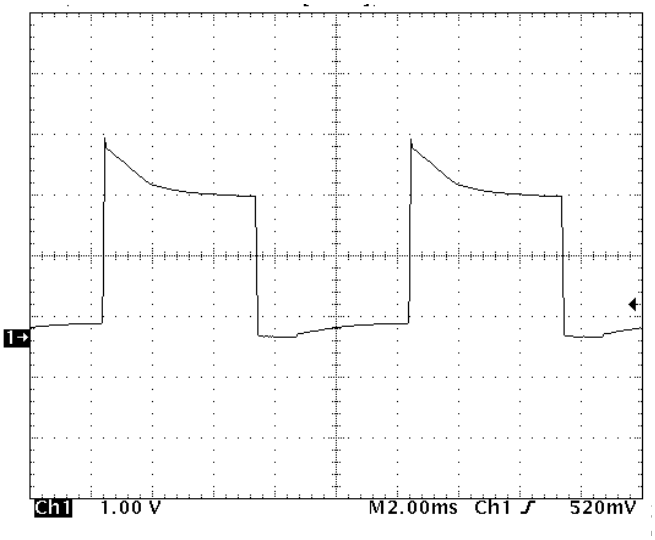


Figure 18: Large signal at bandwidth limit (100 Hz)

Copyright © 2013, Texas Instruments Incorporated

Figure 19 is the same arrangement as used in Figure 17 and Figure 18 except that a small (100 mVp-p) signal with a 500 mV dc offset was applied to the input. The objective of this test is to confirm the stability of the design. The design quickly settles to the final value with a properly damped response without overshoot or ringing. This is a good indication of circuit stability.

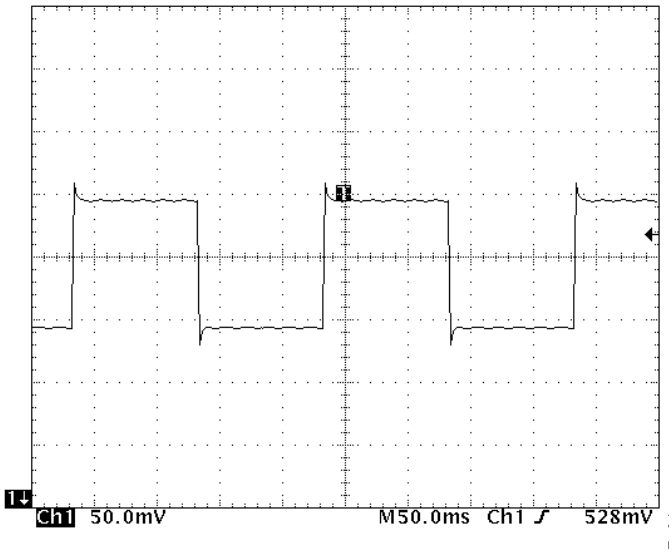


Figure 19: Small-Signal Stability

6.5 Output Compliance

Ideally this circuit would be able to output 0 µA to 5 µA for any load resistance. However, the output current range is only possible over a range of resistances because the current is limited when the op amp output approaches either power supply rail. The compliance defines the output resistance or current limitations and is based on 1) the supply voltage, 2) the load resistance, and 3) the op amp linearity when it's output is near the power supply rails. Thus, it is possible to see limitations for both full scale (e.g. 5 µA) and minimum scale (e.g. 0µA) output current. The maximum output current limitation is given by Equation 14 and 15. This limitation occurs when the op amp output approaches the positive rail. Figure 20 illustrates this relationship graphically. This relationship can be confirmed using TINA-TI™ SPICE. For $I_{OUT\_MAX} < I_{OUT\_FULL\_SCALE}$ Equation 14 can be used to calculate I_{OUT_MAX} otherwise use Equation 15.

$$I_{OUT\_MAX} = \frac{Vs}{R_{SET} + R_{LOAD}} \tag{14}$$

$$I_{OUT\_MAX} = I_{OUT\_MAX\_RANGE} \tag{15}$$

Where I_{OUT_MAX} is the maximum current that can be delivered before compliance limitations and $I_{OUT\_FULL\_SCALE}$ is the full scale range for the design (5 µA in this case).

For example, assume R_{LOAD}= 1 MΩ.

$$I_{OUT\_MAX} = \frac{Vs}{R_{SET} + R_{LOAD}} = \frac{5V}{100k\Omega + 1M\Omega} = 4.54\mu A \tag{14}$$

Since I_{OUT_MAX} < 5 µA, the max output is 4.54 µA.

Now assume R_{LOAD} = 100 kΩ.

$$I_{OUT\_MAX} = \frac{Vs}{R_{SET} + R_{LOAD}} = \frac{5V}{100k\Omega + 100k\Omega} = 25\mu A \tag{14}$$

Since I_{OUT_MAX} > 5 µA, the max output is 5.0 µA.

Copyright © 2013, Texas Instruments Incorporated

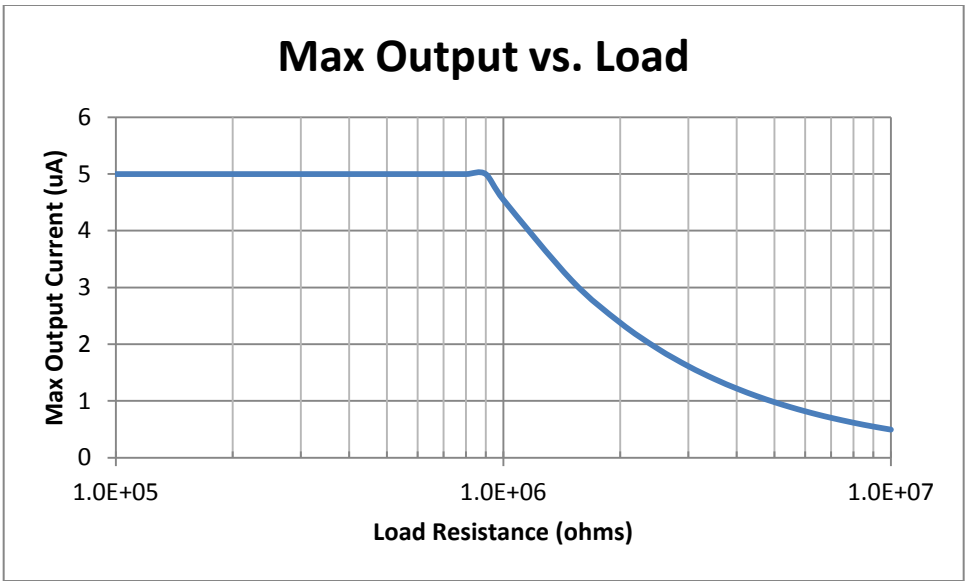


Figure 20: Maximum Output vs. Load Resistance

The minimum output current limitation occurs because the op amp output approaches the negative rail. Note that the op amp output is the sum of the load voltage and the set voltage ($V_{OPA\_OUT} = V_{LOAD} + V_{SET}$). For low currents and low output resistances the op amp output voltage approaches 0 V and becomes nonlinear. Normally the voltage swing from the rail specification is used to determine how close the amplifier output can be to the negative rail as shown in Table 3. However, in this case the op amp output current is very low compared to the test condition in the specification table, so the op amp can swing much closer to ground than the table would indicate. A better specification in this case is the open loop gain AOL specification as shown in Table 4. The test condition in the AOL specification indicates that AOL is not specified for outputs less than 100 mV from the power supply rails. For outputs less than 100 mV from the rails, AOL will be degraded. Degraded AOL will cause nonlinearity errors for outputs less than 100 mV from the rail. This behavior cannot be confirmed using TINA-TI™ SPICE.

Table 3: Excerpt from OPA333 data sheet showing voltage swing from rail

PARAMETER	TEST CODITIONS	MIN	TYP	MAX
Voltage output Swing from Rail	RL = 10k, IL = 250µA		30mV	50mV

Table 4: Excerpt from OPA333 data sheet showing nonlinearity 100mV from rail

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX
Open Loop Gain	Aol	(V-) + 100mV < Vout < (V+) -100mV, RL=10k	106dB	130dB	

Based on Table 4 we know that the output of the OPA333 will become nonlinear for outputs less than 100 mV. The op amp output voltage is across the series circuit R_{SET} and R_{LOAD}. The minimum output current required to avoid the 100 mV non-linear region can be calculated easily using Equation 16 Equations 17 and 18 give example calculations showing the minimum output for 100 Ω and 100 kΩ loads. Figure 21 graphs Equation 16 over a wide range of resistances.

$$I_{OUT\_MIN} = \frac{100mV}{R_{SET} + R_{LOAD}} \tag{16}$$

For example, assume R_{LOAD} = 100 Ω

$$I_{OUT\_MIN} = \frac{100mV}{R_{SET} + R_{LOAD}} = \frac{100mV}{100k\Omega + 100\Omega} = 0.999\mu A \tag{17}$$

Copyright © 2013, Texas Instruments Incorporated

For example, assume R_{LOAD} = 100 kΩ

$$I_{OUT\_MAX} = \frac{100mV}{R_{SET} + R_{LOAD}} = \frac{100mV}{100k\Omega + 100k\Omega} = 0.5\mu A \quad (18)$$

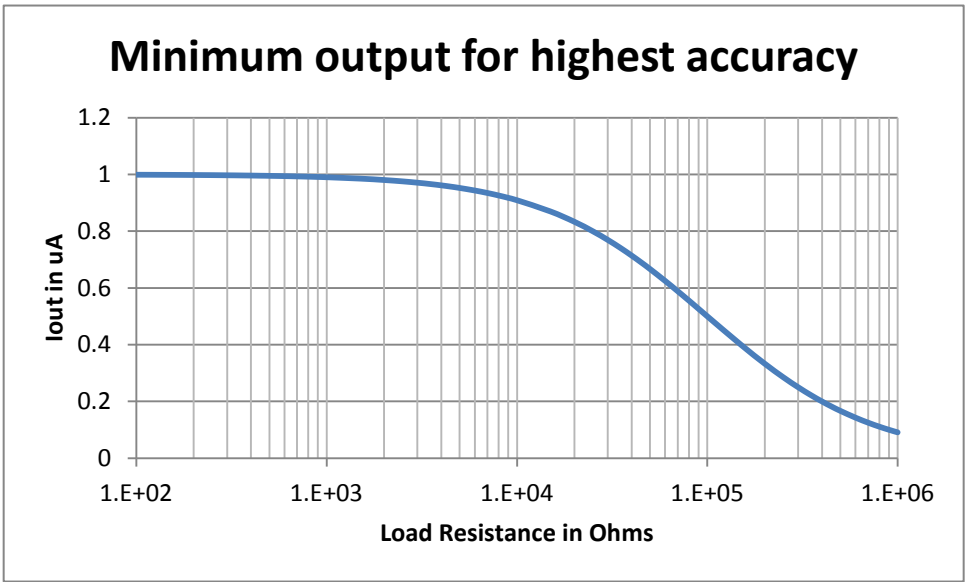


Figure 21: Minimum Output for Highest Accuracy

Copyright © 2013, Texas Instruments Incorporated

The 100 mV limitation is a guideline for highest accuracy. The actual amplifier performance will generally be better than the expected limitations. Figure 22 shows the measured output error for a 50 kΩ load for four different measurement runs. The error for low output currents (i.e. 0 µA to 50 µA) is high compared with the error across the remainder of the range. This is because of the 100 mV minimum output limitation. The measured results correspond well with the theoretical results given in Figure 22.

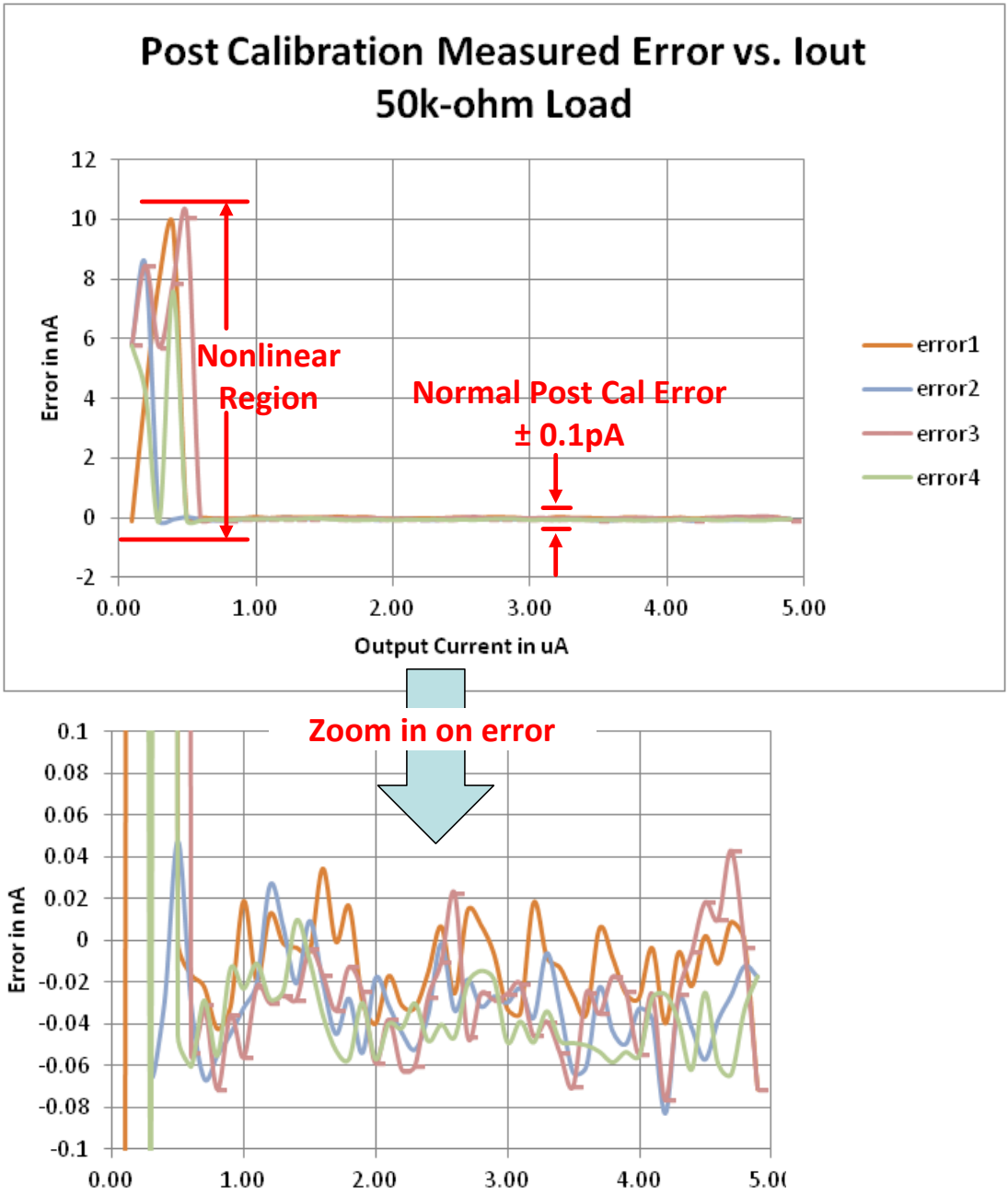


Figure 22: Post calibration error showing nonlinearity error for low op amp outputs

Copyright © 2013, Texas Instruments Incorporated

Figure 23 shows measured results that confirm that the output compliance to ground improves with heavy loads. The limitations shown in Figure 22 correlate with the minimum output limitations given in Figure 21.

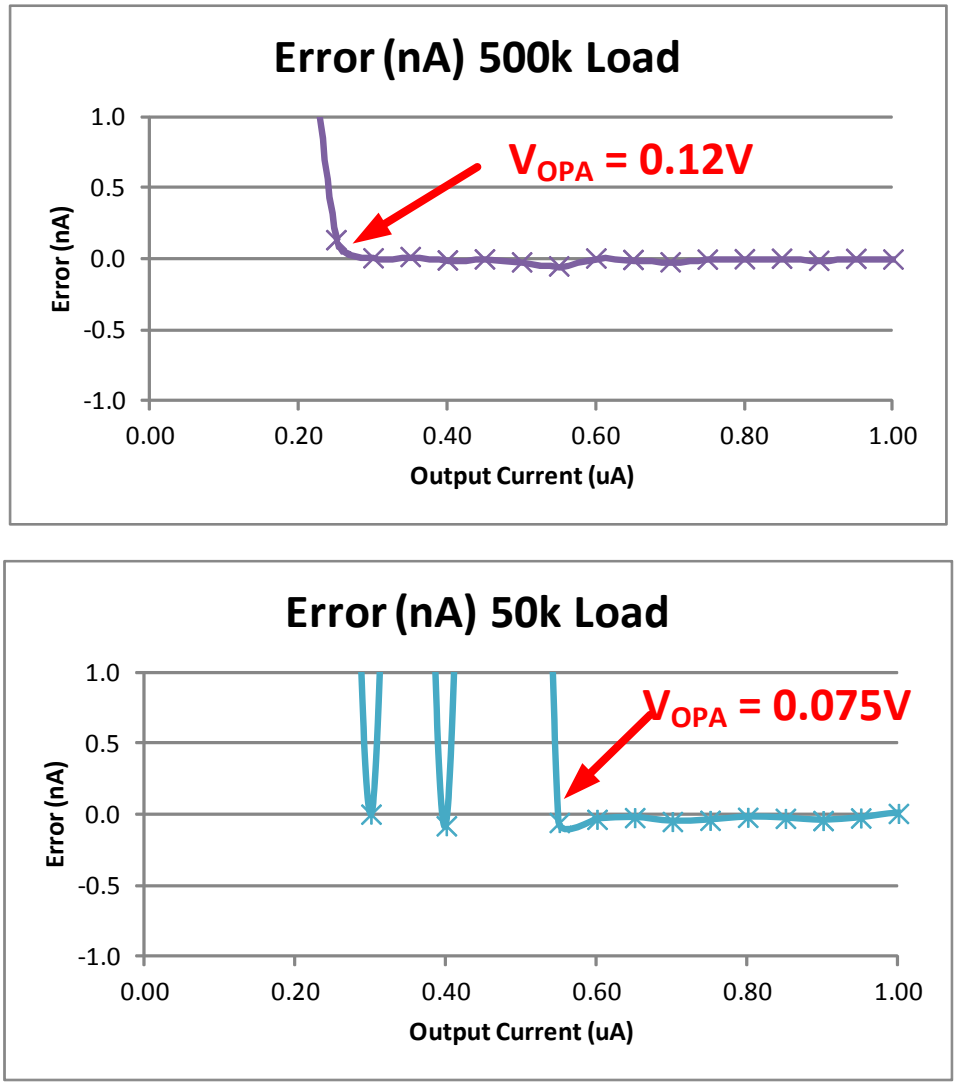


Figure 23: Larger loads have better minimum output compliance limitations

6.6 Measured Result Summary

The final summary comparing measured and simulated results to the goals is given in Table 5.

Table 5: Comparison of Design Goal, Simulation, and Measured Performance

	Goal	Simulated	Measured
Uncalibrated Accuracy (%FSR)	0.2%	0.3%	0.18%
Calibrated Accuracy (%FSR)	0.01%	na	0.001%
Load Compliance 0<R<500 kΩ Max Linear Output (µA)	4.0 µA	4.9 µA	4.9 µA
Load Compliance 0<R<500 kΩ Min Linear Output (µA)	1.0 µA	0 µA	0.6 µA

Copyright © 2013, Texas Instruments Incorporated

7 Modifications

7.1 Selecting different amplifiers

The components selected for this design were based on the design goals outlined at the beginning of the design process. Selecting a chopper-stabilized amplifier such as the OPA333 removes most of the dc errors and drift normally attributed to the amplifier in this design. Calibration can be used to obtain the highest accuracy.

Table 6: Brief Comparison of Amplifiers

Amplifier	Max Supply Voltage (V)	Max Offset Voltage (µV)	Max Offset Drift (µV/C)	Bandwidth (MHz)	Quiescent Current (µA)
OPA333	5.5	10	0.05	0.35	34
OPA335	5.5	5	0.05	2	700
OPA320	5.5	150	5	20	1600
OPA735	12	5	0.05	1.6	1500
OPA188	36	25	0.085	1	950

7.2 Selecting different gain

The gain of the instrumentation amplifier was set to a gain of 10 V/V to improve the compliance. For a full scale input of 5 V the voltage across the set resistor is 0.5 V which allows for load voltages up to 4.5 V. Unfortunately, using a gain of 10 V/V will degrade the performance when low resistance loads are driven by low current levels (e.g. 100 Ω x 0.1 µA). In this case the overall output voltage from the op amp is near ground and it becomes non-linear (e.g. $V_{OPA} = V_{SET} + V_{LOAD} = 0.01\ V + 10\ \mu V = 0.01\ V$).

A lower gain (e.g. $G_{INA} = 1\ V/V$) can be used in the case that low value resistance loads are driven by low current levels. For example, if a 100 µA load is driven by a 0.1 µA current the op amp output voltage will be about 0.1 V. However, making this change will degrade the compliance for larger loads.

7.3 Selecting different current output range

Many of the difficulties in achieving a high degree of accuracy in this design relate to low current design. For example, the careful and thorough cleaning of the board is needed because we are attempting to get a microamp signal that is stable out to nanoamps. If the output range of the circuit is scaled for higher output current (e.g. 100 µA), then special attention to low current considerations (e.g. cleaning) will not be as critical. On the other hand, if the output is scaled for lower current (e.g. 100 nA), then other special low current techniques may be needed to achieve the highest accuracy. For example, an ultra-low current reference may require guarding, low triboelectric effect cables, special materials, special precision resistors, and many other precautions.

7.4 Dual Supply Version

This circuit can be easily modified for dual supply operation. The advantage of the dual supply configuration is that it can both source and sink current.

Copyright © 2013, Texas Instruments Incorporated

8 About the Author

Arthur Kay is an applications engineering manager at TI where he specializes in the support of amplifiers, references, and mixed signal devices. Arthur focuses a good deal on industrial applications such as bridge sensor signal conditioning. Arthur has published a book and an article series on amplifier noise. Arthur received his M.S.E.E. from Georgia Institute of Technology, and B.S.E.E. from Cleveland State University.

9 Acknowledgements & References

1. *Green, T., Operational Amplifier Stability, Parts 1 – 11, November 2008, http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712*

2. *Grohe, P., Design femtoampere circuits with low leakage, Parts 1 – 3, November 2011, http://www.edn.com/design/analog/4368681/Design-femtoampere-circuits-with-low-leakage-part-one?page=3*

3. *Low Level Measurements Handbook, Sixth Edition, Keithley Instruments, 2004*

Copyright © 2013, Texas Instruments Incorporated

Appendix A.

A.1 Electrical Schematic

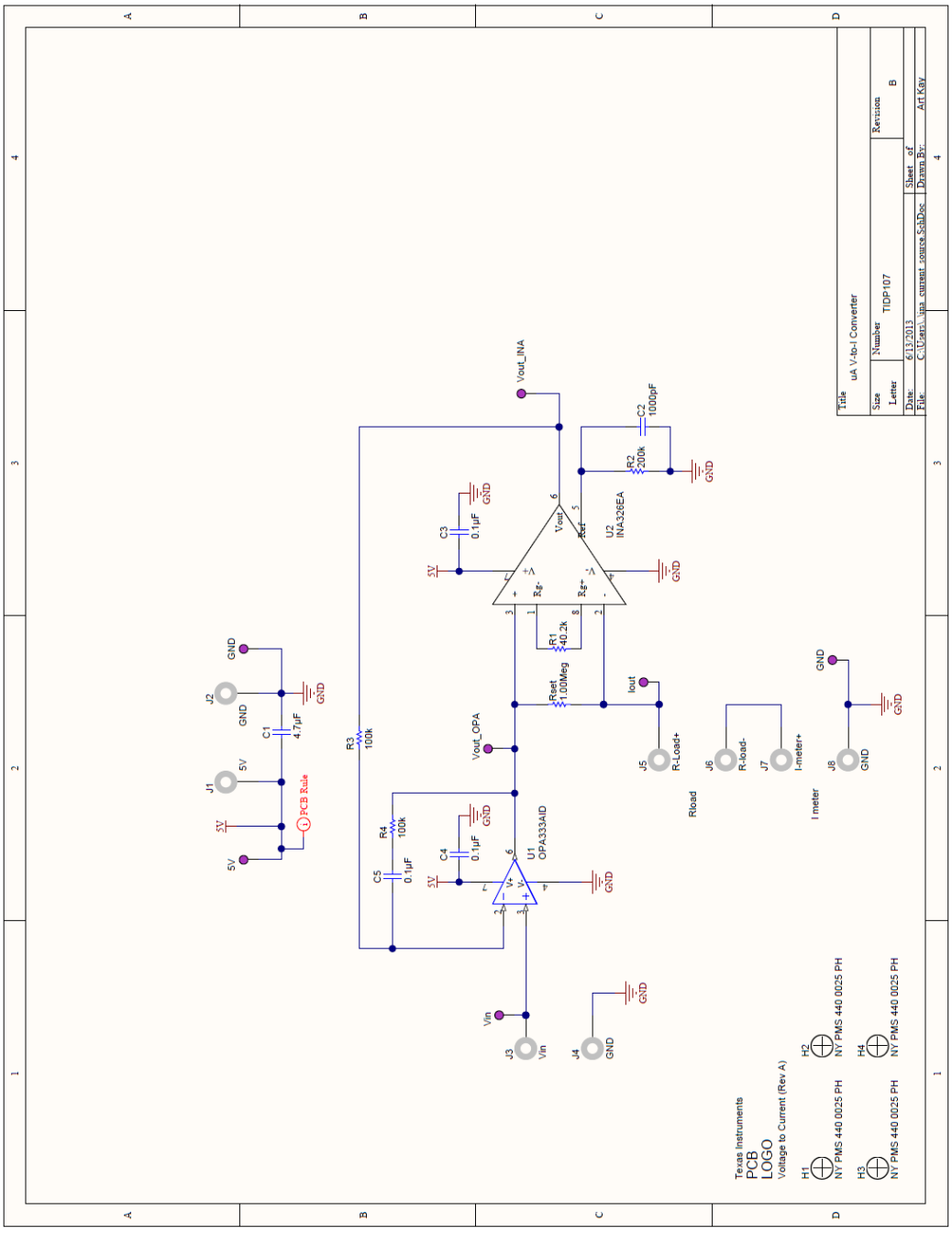


Figure A-1: Electrical Schematic

Copyright © 2013, Texas Instruments Incorporated

A.2 Bill of Materials

Item	Qty	Value	Designator	Description	Manufacturer	Manufacturer Part No.	DigiKey PartNumber
1	1	4.7uF	C1	CAP, CERM, 4.7uF, 16V, +/-20%, X7R, 1206	TDK	C3216X5R1H475K160AB	445-5994-1-ND
2	1	1000pF	C2	CAP, CERM, 1000pF, 50V, +/-1%, C0G/NP0, 0805	AVX	08055A102FAT2A	478-3759-1-ND
3	3	0.1uF	C3, C4, C5	CAP, CERM, 0.1uF, 50V, +/-5%, X7R, 0805	AVX	08055C104JAT2A	478-3352-1-ND
4	4			MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener	PMS 440 0038 PH	H782-ND
5	4		H1, H2, H3, H4	STANDOFF HEX 4-40THR ALUM .500"L	Keystone	2203	2203K-ND
6	8		J1, J2, J3, J4, J5, J6, J7, J8	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	5-4K-ND
7	1	40.2k	R1	RES, 40.2k ohm, 0.1%, 0.125W, 0805	TE Connectivity	676335-2	A102342CT-ND
8	1	200k	R2	RES, 200k ohm, 0.1%, 0.125W, 0805	TE Connectivity	4-1676971-2	A102090CT-ND
9	2	100k	R3, R4	RES, 100k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW0805100KFKEA	541-100KCCT-ND
10	1	1.00Meg	Rset	RES, 1.00Meg ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW08051M00FKEA	541-1.00MCCT-ND
11	2		TP1, TP7	Test Point, TH, Compact, Black	Keystone	5124	5001K-ND
12	1		TP2	Test Point, TH, Compact, Red	Keystone	5005	5005K-ND
13	1		TP3, TP4, TP5, TP6	Test Point, TH, Compact, Purple	Keystone	5124	5124K-ND
14	1		U1	Single JFET Input Op Amp	Texas Instruments	OPA333AID	296-19545-5-ND
15	1		U2	IC OPAMP INSTR R-R 1KHZ 8VSSOP	Texas Instruments	INA326EA/2K5	INA326EA/2K5CT-ND

Figure A-2: Bill of Materials

Copyright © 2013, Texas Instruments Incorporated

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated