TEXAS INSTRUMENTS

Thunderbird TAS5100EVM

Evaluation Module for the TAS5100 Digital Audio PWM Power Output Stage

User's Guide

July 2003

Digital Audio/Application

SLEU009B

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This manual describes the operation of the TAS5100EVM evaluation module from Texas Instruments.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – Introduction
- ❏ Chapter 2 – Description of the EVM Board
- ❏ Chapter 3 – EVM Board Operation Overview
- ❏ Chapter 4 – Hints for Performance Measurements
- ❏ Chapter 5 – Electrical Specifications and Typical Characteristics Graphs

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following is a list of data manual that have detailed descriptions of the integrated circuits used in the design of the TAS5100 EVM. The data manuals can be obtained at the URL http://www.ti.com.

Part Number	Literature Number
TAS5001PFB	SLES009
TAS5010PFB	SLAS328
TAS5100ADAP	SLES030
TAS3002PFB	SLAS307
DIR1703E	SLES007
LMV311IDBVR	SLCS136
SN74LVU04APWR	SCES130
SN74LVC1GU04DBVR	SCES215
SN74AHC1G08DBVR	SCLS314
SN74LVC08APWR	SCAS283
SN74LVC1G14DBVR	SCES218
SN74LVC1G32DBVR	SCES219
SN74LV123APWR	SCLS393
SN74LV132APWR	SCLS394
TPS3705–33DGN	SLVS184
TPS75333QPWP	SLVS241
TPS76433DBVR	SLVS180

Additional TAS5100EVM Documentation

The CD-ROM is attached to the TAS5100EVM package and includes the following documentation:

- ❑ TAS5100EVM User’s Guide (SLEU009) (this document)
- ❑ TAS5100EVM Design Document (SLEU010) (schematic, parts list, PCB layout)
- ❑ TAS5100EVM Data Report (SLEU011) (audio performance and efficiency)
- ❑ TAS5100EVM EMI Test Report (SLEU012)
- ❑ TAS5100EVM Gerber Files
- ❑ Audio Precision Test Files (require AES17 filter installed at the measurement equipment)
- ❑ DCT Software and User’s Guide
- ❑ Application Notes
- ❑ Data Manuals

Photograph of the TAS5100EVM

Components included in the TDAA reference design are surrounded with a white line on the PCB.

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Chapter 1

Introduction

The TAS5100 customer evaluation module (EVM) demonstrates two integrated circuits: the TAS5010 and the TAS5100 from Texas Instruments (TI). The TAS5010 is a cost-effective, high performance 24-bit stereo digital modulator based on Equibit™ technology. This IC converts input PCM serial digital audio data to a pulse width modulated (PWM) audio data stream. The TAS5010 PWM modulator accepts sample rates up to 192 kHz. Maximum sample rate for the TAS5001 is 96 kHz. Pinouts are identical for both modulators. The TAS5010 is designed to be implemented with the TAS5100 true digital output stage for driving a loudspeaker.

Together the TAS5010 and two TAS5100s provide the complete conversion of a 3.3-V digital audio input stream into 30 W for loudspeakers in the 4-Ω to 8-Ω impedance range. The chipset is ideal for applications requiring excellent audio quality, minimum size and weight, and high power efficiency. The chipset can be used in a range of products such as microcomponent systems, home theater in a box, DVD receivers, or TV sets.

The TAS5100EVM is a complete true digital amplifier including a S/DIF receiver, I2S audio interface, volume control, interface to personal computer through the parallel port, and required control logic. The TDAA reference design is surrounded with a white line on the PCB.

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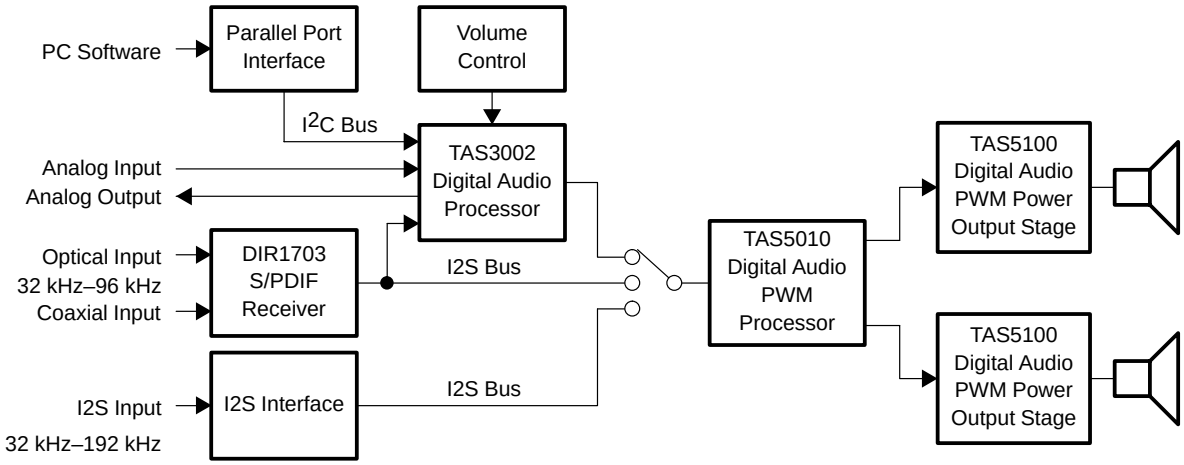
1.1 TAS5100EVM Features

- TDAA reference design (double-sided plated-through PCB layout)
- S/PDIF receiver with coaxial and optical input (sampling rate: 32 kHz–96 kHz)
- I2S audio interface (sampling rate: 32 kHz–192 kHz)
- Onboard volume control
- Auto-mute function
- Self-contained protection system (short circuit and thermal)
- Digital audio processor (DAP), which includes a 24-bit volume control, digital gain, bass and treble control, parametric equalization, dedicated speaker equalization, loudness control, and adjustable dynamic range compression/expansion.
- DAP control through PC software (DCT software from TI)
- Default DAP settings are downloaded to an EEPROM with the DCT software.
- Analog line input (use internal analog-to-digital converter in DAP)

Figure 1–1. Simplified TAS5100EVM Block Diagram



The DIR1703 IC from TI is used as the S/PDIF receiver and system clock generator. The DIR1703 IC is a digital audio interface receiver (DIR) which receives and decodes audio data up to a 96-kHz sampling rate. The DIR1703 is running in a configuration where it automatically switches between PLL mode and crystal mode. When the DIR1703 is connected to an active digital source, it is running in PLL mode. System clock (SCKO) frequency depends on the incoming sampling rate (fs): SCKO = 256 x fs. When no digital source is represented, the DIR1703 switches to crystal mode. The system clock in the crystal mode depends on the external crystal. On the TAS5100EVM board, the crystal-mode system clock is 12.288 MHz.

Crystal-mode operation is used to generate a fixed clock when the TAS5100EVM board is connected to an analog source. The external antialiasing filter for the A/D converter is optimized to the onboard 48-kHz sampling rate.

The TAS3002 IC from Texas Instruments is used as a digital audio processor (DAP). All features in the DAP can be controlled through the I^2C interface. Adjustment of the sound level can be executed through the I^2C bus and with two push buttons on the EVM board.

During power up, the TAS3002 settings and coefficients are loaded from an external serial EEPROM. The TAS3002 coefficients control all features in the DAP. Customized start-up settings can be downloaded to the EEPROM. This operation is easy to execute with a personal computer, DCT software, and a cable between the TAS5100EVM and the computer. The TAS5100EVM is connected to the LPT port at the computer.

Chapter 2

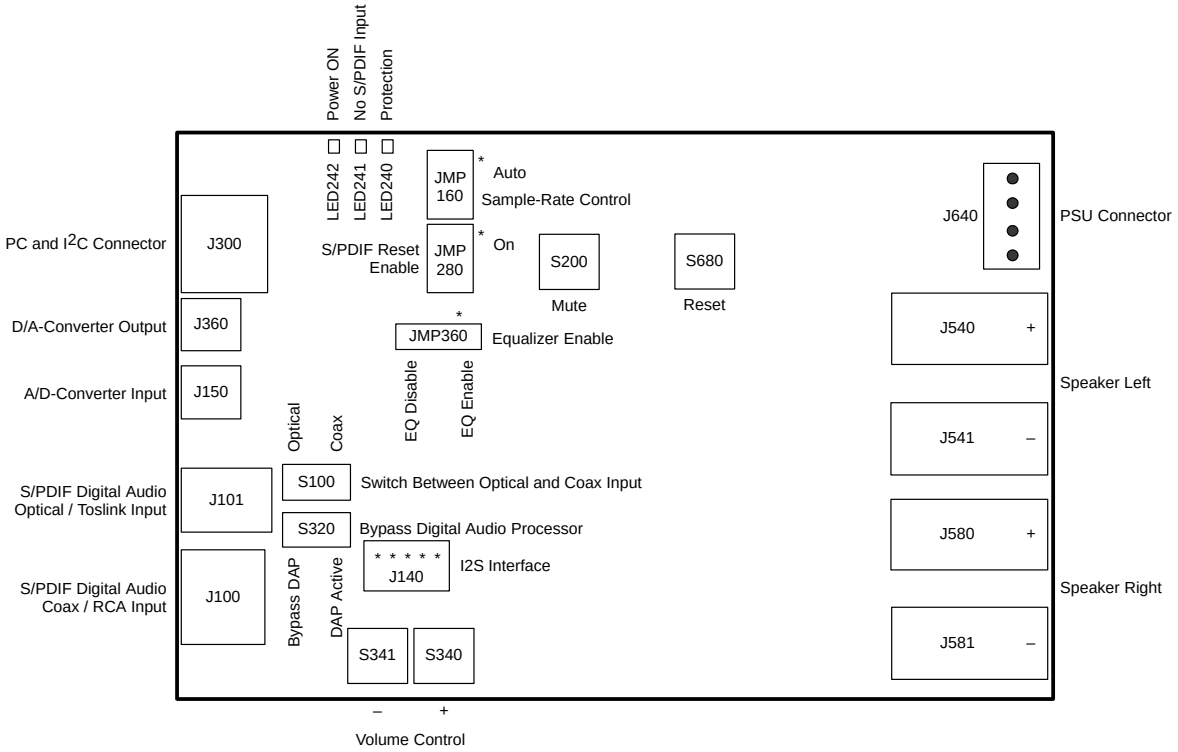
Description of the EVM Board

This chapter describes the TAS5100EVM board layout, jumpers, switches, buttons, and connectors.

Topic **Page**

2.1 Board Outline With Connectors, Switches, Jumpers, and Indicators

Figure 2–1. TAS5100EVM Outline With Reference Designators for Connectors, Switches, Jumpers, and Indicators

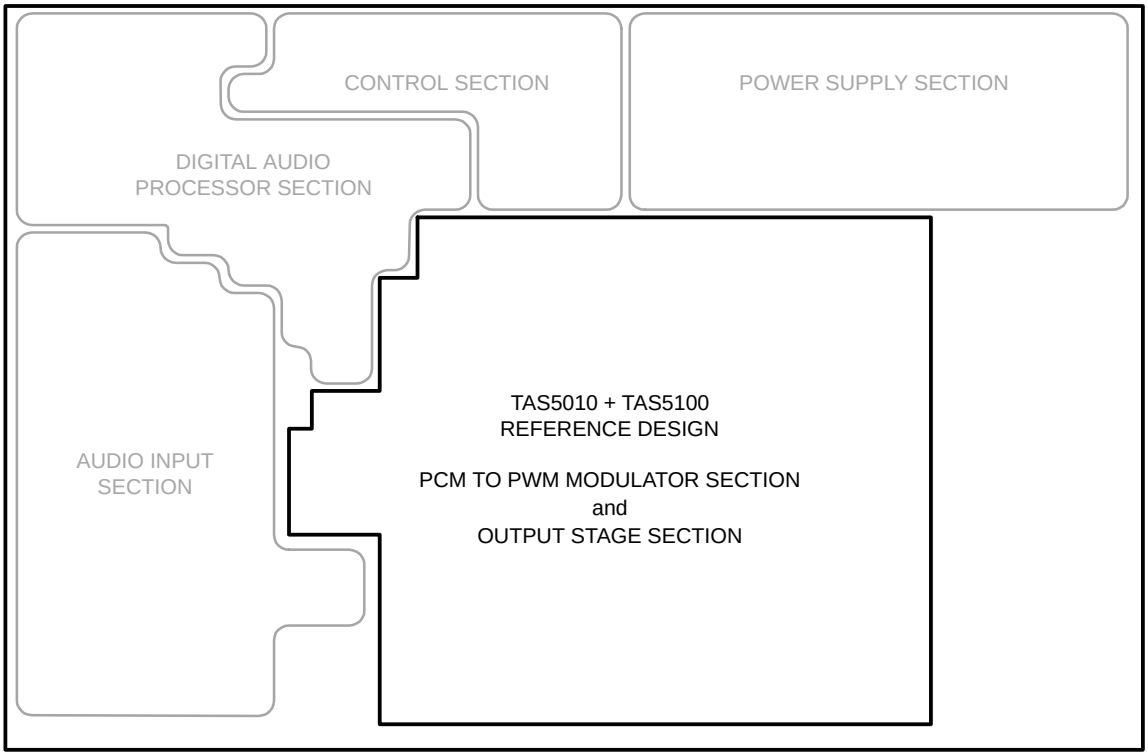


NOTE: * Indicates default jumper position.

2.2 PCB Key Map

The physical structure for the TAS5100EVM is illustrated in Figure 2–2. Block headings refer to page headings in the TAS5100EVM schematic.

Figure 2–2. Physical Structure for the TAS5100EVM (Rough Outline)



2.3 Description of Jumper Settings

There are tree jumpers on the EVM board (J140 is an I2S interface—see the description in Section 2.4.3).

2.3.1 *JMP160: Controls the Double-Speed Pin at the TAS51010*

JMP160 is used to set the double-speed pin at the TAS5010 (DBSPD, pin 39). If the DBSPD is connected to 0 V, the TAS5010 is in single-speed mode and if DBSPD is connected to 3.3 V, the TAS5010 is in double-speed mode. Single-speed mode is required for 32-kHz, 44.1-kHz, 48-kHz, and 192-kHz sampling rates. Double-speed mode is required for 88-kHz and 96-kHz sampling rates.

The S/PDIF receiver automatically controls the DBSPD pin if JMP160 shunts pin 1 and 2 (default setting). If JMP160 shunts pin 2 and 3, the TAS5010 is in single-speed mode. If JMP160 shunts pin 3 and 4, the TAS5010 is in double-speed mode.

2.3.2 *JMP280: Enable/Disable the UNLOCK Signal From the S/PDIF Receiver*

JMP280 is used to disable the UNLOCK warning signal from the S/PDIF receiver. The UNLOCK signal is high until the PLL in the DIR1703 detects and locks on to an incoming digital signal. The warning signal is used to shut down the output stage (the H-bridge stop switching). To obtain click and pop reduced shutdown, it is necessary to mute the output stage before reset on the TAS5010 is pulled down.

When the EVM board is connected to an analog source or to a digital source through the I2S interface, it is necessary to disable the UNLOCK warning. This is done with the JMP280 jumper. When JMP280 shunts pin 1 and 2, the UNLOCK warning is enabled (default setting). If JMP 280 shunts pin 2 and 3, the warning signal is disabled.

2.3.3 *JMP360: Bypass the Equalizer Function in the Digital Audio Processor*

JMP360 is used to disable the equalizer function in the DAP. The equalizer function is enabled if JMP360 shunts pin 1 and 2. The equalizer is disabled when JMP360 shunts pin 2 and 3.

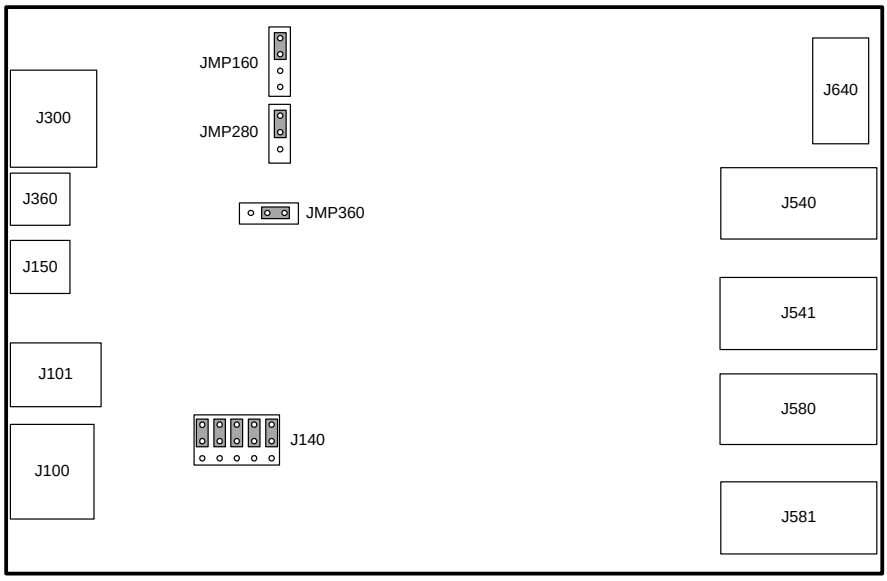
Note:

Bass and treble control is bypassed when the equalizer is bypassed.

2.3.4 Default Jumper Positions

Default jumper positions are illustrated in Figure 2–3.

Figure 2–3. Default Jumper Positions



2.4 Description of Connectors

2.4.1 S/PDIF Digital Audio Coax/RCA Input (J100)

The RCA connector can be connected to a digital S/PDIF source through a coaxial cable with 75-Ω characteristic impedance (e.g. RG59 cable). Maximum sampling rate at this input is 96 kHz.

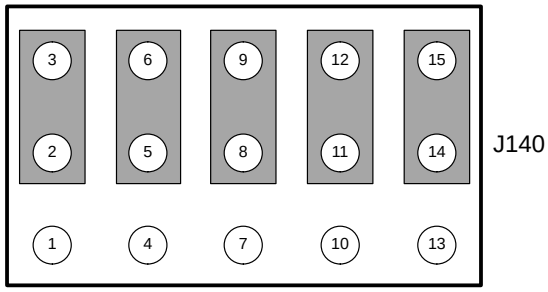
2.4.2 S/PDIF Optical (J100)

The Toslink connector can be connected to a digital S/PDIF signal through an optical cable. Maximum sampling rate at this input is 96 kHz.

2.4.3 I2S Connector (J140)

The I2S connector interfaces directly with the TAS5010. Jumpers are needed for normal operation using the S/PDIF input signal. When the I2S connector is used, the DAP is not in the signal path. Maximum sampling rate at this input is 192 kHz.

Figure 2–4. Pin Numbers at the I2S Interface (J140)



Note: Rectangles indicate default jumper positions.

Table 2–1. I2S Interface Pin Connections

Pin #	Pin Description	Net Name at TAS5100EVM Schematic
2	System master clock input (256 × f_S)	TA50XX–MCLK
5	Audio bit clock input (64 × f_S)	TA50XX–SCLK
8	Left/right clock input (f_S)	TA50XX–LRCLK
11	I2S data input	TA50XX–SDATA
14	Reset output stage input (active low)	$\overline{\text{RESET}}$–I2S–INTERFACE
1, 4, 7, 10, 13	0 V	GND

The serial interface adaptor (SIA–2322) from audio precision can be connected to the I2S interface.

Note:

The unlock signal from S/PDIF must be disabled (JMP280) when the I2S interface is connected to an external source.

2.4.4 Analog Input (J150)

Analog sources can be connected to the A/D converter through J150. The analog line input is optimized for an input signal with a maximum voltage of 2.1 V_{RMS}.

Figure 2–5. Pin Numbers at the Line Input Connector and the Line Output Connector (Top View)

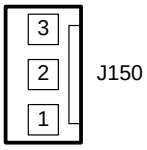


Table 2–2. J150 Pin Description

Pin #	Description
1	Left channel input
2	Ground
3	Right channel input

2.4.5 Analog Output (J360)

Analog output from the digital audio processor is available at the connector. The maximum output level is 0.7 V_{RMS}.

Figure 2–6. Pin Numbers at J360

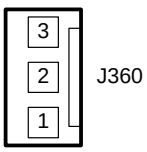


Table 2–3. J360 Pin Description

Pin #	Description
1	Left channel output
2	Ground
3	Right channel output

2.4.6 PC and I²C Interface (J300)

The PC interface, using the attached special cable to parallel/printer port on the PC, makes it possible to control the TAS3002 digital audio processor totally from the PC using the special EQ-GUI software saved on the TDAA CD-ROM.

Figure 2–7. Pin Numbers at Parallel Port Interface/I²C Interface (J300)

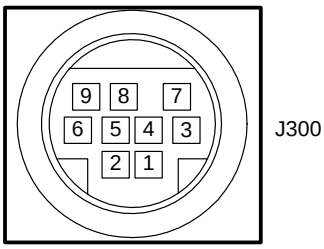


Table 2–4. J300 Pin Description

Pin #	Pin Description	I/O	Net Name at Schematics
1	Power ON reset	Output	$\overline{\text{POWER-ON-RESET}}$
2	Serial data line (SDA)	Bidirectional	SDA–BI
3	Serial clock line (SCL)	Bidirectional	SCL–BI
4	Serial data line in	Input	SDA–IN
5	Serial clock line out	Output	SCL–OUT
6	Not used	–	–
7	Serial data line out	Output	SDA–OUT
8	Serial clock line in	Input	SCL–IN
9	0 V	–	GND

Note: Pin 2 (SDA) and pin 3 (SCL) are used for communication between an external microcontroller and the digital audio processor.

The connector can also be used to control the TAS3002 from an external microcontroller of your choice.

2.4.7 Loudspeaker Connectors (J540, J541, J580, and J581)

All speaker connectors accept standard 4 mm plugs. Use of high quality plugs and speaker cable is recommended.

Caution

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g. through an oscilloscope).

Table 2–5. Description of Loudspeaker Connectors

Pin #	Pin Description
J540	Left speaker positive output terminal
J541	Left speaker negative output terminal
J580	Right speaker positive output terminal
J581	Right speaker negative output terminal

2.4.8 Power Supply Connector (J640)

Figure 2–8. Pin Numbers at the PSU Connector (J640) (Top View)

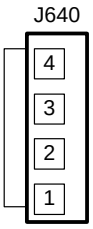


Table 2–6. J640 Pin Description

Pin #	Description	Net Name at Schematics
1	Supply voltage for output stage (VHBR)	Power output stage
2	Supply voltage for control and gate-drive (V+)	—
3	Ground	GND
4	Ground	GND

2.5 Description of Switches and Buttons

2.5.1 S/PDIF Input Selector Switch (S100)

The S100 switches between the optical and coaxial S/PDIF input. When the lever is pressed in the direction of J101, the optical S/PDIF input is selected. When the lever is pressed in the direction of the output stage, the coaxial S/PDIF input is selected.

2.5.2 Bypass Digital Audio Processor Switch (S320)

When the lever is pressed in the direction of J101, the DAP is bypassed. When the lever is pressed in the direction of the output stage, the DAP is in the signal path. Below S320 is a label (DAP ON), which indicates the position of the lever for the DAP inserted in the signal path.

Warning

Bypassing the DAP is equal to the maximum output power (attenuation = 0 dB). This might be loud and could possibly damage your loudspeakers and ears.

2.5.3 Reset Board Button (S680)

Master reset for the EVM board. While this button is held down, the DIR1703, TAS3002, TAS5010, and TAS5100 are held reset and latching errors are cleared. Note that while the RESET button is held down, the No S/PDIF Input LED lights up, even if a valid S/PDIF input signal is present because the DIR1703 S/PDIF receiver is held reset.

2.5.4 Mute Button (S200)

The output stage mutes when the mute button is pressed down and unmutes when the mute button is released.

2.5.5 Volume Control (S340 and S341)

Volume control of the TAS3002 DAP is controlled by S340 and S341. Press and hold the S341 button to decrease the output power level. Press and hold the S340 button to increase the output power level.

Note:

Change of listening level is slow. It takes approximately 25 seconds to change attenuation from –70 dB to 0 dB.

The TAS3002 device implements a soft volume control. This feature allows a change from one volume level to another over the entire range of volume control (18 dB to mute). Above 0 dB there is risk of signal clipping. Distortion of output signals is the result of signal clipping.

Note:

Significant signal clipping might result in activation of the current protection system.

2.6 Description of Indicators

2.6.1 Power ON LED (LED242)

The green LED indicates that the TAS5100 EVM board control circuit is powered on.

2.6.2 No S/PDIF Input LED (LED241)

The yellow LED indicates that the S/PDIF input signal is missing.

Reasons for an S/PDIF warning:

- ❏ The lever at the S/PDIF input selector switch (S100) is placed in the wrong position.
- ❏ The S/PDIF signal is missing. Some DVD players remove the S/PDIF output signal when the drawer is opened.

Note:

When the UNLOCK signal from the S/PDIF receiver is disabled (JMP280 shunted pin 2 and pin 3), the yellow LED is disabled.

2.6.3 Protection LED (LED240)

The red LED indicates that the protection circuit is engaged and the output is in the shutdown mode.

There are four reasons for the shutdown mode.

- ❏ Two speaker terminals are shorted.
- ❏ The amplifier is constantly overloaded (decrease volume level).
- ❏ Speaker terminal is shorted to ground (e.g. through an oscilloscope).
- ❏ Output stage is in thermal shutdown.

Check the setup and board carefully and remove the causing failure before pressing RESET (S680) to disengage the protection mode.

Chapter 3

EVM Board Operation Overview

This chapter describes the TAS5100EVM board operation.

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3.1 Powering the TAS5100EVM

The TAS5100EVM can be powered from one or two external power supplies. High-end audio performance requires a stabilized power supply with low ripple voltage and low output impedance.

Note:

The length of the power supply cable must be minimized. Increasing the length of the PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

3.1.1 Powering the EVM With One Power Supply

A single power supply can be connected to the TAS5100EVM board. Short VHBR and V+ at the power cable (red and white plugs).

Voltage for the connected power supply is not allowed to be below 18 V. Maximum supply voltage depends on the speaker load resistance. Check the recommended maximum supply voltage in the TAS5100 data sheet (SLLS419).

	R_L = 4 Ω	R_L = 6 Ω	R_L = 8 Ω
Supply voltage (VHBR and V+)	18 V–20 V	18 V–23 V	18 V–26 V

3.1.2 Powering the EVM With Two External Power Supplies

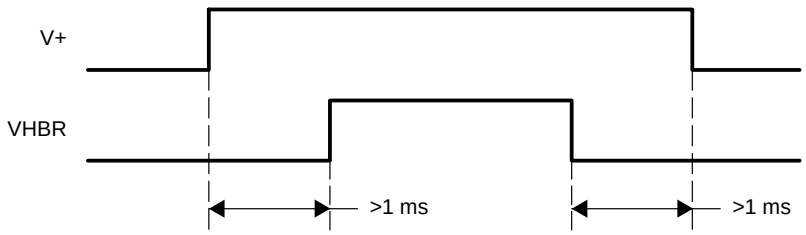
When powering the TAS5100EVM with two power supplies, it is possible to adjust the listening level with the level of the voltage VHBR (pin 1 at J640). Minimum VHBR voltage is 0 V. Maximum voltage depends on the load resistance. Check the recommended maximum supply voltage in the TAS5100 data sheet (SLS419).

	R_L = 4 Ω	R_L = 6 Ω	R_L = 8 Ω
Maximum VHBR voltage	20 V	23 V	26 V
V+ voltage	18 V–27 V	18 V–27 V	18 V–27 V

3.1.3 Recommended Power-Up and Power-Down Sequence

Figure 3–1 shows the recommended power-up and power-down sequence.

Figure 3–1. Recommended Power-Up and Power-Down Sequence

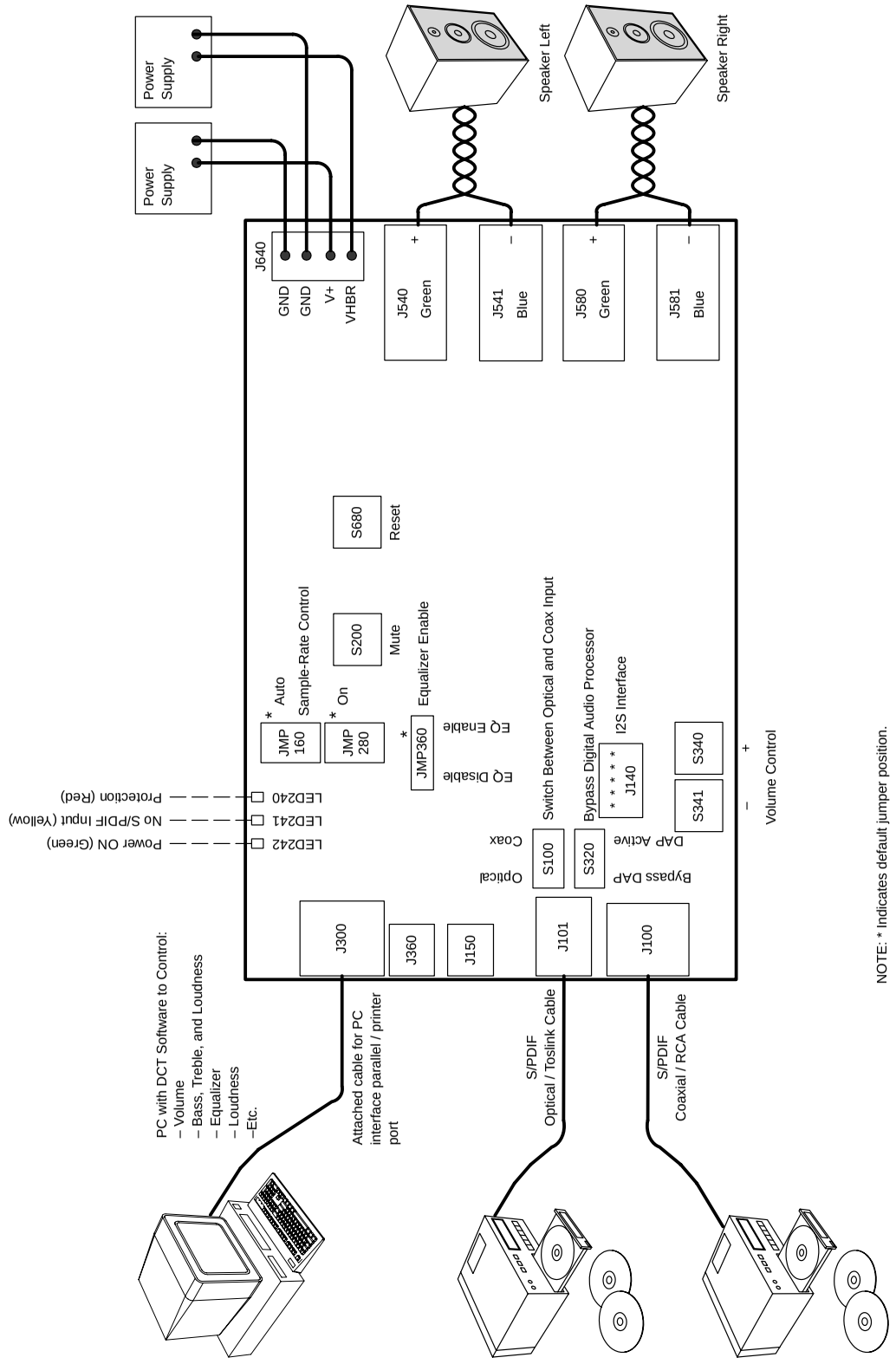


3.2 Setting Up the TAS5100EVM With S/PDIF Input

Connect the EVM board as shown in Figure 3–2. Select between the coaxial or optical input signal at the input selector switch (S100).

Press the lever at S320 in the direction of the output stage if the TAS3002 DAP is wanted in the signal path (recommended during normal listening tests). There is no attenuation if the DAP is bypassed. If the DAP is in the signal path, the start up volume level depends on what is programmed in the serial EEPROM on the EVM board. Default startup volume level is initially programmed to 12 dB below full scale, which on some speakers still may be loud. The default volume level can be changed with the DCT software on the PC.

Figure 3–2. Board Connected to S/PDIF Sources and Personal Computer



Notes: 1) All jumpers are in the default position.

2) Speakers, power supply, and if required a cable for PC communication are initially connected to the EVM board.

3) The TAS5100EVM can be powered with either one or two power supplies (see section 3.1). Power supplies are initially switched off.
4) Music player is initially switched off.
5) PC connection is optional.

3.2.1 Start-Up Sequence

1) Turn on power supply/supplies. Follow the power-up and power-down sequence described in section 3.1. Observe that the green power ON LED and the yellow LED are illuminated.
2) Run the DCT software from a PC desktop if the DAP is activated (S320) and the attached cable is connected from J300 to the PC.
3) Turn on the CD/DVD player and play the test CD. Observe that the yellow No S/PDIF is now off.
4) Observe digital audio coming from the left and right speaker.

3.3 Setting Up the TAS5100EVM With Analog Line Input

1) Disable the UNLOCK warning from the S/PDIF receiver (JMP280: jumper shunts pin 2 and 3).
2) Connect the TAS5100EVM board and the PC with the attached cable.
3) Connect the analog source to the analog input (J150).
4) Power up the TAS5100EVM board.
5) Enable the TAS3002 analog input with the DCT software.
6) Disable the TAS3002 digital input (both SDIN1 and SDIN2) with the DCT software.
7) The TAS5100EVM board is ready to play with an analog source.

3.4 Interfacing the Analog Line Output

The default is the analog line output (J360) being active. The analog line output can be connected to analog tape recorders or analog amplifiers (e.g. subwoofer).

3.5 Controlling the DAP With PC Software

Operating instructions for the DCT software are described in the user's guide Digital Audio Processor (DAP) Configuration Tool Operating Instruction.

Chapter 4

Hints for Performance Measurements

Read the Digital Audio Measurements application note, TI literature number SLAA114, for an introduction to measurements on true digital audio amplifiers.

Use the audio precision test files available on the TDAA CD-ROM. Note that an AES17 filter is required to reach the shown measurements. Specifications for the AES17 filter are described in the AES standard method for digital audio engineering—measurement of digital audio equipment (the AES17 standard is available from Audio Engineering Society— www.aes.org).

When evaluating the performance of the digital amplifier section, bypass the digital audio processor with S320 or adjust all settings to neutral and attenuation to 0 dB.

Connect the TAS5100EVM to a regulated power supply with a cable. The length of the cable must not exceed 0,3 meters.

Chapter 5

Electrical Specifications and Typical Characteristics Graphs

This chapter contains the electrical specifications and the typical characteristics graphs.

Topic **Page**

5.1 TAS5100EVM Electrical Specifications

General Test Conditions					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Power supply	Laboratory power supply (EA–PS 7065–10A)		23		VDC
Load impedance			6		Ω
S/PDIF sampling frequency			44.1		kHz
Electrical Data					
Continuous output power	<0.09% THD+N, 1 kHz, T_A = 25°C		2 x 30		W
Output stage efficiency	P_{OUT} = 2 x 30 W		90%		
Total board idle power consumption			2.8		W
Rated load impedance			4 to 8		Ω
Maximum peak current	1-kHz burst		>7		A
Damping factor	1 kHz, load = 8 Ω		15		
Coaxial S/PDIF Input					
THD+N, 1 W	1 kHz		0.034%		
THD+N, 30 W	1 kHz		0.079%		
Dynamic range, A-weighted	Reference: rated power, AES17 filter		93		dB
Channel separation	1 kHz, P_{OUT} = 30 W		70		dB
Frequency response	0.5 dB – 0.1 dB, 25 W		20 Hz – 20 kHz		
Analog Line Input					
THD+N, 1 W	1 kHz		0.03%		
THD+N, 30 W	1 kHz		0.08%		
Dynamic range, A-weighted	Ref: rated power, AES17 filter		91		dB
Channel separation	1 kHz, P_{OUT} = 30 W		70		dB
Frequency response	±0.5 dB, 25 W		35 Hz – 20 kHz		
Sensitivity	30 W		2.25		V_{RMS}
Input impedance	1 kHz		10		kΩ
Analog Line Output					
Maximum output voltage			0.71		V_{RMS}
Output impedance	1 kHz		75		Ω

Note: All electrical and audio specifications are typical values.

5.2 Physical Specifications

PCB dimensions	85 x 130 mm (3.35 x 5.12”)	Height x Width
Aluminum plate dimension	115 x 160 mm (4.52 x 6.3”)	Height x Width
Board weight	0,15 kg (0.33 lb)	Components + PCB
Total weight	0,25 kg (0.55 lb)	Components + PCB + Mechanics

5.3 Typical Characteristics Graphs

Figure 5–1. THD+N vs Frequency – Left Channel

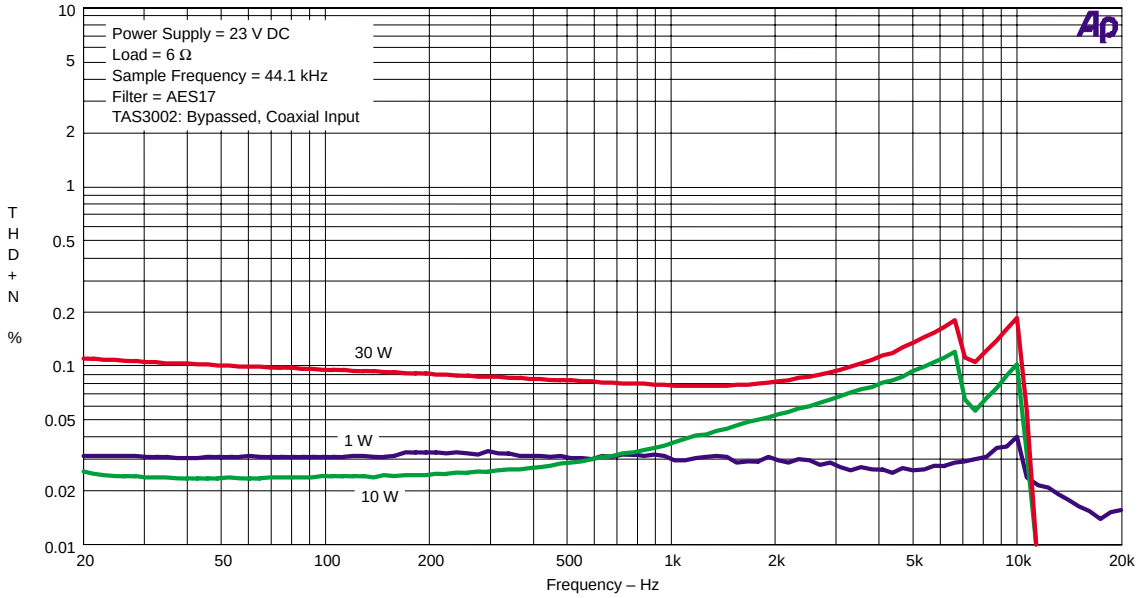


Figure 5–2. THD+N vs Frequency – Right Channel

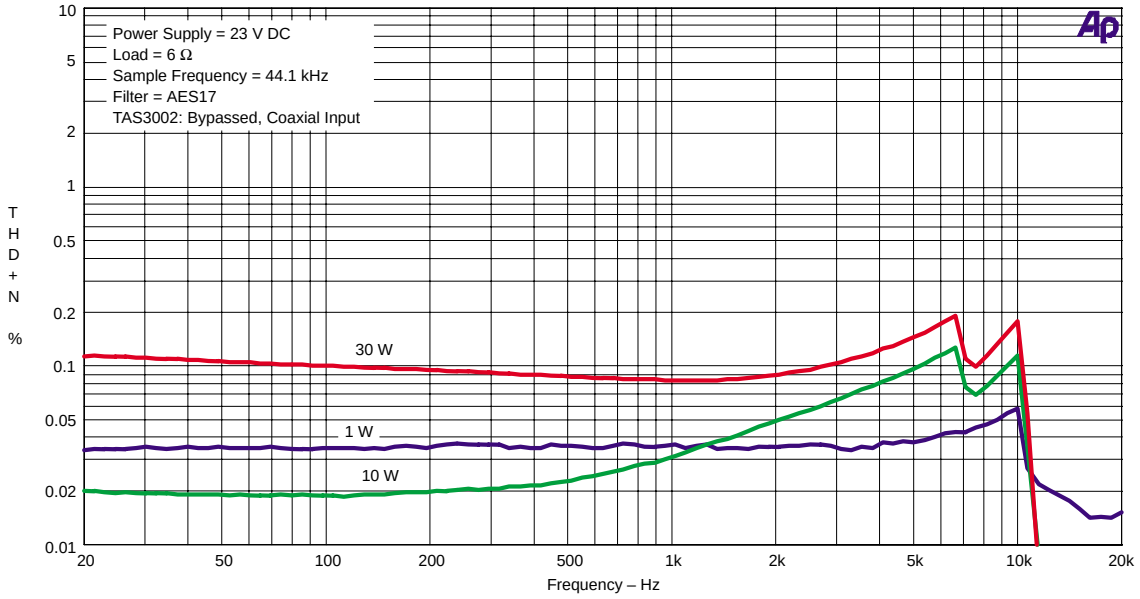


Figure 5–3. THD+N vs Power – Left Channel

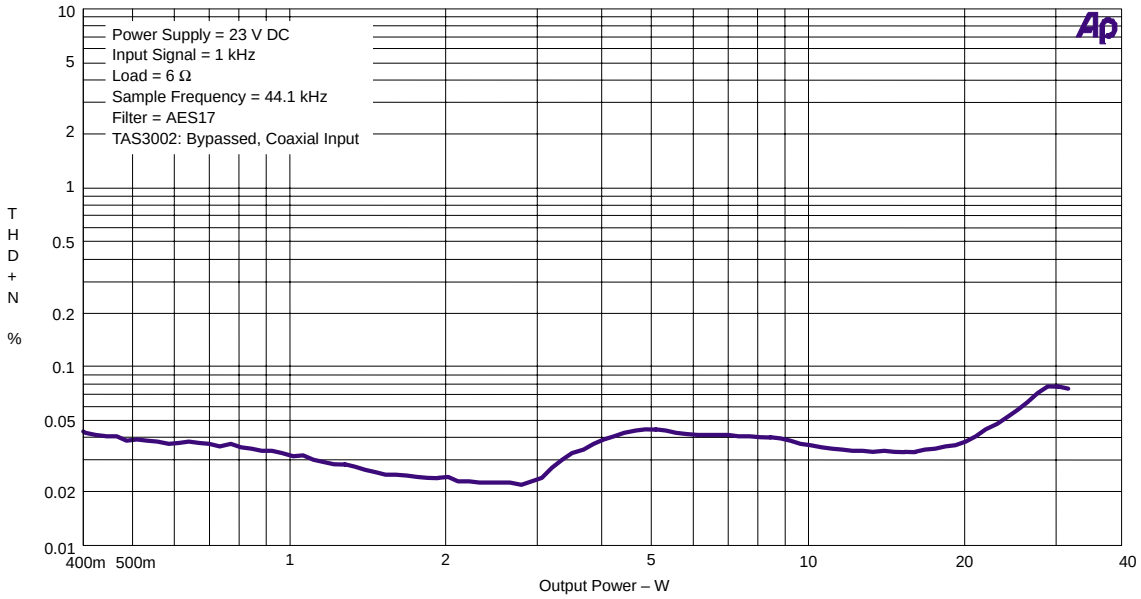


Figure 5–4. THD+N vs Power – Right Channel

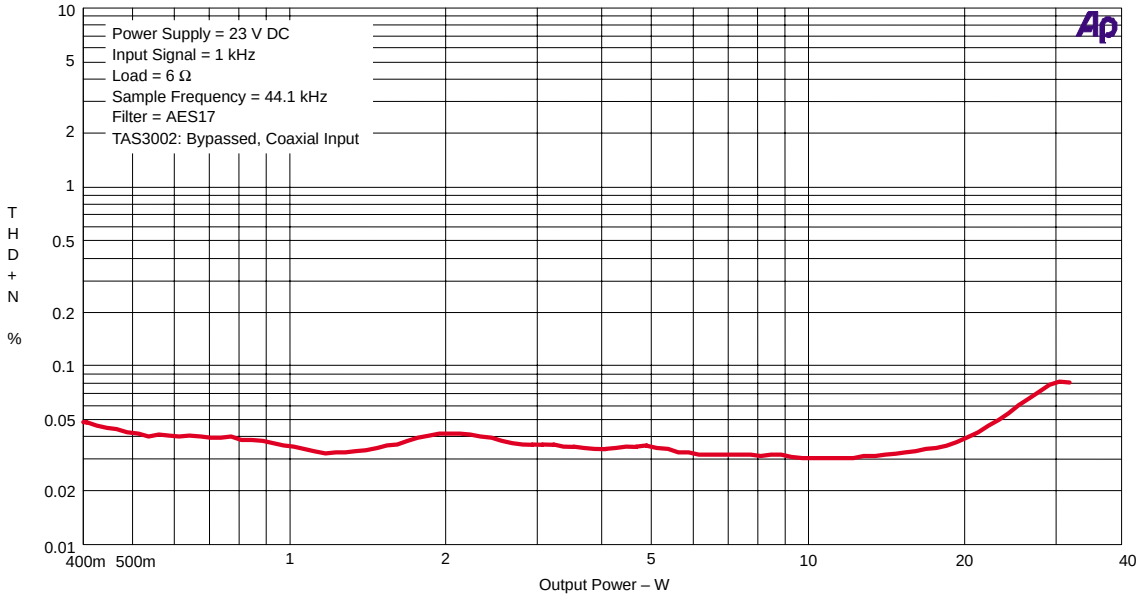


Figure 5–5. Signal-to-Noise FFT With –60 dB 1-kHz Signal – Left Channel

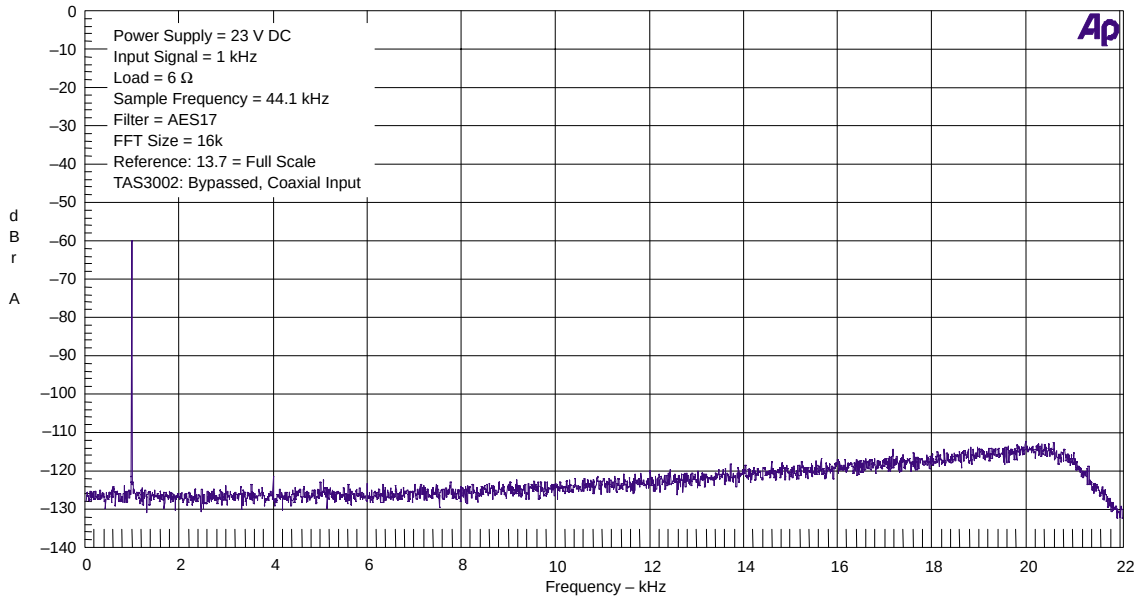


Figure 5–6. Signal-to-Noise FFT With –60 dB 1-kHz Signal – Right Channel

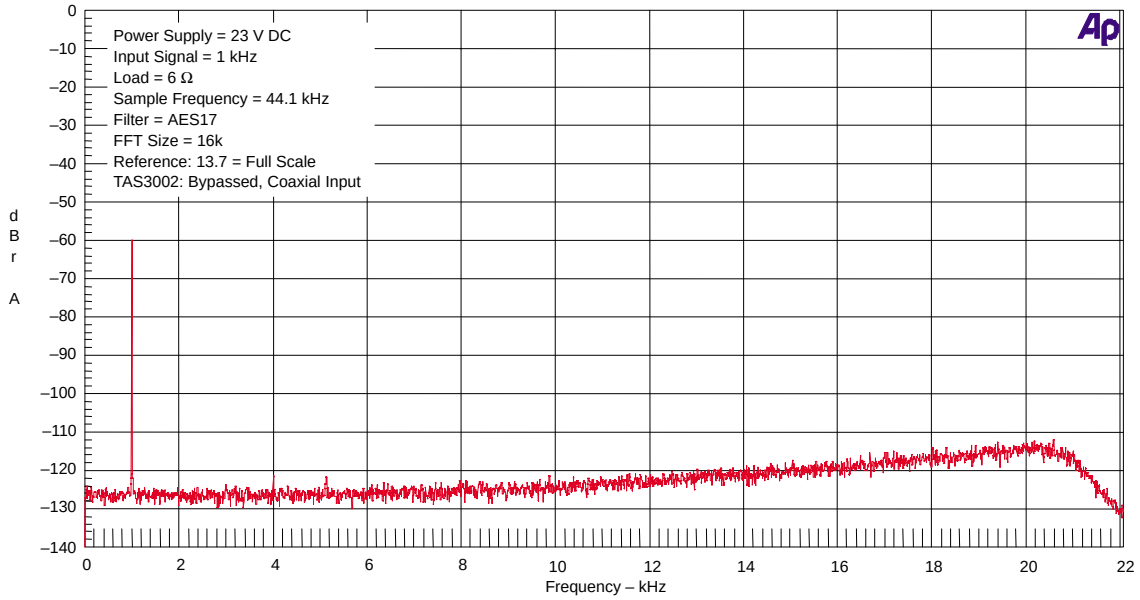


Figure 5–7. FFT at 30-W Output Power – Left Channel

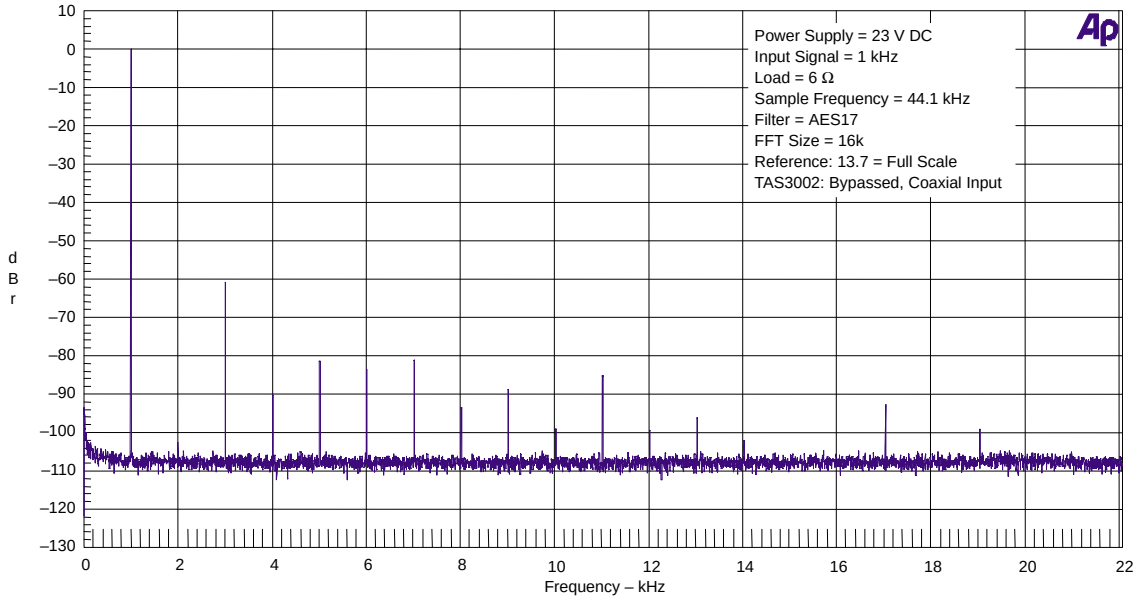


Figure 5–8. FFT at 30-W Output Power – Right Channel

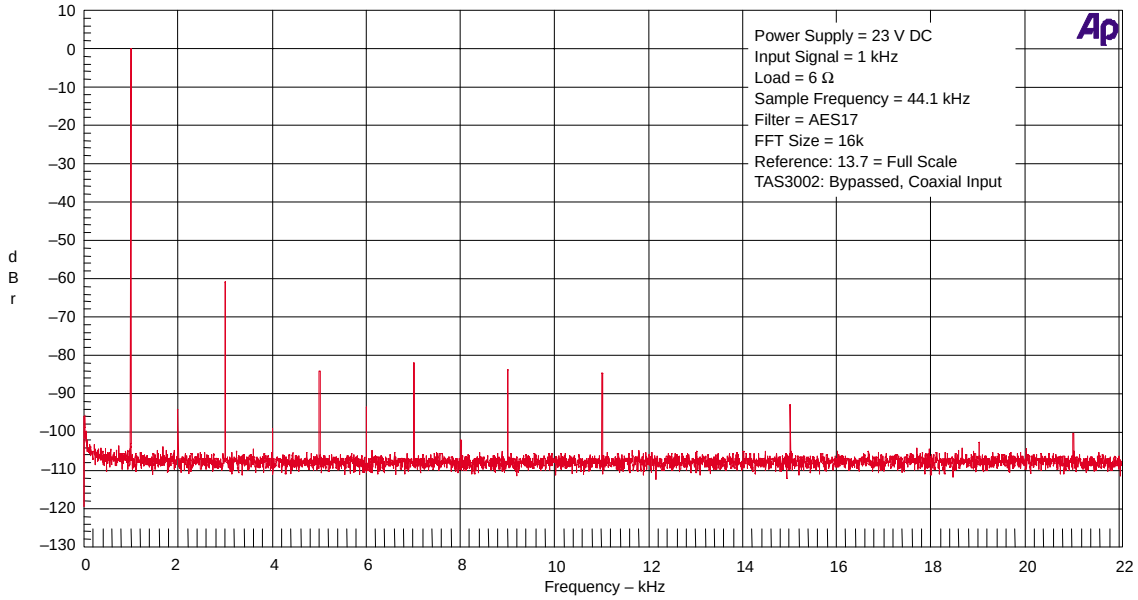


Figure 5–9. Noise Floor – Left Channel

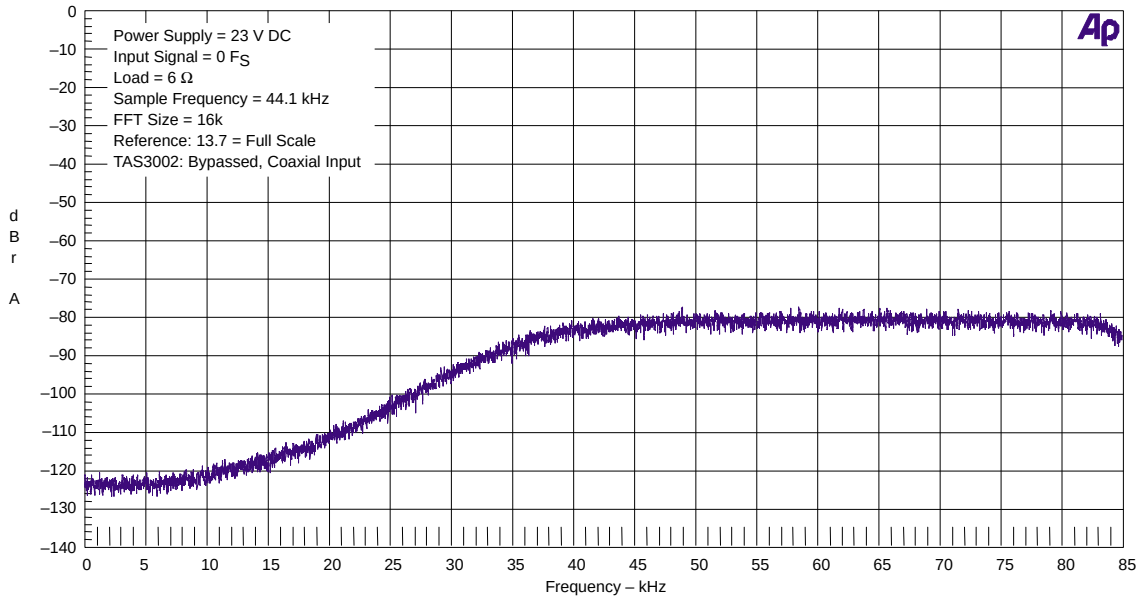


Figure 5–10. Noise Floor – Right Channel

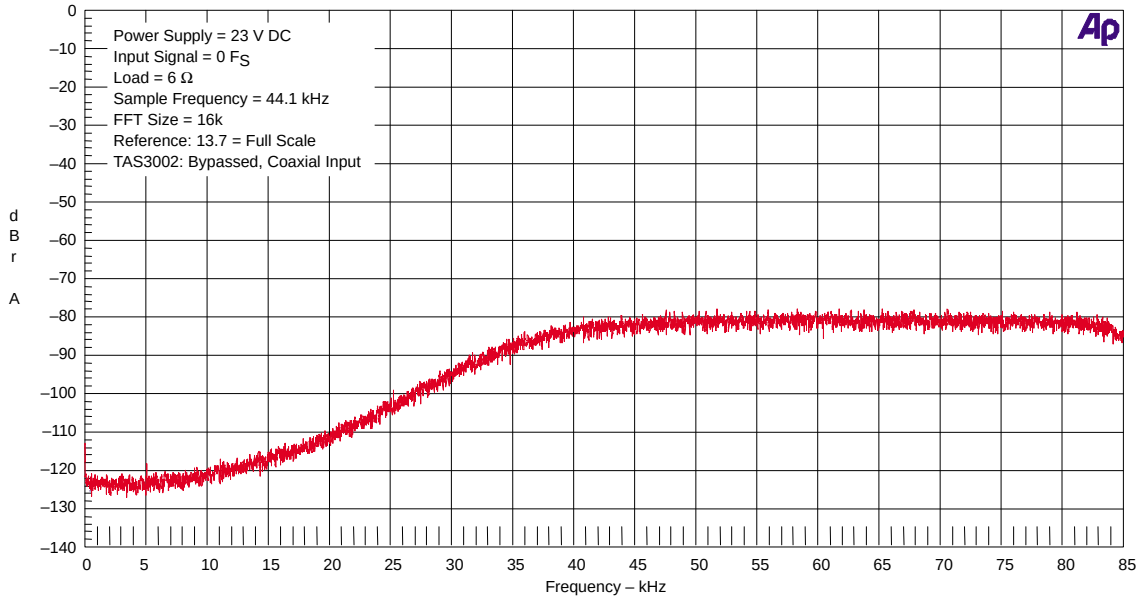


Figure 5–11. Channel Separation – Left Channel

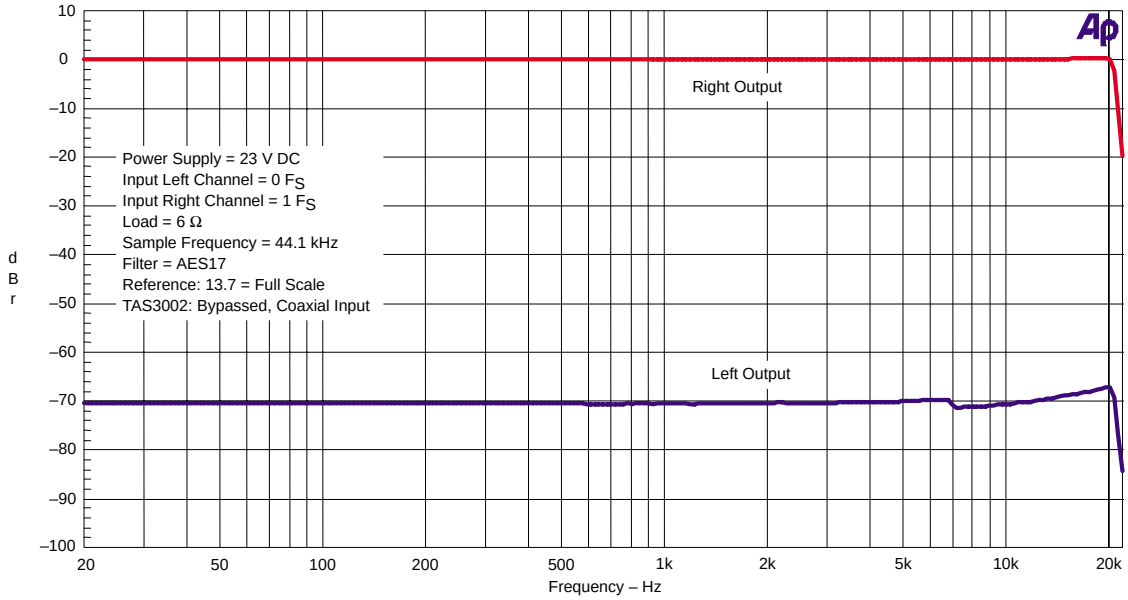


Figure 5–12. Channel Separation – Right Channel

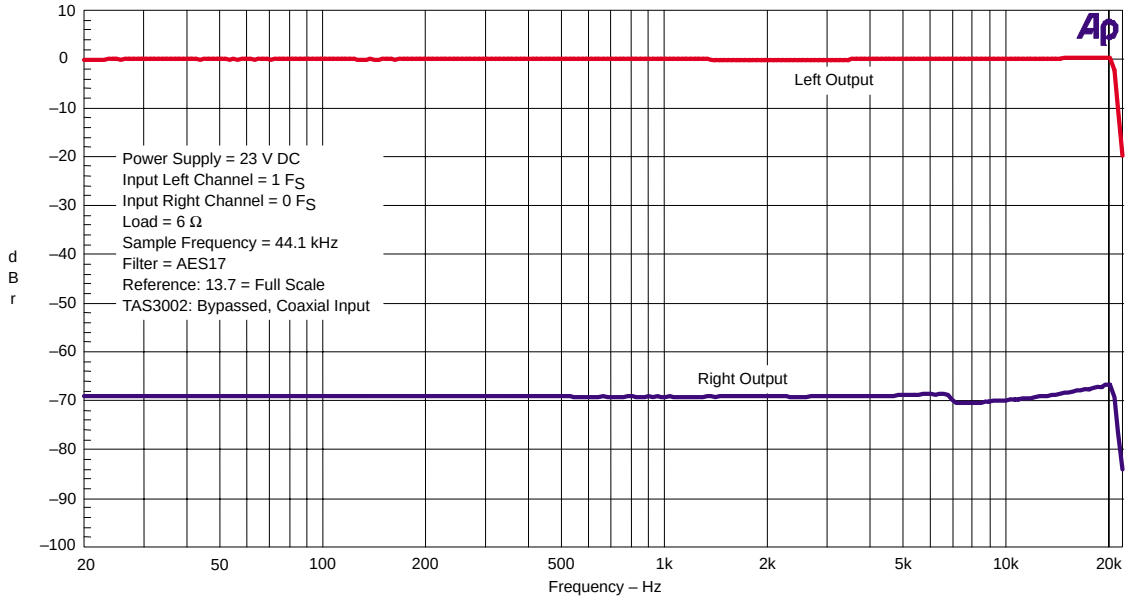


Figure 5–13. Channel Separation FFT – Left Channel

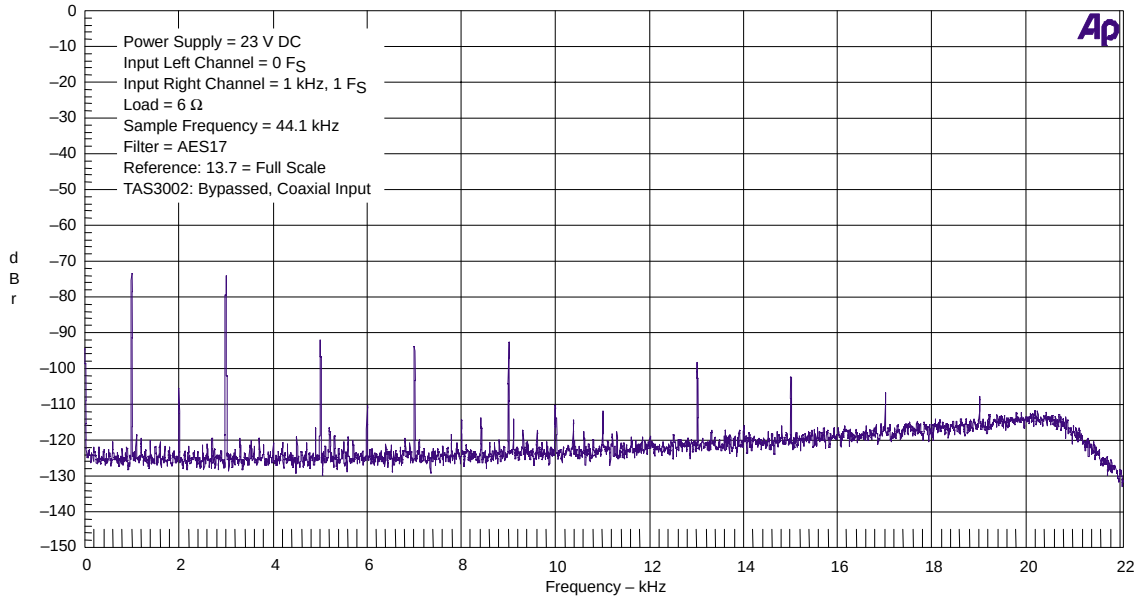


Figure 5–14. Channel Separation FFT – Right Channel

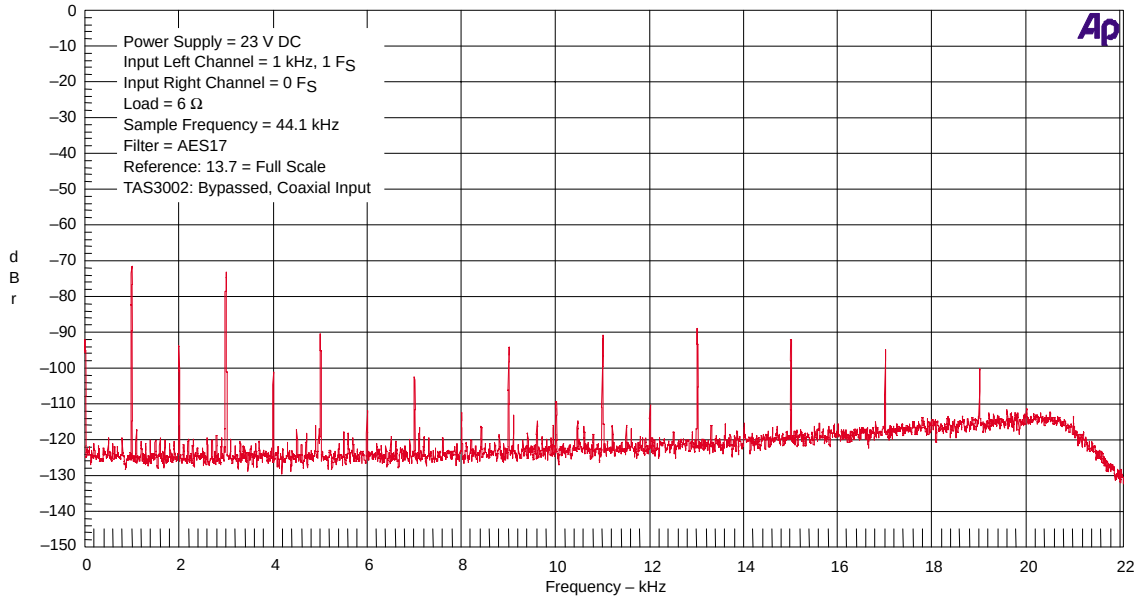


Figure 5–15. Frequency Response – Left Channel

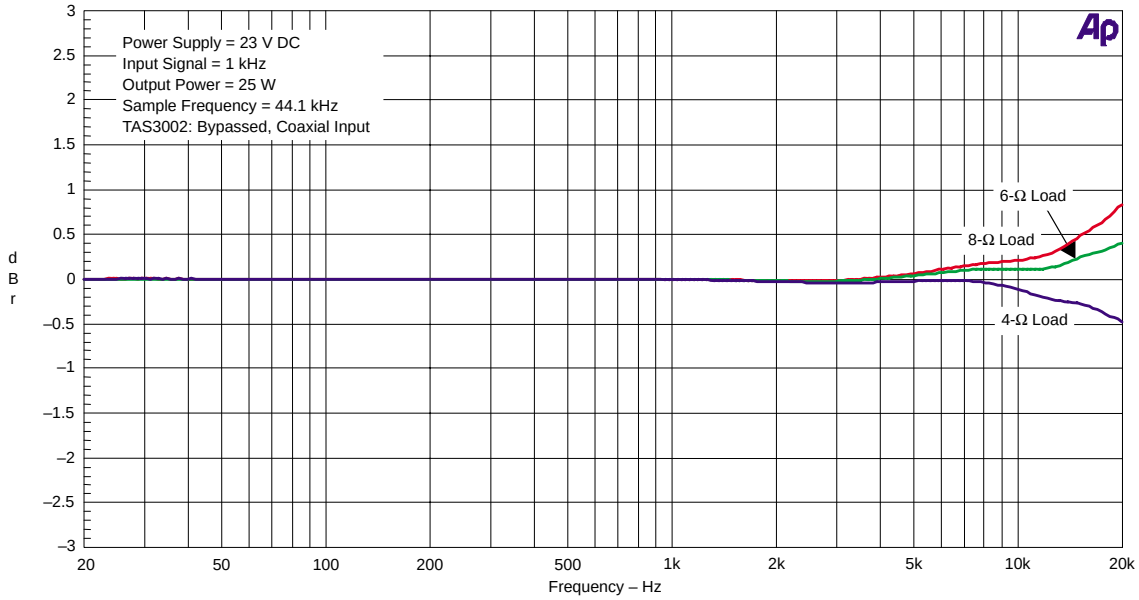


Figure 5–16. Frequency Response – Right Channel

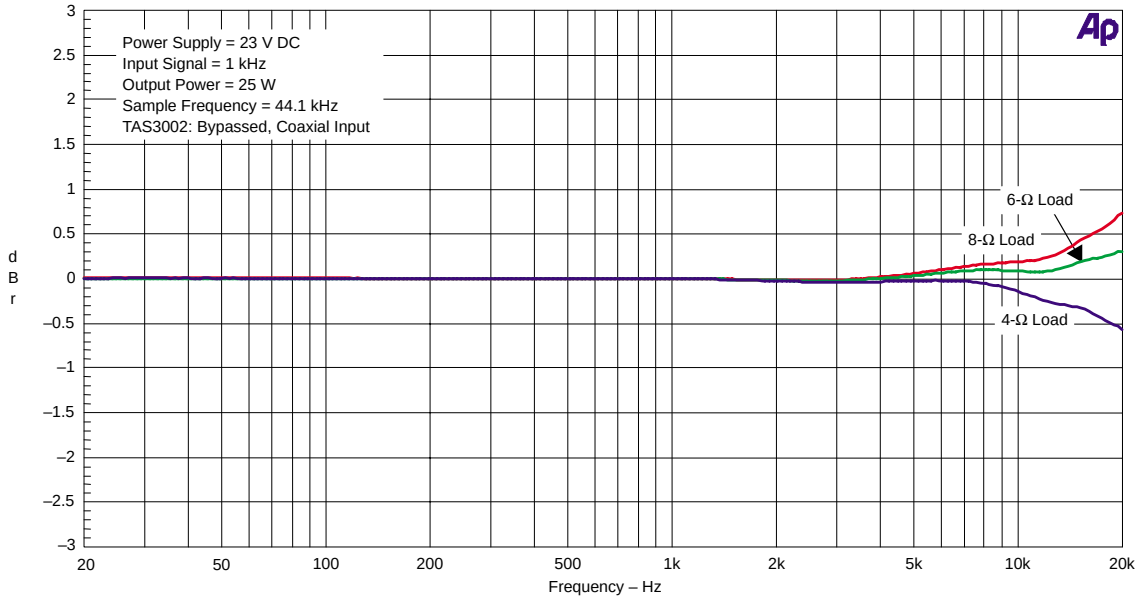


Figure 5–17. Peak Current – Left Channel

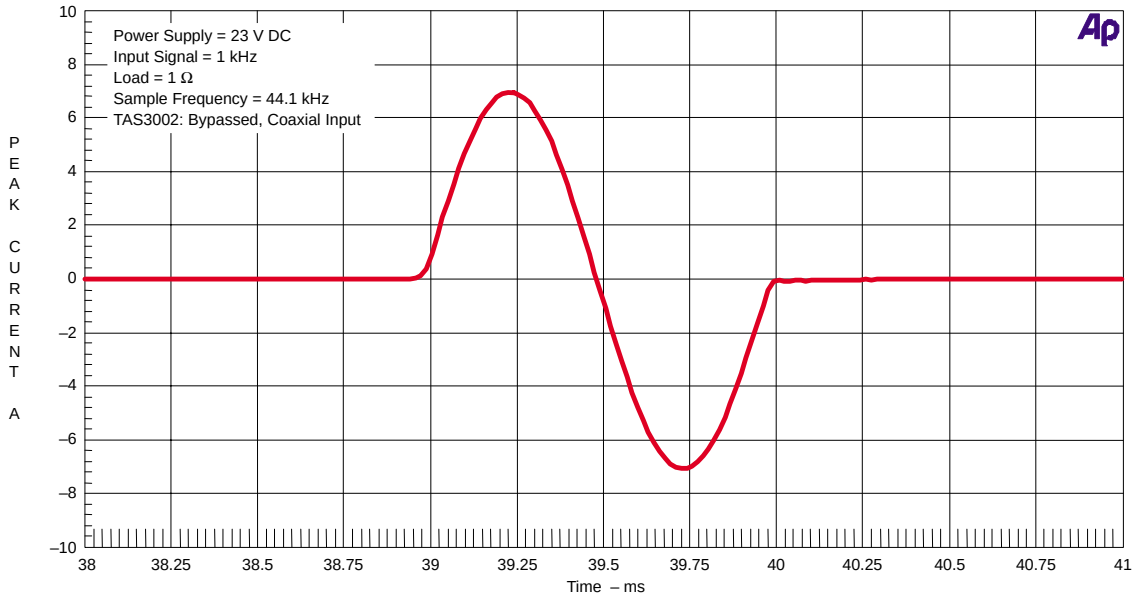


Figure 5–18. Amplifier Efficiency vs Total Delivered Power

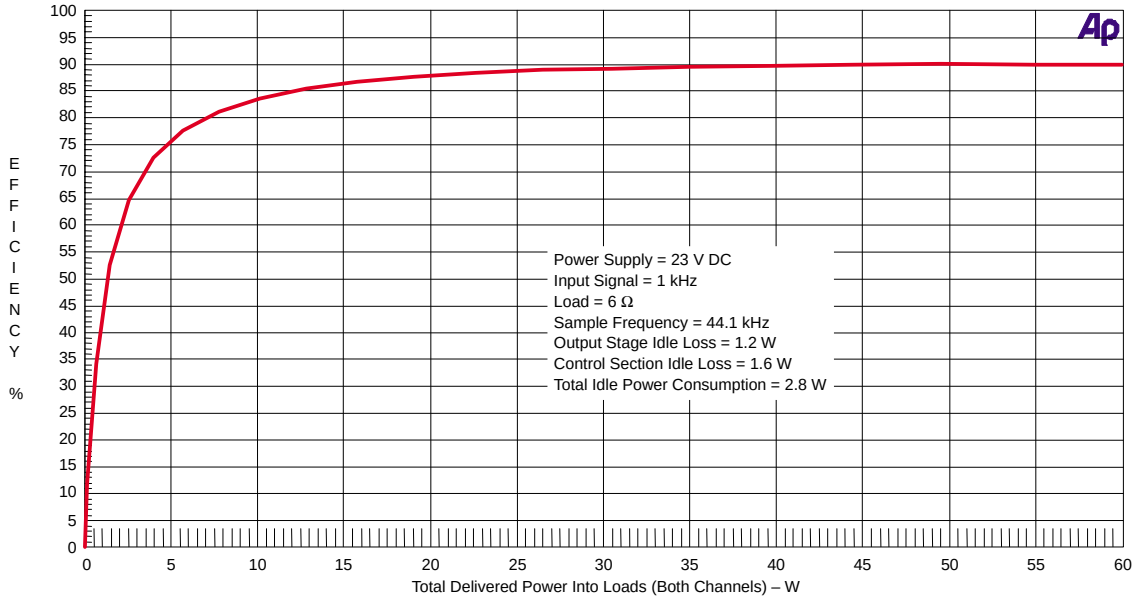


Figure 5–19. Power Losses in Amplifier vs Total Delivered Power