User's Guide

TRS3221 EVM User's Guide

ABSTRACT

This user's guide describes the evaluation module (EVM) for a RS232 transceiver TRS3221 with the RGT package. This EVM helps designers evaluate the device performance for fast development and analysis of data transmission.

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Trademarks

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1 Introduction

The TRS3221RGTEVM is an evaluation module for the TRS3221RGT and TRSF3221RGT devices, normal and high-speed RS-232 transceivers.

Features

- Interface with MCUs or processor from 3 V up to 5.5 V
- High-speed RS-232 communication, up to 1 Mbps
- Robust IEC 61000-4-2 qualification provides robust protection from electrostatic discharge events
- DB9 female connector for direct connection with a computer's RS-232 port
- Headers for easy connection to all power and logic signals

Applications

Any application that needs short range point-to-point full duplex data communications with hardware flow control.

- Remote Radio Unit (RRU)
- Base Band Unit (BBU)
- Electronic Point of Sale (EPOS)
- Diagnostics & Data Transmission Battery-Powered Equipment

Description

The TRS3221RGTEVM is an evaluation module for the TRS3221RGT and TRSF3221RGT devices, normal and high-speed RS-232 transceivers. The module enables device evaluation using the installed DB9 connector and headers. The board interfaces data and controls TTL logic levels on the headers to RS-232 levels supporting data [RX, TX] channels on the DB9 connector. The EVM has pull up resistors on the device's $\overline{\text{FORCEOFF}}$ and FORCEON pins and pull down resistor on the $\overline{\text{EN}}$ pin to keep both driver and receiver active. If desired, these signal can be driven by the external system to fully control all the features of auto-power down plus circuitry. The system may also benefit from monitoring the $\overline{\text{INVALID}}$ output to detect if an active connection has been made to the RS-232 port.

2 Test Setup

VCC is supplied with external power; 3.3 V or 5 V is recommended. The GND header pins are the ground connection for the TRS3221RGTEVM. The DB9 connector mates with a personal computer's RS-232 port or a USB to RS-232 adapter. For initial testing, external wires can be added. The ideal usage involves connecting the terminal block data and control lines to a system that has an UART (Universal asynchronous receiver/ transmitter) onboard.

2.1 Overview and Basic Operation Settings

Transceiver V_{CC} power supply (pin 16 of J2) and GND (pin 15 of J2): The basic setup of the TRS3221RGTEVM uses a single 3.3-V or 5-V power supply to evaluate the transceiver's performance. To power the transceiver, connect the 3.3-V or 5-V Vcc supply to pin 16 of J2 and GND to pin 15 of J2. The power supplied should meet the required specification of VCC for the transceiver being tested.

The capacitors installed on the TRS3232RGTEVM were selected for V_{CC} = 3.3-V operation. It is required to change some of the onboard capacitors for 5-V testing (Table 2-1).

Table 2-1. Capacitor configuration

	C1	C2	C3	C4
3.3V	100nF	100nF	100nF	100nF
5.0V	47nF	330nF	330nF	330nF

(optional) Charge pump output (V+ and V-): TRS3221RGT has an internal charge pump circuit to generate RS-232 signaling (Ref 1). Before starting the communication, the charge pump operation can be checked by monitoring these two test points.

TIN input (pin 8 of J2): Connect the function generator to pin 8 of the J2 header on the board. Set the function generator to generate a square wave of a certain frequency, 50% duty cycle, the low voltage level to 0 V, and the high level to 5-V. This clock signal simulates the TTL data from MCU. Alternatively PRBS data from a signal generator can be transmitted. Please note the data rate is not recommended to be faster than the specification in the datasheet.

DOUT output (pin 2 of J1): Connect an oscilloscope probe to pin 2 of J1 on the board. Setup the oscilloscope for proper time and voltage per division. Allow room to show three periods of bit-long waveform on the oscilloscope. The received RS-232 signal should match the transmitted logic data. This indicates that the driver of TRS3221RGT is operating correctly.

(optional) Loopback: Connect pin 3 of J1 to pin 2 of J1. By shorting these two pins, the transmitted RS-232 signal is looped back to the receiver of TRS3232RGT. Connect an oscilloscope probe to pin 6 of J2 on the board. Setup the oscilloscope for proper time and voltage per division. Allow room to show three periods of bit-long waveform on the oscilloscope. The received TTL signal should match the loopback data. This indicates that the receiver of TRS3221RGT is operating correctly.

3 Schematic and Layout

The TRS3221RGTEVM has simple connections to all necessary pins of the TRS3221RGT transceiver device, and jumpers where necessary to provide flexibility for device. The TRS3221RGTEVM provides test points for all RS-232 (TX1, RX1) and logic (TX2, RX2) communication lines. Additionally test points of GND, VCC, and charge pump output voltage are available for probing and evaluation.

3.1 Schematic

The schematic is shown in Figure 3-1. The function of each jumper and test point is listed in Table 3-1.

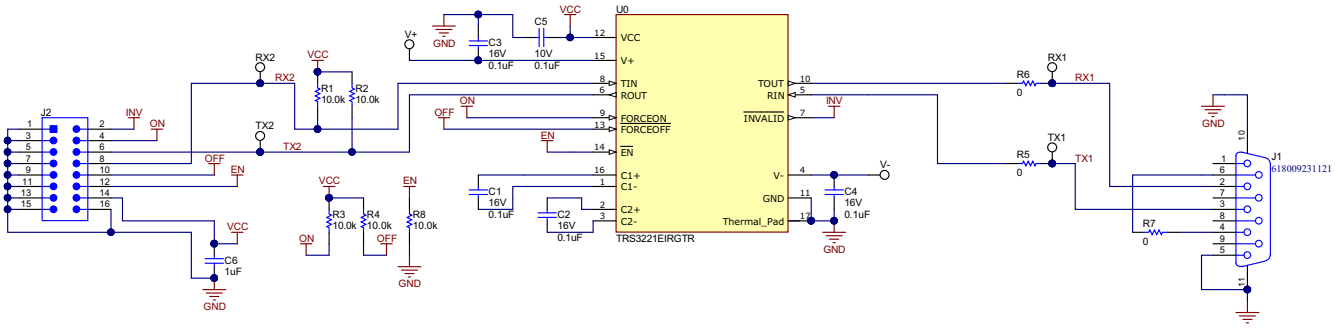

Figure 3-1. TRS3221RGTEVM Schematic

Table 3-1. Jumpers and Test Points

Connection	Type	Description
J1	9-pin connector	Female DB9 connector to connect to PC
J2	16-pin jumper	Used for supply and TTL signal
V+	Test point	Charge pump positive output
V-	Test point	Charge pump negative output

Power and logic signal go through the J1 connector. Table 3-2 lists each pin's connection.

Table 3-2. J1 pin connection

Connection	Type	Description
1	NC	Not connected
2	Output	RX1, pin 10 of transceiver
3	Input	TX1, pin 5 of transceiver
4	Loopback	Connected to pin 6
5	GND	Ground
6	Loopback	Connected to pin 4
7	NC	Not connected
8	NC	Not connected
9	NC	Not connected

The female DB9 port (Figure 3-2) provides access to the TRS3221RGT device through a standard RS-232 pinout. The TRS3221RGT female port is DCE to mate with a computer male DTE port. The pin names are counterintuitive on the DCE side. For example, the RX pin on EVM is connected to a driver and TX connects to a receiver. The reason pins 4 and 6 are shorted together by a 0 Ω resistor is to loopback the unused handshaking lines.

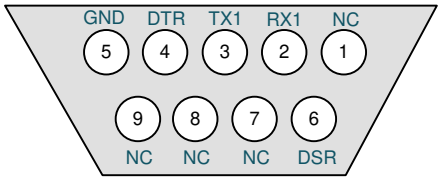

Figure 3-2. Female DB9 Connector Pinout

The pin connection of 16-pin jumper connector is listed in Table 3-3, which provides access to the TRS3221 device communication pins as well as control, output, and power pins. Pin 2 connects to the $\overline{\text{INVALID}}$ pin, which has the function described by the Table 3-4. Pin 10 connects to the $\overline{\text{FORCEOFF}}$ pin, and Pin 4 connects to the FORCEON pin. Please see the Table 3-5 and the Table 3-6 for pin functions.

Table 3-3. J2 jumper pin connection

Connection	Type	Description
1	GND	Ground
2	Output	INV, pin 7 of transceiver
3	GND	Ground
4	Input	ON, pin 9 of transceiver
5	GND	Ground
6	Output	TX2, pin 6 of transceiver
7	GND	Ground
8	Input	RX2, pin 8 of transceiver
9	GND	Ground
10	Input	OFF, pin 13 of transceiver
11	GND	Ground
12	Input	EN, pin 14 of transceiver
13	GND	Ground
14	Power	Vcc
15	GND	Ground
16	GND	Ground

Table 3-4. $\overline{\text{INVALID}}$Pin Function

INPUTS(1)				OUTPUT
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{EN}}$	$\overline{\text{INVALID}}$
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 3-5. Driver Function Table

INPUTS(1)				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with automatic power down enabled
H	L	H	Yes	L	

Table 3-5. Driver Function Table (continued)

INPUTS(1)				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
L	L	H	No	Z	Powered off by automatic power-down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, Yes = |RIN| > 2.7 V, No = |RIN| < 0.3 V

Table 3-6. Receiver Function Table

INPUTS(1)			OUTPUT	RECEIVER STATUS
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	ROUT	
X	H	X	Z	Output off
L	L	X	H	Normal operation
H	L	X	L	
Open	L	No	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

3.2 Layout

TRS3221RGTEVM board layout is shown in Figure 3-3.

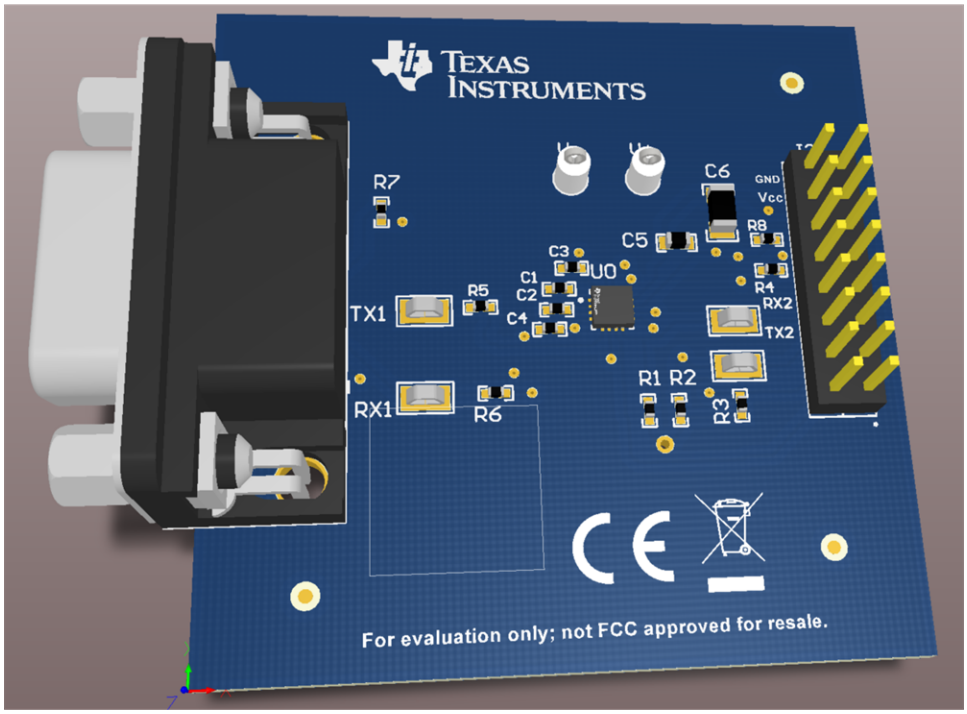

Figure 3-3. TRS3221RGTEVM layout

3.3 Bill of Materials

Table 3-7. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C2, C3, C4	4	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
C5	1	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603	0603	C0603C104K8RACTU	Kemet
C6	1	1uF	CAP, CERM, 1 uF, 10 V, +/- 10%, X7R, 0603	0603	GRM188R71A105KA61D	MuRata
RX1, RX2, TX1, TX2	4		Test Point, Miniature, SMT	Testpoint_Keystone_Miniature	0515	Keystone
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1	1		Receptacle, D-Sub, 9 Position, R/A, TH	Receptacle, D-Sub, 9 Position, R/A, TH	1734354-1	TE Connectivity
J2	1		Header, 100mil, 8x2, Gold, TH	PBC08DAAN	PBC08DAAN	Sullins Connector Solutions
R1, R2, R3, R4, R8	5	10.0k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R5, R6, R7	3	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
U0	1		RS-232 Transceiver Portfolio Refresh, RGT0016C (VQFN-16)	RGT0016C	TRS3221RGT	Texas Instruments
V+, V-	2		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone

4 Related Documentation

How the RS-232 transceiver’s regulated charge-pump circuitry works

https://e2e.ti.com/blogs_/b/analogwire/archive/2018/06/28/how-the-rs-232-transceiver-s-regulated-charge-pump-circuitry-works

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial Release

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265