User's Guide

BOOSTXL-IOLINKM-8 EVM User's Guide

ABSTRACT

This BoosterPack™ was designed to operate with the LP-AM243 TI LaunchPad™ kit with Sitara™ AM243x MCU. Together this design implements an eight port IO-Link Master with fast and deterministic timing and independent cycle and bit rate configuration. This design can be used to build a remote IO gateway to connect to OPC UA, Profinet, EtherCAT, or Ethernet IP. The Programmable Real-Time Unit (PRU) for Sitara ™ Processors based frame handler provides a flexible way of controlling timing and synchronization.

Table of Contents

Trademarks

Get Started

1. Order the BOOSTXL-IOLINKM-8 BoosterPack™ and the LP-AM243 LaunchPad™
2. Download and read the comprehensive reference design files and User's Manuals
3. Download the latest firmware libraries and follow the LaunchPad™programming instructions
4. Assemble the BoosterPack™ and LaunchPad™

Features

- Eight IO-Link ports
- Supports IO-Link transmission rates COM1, COM2, and COM3
- Supports 400-µs cycle time
- Can provide 500-mA of current per port
- Overcurrent protection and limiting on all ports
- PRU frame handler enables flexible timing

Applications

- Stand-Alone Remote IO
- Communication Module

1 Evaluation Module Overview

1.1 Introduction

This BoosterPack contains all of the analog circuitry needed to create an eight-port IO-Link Master when combined with the LP-AM243 LaunchPad containing the processor and framehandler. Each identical port contains a M12 connector with an IO-Link communication line (CQ), a 24-V power supply (L+) with a power supply return or ground (L-), and a digital input line (DI).

Each port uses an IO-Link TIOL112 transceiver configured for master-mode, which implements the physical layer interface for an IO-Link Master interface, including the required integrated current sink on the CQ line. The TIOL112 offers a current limit of 700mA during the wake-up pulse, which exceeds the minimum 500-mA requirement, but not enough to overload the cables or power supplies and generate fault conditions. The TIOL112 also limits the slew rate of the CQ line to minimize overshoots, reduce emissions and improve communication while still achieving COM3 performance with 230 kbps data rates.

The eight 24-V power supply channels are implemented with two TPS274160 quad-channel high side switches offering individual current monitoring and a configurable current limit to protect against overloaded outputs and fault conditions.

An eight-channel, 24-V, SN65HVS883 digital input serializer is used to monitor the Digital Input (DI) pins of each port when read by the processor as well as drive blue Status LEDs to reflect the line values.

General port status is provided by the processor through red and green status LEDs on each port controlled by a TCA6424A I2C-to-GPIO Expander.

The BoosterPack is protected from over-voltage, under-voltage, over-current, reverse polarity and other fault conditions on the primary 24-V power supply through the TPS26631 eFuse. The supply current is also monitored for diagnostic use by the processor.

A 3.3-V digital voltage rail is created from the 24-V supply with an LMR36503 DC/DC buck converter allowing the entire BoosterPack board to be powered from the single 24-V power supply. However, the 3.3-V supply from the LaunchPad could be used instead with a simple jumper configuration.

1.2 Kit Contents

- EVM Board (Qty 1)
- M12 Connector Stiffener Plate (Qty 1)
- M2.5x0.45 Pan Head Machine Screw (Qty 5)

1.3 Specification

1. Texas Instruments, IO-Link Master Demo
2. Texas Instruments, TIOL112 and TIOL112x IO-Link Device Transceivers with Low Residual Voltage andIntegrated Surge Protection in Small Packages data sheet
3. Texas Instruments, AM243x Sitara™ Microcontrollers data sheet
4. IO-Link Interface and System Specification V1.1.3
5. IO-Link Test Specification V1.1.3

1.4 Device Information

1.4.1 TIOL112

The TIOL112(x) family of transceivers implements the IO-Link interface for industrial bidirectional, point-to-point communication. When the device is connected to an IO-Link master through a three-wire interface, the master initiates communication and exchange data with the remote node while the TIOL112(x) acts as a complete physical layer for the communication. These devices are capable of withstanding up to 1.2 kV (500 Ω) of IEC 61000-4-5 surge and feature integrated reverse polarity protection. A simple pin programmable interface allows easy interfacing with the controller circuits. The output current limit can be configured using an external resistor. TIOL112(x) can be configured to generate wake-up pulse and be used in IO-link master applications. Fault reporting and internal protection functions are provided for undervoltage, overcurrent and overtemperature conditions.

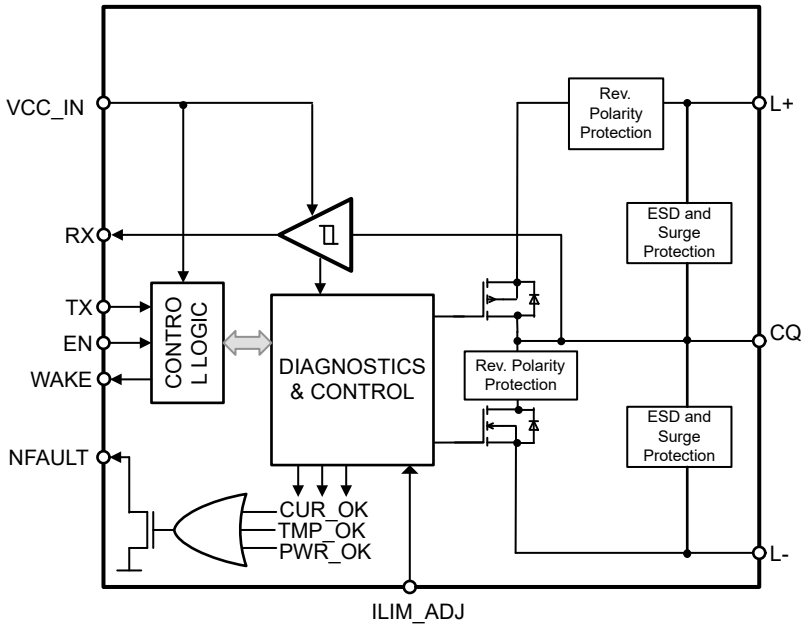


Figure 1-1. TIOL112 Functional Block Diagram

1.4.2 TPS26631

The TPS2663x devices are easy to use, positive 60 V and 6-A eFuse with a 31-mΩ integrated FET. It features a B-FET driver to control an external N-channel FET in the system designs that require protection from input reverse polarity faults and reverse current blocking. The device incorporates robust protection features that simplify system designs requiring protection during system tests like IEC61000-4-5 industrial surge tests. The device features an adjustable output power limiting (PLIM) functionality that simplifies the system design requiring compliance in accordance to the standards like IEC61010-1 and UL1310. Additional protection features include adjustable overcurrent protection, fast short circuit protection, output slew rate control, overvoltage protection and undervoltage lockout. For system status monitoring and downstream load control, the device provides fault and a precise current monitor output. PGOOD can be used for enable and disable control of the downstream DCDC converters. The MODE pin allows flexibility to configure the device between the two current-limiting fault responses (latch off and auto-retry).

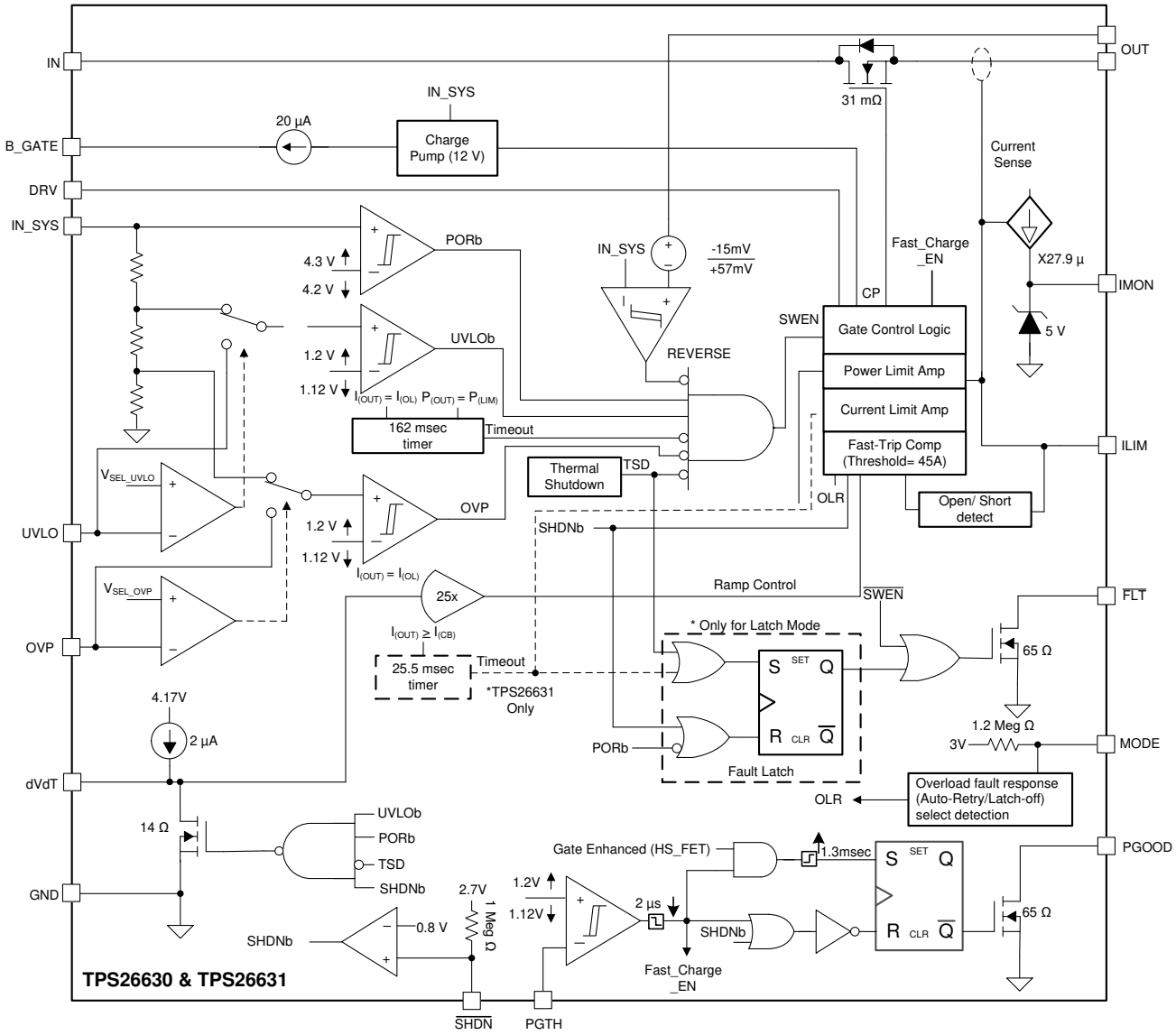


Figure 1-2. TPS26631 Functional Block Diagram

1.4.3 LMR36503

The LMR36503 is the industry smallest 65 V, 0.3 A synchronous step-down DC/DC converter in 2- mm × 2-mm HotRod™ package. This easy-to-use converter can handle input voltage transients up to 70 V, provide excellent EMI performance and support fixed 5 V and other adjustable output voltages. The transient tolerance reduces the necessary design effort to protect against input overvoltage and meets the surge immunity requirements of IEC 61000-4-5. The LMR36503 uses the peak current mode control architecture with internal compensation to maintain stable operation with minimal output capacitance. The LMR36503 with the right resistor selection from the RT pin to ground can be externally programmed to any desired switching frequency of operation over a wide range from 200 kHz to 2.2 MHz. The precision EN/UVLO feature allows precise control of the device during the start-up and shutdown. The power-good flag, with built-in glitch filter and delayed release, offers a true indication of the system status, eliminating the requirement for an external supervisor. The compact size and feature set of LMR36503 simplifies implementation for a wide range of industrial applications.

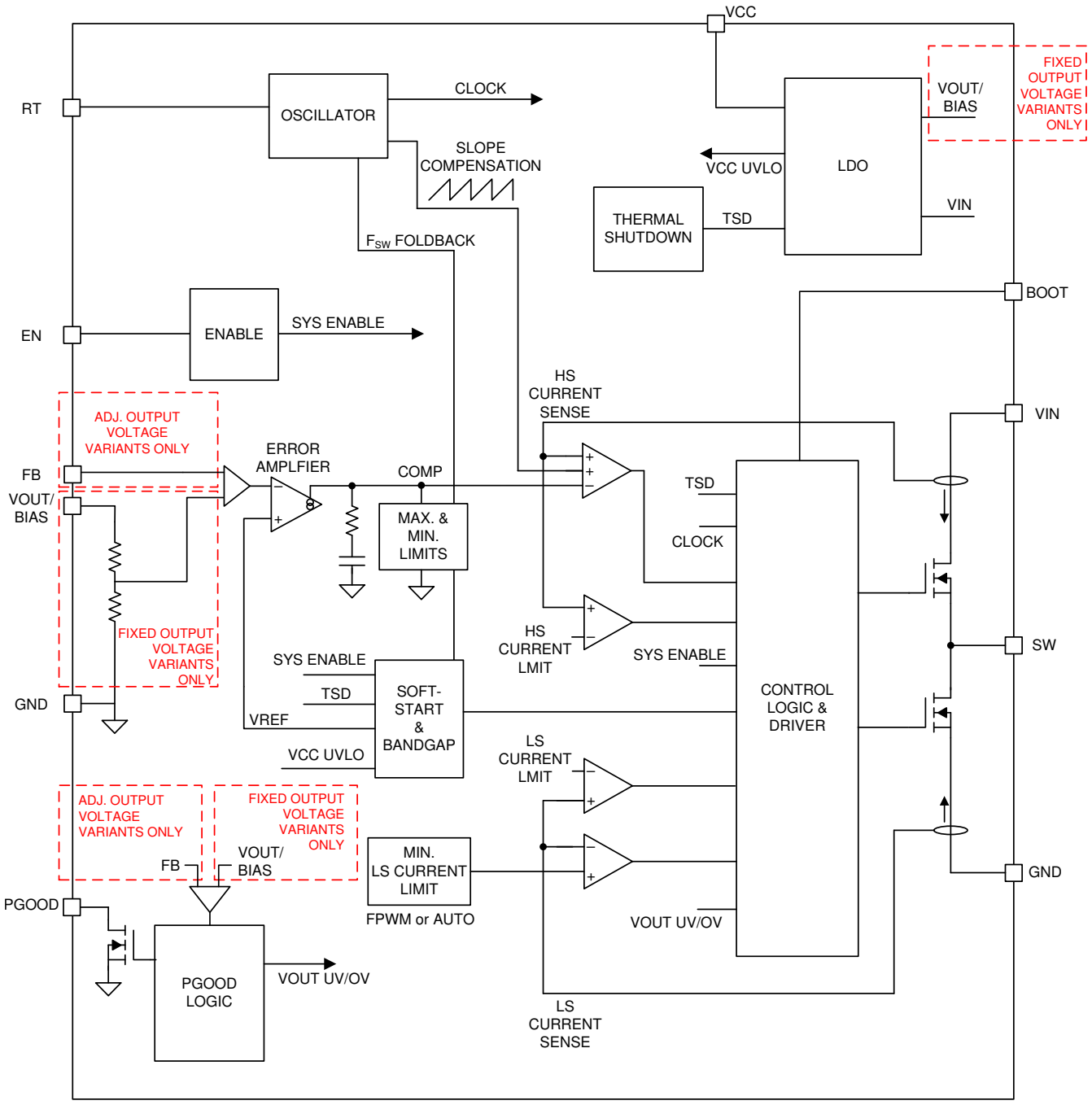


Figure 1-3. LMR36503 Functional Block Diagram

1.4.4 TLV9001

The TLV900x family includes single (TLV9001), dual (TLV9002), and quad-channel (TLV9004) low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective solution for space-constrained applications such as smoke detectors, wearable electronics, and small appliances where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV900x family is 500 pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the TLV600x devices. The robust design of the TLV900x family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

The TLV900x devices include a shutdown mode (TLV9001S, TLV9002S, and TLV9004S) that allow the amplifiers to switch off into standby mode with typical current consumption less than 1 µA. Micro-size packages, such as SOT-553 and WSON, are offered for all channel variants (single, dual, and quad), along with industry-standard packages such as SOIC, MSOP, SOT-23, and TSSOP packages.

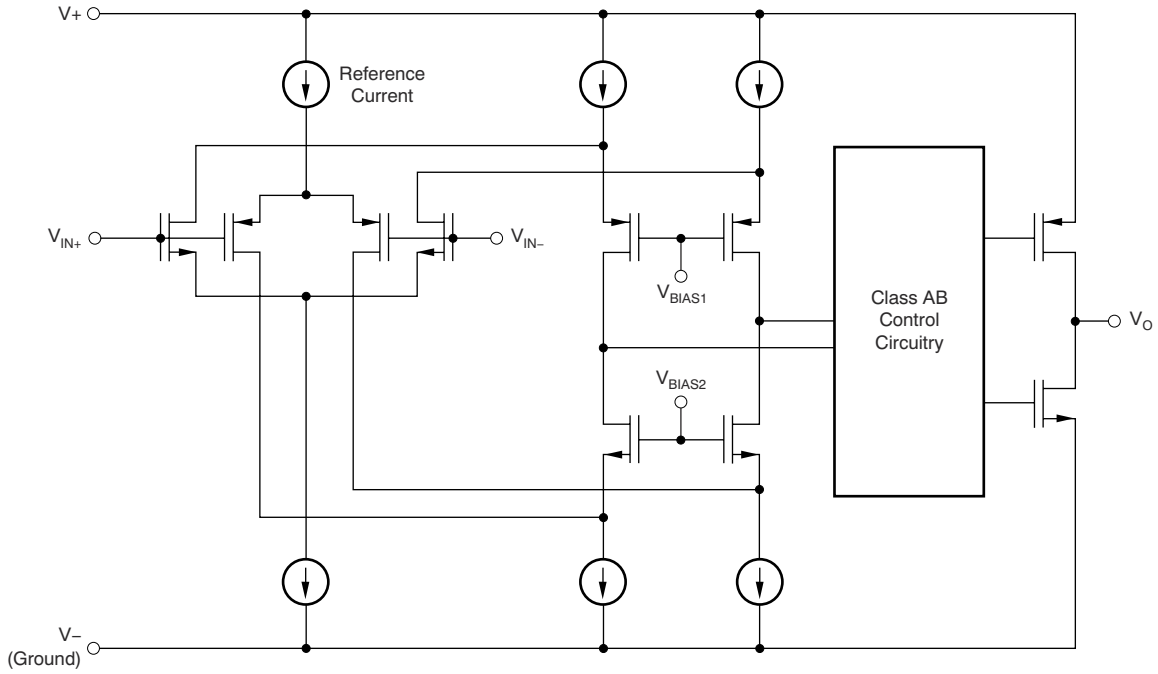


Figure 1-4. TLV9001 Functional Block Diagram

1.4.5 TCA6424A

This 24-bit I/O expander for the two-line bidirectional bus (I2C) is designed to provide general-purpose remote I/O expansion for most microcontroller families via the I2C interface [serial clock (SCL) and serial data (SDA)]. The major benefit of this device is its wide VCC range. It can operate from 1.65 V to 5.5 V on the P-port side and on the SDA/SCL side. This allows the TCA6424A to interface with next-generation microprocessors and microcontrollers on the SDA/SCL side, where supply levels are dropping down to conserve power. In contrast to the dropping power supplies of microprocessors and microcontrollers, some PCB components, such as LEDs, remain at a 5-V power supply.

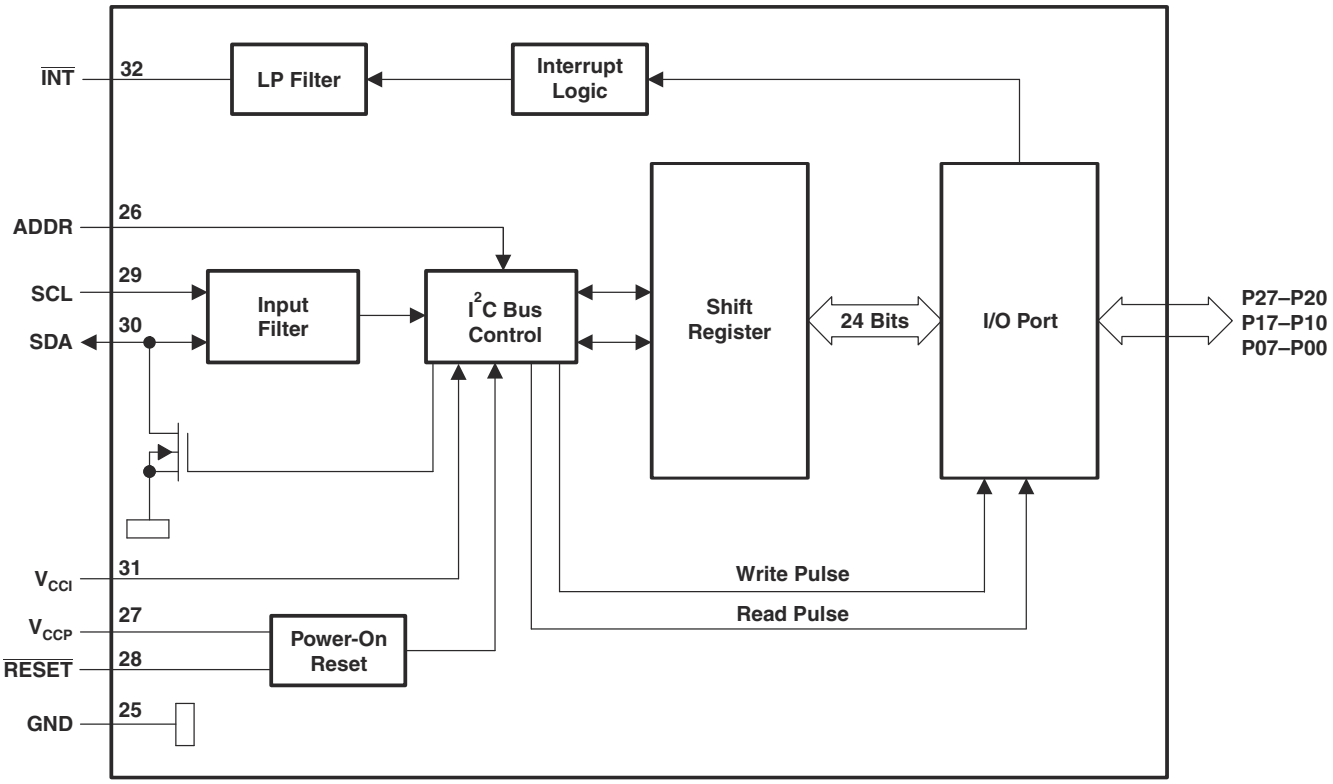


Figure 1-5. TCA6424A Functional Block Diagram

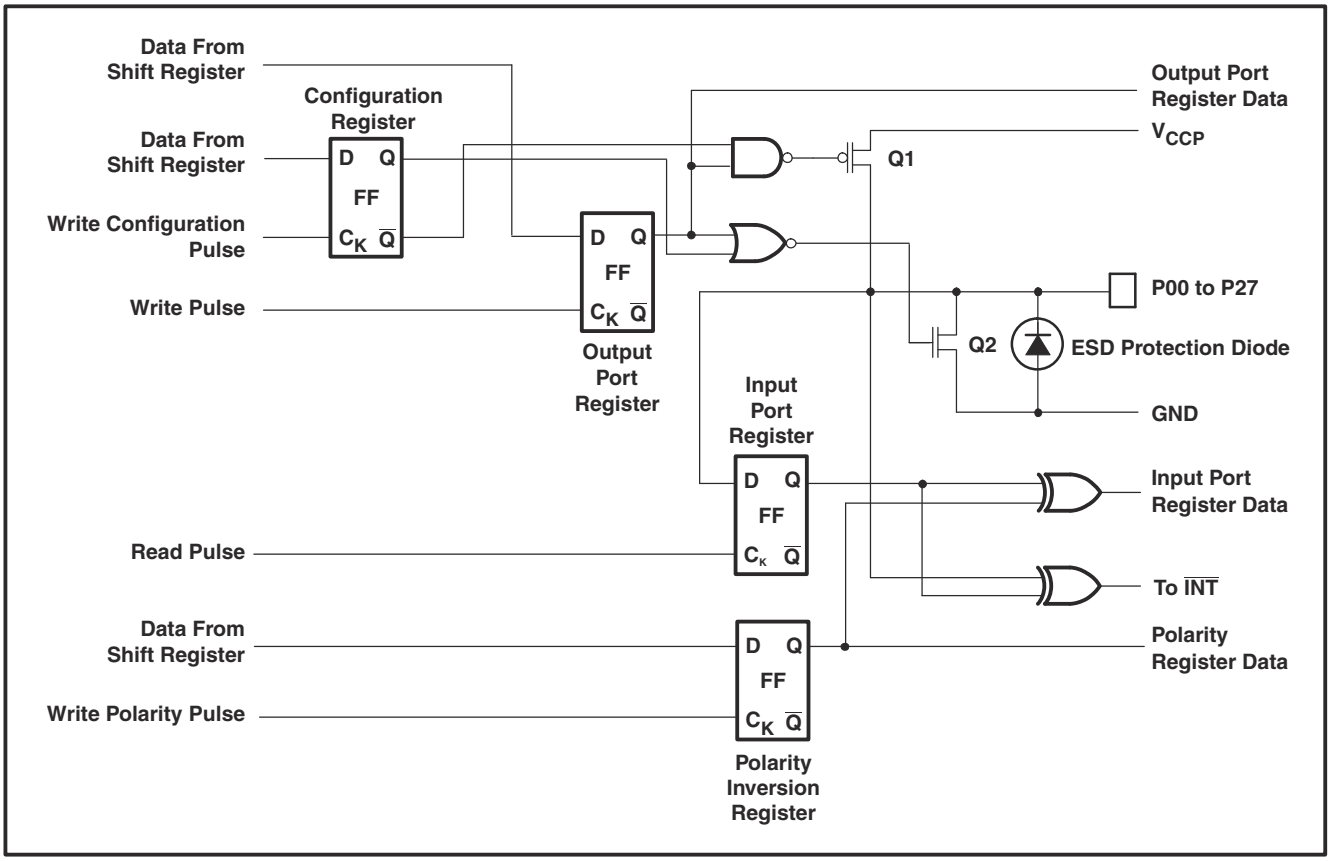


Figure 1-6. TCA6424A Simplified Schematic of P00 to P27

1.4.6 TPS274160

The TPS274160 device is a smart high-side switch with four integrated 160-mΩ NMOS power FETs and a charge pump to drive the gates. The device offers robust protection and diagnostic features to drive various loads (inductive, capacitive, and resistive) such as low wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules. The part enables flexible, multi-channel output configurations through paralleling channels and is in a very small WQFN package to enable usage in space constrained applications. The device is protected against short circuit events and over-temperature events, safely shutting off the output during fault events. The device also implements an external adjustable current limiting feature. This feature improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current thereby eliminating system supply brown out condition. The device also integrates diagnostic features like output current monitoring (version B) and open load detection to enable improved intelligence in modules and to enable predictive maintenance functionality.

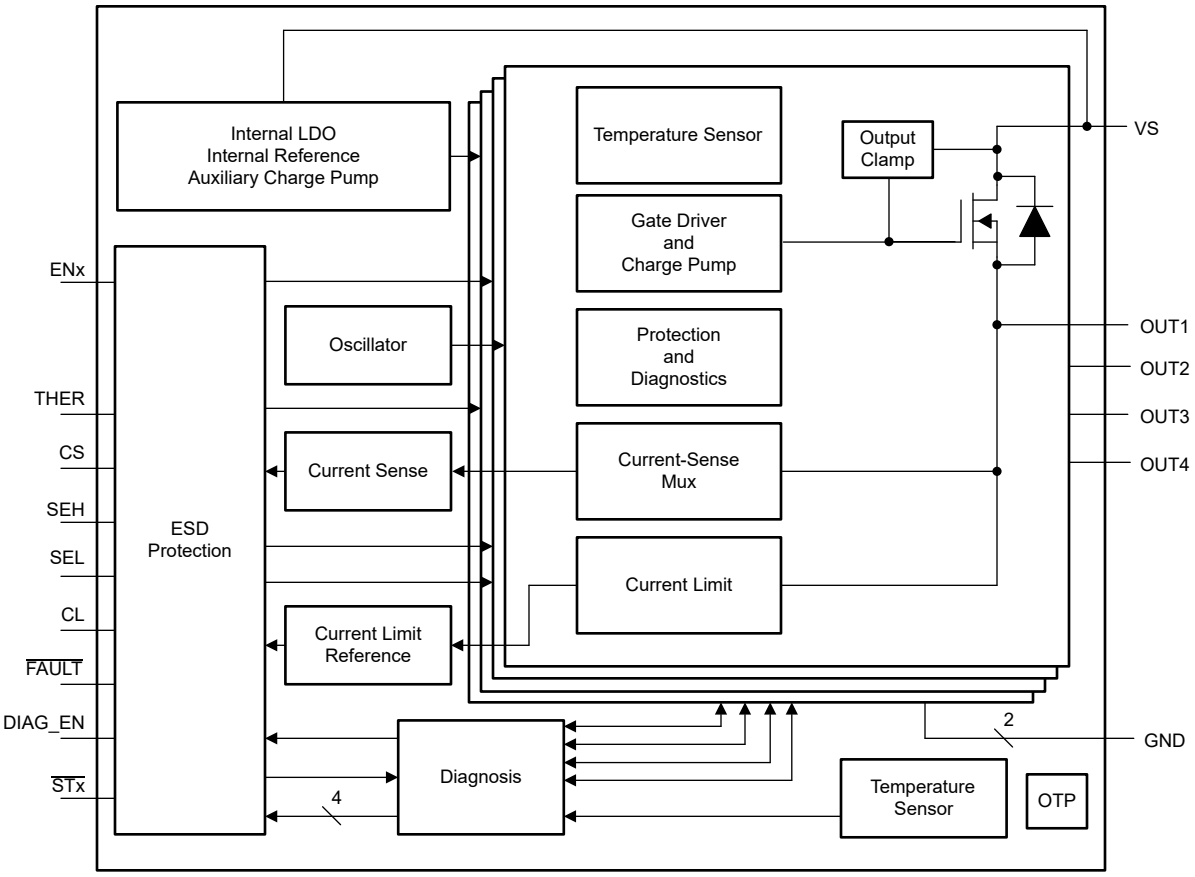


Figure 1-7. TPS274160 Functional Block Diagram

1.4.7 SN65HVS883

The SN65HVS883 is a 24-V, eight-channel, digital input serializer for high-channel density digital input modules of PC and PLC-based systems in industrial automation. In combination with galvanic isolators, the device completes the interface between the 24-V sensor outputs of the field-side and the low-voltage controller inputs at the control-side. Input signals provided by EN60947-5-2 compliant 2-wire and 3-wire proximity switches are current-limited and then validated by internal debounce filters. The input switching characteristic is in accordance with IEC61131-2 for Type 1, 2, and 3 sensor switches.

Upon the application of load and clock signals, input data is latched in parallel into the shift register and afterwards clocked out serially via a subsequent isolator into a serial PLC input.

Cascading of multiple SN65HVS883 is possible by connecting the serial output of the leading device with the serial input of the following device, enabling the design of high-channel count input modules. Input status is indicated via 3-mA constant current LED outputs. An external precision resistor is required to set the internal reference current. The integrated voltage regulator provides a 5-V output to supply low power isolators. An internal supply voltage monitor provides a chip-okay (CHOK) indication.

The SN65HVS883 comes in a 28-pin PWP PowerPAD™ package allowing for efficient heat dissipation. The device is specified for operation at temperatures from –40°C to 85°C.

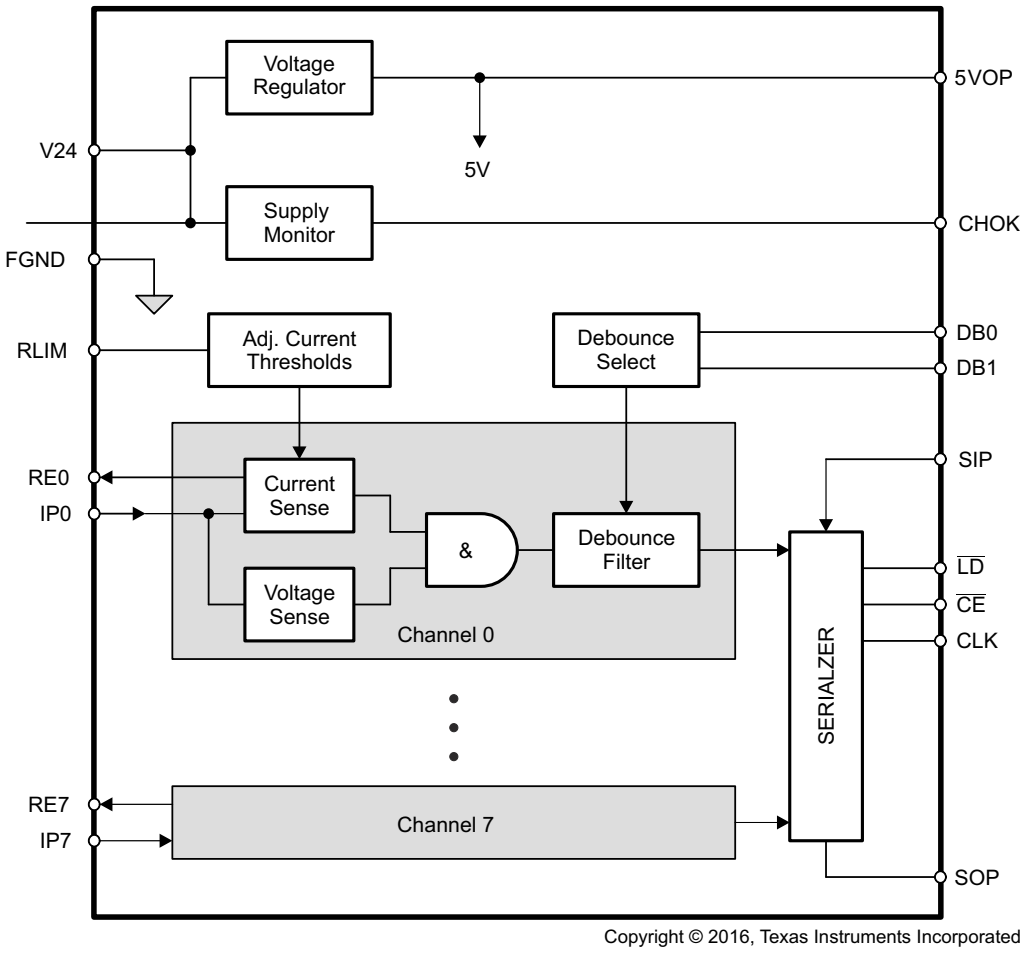


Figure 1-8. SN65HVS883 Functional Block Diagram

2 Hardware

2.1 Power Requirements

The IO-Link Master BoosterPack™ is powered from an 24-V supply connected to either the DC Power Jack (2.0 mm I.D x 6.5 mm O.D max) J6, or the 2-pin screw terminal block J7.

PARAMETER	SPECIFICATION
Input voltage	External 24-V power supply
Input current	Dependent on connected load (5 A recommended)
Output voltage	24 V
Output current per port	500 mA
Number of IO-Link master ports	8
Total output current	4 A

To avoid damaging the inputs of the LaunchPad, the BOOSTXL-IOLINKM-8 board should not be powered prior to the LaunchPad. The Shutdown (SHDN) pin of the TPS26631 eFuse device can be used disconnect the 24-V supply to the board when the LaunchPad board is not powered by using the LaunchPad 3V3 supply voltage to control the shutdown (SHDN) pin.

The BOOSTXL-IOLINKM-8 board can be used when disconnected from the LaunchPad board such as when doing certain physical layer testing with test equipment. In this configuration the Shutdown (SHDN) pin of the TP26631 eFuse should be connected to the external 24-V supply so that the board is powered when the 24-V supply is active.

The Digital IO voltage level of 3.3 V is used for the signals between the LaunchPad and BOOSTXL-IOLINKM-8 boards. The LMR36503 DC-DC stepdown buck converter can be used to create the 3V3 supply rail from the 24V rail controlled by the eFuse. However, it is possible to disable the LMR36503 and directly use the 3.3-V supply rail from the LaunchPad with a jumper configuration.

2.2 Power Configuration Headers

The board has three headers used in the power supply configuration shown in Figure 2-1, and the shunt jumpers should be applied before power is applied to the board.

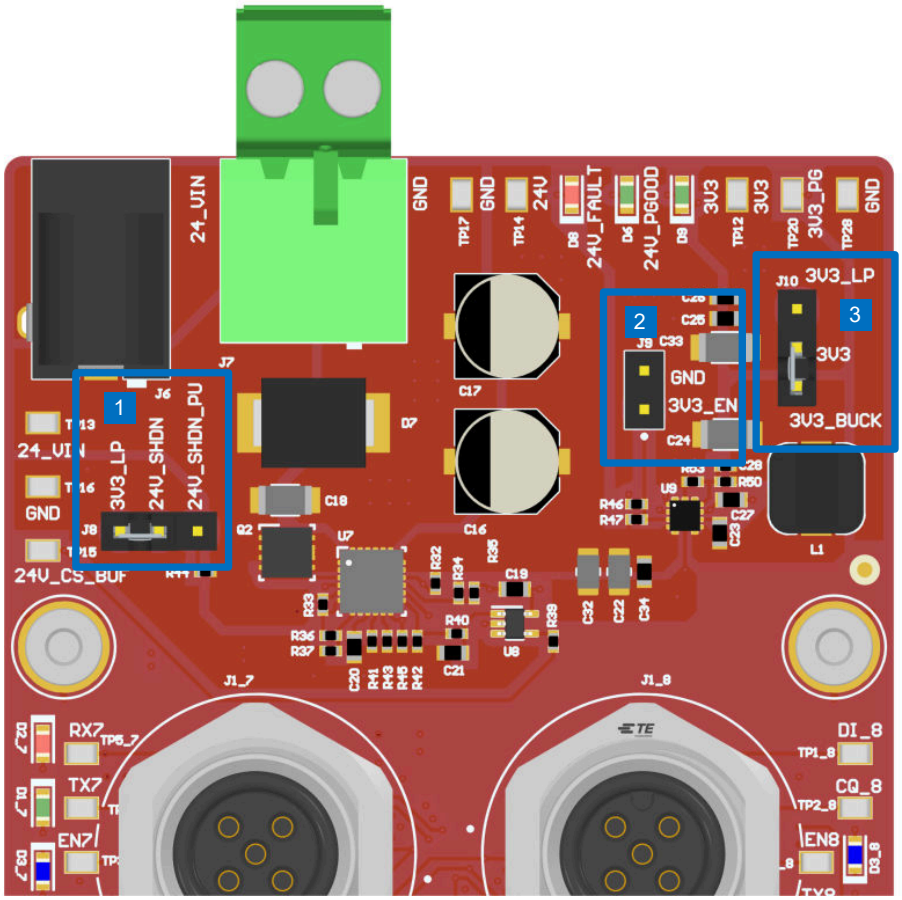


Figure 2-1. Power Configuration Headers

1. Header J8 is used to configure the TP26631 eFuse Shutdown (SHDN) pin configuration. Placing the shunt jumper between the pins labeled “3V3_LP” and “24V_SHDN” disables the 24 V supply rail when there is no voltage coming from the 3V3_LP (LaunchPad) supply rail. This is the default configuration and protects the LaunchPad MCU by disabling the BOOSTXL-IOLINKM-8 when the LaunchPad is not properly powered. Placing the shunt jumper between the pins labeled “24V_SHDN” and “24V_SHDN_PU” connects the TPS26631 Shutdown (SHDN) pin to the external 24-V supply voltage through a 100 kΩ pullup resistor. In this configuration, the BOOSTXL-IOLINKM-8 is powered whenever the external 24-V supply is active.
2. Header J9 is connected to the enable pin of the LMR36503 DC-DC stepdown buck converter. Placing a shunt jumper on this header disables the converter when the 3V3 rail is powered from the LaunchPad through the 3V3_LP rail or from an external 3.3-V supply.
3. Header J10 is used to configure which 3.3V source is used to supply the 3V3 rail. Placing a shunt jumper between the pins labeled “3V3_BUCK” and “3V3” connects the output of the LM36503 DC-DC step down buck converter to the board’s 3V3 supply rail. This is the default configuration. Placing a shunt jumper between the pins labeled “3V3” and 3V3_LP” connects the 3V3_LP supply rail coming from the LaunchPad to the board 3V3 supply rail.

2.3 BoosterPack Pinout Headers

The BOOSTXL-IOLINKM-8 BoosterPack requires both sets of BoosterPack XL connectors (J1/J3, J2/J4) and (J5/J7, J6/J8), and uses most of the signals available from the LaunchPad for the application. The eight standard IO-LINK Port 5-pin M12 connectors must be mounted in a manner that eliminates the ability to stack another BoosterPack board on top of the BOOSTXL-IOLINKM-8 board. As a result, the standard BoosterPack XL connectors, with both a socket portion on the bottom of the board and a pin portion on top of the board, have been replaced with a surface mount socket header type that allows the BoosterPack to mate with the LaunchPad, but removes the top side pins that conflict with the M12 connectors. The majority of these signals have also been brought out to test points located on the perimeter of the Boosterpack to maintain access to these signals during testing. Figure 2-2 shows the header pinout as viewed from the bottom side of the board.

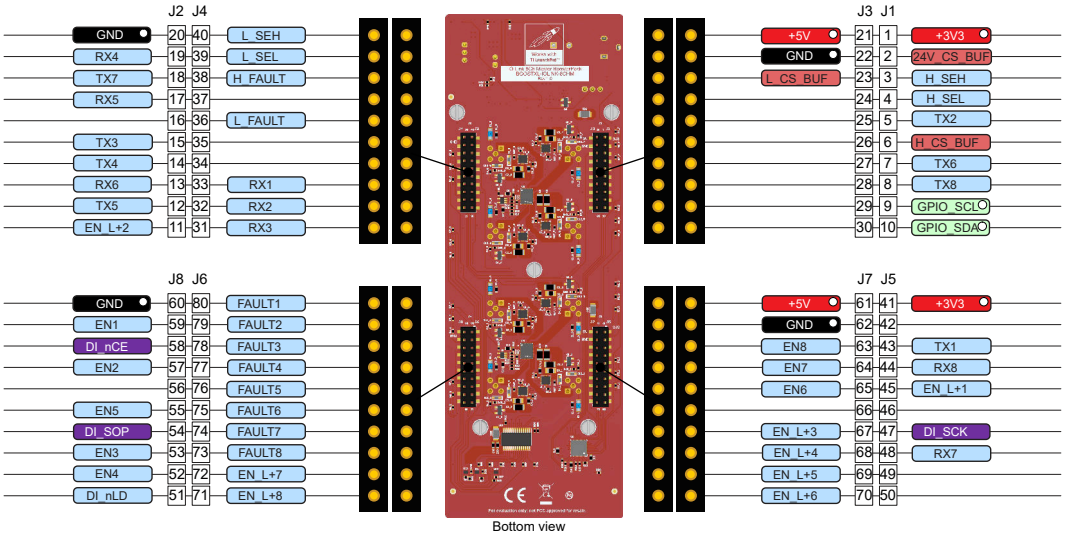


Figure 2-2. LaunchPad-BoosterPack Pinout

2.4 Push Buttons

The board has one push button shown in Figure 2-3. Due to the limited GPIO pins available between the LaunchPad and BOOSTXL-IOLINKM-8 boards through the board-to-board mating headers, additional GPIO pins were created using a TCA6424A I2C-to-GPIO Expander. The MCU firmware should configure these GPIO pins to the proper direction (Input or Output) as well as the High or Low state through communication on the I2C bus. Pressing this push button switch S1 labeled “GPIO_RST” reset the TCA6424A registers to their default values. It is not expected that the user needs to use this push button during normal operation.

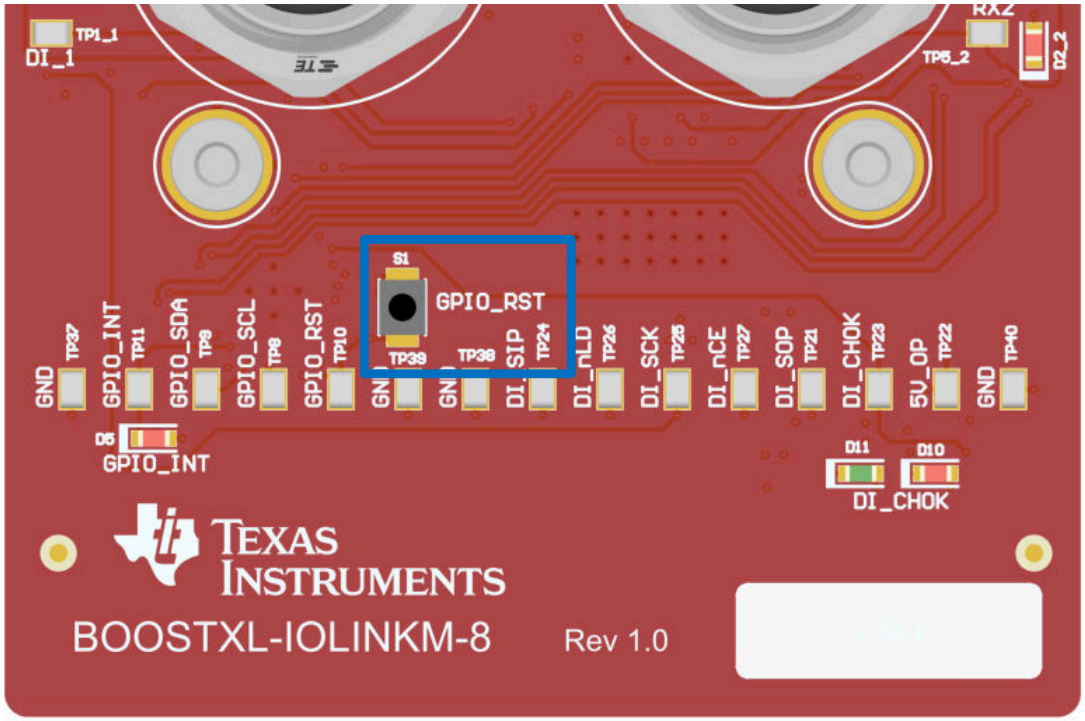


Figure 2-3. GPIO Reset Push Button

2.5 Test Points and Status LEDs

Most of the signals are brought out to test points or status LEDs located on the perimeter of the board. Care must be taken when working with the test points to avoid shorting two test points together when connecting test leads, scope probes, and so on. The recommendation is to make the test equipment connections to the test points before turning on the 24-V power supply.

The test points and status LEDs associated with the 24-V supply voltage are shown in Figure 2-4.

Reference Designator	Label	Description
TP13	24_VIN	External 24-V supply test point
TP16, TP17, TP14	GND	Ground test point
TP14	24 V	TP26631 eFuse protected 24-V supply for the 24 V supply rail
TP15	24V_CS_BUF	TP26631 eFuse current sense output voltage
D6	24V_PGOOD	TP26631 eFuse Power Good LED indicator for the 24 V supply rail
D8	24V_FAULT	TP26631 eFuse Fault LED Indicator for the 24 V supply rail

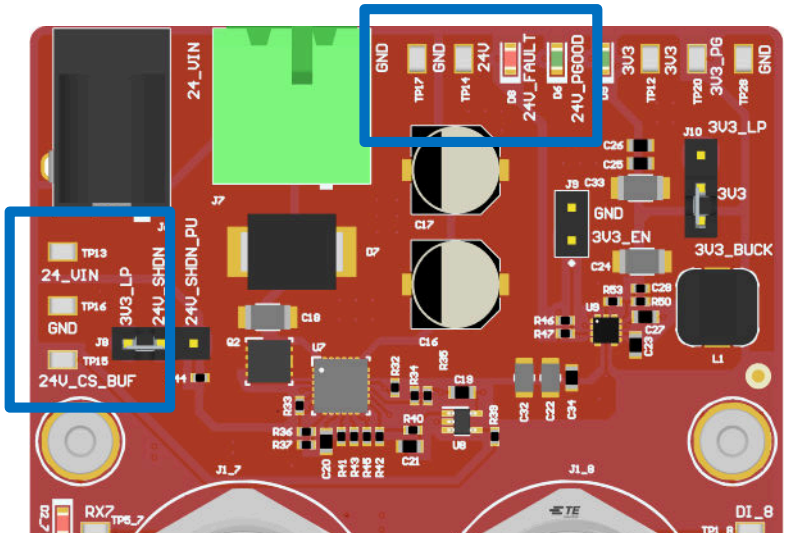


Figure 2-4. 24-V Test Points and LEDs

The test points and status LEDs associated with the 3.3-V and 5V_LP supply voltages are shown in Figure 2-5.

Reference Designator	Label	Description
TP12	3V3	Test point for the 3V3 supply rail
TP28, TP32	GND	Ground test point
TP20	3V3_PG	3V3_BUCK Power Good LED indicator for the 3V3 supply rail
D9	3V3	LED indicator for the 3V3 supply rail
TP31	5V_LP	Test point for the 5V_LP supply rail (not used on the board)

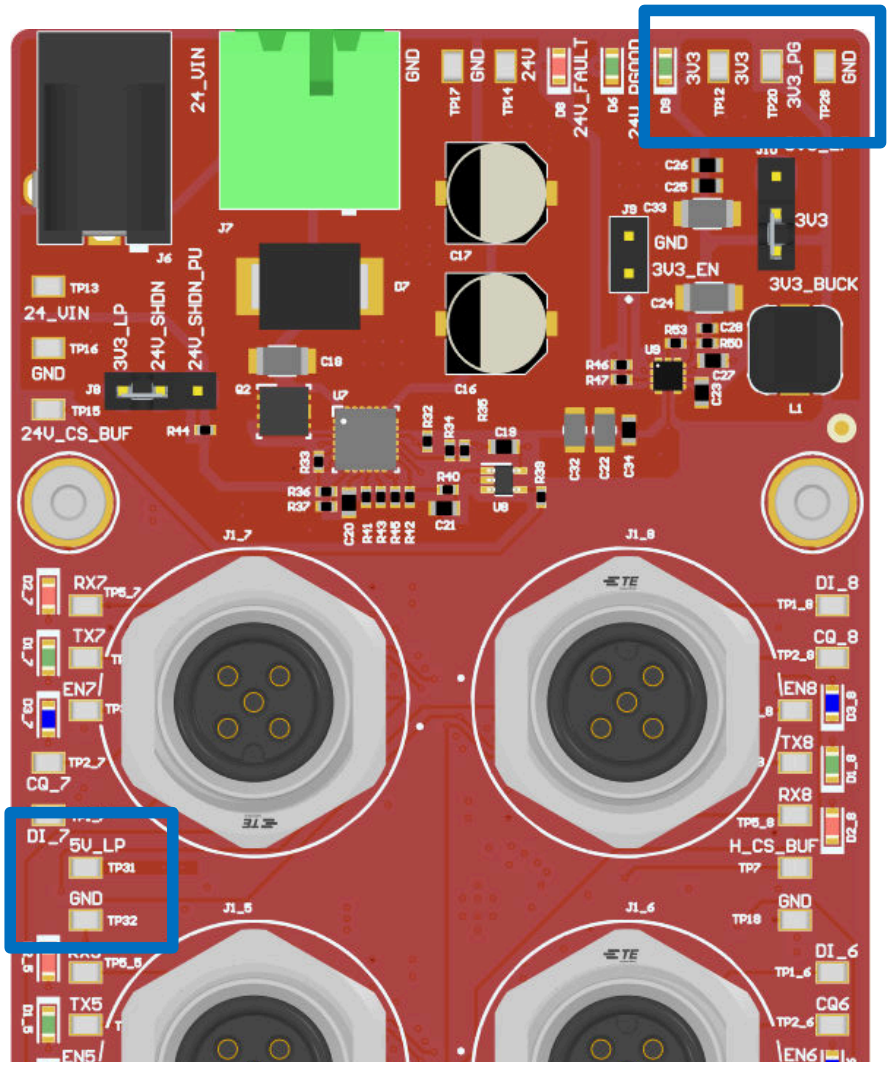


Figure 2-5. 3V3 and 5V_LP Test Points and LEDs

The M12 connector, test points and status LEDs associated with the IO-Link Ports are shown in Figure 2-6. Each port is identically routed and a detailed view for port 1 is shown in Figure 2-7. The reference designators for the components associated with the port have the same base reference designator followed by the port number. For example the reference designators for the eight M12 connectors are J1_[1:8].

Reference Designator	Label	Description
TP1_[1:8]	DI_[1:8]	Digital Input test point (24-V signal level)
TP2_[1:8]	CQ_[1:8]	TIOL112 CQ pin test point (24-V signal level)
TP3_[1:8]	EN[1:8]	TIOL112 Enable (EN) pin test point (3.3-V signal level)
TP4_[1:8]	TX_[1:8]	TIOL112 TX pin test point (3.3-V signal level)
TP5_[1:8]	RX_[1:8]	TIOL112 RX pin test point (3.3-V signal level)
D1_[1:8]	N/A (Green LED)	Port status Good LED Indicator
D2_[1:8]	N/A (Red LED)	Port status Fault LED Indicator
D3_[1:8]	N/A (Blue LED)	Digital Input LED Indicator

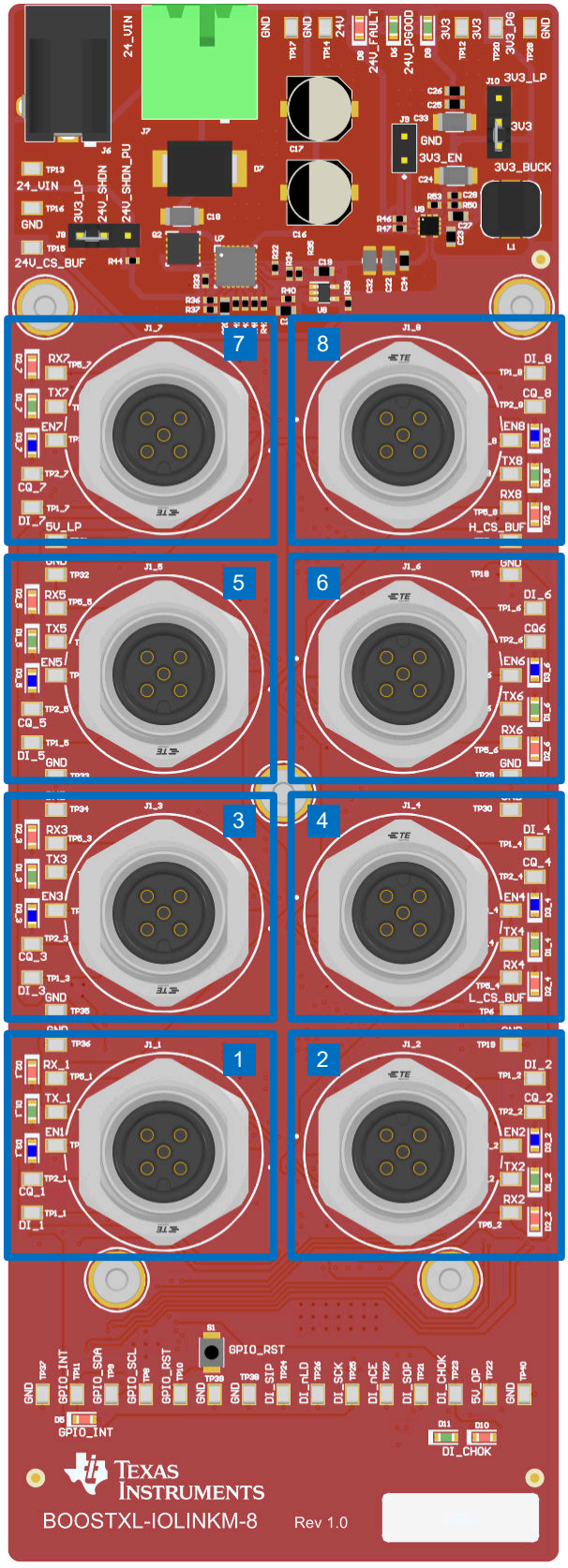


Figure 2-6. IO-Link Port M12 Connectors, Test Points, and LEDs

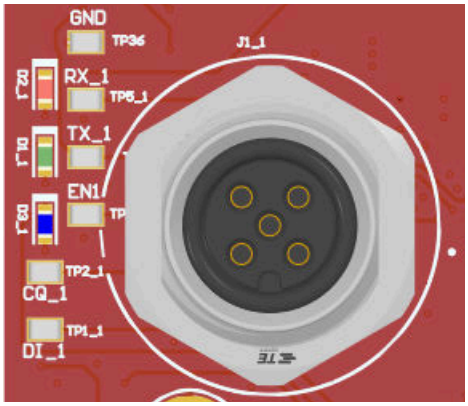


Figure 2-7. IO-Link Port 1 M12 Connector, Test Points, and LEDs

The test points and status LEDs associated with the TCA6424A I2C-to_GPIO Expander are shown in Figure 2-8.

Reference Designator	Label	Description
TP8	GPIO_SCL	TCA6424A I2C SCL signal test point (3.3-V signal level)
TP9	GPIO_SDA	TCA6424A I2C SDA signal test point (3.3-V signal level)
TP10	GPIO_RST	TCA6424A Reset pin test point (3.3-V signal level)
TP11	GPIO_INT	TCA6424A Interrupt pin test point (3.3-V signal level)
D5	GPIO_INT	TCA6424A Interrupt pin LED Indicator
TP37, TP39	GND	Ground test point

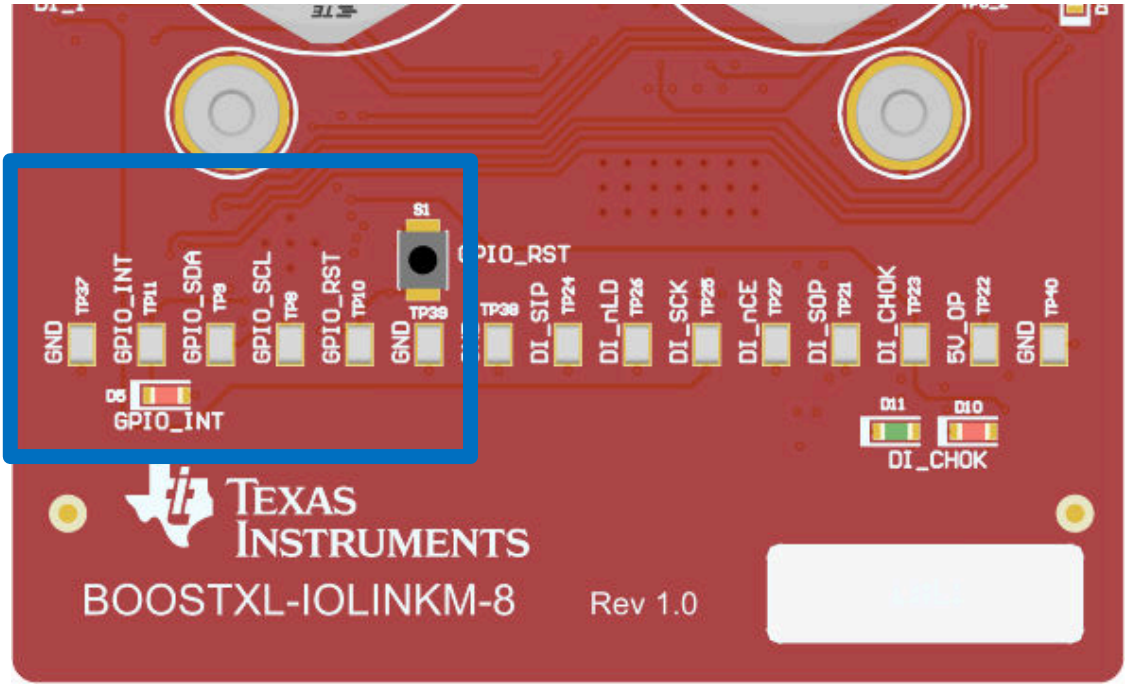


Figure 2-8. GPIO Test Points and Interrupt LED

The test points and status LEDs associated with the SN65HVS883 digital input serializer are shown in Figure 2-9.

Reference Designator	Label	Description
TP21	DI_SOP	SN65HVS883 serial data output (SOP) pin test point (3.3-V signal level)
TP24	DI_SIP	SN65HVS883 serial data input (SIP) pin test point (3.3-V signal level)
TP25	DI_SCK	SN65HVS883 serial clock input (CLK) pin test point (3.3-V signal level)
TP27	DI_nCE	SN65HVS883 clock enable input (nCE) pin test point (3.3-V signal level)
TP24	DI_nLD	SN65HVS883 load pulse input (nLD) pin test point (3.3-V signal level)
TP23	DI_CHOK	SN65HVS883 chip okay output (CHOK) pin test point (3.3-V signal level)
TP22	5V_OP	SN65HVS883 5 V output (5VOP) pin test point (5-V signal level)
TP38, TP40	GND	Ground test point
D10	DI_CHOK (Red LED)	SN65HVS883 chip okay output status Fault LED Indicator
D11	DI_CHOK (Green LED)	SN65HVS883 chip okay output status Good LED Indicator

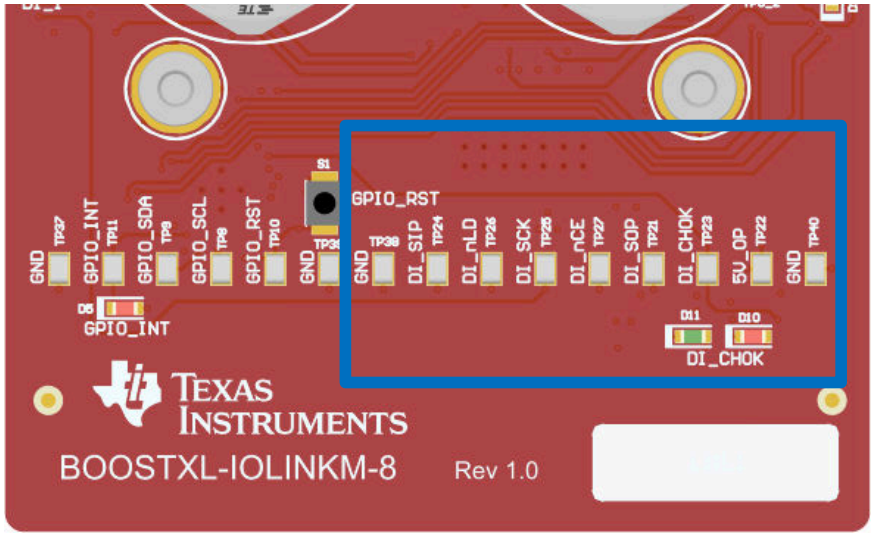


Figure 2-9. Digital Input Test Points and Status LEDs

The test points associated with the TP26631 eFuse and TPS274160 High Side Switches current sense outputs digital input serializer are shown in Figure 2-10.

Reference Designator	Label	Description
TP15	24V_CS_BUF	TP26631 eFuse current sense output voltage (3.3-V max signal level)
TP7	H_CS_BUF	TPS274160 High Side Switch current sense output voltage for L+[5:8] (3.3-V max signal level)
TP6	L_CS_BUF	TPS274160 High Side Switch current sense output voltage for L+[1:4] (3.3-V max signal level)
TP16, TP18, TP19		Ground test point

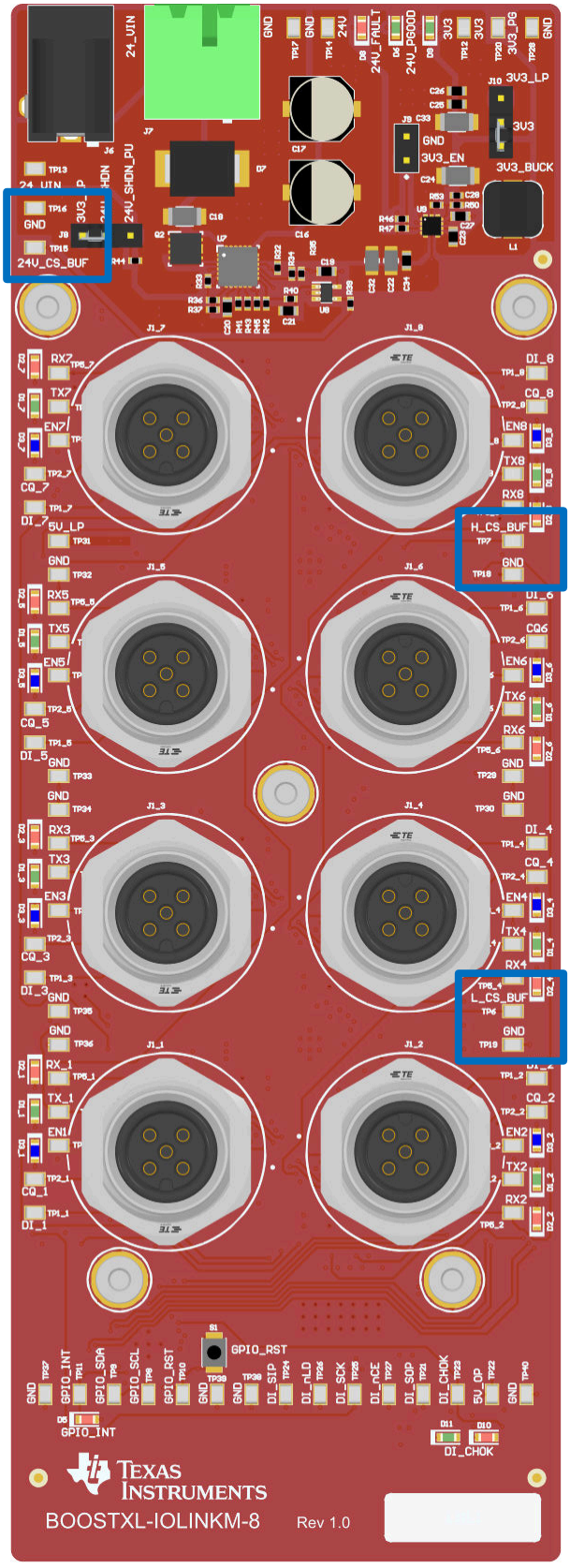


Figure 2-10. Current Sense Buffer Test Points

2.6 M12 Connector Mechanical Stiffener Plate

The M12 connectors are intended to be mechanically stabilized by mounting in a panel or enclosure. Because the BOOSTXL-IOLINKM-8 is provided without an enclosure, a second blank PCB is included to be used as a mechanical Stiffener Plate and relive the strain placed on the solder joints of the M12 connector from the weight of the cables. This plate is shown in Figure 2-11, and can be removed for better access to the primary board. However, when removed, extra care must be taken to prevent damaging the solder joints of the M12 connectors and board footprint.

Also note that the mounting standoffs are connected to the ground plane of the primary board bringing the ground up to the shield of the M12 connectors. This also provides additional ground connection locations for test equipment such as the ground reference lead of a scope probe or digital multimeter.

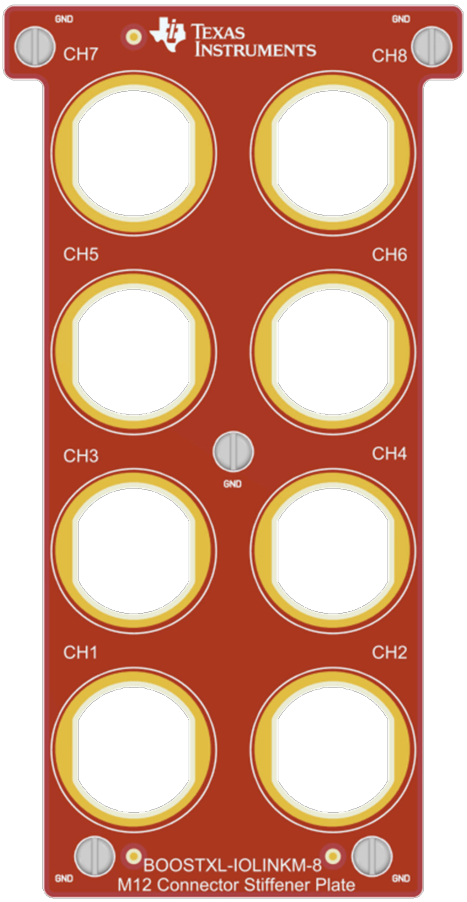


Figure 2-11. M12 Connector Mechanical Stiffener Plate

2.7 Assembly Instructions

Figure 2-12 shows the complete mechanical assembly of all three boards in the system. The M12 Connector mechanical stiffener plate is the top board in the assembly and is assembled on the primary BOOSTXL-IOLINKM-8 board. Then this BOOSTXL-IOLINKM-8 assembly is assembled onto the LaunchPad board represented by the LP-AM243 LaunchPad board in Figure 2-12.

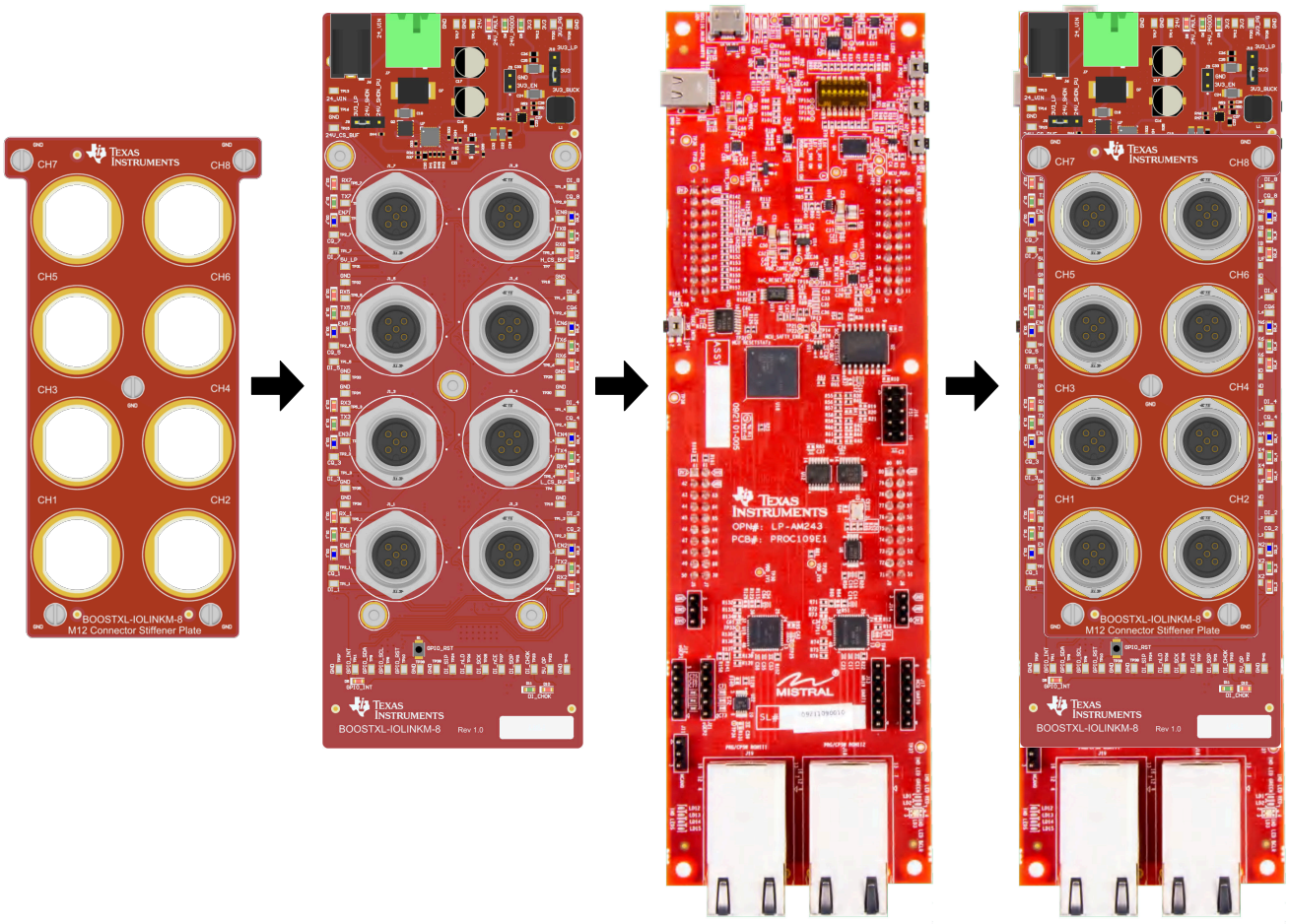


Figure 2-12. BoosterPack and LunchPad Mechanical Assembly

2.8 What to Do and What Not to Do

- Make sure all boards are firmly seated but not such that any other components between the LaunchPad and BoosterPack are touching and creating possible electrical shorts.
- Always make sure the LaunchPad is powered up properly prior before the BoosterPack is powered in order to avoid damaging the GPIO and ADC input pins on the LaunchPad. Placing the shunt jumper between the pins labeled “3V3_LP” and “24V_SHDN” on Header J8 will disable the 24V supply rail output of the TP26631 eFuse when there is no voltage coming from the 3V3_LP (LaunchPad) supply rail. This is the default configuration and should protect the LaunchPad MCU by disabling the BOOSTXL-IOLINKM-8 when the LaunchPad is not properly powered.
- Be aware that some of the signals on this board are of a 24-V level, and others are of a 3.3-V or 5-V level. Be careful when working with the board to avoid connecting or shorting two signals of different levels together which may result in damage to the board.

3 Software

3.1 Software Description

The BOOSTXL-IOLINKM-8 was primarily designed to operate with the LP-AM243 LaunchPad running the IO-Link ® Master Stack and example application. There are two different APIs to communicate with the IO-Link stack library, but only one API can be used in an application:

- SMI – The Standardized Master Interface (SMI) is a generic interface, which is set on top of the stack's regular API. It matches the interface with other IO-Link standards and acts as a connecting interface for multiple clients. Also included is the configuration management and event dispatching.
- API without SMI – Use this API if you want to directly access the lower level System Management and Application Layer services.

3.2 Software Installation

The Integration manual and example application documentation can be found at the following link: IO-Link ® Master stack

Note: Newer revisions may exist and can be found by editing the link to match the latest SDK revision value.

3.3 GUI Installation

The IO-Link Master GUI download link and documentation can be found at the SMI – Graphical User Interface section of the IO-Link Master Example Project quick start guide.

Newer revisions may exist and can be found by editing the link to match the latest SDK revision value.

3.4 Software Development

The AM243x software development kit (SDK) for Sitara ™ microcontrollers and the LP-AM243 LaunchPad can be found at the following link: AM243x software development kit (SDK) for Sitara ™ microcontrollers

4 Implementation Results

4.1 Test Setup

To test the different physical parameters, the IO-Link board, BOOSTXL-IOLINKM-8, is connected to a 24-V supply without the AM243x Launchpad. The necessary signals for each test are explained in the following sections. See the Eight Port IO-Link Master Reference Design Guide: TIDA-010234 for additional information.

4.2 Test Results

This section outlines the physical layer tests as described by the described by the IO-Link community in IO-Link Interface and System Specification publication. Figure 4-1 shows the structure of the test names.

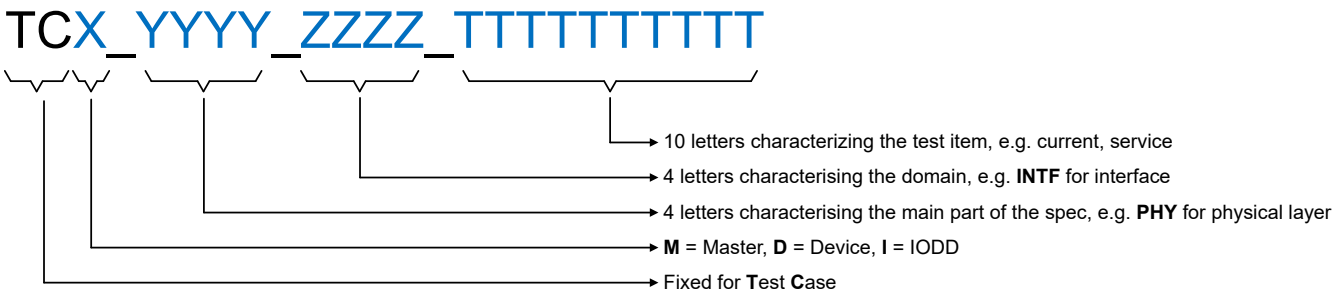


Figure 4-1. Test Names

4.2.1 Power-On Supply Current Capability of Master Port L+ (TCM_PHYL_INTF_ISIRM)

The IO-Link standard defines the current pulse capability for Devices as $ISIR_M$ = 400 mA (min) which is essentially the inrush current from charging the Device decoupling capacitance at power-on. For support, the Master provides a charge of at least 400 mA x 50 ms = 20 mAs after power-on without shutting down from an overload condition.

The test consists of observing the current and voltage between the L+ and L- supply during power-on when a current sink load of at least 1000 mA ($ISIR_M$) is connected. The resulting charge calculation must be greater than 20 mAs for both the PSM power supply min (20 V) and max (30 V) levels to pass.

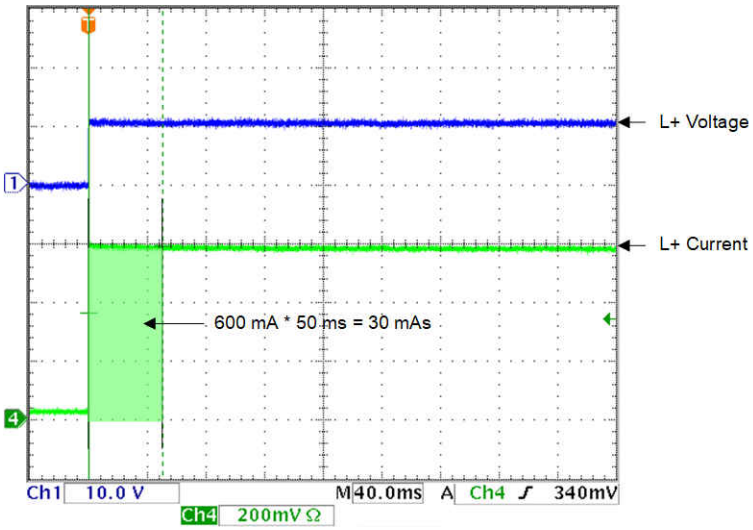


Figure 4-2. TCM_PHYL_INTF_ISIRM with 20 V

Figure 4-2 shows the behavior at a supply voltage of 20 V and a resistive load of about 18 Ω. The TPS274160 high-side switch used to control the L+ supply to the Device limits the current to 600 mA which limits the output voltage to 10 V. The test results in a charge provided by the Master of 30 mAs for the first 50 ms and a passing test result.

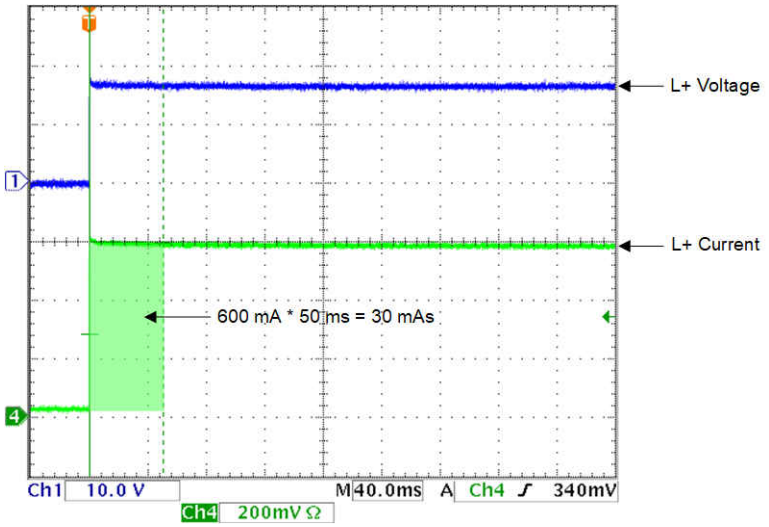


Figure 4-3. TCM_PHYL_INTF_ISIRM with 30 V

Figure 4-3 shows the same test with a supply voltage of PSM = 30 V and a resistive load of 28 Ω. Because the TPS274160 high-side switch still limits the current to 600 mA, the observed voltage increases to about 16 V, but the charge is still the same at 30 mAs resulting in a passing test result.

4.2.2 Interface Wake-Up Voltages (TCM_PHYL_INTF_IQWUH and TCM_PHYL_INTF_IQWUHL)

The IO-Link standard defines the wake-up request (WURQ) as a method to request a Device switch to the COMx mode. The Master induces a pulse of current for a period of time T_{WU} and then waits for a delay time T_{REN} needed by the Device to switch to the COMx mode before communicating with the Device. The direction of current depends on the voltage level of the C/Q line. The Master will source current if the input signal is equivalent to a logic “1”, or the Master will sink current if the input signal is equivalent to a logic “0.”

The Wake-up current pulse high test verifies the high-side driver and consists of observing the voltage VIM during the Wake-up pulse when a resistive load resulting in 500 mA current is connected. If the voltage VIM is above the threshold VTHHmax during a Wake-up pulse, this indicates the minimum requirement is met and results in a passing test result.

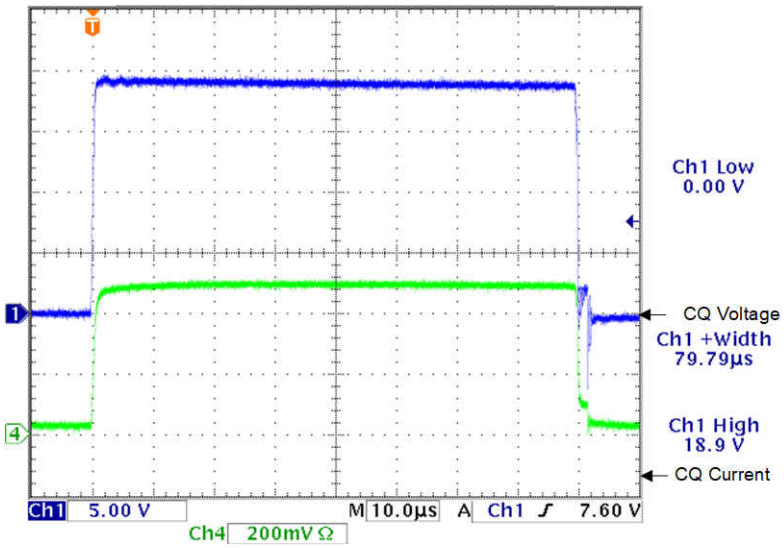


Figure 4-4. TCM_PHYL_INTF_IQWUH with 20 V

Figure 4-4 shows the test results with a supply voltage of 20 V and a 40 Ω resistive load that creates 500 mA of current. The voltage during the Wake-up pulse is observed to be 18.9 V which is greater than the VTHHmax requirement of 13 V resulting in a passing test result.

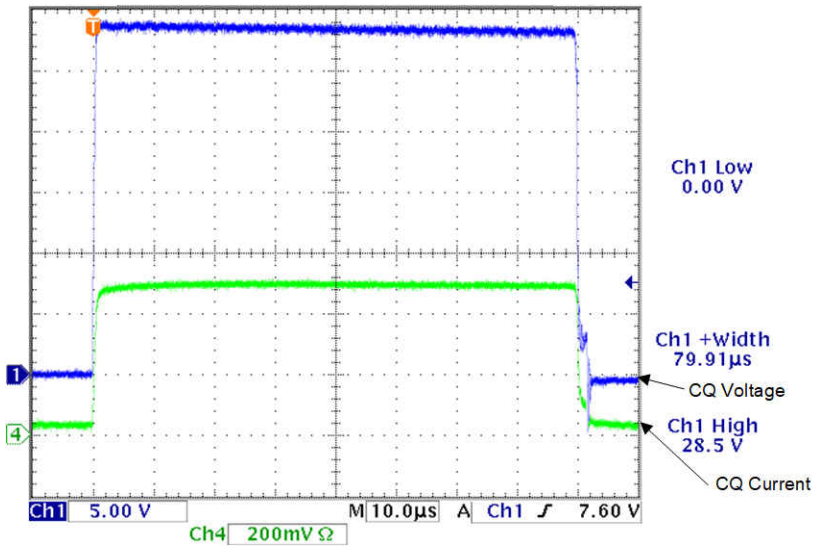


Figure 4-5. TCM_PHYL_INTF_IQWUH with 30 V

Figure 4-5 shows the test results with a supply voltage of 30 V and a 60 Ω resistive load that creates 500 mA of current. The voltage during the Wake-up pulse is observed to be 28.5 V which is also greater than the VTHHmax requirement of 13 V resulting in a passing test result.

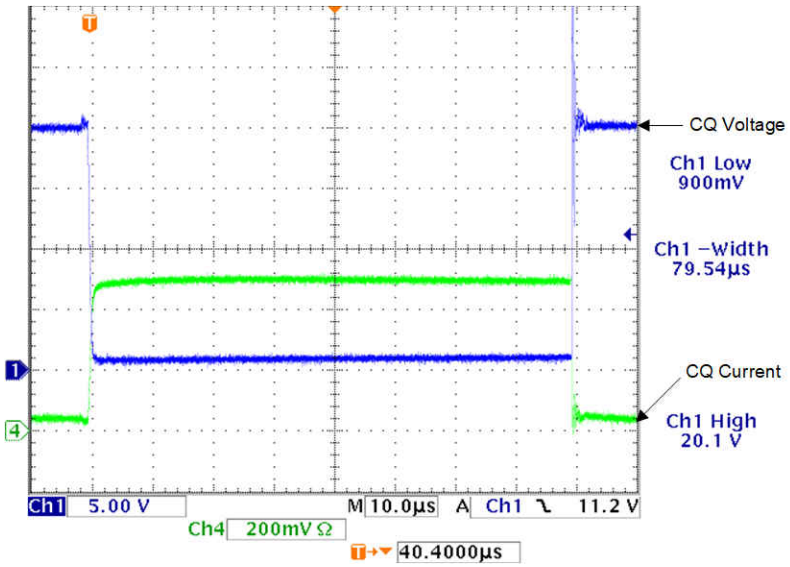


Figure 4-6. TCM_PHYL_IQWUL with 20 V

The Wake-up current pulse low test verifies the low-side driver and consists of observing the voltage VIM during the Wake-up pulse when a resistive load resulting in 500 mA current is connected. If the voltage VIM is below the threshold VTHLmin during a Wake-up pulse, this indicates the minimum requirement is met and results in a passing test result.

Figure 4-6 shows the test results with a supply voltage of 20 V and a resistive load between L+ and C/Q that creates 500 mA of current. The voltage during the Wake-up pulse is observed to be 0.9 V which is less than the VTHLmin requirement of 8 V resulting in a passing test result.

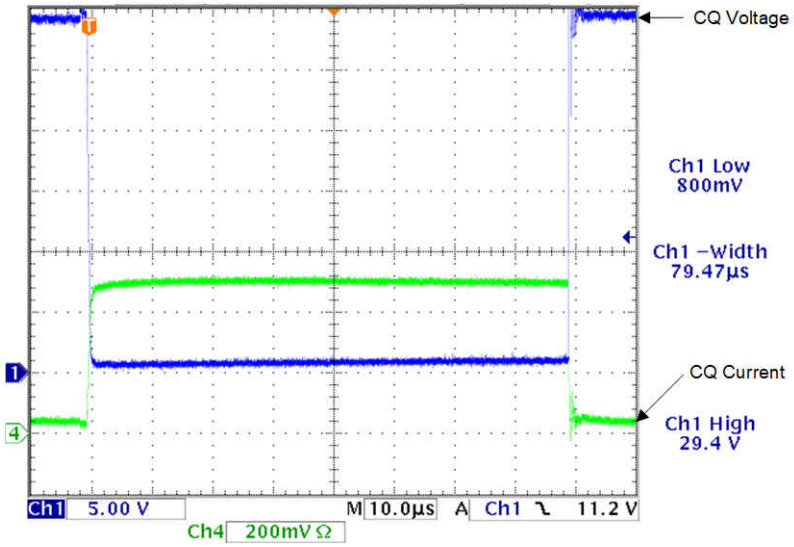


Figure 4-7. TCM_PHYL_INTF_IQWUL with 30 V

Figure 4-7 shows the test results with a supply voltage of 30 V and a resistive load between L+ and C/Q that creates 500 mA of current. The voltage during the Wake-up pulse is observed to be 0.9 V which is less than the VTHLmin requirement of 8 V resulting in a passing test result.

Table 4-1 lists all physical layer tests in summary and the results.

Table 4-1. IO-Link® Physical Layer Test

ID	Name	Configuration	Specification (Clause)	Comment	Result
SDCI_TC_0001	TCM_PHYL_INTF_ISM	The supply current at the Master port is monitored.	See *Section 5.3.2.3*, *Table 6* in *IO-Link Interface and System Specification Version 1.1.3*	Test with 500 mA	20 V: Pass 30 V: Pass
SDCI_TC_0002	TCM_PHYL_INTF_ISIRM	The supply current at the Master port is monitored.		Test with 500 mA	20 V: Pass 30 V: Pass
SDCI_TC_0003	TCM_PHYL_INTF_ILLM	The input current at C/Q at the Master port is monitored.			ILLM (VIM = 5 V, VSM = 20 V): 8.56mA Pass ILLM (VIM = 5,1 V, VSM = 20 V): 8.56 mA Pass ILLM (VIM = 15 V, VSM = 20 V): 8.57 mA Pass ILLM (VIM = VSM = 20 V): 8.57 mA Pass ILLM (VIM = 5 V, VSM = 30 V): 8.57 mA Pass ILLM (VIM = 5,1 V, VSM = 30 V): 8.57 mA Pass ILLM (VIM = 15 V, VSM = 30 V): 8.58 mA Pass ILLM (VIM = VSM = 30 V): 8.59 mA Pass
SDCI_TC_0004	TCM_PHYL_INTF_VREShigh	The output level at the Master C/Q output is measured.			VRQHM (VSM = 20 V): 0.23 V VRQHM (VSM = 30 V): 0.228 V Pass
SDCI_TC_0005	TCM_PHYL_INTF_VRESLOW	The output level at the Master C/Q output is measured.			VRQLM (VSM = 20 V): 0.225 V VRQLM (VSM = 30 V): 0.225 V Pass
SDCI_TC_0006	TCM_PHYL_INTF_VTHHM	The digital input signal for C/Q input is monitored	See *Section 5.3.2.2*, *Table 5* in *IO-Link Interface and System Specification Version 1.1.3*		VIM@VTHHM (VSM = 20 V): 11.1 V VIM@VTHHM (VSM = 30 V): 11.1 V Pass
SDCI_TC_0007	TCM_PHYL_INTF_VTHLM	The digital input signal for C/Q input is monitored			VIM@VTHLM (VSM = 20 V): 10.35 V VIM@VTHLM (VSM = 30 V): 10.35 V Pass
SDCI_TC_0008	TCM_PHYL_INTF_VHYSM	Comparison of values from SDCI_TC_0006 and SDCI_TC_0007			VHYSM (VSM = 20 V): 0.75 V VHYSM (VSM = 30 V): 0.75 V Pass
SDCI_TC_0299	TCM_PHYL_INTF_VOLTRANGECQ	Test if working after connecting CQ to 0 V and 30 V via 1 Ω	See *Section 5.3.2.2*, *Table 5* - VIL and VIH, in *IO-Link Interface and System Specification Version 1.1.3*		Pass

Table 4-1. IO-Link® Physical Layer Test (continued)

ID	Name	Configuration	Specification (Clause)	Comment	Result
SDCI_TC_0021	TCM_PHYL_INTF_IQWUH		See *Section 5.3.3.3*, *Table 9* in *IO-Link Interface and System Specification Version 1.1.3*	Wake-up pulse from function generator	VIM@WURQ (VSM = 20 V): 18.9 V VIM@WURQ (VSM = 30 V): 28.5 V Pass
SDCI_TC_0022	TCM_PHYL_INTF_TWUH			Wake-up pulse from function generator	TWUH@WURQ (VSM = 20 V): 80 µs TWUH@WURQ (VSM = 30 V): 80 µs Pass
SDCI_TC_0023	TCM_PHYL_INTF_IQWUL			Wake-up pulse from function generator	VIM@WURQ (VSM = 20 V): 0.9 V VIM@WURQ (VSM = 30 V): 0.9 V Pass
SDCI_TC_0024	TCM_PHYL_INTF_TWUL			Wake-up pulse from function generator	TWUL@WURQ (VSM = 20 V): 80 µs TWUL@WURQ (VSM = 30 V): 80 µs Pass

4.2.3 Current Sink (TCM_PHYL_INTF_ILLM)

The Master has an Integrated current sink to discharge the load when idle and create a minimum quiescent current at the Master Port C/Q in input mode. This current is specified as ILL_M = 5 mA to 15 mA for 5 V < VI_M < 30 V. Figure 4-8 shows the current flowing into the C/Q line when the TX is disabled and the current sink is active across the input voltage range of 0 V to 24 V. The test results show the current is about 8.5 mA when the VI_M is between 5 V and 24 V which is well within the allowed range of 5 – 15 mA for a passing test result.

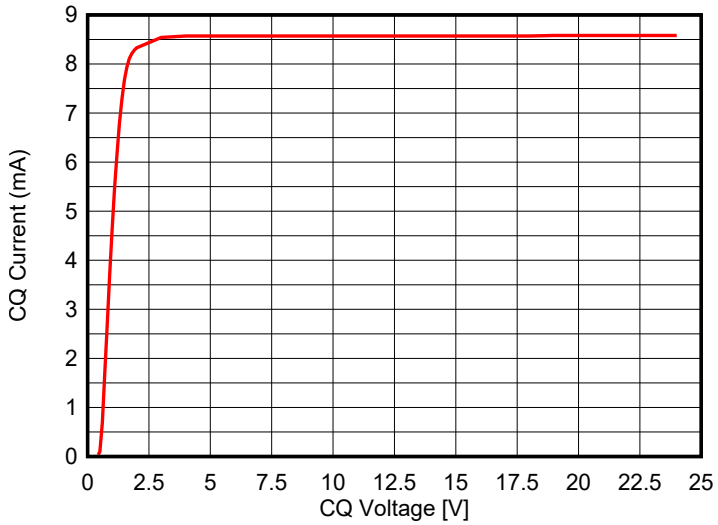


Figure 4-8. Current Sink of TIOL112

4.2.4 Cycle Time and Jitter (TCM_ PHYL_TIME_MASTERCYCLETIMEREAL)

The timing related tests such as the Cycle Time and Jitter require the BOOSTXL-IOLINKM-8 BoosterPack to be mated with the LP-AM243 LaunchPad running the example MCU + SDK firmware. The fastest communication mode COM3 has a recommended minimum cycle time (MinCycleTime) of 400 µs. The cycle time t_{CYC} is equal to the sum of the M-sequence time $t_{M\text{-}sequence}$ plus the idle time t_{idle} which is the time between the end of the message from the device and the beginning of the next message from the Master. The measured cycle time should be within -1% and +10% of the expected cycle time. For COM3, this is between 396 µs and 440 µs.

Figure 4-9 shows a cycle time to be approximately 412 µs using a repetitive scope plot enabled with infinite persistence. There were no visible signs of significant cycle-to-cycle jitter in the waveforms.

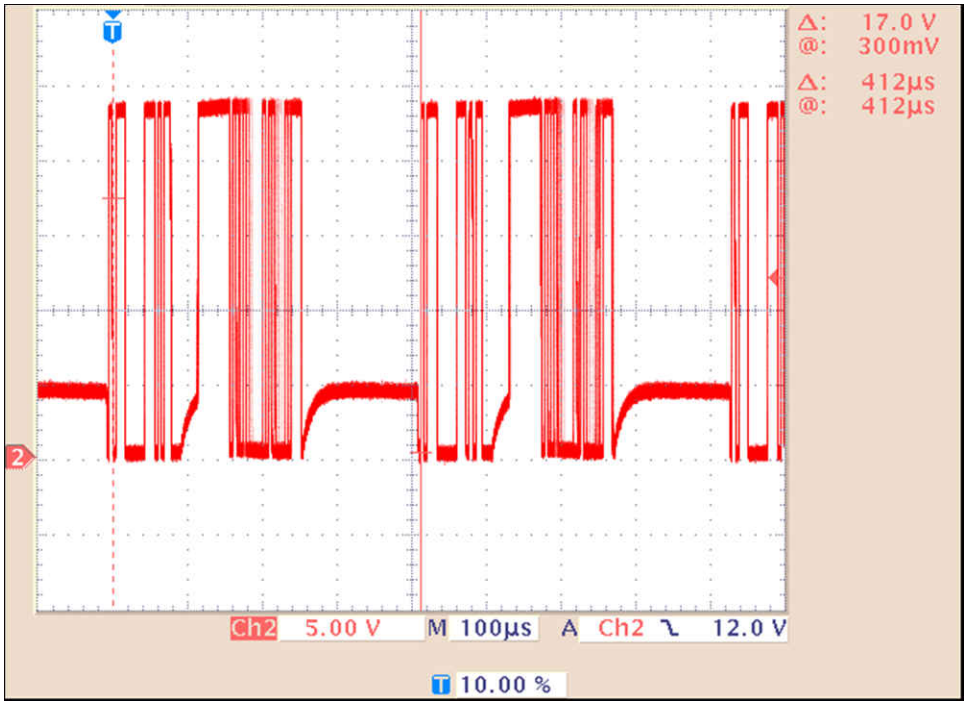


Figure 4-9. CQ Line Communication

Figure 4-10 shows the cycle time to be about 417 µs when captured on a logic analyzer which is, well within the -1% to +10% range allowed by the standard and a passing test result. The answer time of the connected device can also be seen in this plot.

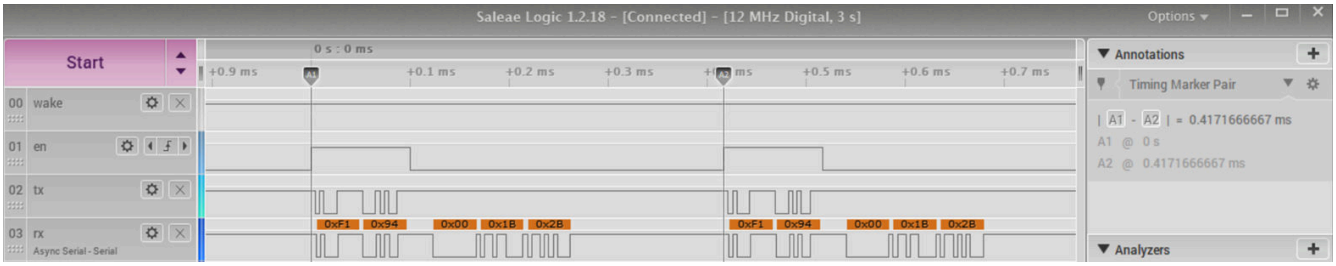


Figure 4-10. Master Cycle Timing

The cycle-to-cycle jitter can be seen in Figure 4-11 which shows a zoomed in view of the second communication cycle on the CQ line while the scope is triggered on the first cycle. With infinite persistence enabled, the transition edge widens to a show a jitter of approximately 50 ns. Compared to the rise and fall times, as well as the cycle timing, this amount of jitter is neglect able and does not degrade the system performance.

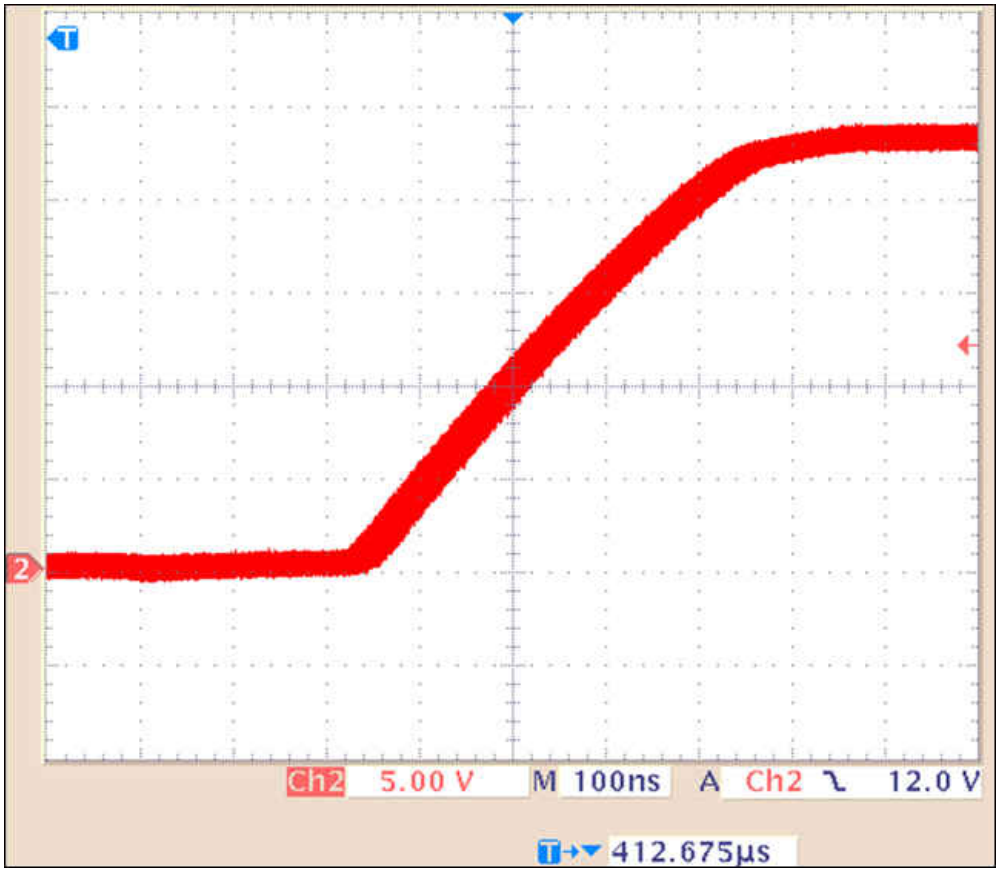


Figure 4-11. Master Cycle Jitter

5 Hardware Design Files

5.1 Schematics

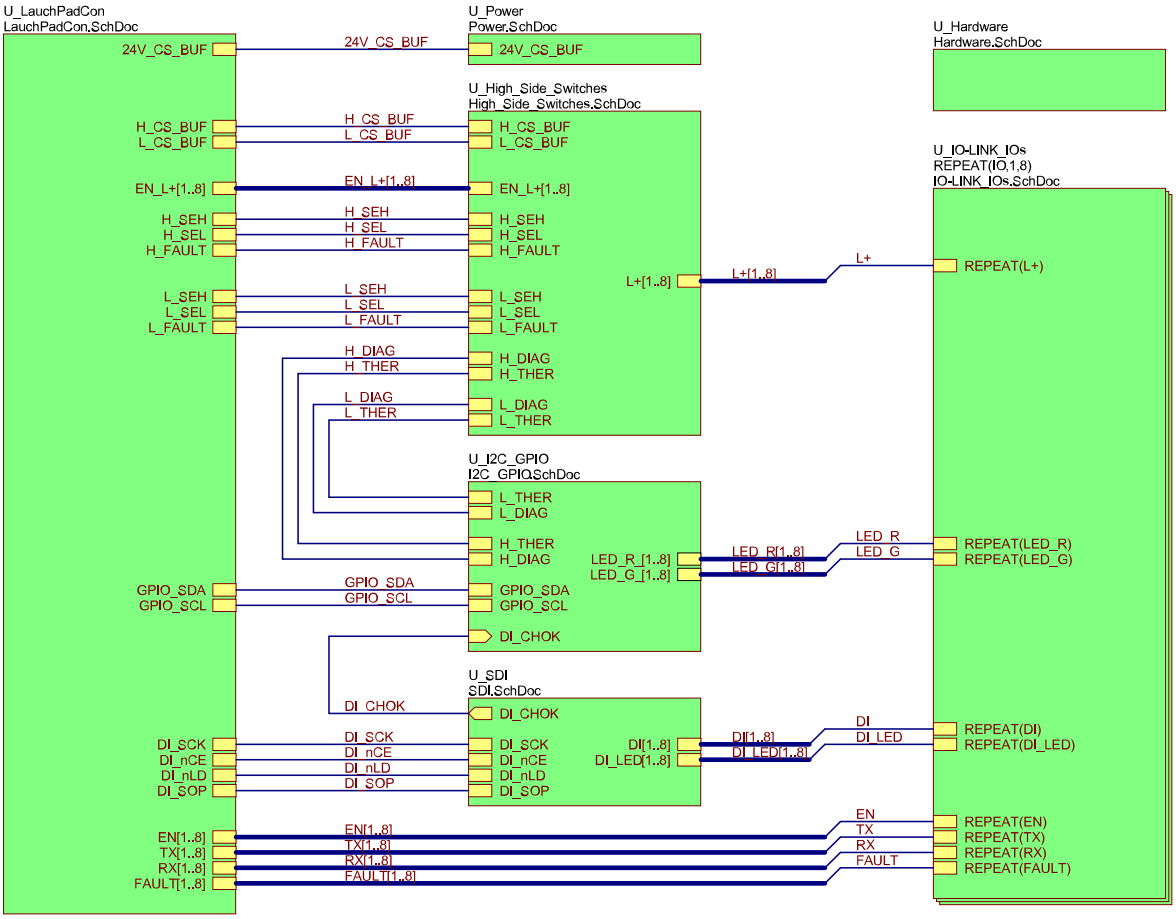
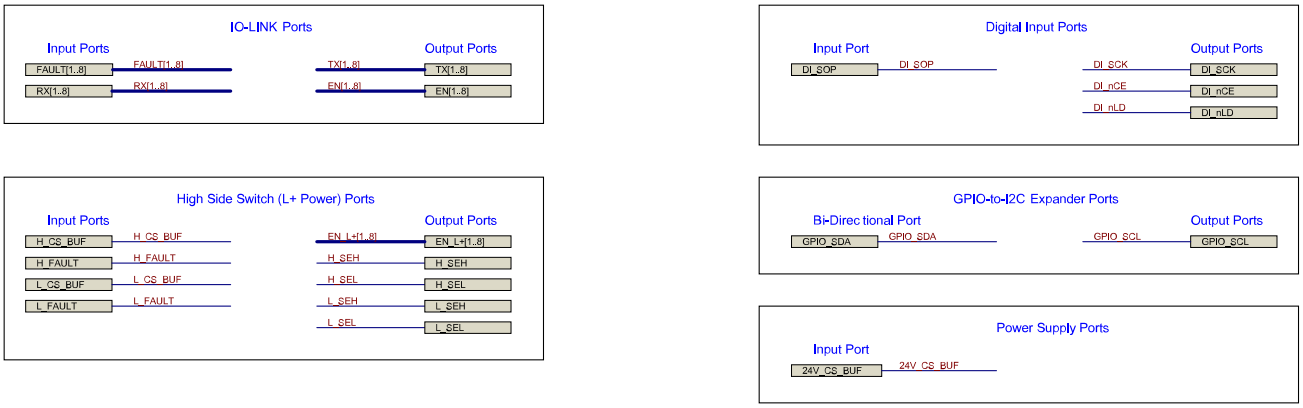


Figure 5-1. Schematic - Top Level



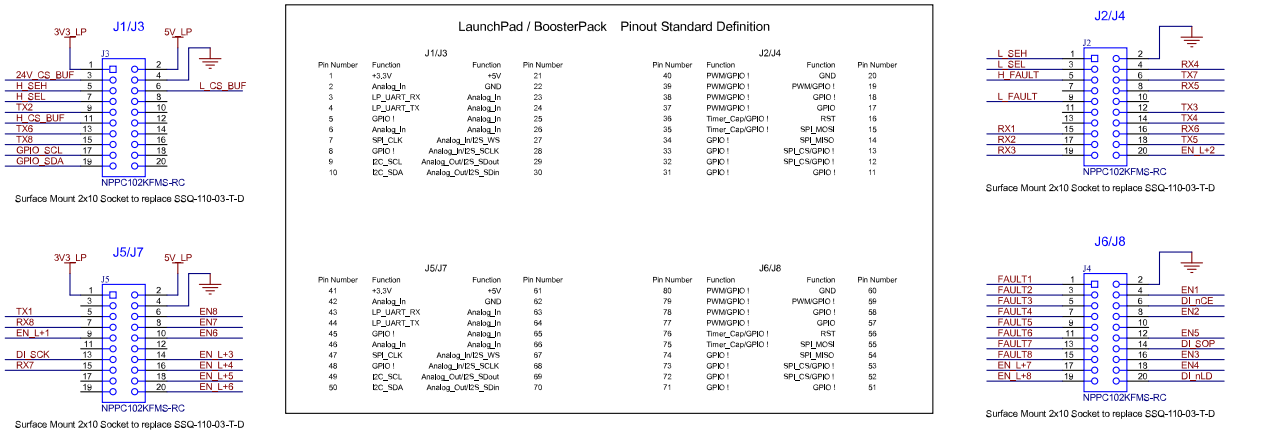


Figure 5-2. Schematic - LaunchPad Connectors

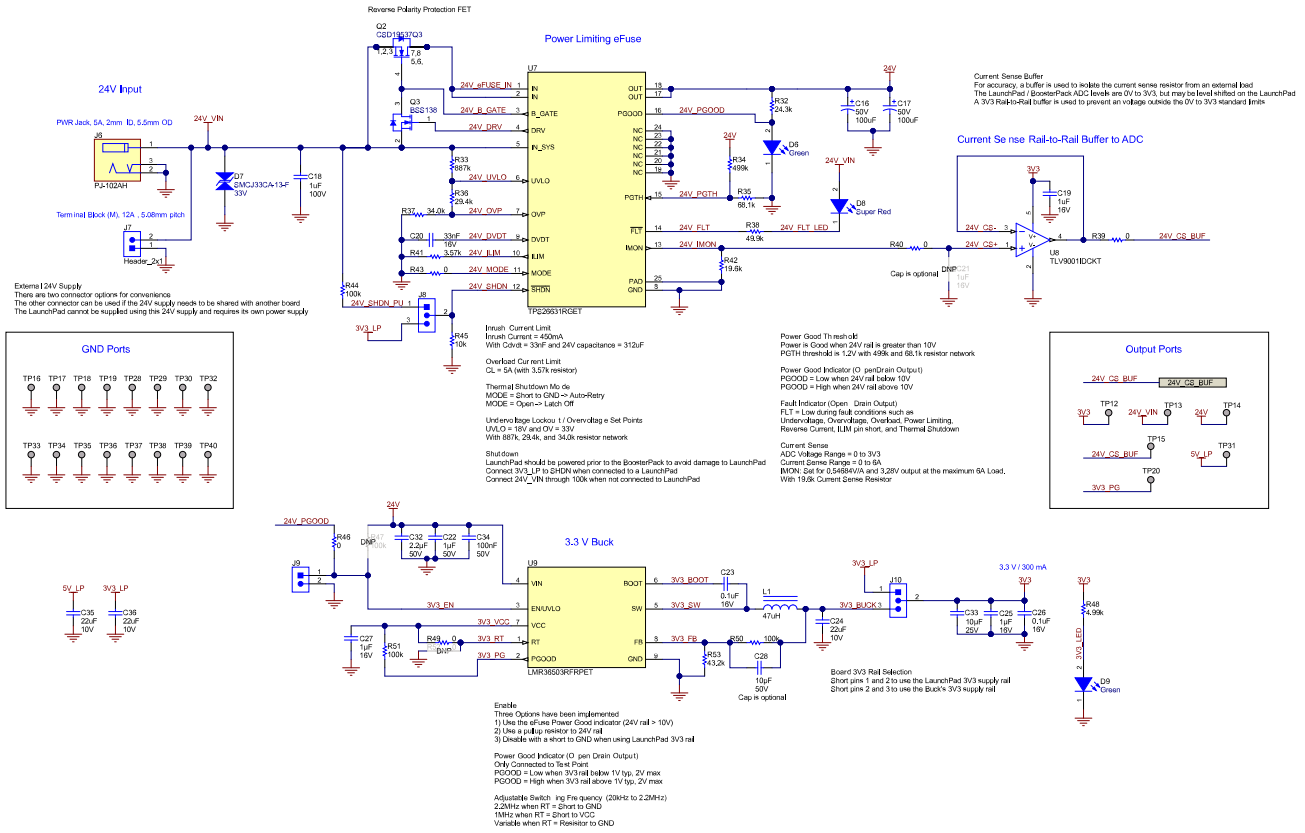


Figure 5-3. Schematic - Power

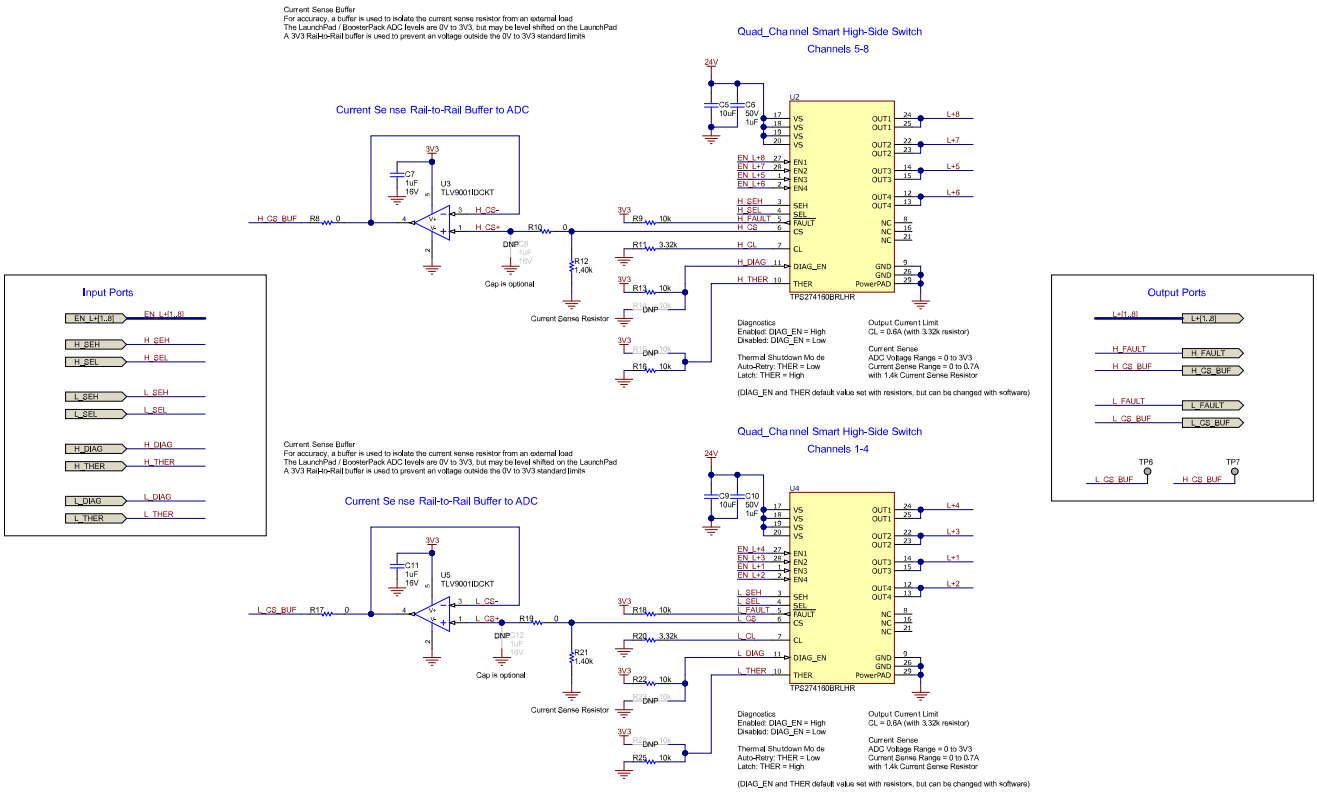


Figure 5-4. Schematic - High Side Switches

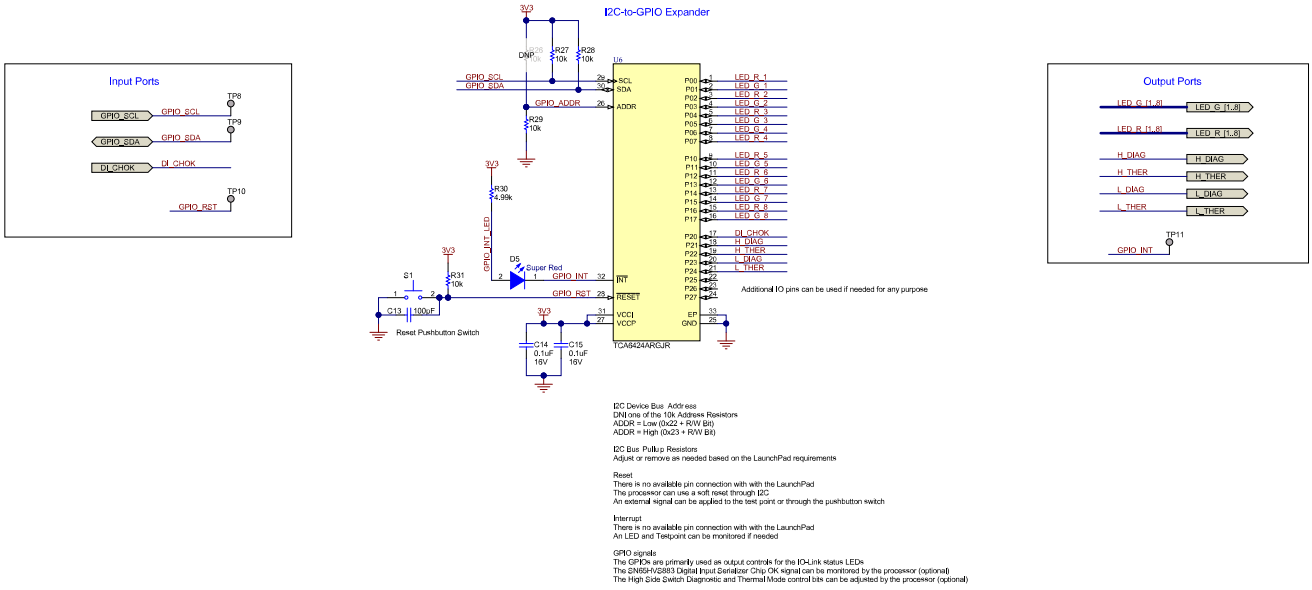


Figure 5-5. Schematic - I2C GPIO

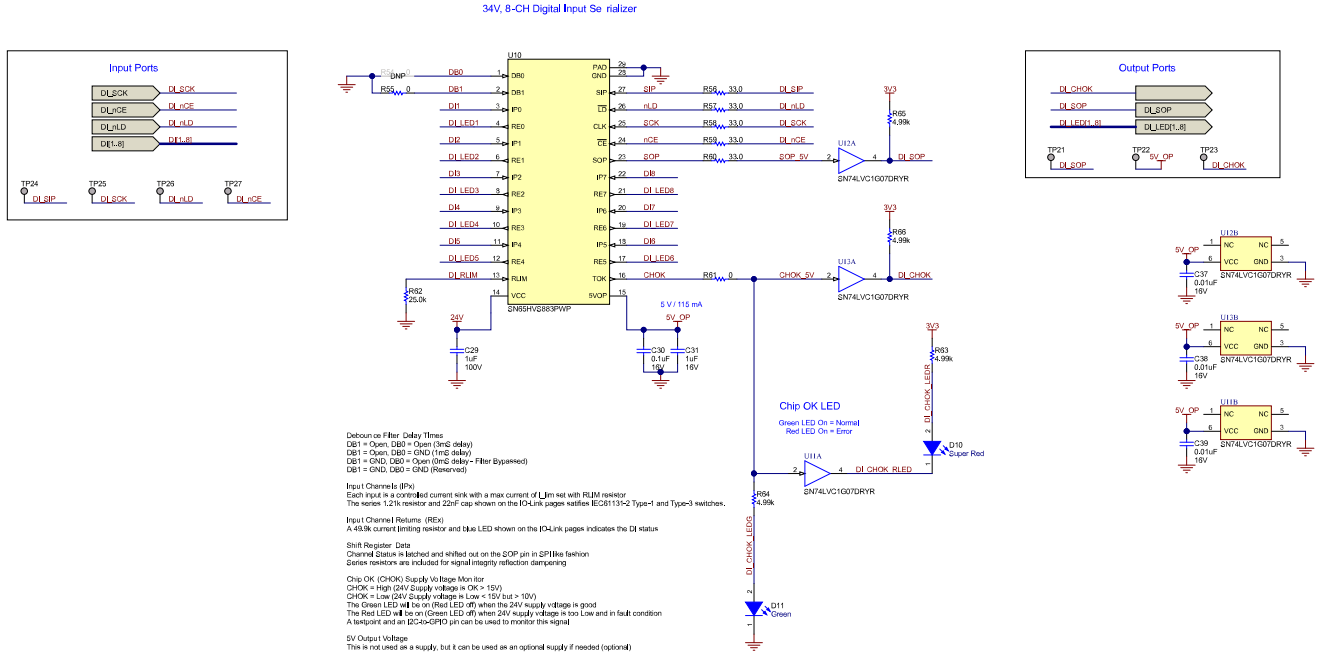


Figure 5-6. Schematic - Digital Input Serializer

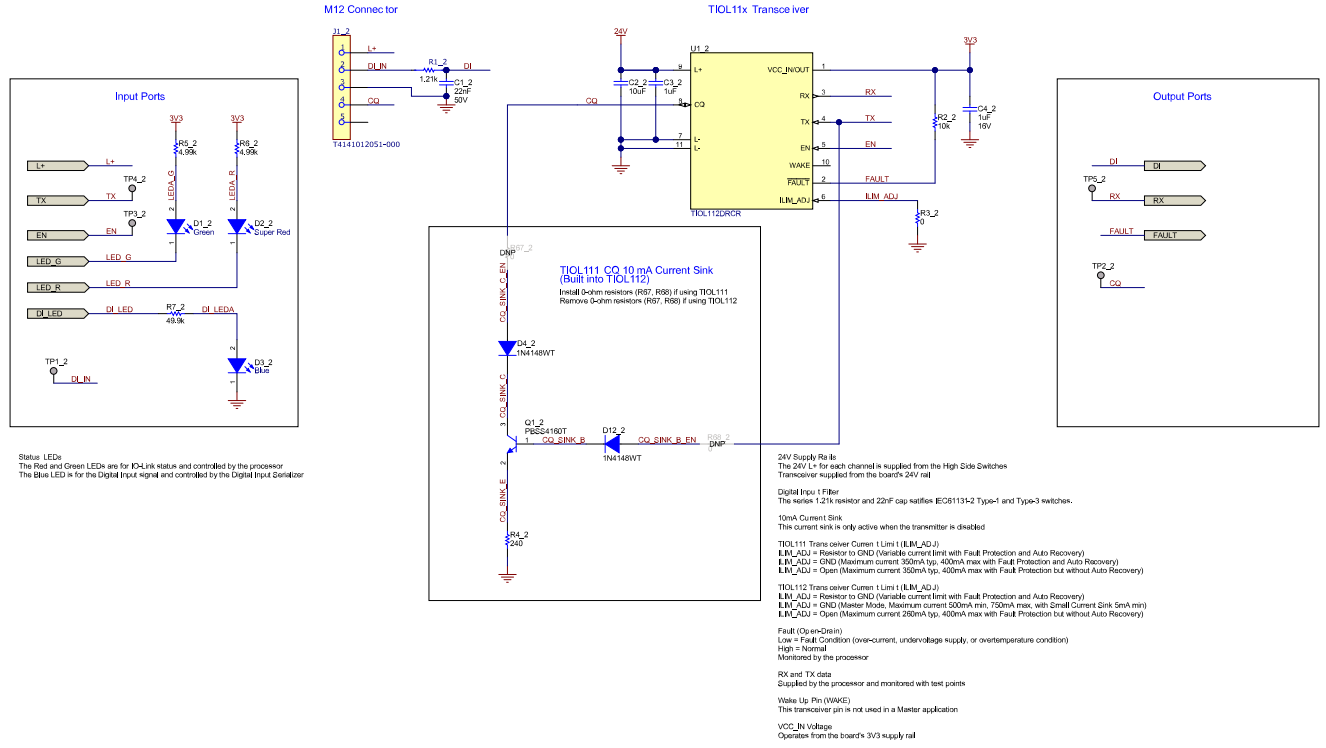


Figure 5-7. Schematic - IO-Link Channel IO Port 1

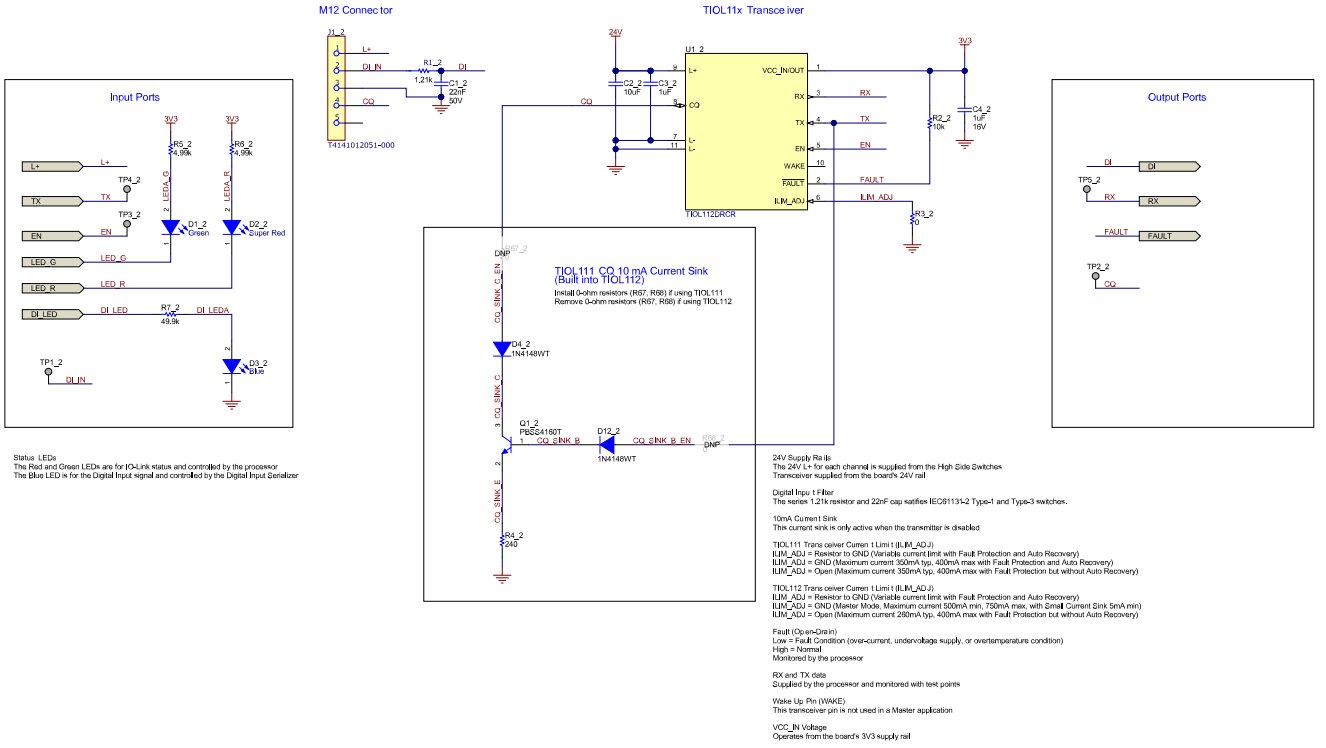


Figure 5-8. Schematic - IO-Link Channel IO Port 2

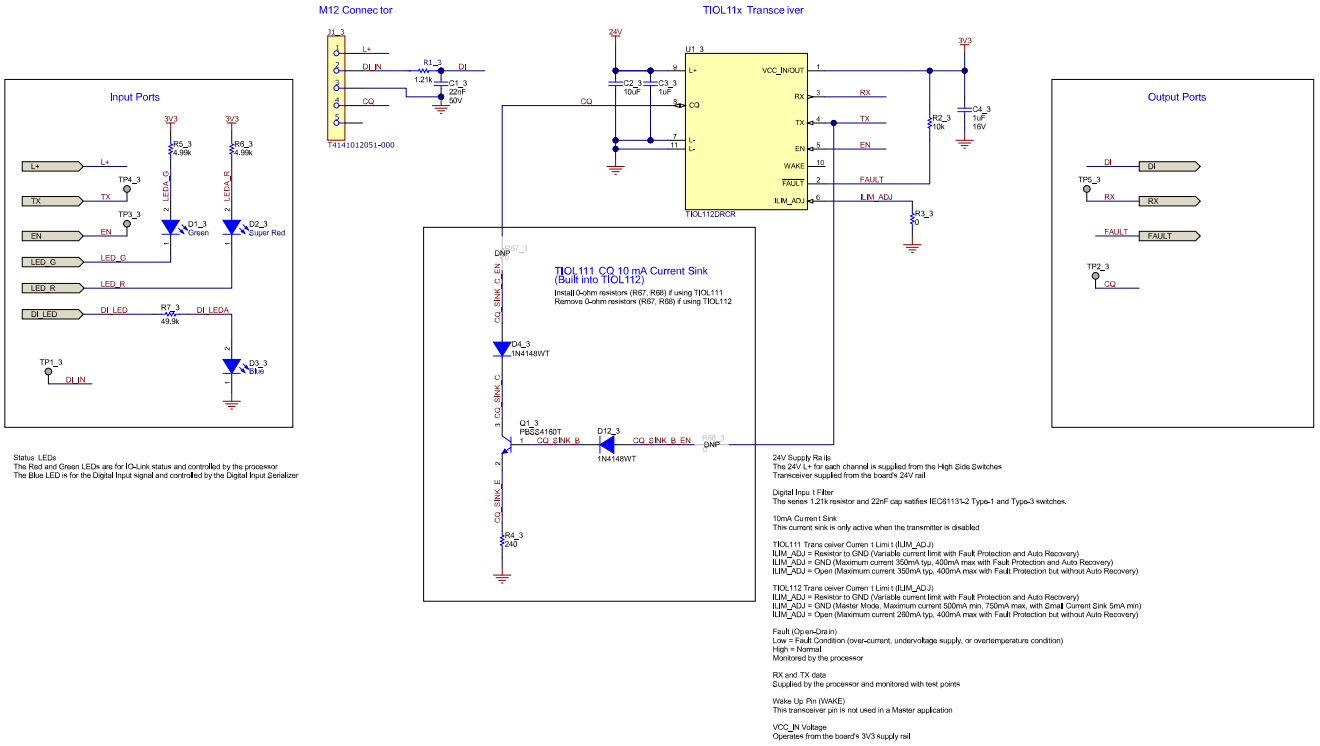


Figure 5-9. Schematic - IO-Link Channel IO Port 3

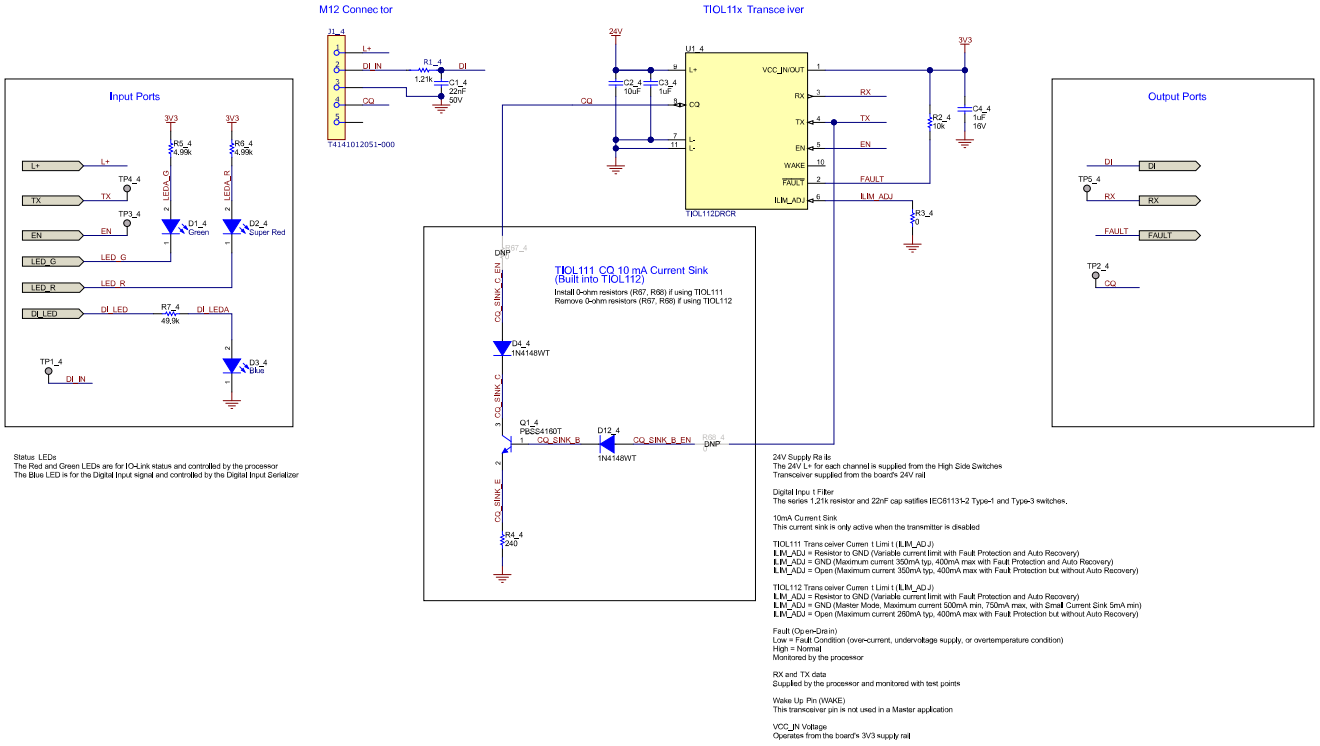


Figure 5-10. Schematic - IO-Link Channel IO Port 4

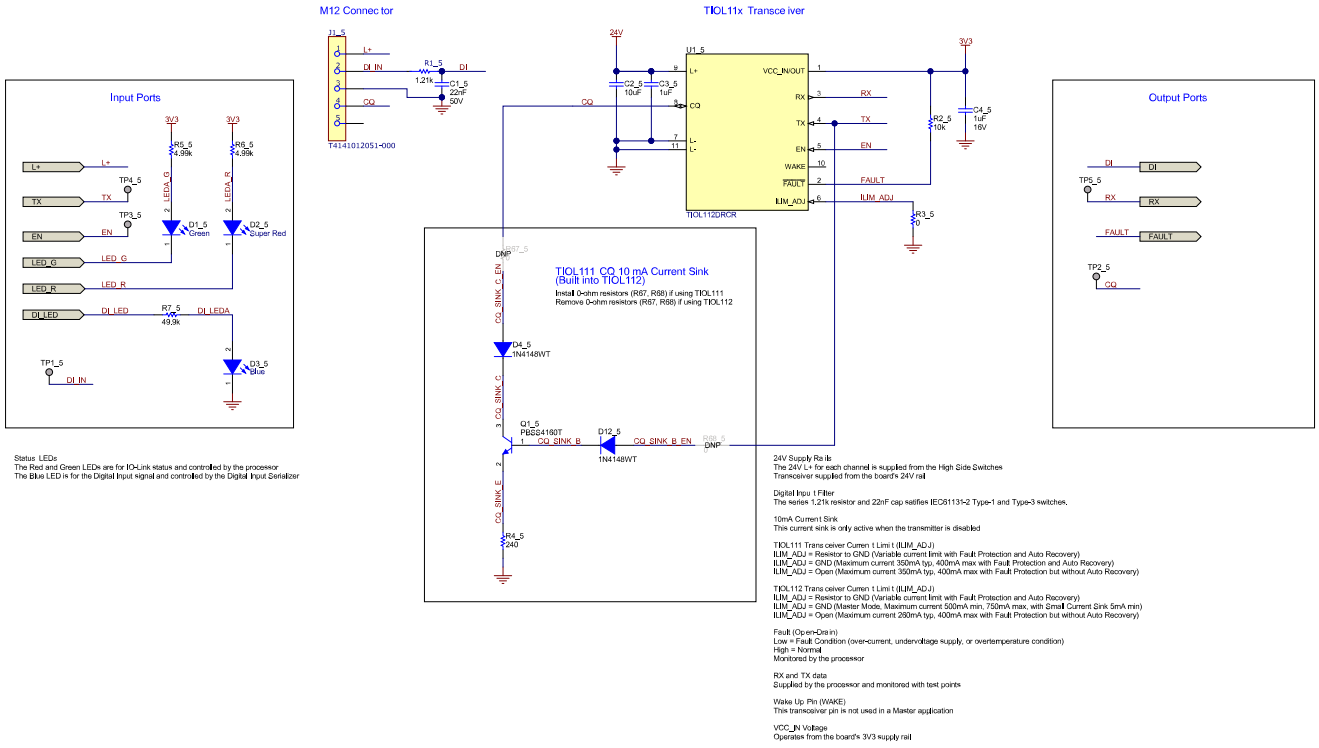


Figure 5-11. Schematic - IO-Link Channel IO Port 5

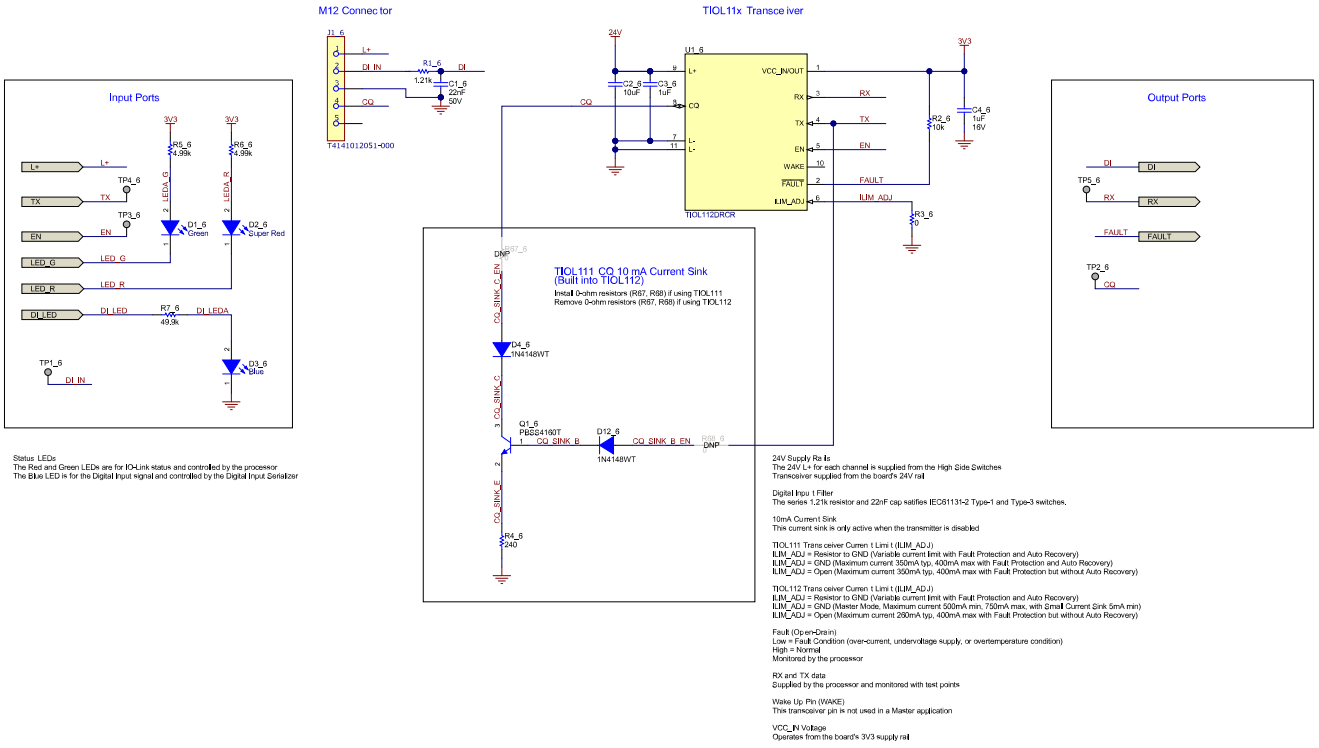


Figure 5-12. Schematic - IO-Link Channel IO Port 6

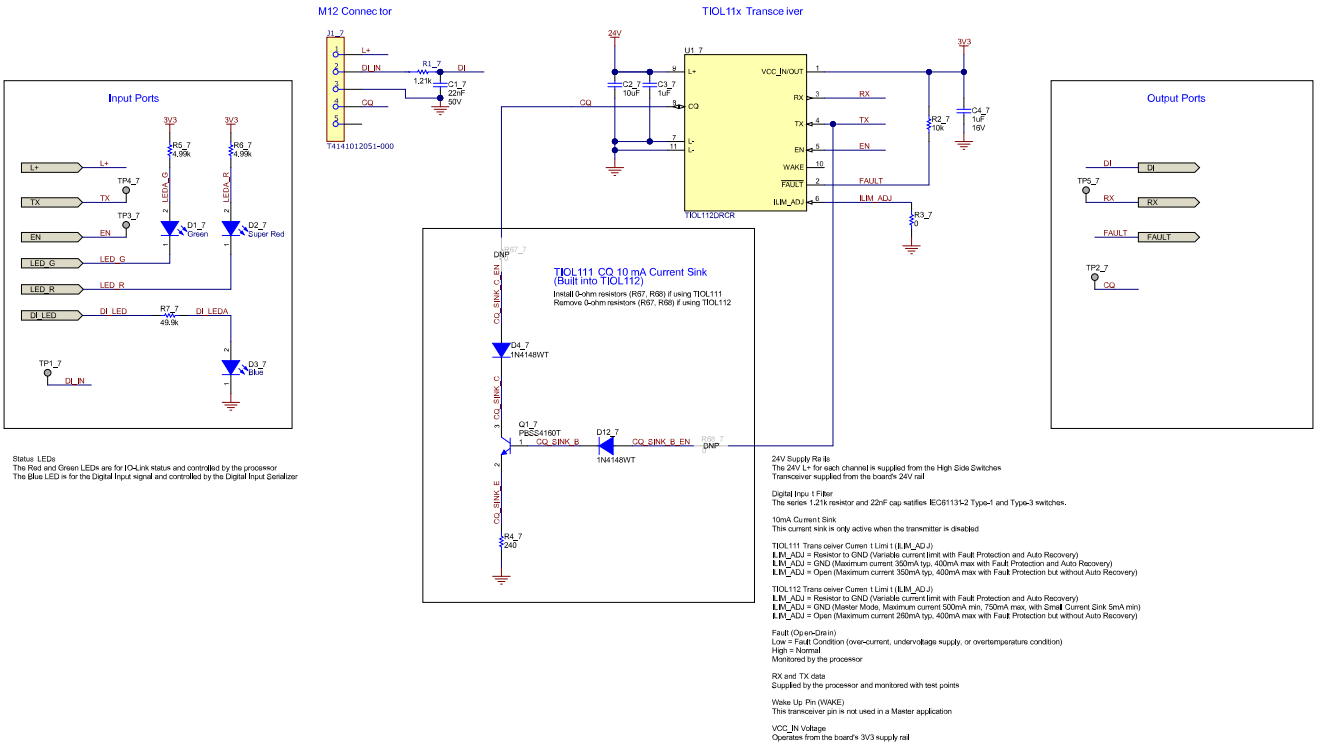


Figure 5-13. Schematic - IO-Link Channel IO Port 7

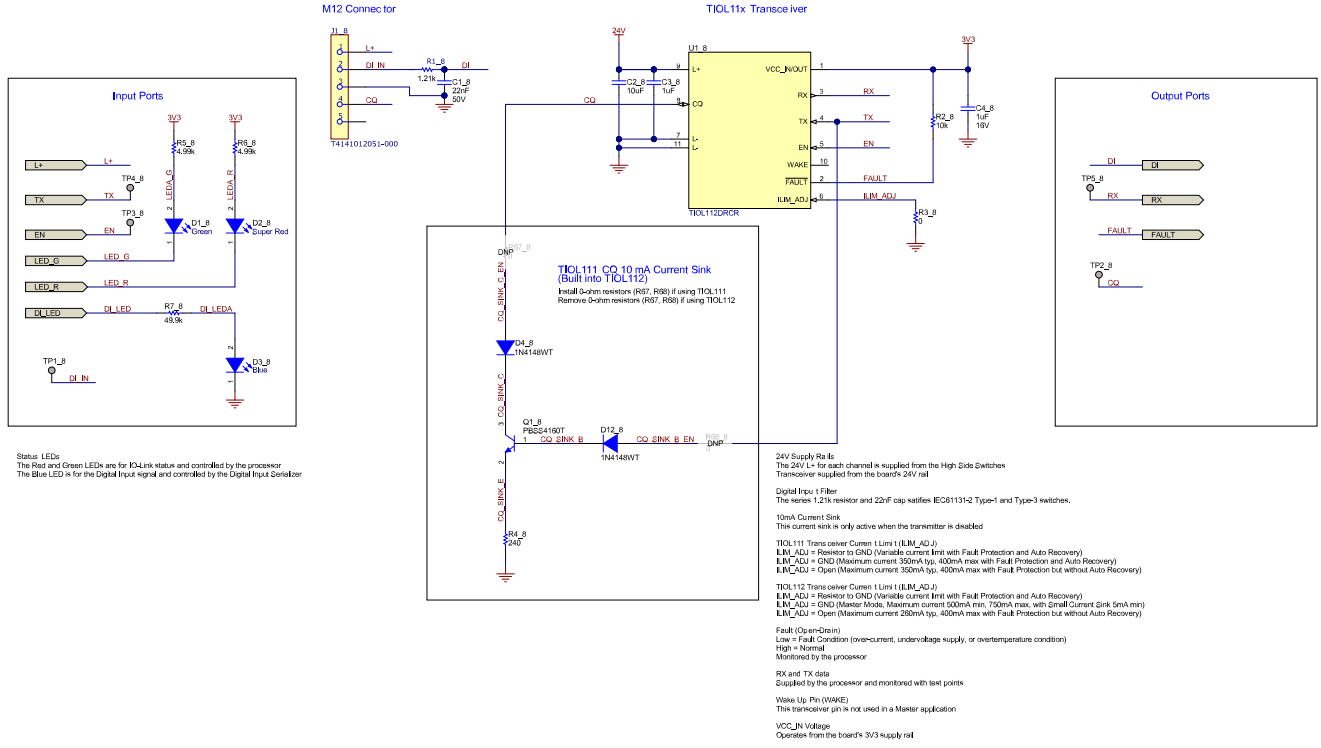


Figure 5-14. Schematic - IO-Link Channel IO Port 8

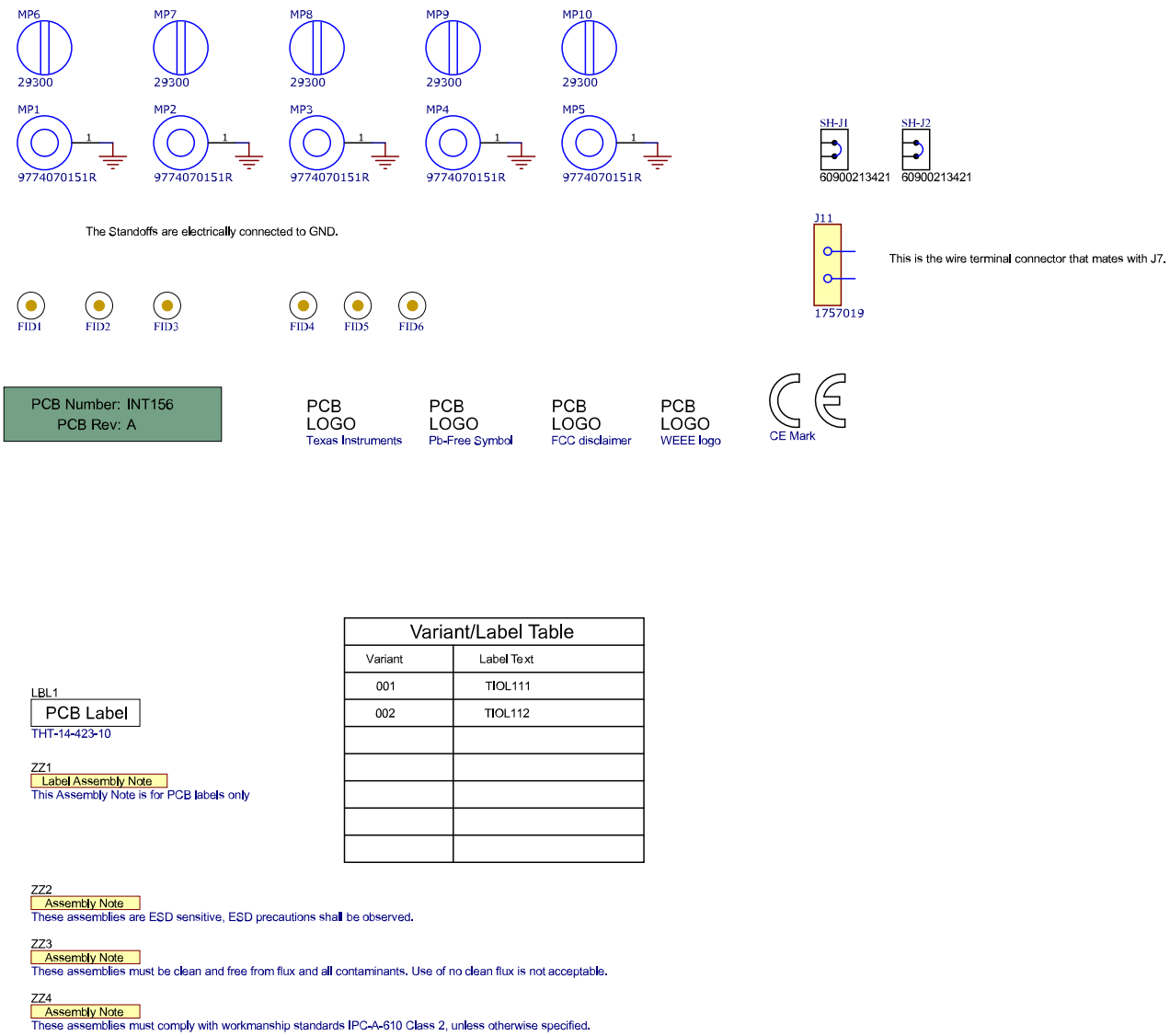


Figure 5-15. Schematic - Hardware

5.2 PCB Layouts

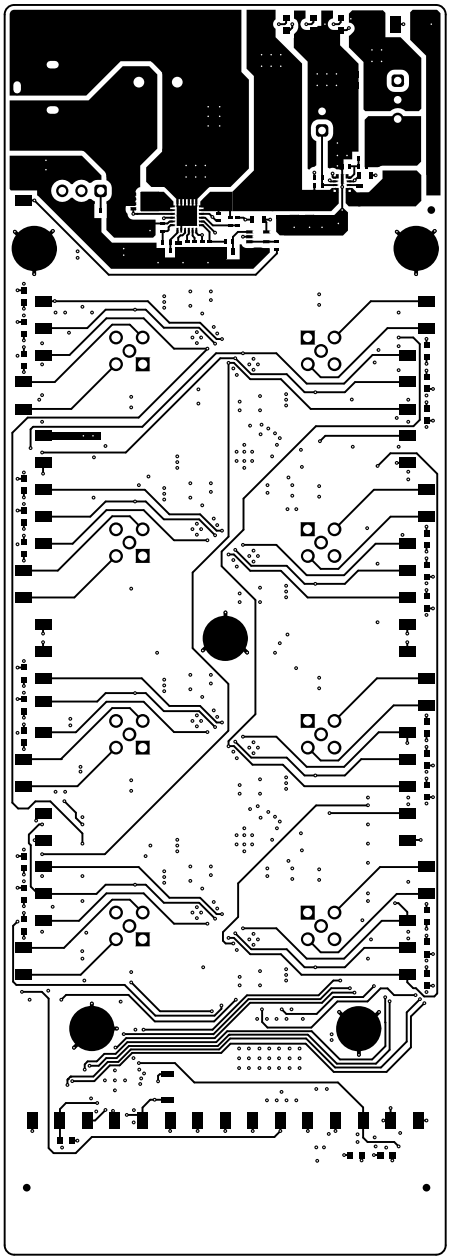


Figure 5-16. Top Layer

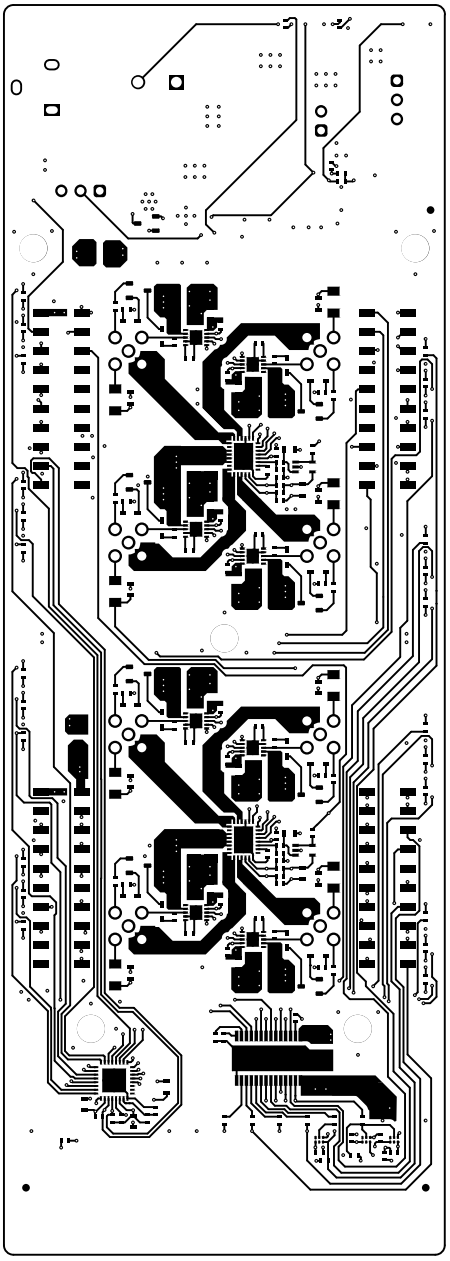


Figure 5-17. Bottom

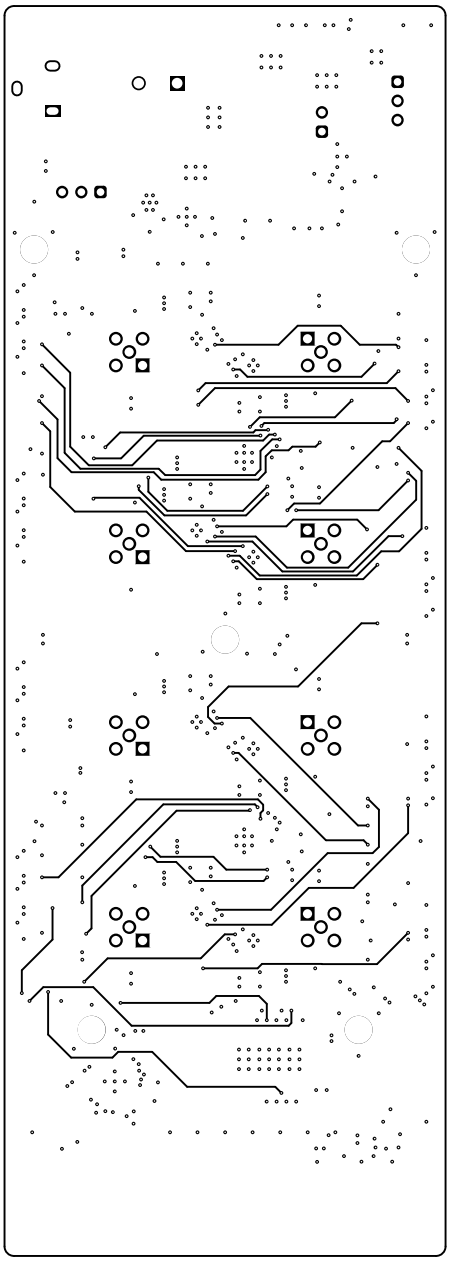


Figure 5-18. Signal Layer 2

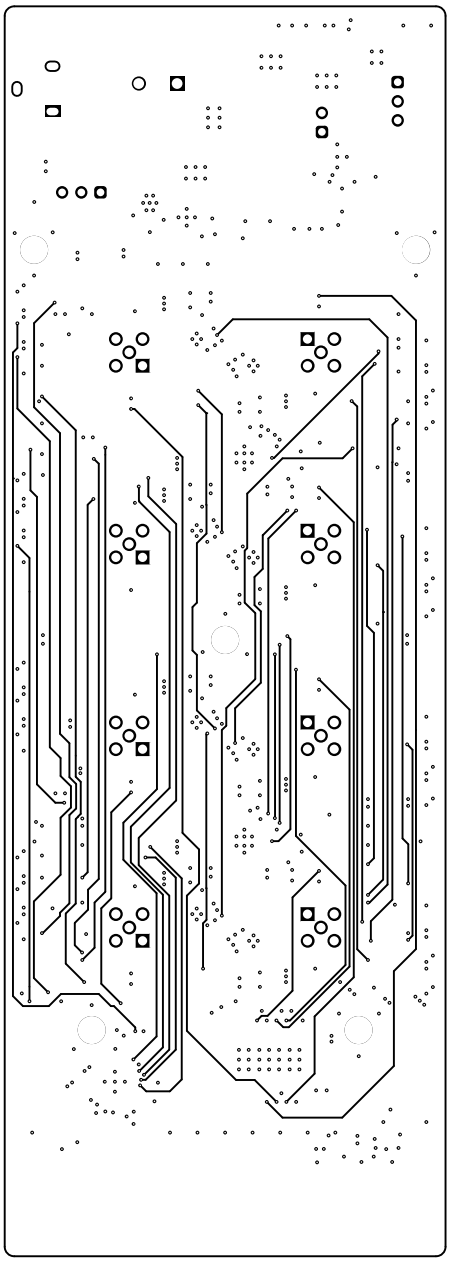


Figure 5-19. Signal Layer 3

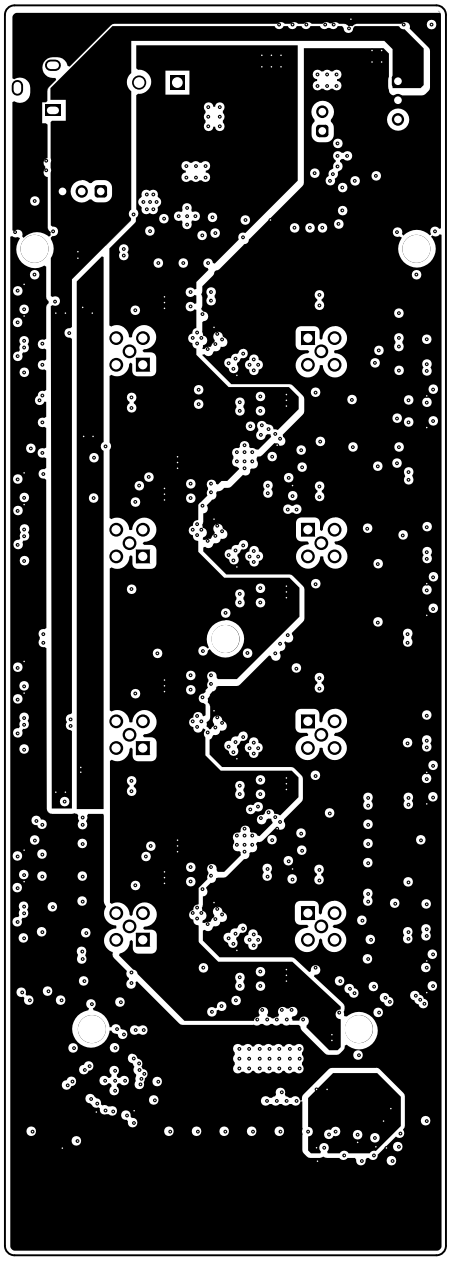


Figure 5-20. Power Layer

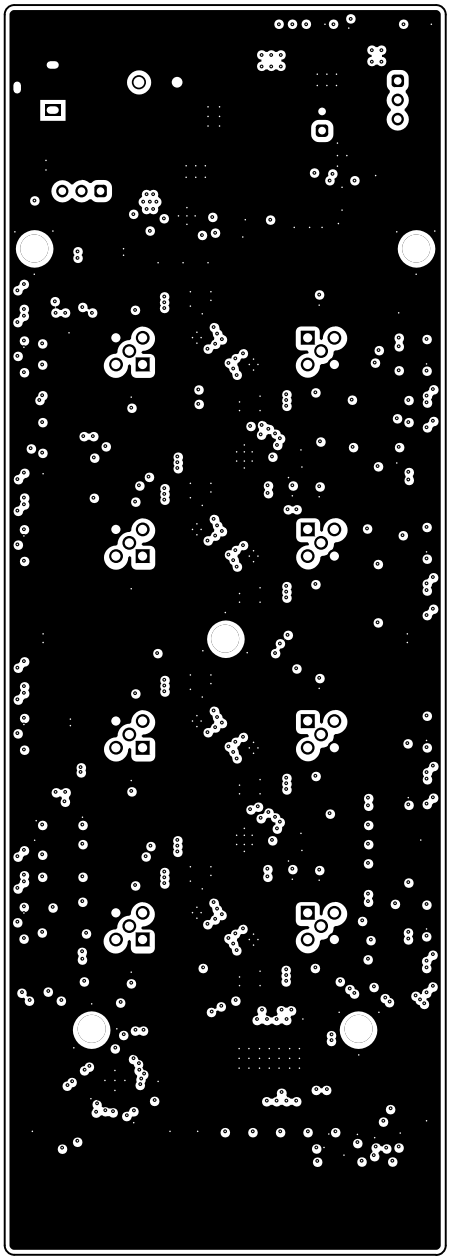


Figure 5-21. Ground

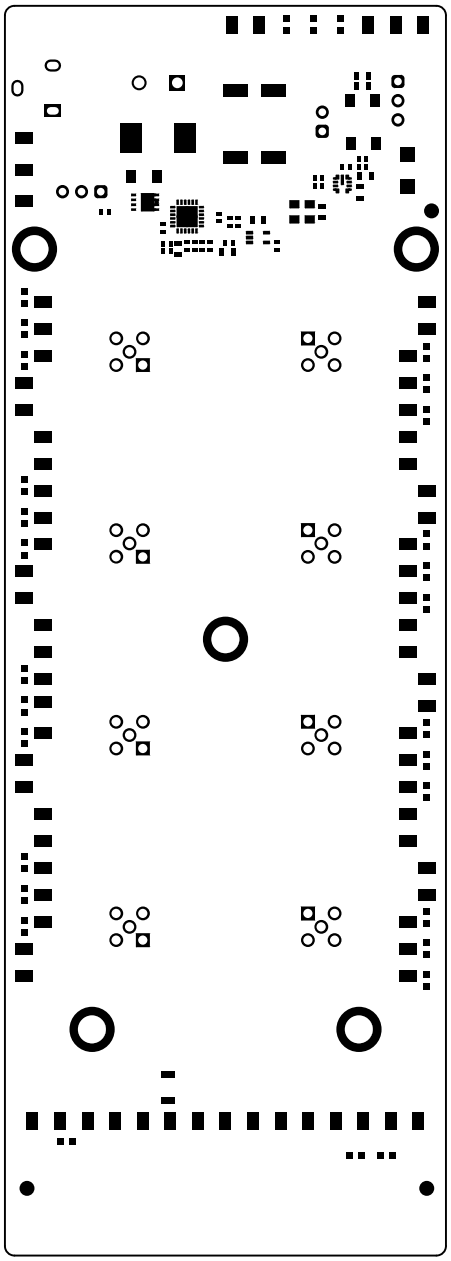


Figure 5-22. Top Solder Layer

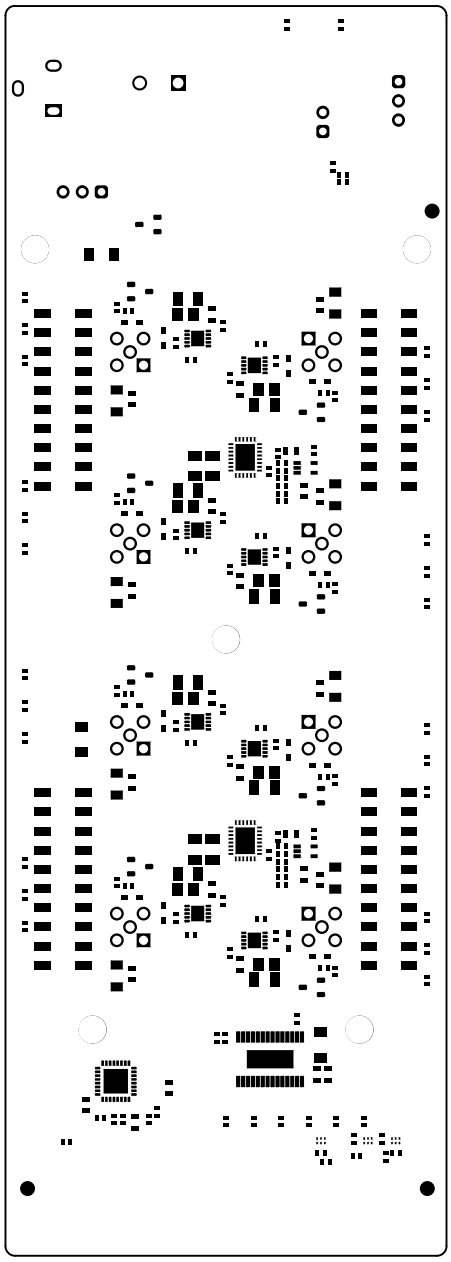


Figure 5-23. Bottom Solder

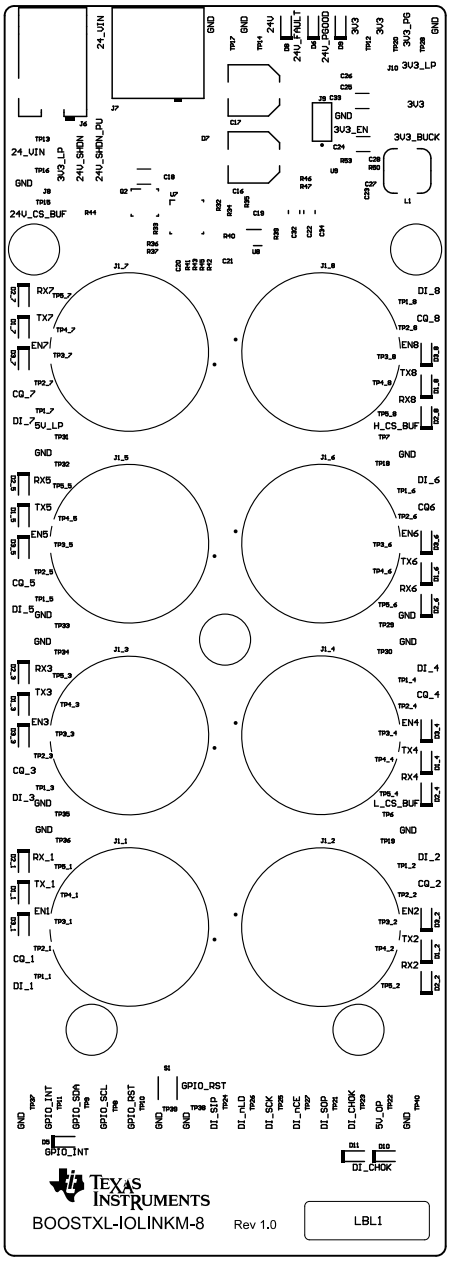


Figure 5-24. Top Overlay

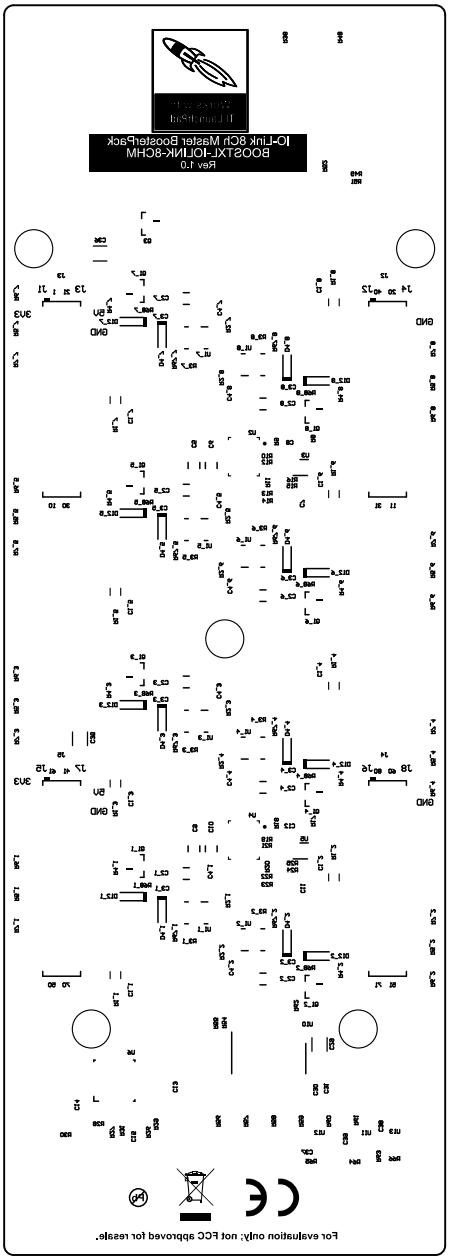


Figure 5-25. Bottom Overlay

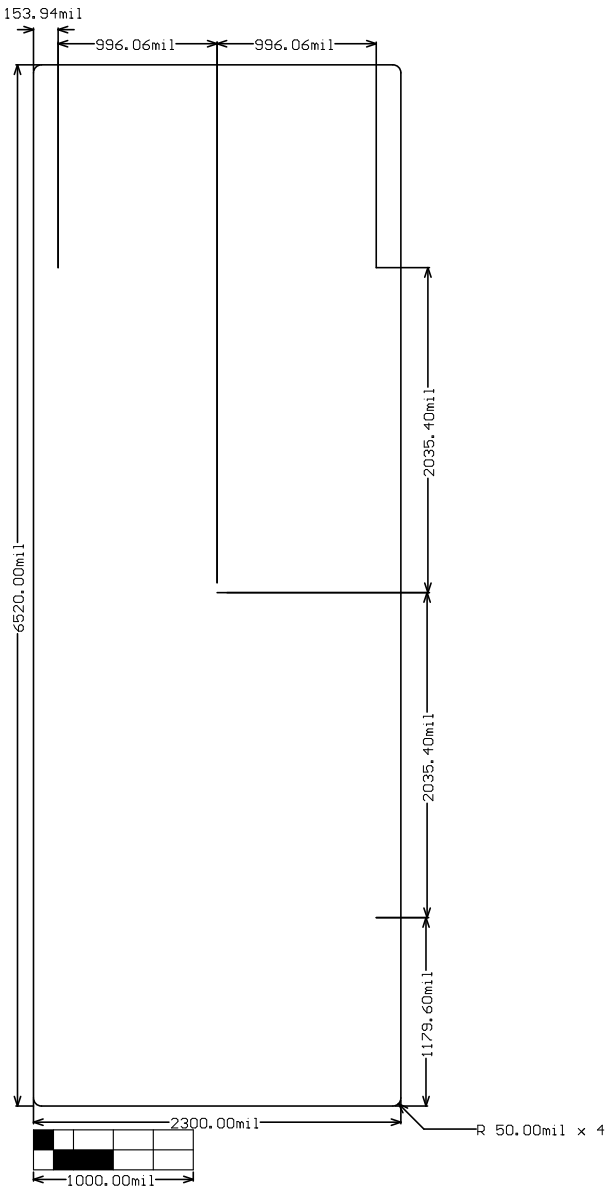


Figure 5-26. Board Dimensions

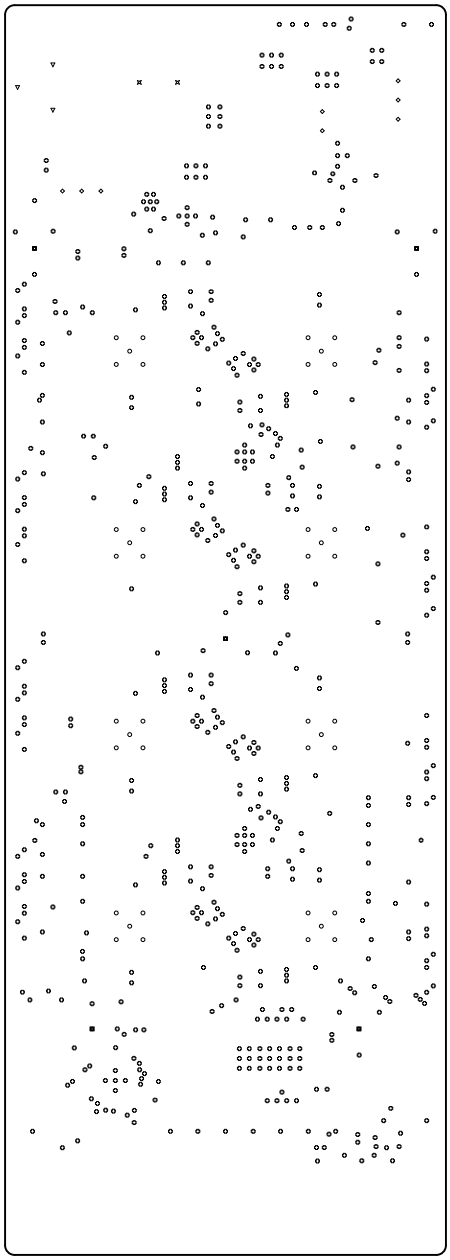


Figure 5-27. Drill Drawing

5.3 Bill of Materials (BOM)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate PartNumber	Alternate Manufacturer
!PCB1	1		Printed Circuit Board		INT156	Any		
C1_1, C1_2, C1_3, C1_4, C1_5, C1_6, C1_7, C1_8	8	0.022uF	CAP, CERM, 0.022 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603X223K5RACTU	Kemet		
C2_1, C2_2, C2_3, C2_4, C2_5, C2_6, C2_7, C2_8, C5, C9	10	10uF	CAP, CERM, 10 uF, 50 V, +/- 20%, X5R, AEC-Q200 Grade 3, 1206	1206	CGA5L3X5R1H106M160AB	TDK		
C3_1, C3_2, C3_3, C3_4, C3_5, C3_6, C3_7, C3_8	8	1uF	CAP, CERM, 1 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805	0805	CGA4J3X7S2A105K125AB	TDK		
C4_1, C4_2, C4_3, C4_4, C4_5, C4_6, C4_7, C4_8, C7, C11, C19, C25, C27, C31	14	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, 0603	0603	885012206052	Wurth Elektronik		
C6, C10	2	1uF	CAP, CERM, 1 µF, 100 V,+/- 10%, X7R, 1206	1206	12061C105KAT2A	AVX		
C13	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A101JAT2A	AVX		
C14, C15, C23, C26, C30	5	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	0603	C0603C104K4RACTU	Kemet		
C16, C17	2	100uF	CAP, AL, 100 uF, 50 V, +/- 20%, 0.34 ohm, AEC-Q200 Grade 2, SMD	D6.3xL7.7mm	EEEFTH101XAP	Panasonic		
C18, C29	2	1uF	CAP, CERM, 1 uF, 100 V, +/- 10%, X7R, 1206	1206	C3216X7R2A105K160AA	TDK		
C20	1	0.033uF	CAP, CERM, 0.033 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C333J3RACTU	Kemet		
C22	1	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805	0805	885012207103	Wurth Elektronik		
C24, C35, C36	3	22uF	CAP, CERM, 22 uF, 10 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206	1206	GCM31CR71A226KE02L	MuRata		

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate PartNumber	Alternate Manufacturer
C28	1	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	0402	CGA2B2C0G1H100D050BA	TDK		
C32	1	2.2uF	CAP, CERM, 2.2 uF, 50 V, +/- 10%, X7R, 0805	0805	C2012X7R1H225K125AC	TDK		
C33	1	10uF	CAP, CERM, 10 µF, 25 V,+/- 10%, X7R, 1206	1206	C3216X7R1E106K160AB	TDK		
C34	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	0603	C0603C104K5RACTU	Kemet		
C37, C38, C39	3	0.01uF	CAP, CERM, 0.01 µF, 16 V,+/- 10%, X7R, 0402	0402	CC0402KRX7R7BB103	Yageo		
D1_1, D1_2, D1_3, D1_4, D1_5, D1_6, D1_7, D1_8, D6, D9, D11	11	Green	LED, Green, SMD	LED_0603	150060VS75000	Wurth Elektronik		
D2_1, D2_2, D2_3, D2_4, D2_5, D2_6, D2_7, D2_8, D5, D8, D10	11	Super Red	LED, Super Red, SMD	LED_0603	150060SS75000	Wurth Elektronik		
D3_1, D3_2, D3_3, D3_4, D3_5, D3_6, D3_7, D3_8	8	Blue	LED, Blue, SMD	LED_0603	150060BS75000	Wurth Elektronik		
D4_1, D4_2, D4_3, D4_4, D4_5, D4_6, D4_7, D4_8, D12_1, D12_2, D12_3, D12_4, D12_5, D12_6, D12_7, D12_8	16	75V	Diode, Switching, 75 V, 0.3 A, SOD-523F	SOD-523F	1N4148WT	Fairchild Semiconductor		
D7	1	33V	Diode, TVS, Bi, 33 V, 53.3 Vc, 1500 W, 200 A, SMC	SMC	SMCJ33CA-13-F	Diodes Inc.		
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
J1_1, J1_2, J1_3, J1_4, J1_5, J1_6, J1_7, J1_8	8		Sensor Connector, M12, Receptacle, 5 Contacts, PCB Socket, Straight Panel Mount	PTH_CIRCULAR_CONNECTOR	T4141012051-000	TE Connectivity		
J2, J3, J4, J5	4		Receptacle, 2.54mm, 10x2, Gold, SMT	Receptacle, 2.54mm, 10x2, SMT	NPPC102KFMS-RC	Sullins Connector Solutions		

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate PartNumber	Alternate Manufacturer
J6	1		DC POWER JACK, R/A, TH	DC POWER JACK, R/A, TH	PJ-102AH	CUI Inc.		
J7	1		Header (Shrouded), 5.08 mm, 2x1, Tin, R/A, TH	Header, 5.08 mm, 2x1, R/A, TH	1757242	Phoenix Contact		
J8, J10	2		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
J9	1		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
J11	1			HDR2	1757019	Phoenix Contact		
L1	1	47uH	Inductor, Shielded Drum Core, Metal Composite, 47 uH, 0.74 A, 0.5 ohm, SMD	SMD	7447785147	Wurth Elektronik		
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady		
MP1, MP2, MP3, MP4, MP5	5		Round Standoff Threaded M2.5x0.45 Steel 0.276" (7.00mm)	SPACER_RADIAL_M2	9774070151R	Wurth Electronics		
MP6, MP7, MP8, MP9, MP10	5		M2.5x0.45 Pan Head Machine Screw Slotted Drive Steel	SCREW_M2.5	29300	Keystone Electronics		
Q1_1, Q1_2, Q1_3, Q1_4, Q1_5, Q1_6, Q1_7, Q1_8	8	60 V	Transistor, NPN, 60 V, 0.9 A, SOT-23	SOT-23	PBSS4160T	NXP Semiconductor		
Q2	1	100V	MOSFET, N-CH, 100 V, 50 A, DQG0008A (VSON-CLIP-8)	DQG0008A	CSD19537Q3	Texas Instruments		None
Q3	1	50V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor		None
R1_1, R1_2, R1_3, R1_4, R1_5, R1_6, R1_7, R1_8	8	1.21k	Surface Mount MELF Resistor, 1.21 kohm, 200 V, 250 mW, 1%, Thin Film ,AEC-Q200	0204	SMM02040C1211FB300	Vishay		

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R2_1, R2_2, R2_3, R2_4, R2_5, R2_6, R2_7, R2_8, R9, R13, R16, R18, R22, R25, R27, R28, R29, R31, R45	19	10k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0JNED	Vishay-Dale		
R3_1, R3_2, R3_3, R3_4, R3_5, R3_6, R3_7, R3_8	8	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R4_1, R4_2, R4_3, R4_4, R4_5, R4_6, R4_7, R4_8	8	240	RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402240RJNED	Vishay-Dale		
R5_1, R5_2, R5_3, R5_4, R5_5, R5_6, R5_7, R5_8, R6_1, R6_2, R6_3, R6_4, R6_5, R6_6, R6_7, R6_8, R30, R48, R63, R65, R66	21	4.99k	RES, 4.99 k, 1%, 0.063 W, 0402	0402	RC0402FR-074K99L	Yageo America		
R7_1, R7_2, R7_3, R7_4, R7_5, R7_6, R7_7, R7_8, R38	9	49.9k	RES, 49.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040249K9FKED	Vishay-Dale		
R8, R10, R17, R19, R39, R40, R43, R46, R49, R55, R61	11	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America		
R11, R20	2	3.32k	RES, 3.32 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K32FKED	Vishay-Dale		
R12, R21	2	1.40k	RES, 1.40 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K40FKED	Vishay-Dale		
R32	1	24.3k	RES, 24.3 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040224K3FKED	Vishay-Dale		
R33	1	887k	RES, 887 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402887KFKED	Vishay-Dale		
R34	1	499k	RES, 499 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402499KFKED	Vishay-Dale		
R35	1	68.1k	RES, 68.1 k, 1%, 0.063 W, 0402	0402	RC0402FR-0768K1L	Yageo America		
R36	1	29.4k	RES, 29.4 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040229K4FKED	Vishay-Dale		

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R37	1	34.0k	RES, 34.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040234K0FKED	Vishay-Dale		
R41	1	3.57k	RES, 3.57 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K57FKED	Vishay-Dale		
R42	1	19.6k	RES, 19.6 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040219K6FKED	Vishay-Dale		
R44, R50, R51	3	100k	RES, 100 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100KFKED	Vishay-Dale		
R53	1	43.2k	RES, 43.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040243K2FKED	Vishay-Dale		
R56, R57, R58, R59, R60	5	33.0	RES, 33.0, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT33R0	Stackpole Electronics Inc		
R62	1	25.0k	RES, 25.0 k, 0.1%, 0.05 W, 0402	0402	PNM0402E2502BST1	Vishay-Dale		
R64	1	4.99k	RES, 4.99 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04024K99FKED	Vishay-Dale		
S1	1		SWITCH TACTILE SPST-NO 0.05A 12V	3x1.6x2.5mm	B3U-1000P	Omron Electronic Components		
SH-J1, SH-J2	2		Shunt, 2.54mm, Gold, Black	Shunt, 2.54mm, Black	60900213421	Wurth Elektronik		

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate PartNumber	Alternate Manufacturer
TP1_1, TP1_2, TP1_3, TP1_4, TP1_5, TP1_6, TP1_7, TP1_8, TP2_1, TP2_2, TP2_3, TP2_4, TP2_5, TP2_6, TP2_7, TP2_8, TP3_1, TP3_2, TP3_3, TP3_4, TP3_5, TP3_6, TP3_7, TP3_8, TP4_1, TP4_2, TP4_3, TP4_4, TP4_5, TP4_6, TP4_7, TP4_8, TP5_1, TP5_2, TP5_3, TP5_4, TP5_5, TP5_6, TP5_7, TP5_8, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40	75		Test Point, SMT	Test Point, SMT	S2751-46R	Harwin		
U1_1, U1_2, U1_3, U1_4, U1_5, U1_6, U1_7, U1_8	8		IO-Link Device Transceiver with Low Residual Voltage and Integrated Surge Protection	VSON10	TIOL112DRCR	Texas Instruments		
U2, U4	2		40-V, 160-m? Quad-Channel Industrial Smart High-Side Switch	WQFN28	TPS274160BRLHR	Texas Instruments		
U3, U5, U8	3		Low-Power, Rail-to-Rail In and Out, 1-MHz Operational Amplifier, DCK0005A (SOT-SC70-5)	DCK0005A	TLV9001IDCKT	Texas Instruments	TLV9001IDCKR	Texas Instruments

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate PartNumber	Alternate Manufacturer
U6	1		Low-Voltage 24-Bit I2C and SMBus I/O Expander, 24 Outputs, 1.65 to 5.5 V, -40 to 85 degC, 32-pin UQFN (RGJ), Green (RoHS & no Sb/Br)	RGJ0032A	TCA6424ARGJR	Texas Instruments		
U7	1		4.5V - 60V, 6A 29m? eFuse with Reverse Polarity Protection, RGE0024H (VQFN-24)	RGE0024H	TPS26631RGET	Texas Instruments	TPS26631RGER	Texas Instruments
U9	1		LMR36503/06-Q1 Wide Input 60-V Synchronous, DC-DC Buck Converter, RPE0009A (VQFN-9)	RPE0009A	LMR36503RFRPET	Texas Instruments	LMR36503RFRPER	Texas Instruments
U10	1		8 input, wide 10-34V digital-input serializer for industrial digital inputs, PWP0028E (TSSOP-28)	PWP0028E	SN65HVS883PWP	Texas Instruments		Texas Instruments
U11, U12, U13	3		Single Buffer/Driver With Open-Drain Output, DRY0006A (USON-6)	DRY0006A	SN74LVC1G07DRYR	Texas Instruments		

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