Using the TPS51103EVM Integrated 3.3-V/5-V Power LDO with Clock Output

This document includes information regarding absolute operating conditions, power-supply requirements, and hardware configuration for the evaluation module. The electrical schematics and bill of materials are also included for reference purposes. Throughout this document, the phrase *evaluation module* and the abbreviation *EVM* are both synonymous with the TPS51103EVM.

Contents

List of Figures

List of Tables

1 Introduction

The TPS51103EVM evaluation module (EVM) is an integrated power LDO solution platform for testing and evaluation of the TPS51103, an integrated LDO with switch-over circuit for notebook computers (TI Literature Number SLUS808) The EVM delivers 3.3-V and 5-V of output voltage at 100 mA. It also produces an *always-on* 3.3-V low-dropout (LDO) output at 5 mA.

1.1 Description

The EVM generates 3.3-V and 5-V LDO output from a wide input range of 5.5 V to 28 V. The rated current for each output is 100 mA. The EVM also delivers an *always-on* 3.3-V, 5 m-A output. The glitch-free switchover function offers better system efficiency under light load conditions. When the switchover function is enabled, the LDO load is supplied by an external input source that eliminates the power loss generated as a result of the voltage drop across the LDO. A 250-kHz clock is generated for the charge pump feature. The clock is enabled when 5VIN is greater than 2 V. On the EVM, 15V_OUT is generated by a charge pump and is only available when 5VIN is applied and the 250-kHz clock is generated.

1.2 Applications

- Computing power, including notebooks and servers
- Networking equipment
- Telecommunications equipment
- Distributed dc power systems
- Broad market

1.3 Features

- 5.5-V to 28-V wide input range
- 3.3-V/5-V, 100-mA LDO output with enable
- *Always-on* 3.3-V LDO output at 5 mA
- 250-kHz clock output for charge pump
- Glitch-free switchover circuit

2 TPS51103EVM Electrical Performance Specifications

Table 1. Electrical Performance Specifications

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		5.5		28	V
OUTPUT1 (5V_OUT)						
	Output voltage			5		V
	Load regulation	0 A < I_{OUT1} < 100 mA, V_{IN} = 12 V			5%	
	Output load current	I_{OUT1}	0		100	mA
	Output overcurrent			160		
OUTPUT1 (3.3V_OUT)						
	Output voltage			3.3		V
	Load regulation	0 A < I_{OUT2} < 100 mA, V_{IN} = 12 V			5%	
	Output load current		0		100	mA
	Output overcurrent			150		
OUTPUT1 (3.3V_RTC)						
	Output voltage			3.3		V
	Load regulation	0 A < I_{OUT3} < 5 mA, V_{IN} = 12 V			5%	
	Output load current	I_{OUT3}	0		5	mA
OUTPUT1 (15V_OUT)						
	Output voltage			12		V
	Output load current		0		10	mA

3 Schematic

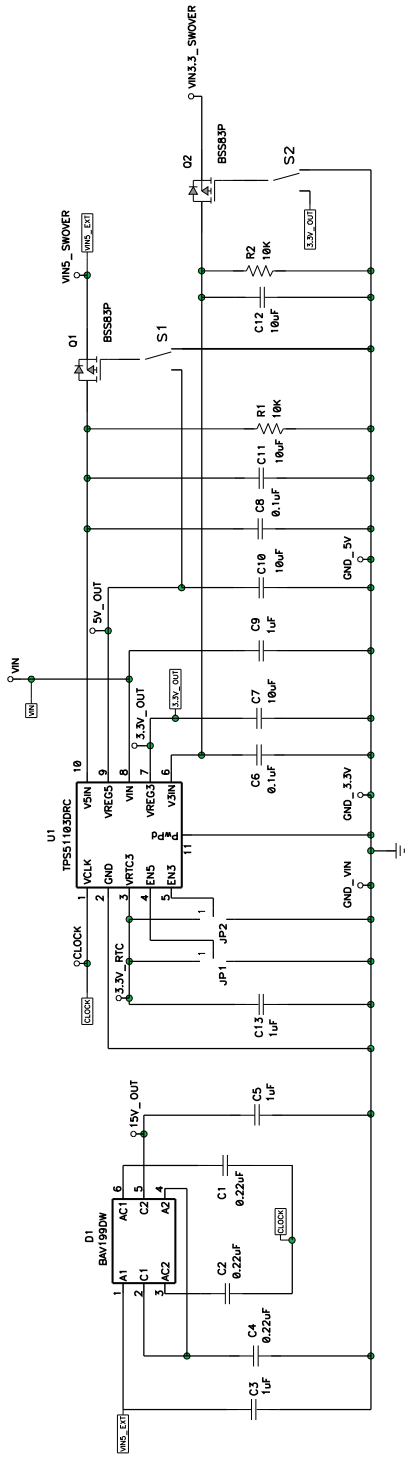

Figure 1. TPS51103EVM Power Stage/Control Schematic

Note: For reference only; see the enclosed Bill of Materials for specific values.

4 Test Setup

4.1 Recommended Test Equipment

4.1.1 Voltage Source

4.1.1.1 V_{IN}

The input voltage source, V_{IN}, should be a variable dc source, capable of 1-A dc, between 0 V and 30 V. Connect V_{IN} as shown in Figure 2.

4.1.1.2 VIN5

This voltage source is applied only when the switchover function is tested. The voltage source should be a variable dc source, capable of 1-A dc, between 0 V and 6 V .

4.1.1.3 VIN3.3

This voltage source is applied only when the switchover function is tested. The voltage source should be a variable dc source, capable of 1-A dc, between 0 V and 6 V.

4.1.2 Meters

Table 2. Meters

NODE	SOURCE	VOLTMETER RANGE (V)
V1	VIN	0-30
V2	VIN5	0-6
V3	VIN3.3	
V4	5V_OUT	
V5	3.3V_OUT	
V6	3.3V_RTC	
V7	15V_OUT	0-20

4.1.3 Loads

Either electronic load resistors or adjustable resistors can be used.

4.2 Equipment Setup

4.2.1 Electrostatic Discharge Warning

CAUTION

Failure to observe proper ESD handling procedures may result in damage to the EVM components.

Many of the components used in the assembly of the TPS51103EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling procedures when unpacking and handling the TPS51103EVM. All handling should be performed at an approved ESD workstation or test bench, using a grounded wrist strap. Failure to observe proper handling procedures may result in damage to EVM components. An electrostatic smock and safety glasses should also be worn.

4.2.2 Input Connections

Figure 2 shows the recommended test setup to evaluate the TPS51103EVM.

Before connecting the dc input sources, make sure that all sources are initially set to 0 V and connected as shown in Figure 2.

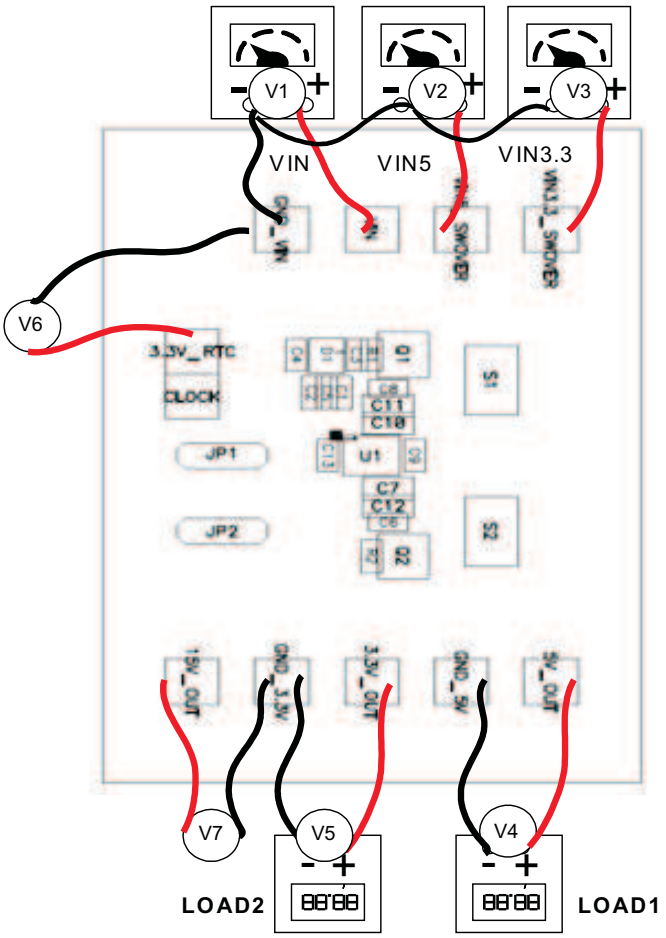

Figure 2. TPS51103EVM Recommended Test Setup

4.2.3 Output Connections

Configure the output connections in the following order.

Step 1. Connect LOAD1 and LOAD2 to 5V_OUT and 3.3V_OUT, respectively. Set LOAD1 and LOAD2 to sink 0 A dc before V_{IN} is applied.

Step 2. Connect voltmeters V4-V7 as shown in Figure 2.

4.3 Startup and Test Procedure

1. Ensure that LOAD1 and LOAD2 are set to constant current mode and to sink 0 A dc.
2. Increase V_{IN} (V1) from 0 V to 10 V dc. 5V_OUT (V4), 3.3V_OUT (V5), and 3.3V_RTC (V6) should correspond to the specifications shown in Table 1.
3. Vary the LOAD of 5V_OUT and 3.3V_OUT from 0 mA dc to 100 mA dc. 5V_OUT and 3.3V_OUT should remain within the specifications given Table 1 for all load combinations on LOAD up to 100 mA.
4. Vary V_{IN} from 5.5 V dc to 28 V dc. 5V_OUT (V4), 3.3V_OUT (V5), and 3.3V_RTC (V6) should correspond to the specifications shown in Table 1.
5. Keep V_{IN} at 12 V. Increase VIN5 (V2) to 5.5 V; then toggle switch S1 as shown in the following EVM configuration to enable a 5-V switchover function. Measure 5V_OUT (V4) at a no load condition; V4 should be very close to V2. Measure 15V_OUT (V7) at a no load state; it should be within the limits given in Table 1.
6. Keep V_{IN} at 12 V. Increase VIN3.3 (V3) to 3.5 V, and toggle switch S2 as shown in the following EVM configuration to enable a 3.3-V switchover function. Measure 3.3V_OUT (V5) at a no load condition; V5 should be very close to V3.

4.4 Evaluation Module Configuration

By default, the switchover function is disabled. To enable the switchover function, simply toggle switches S1 and S2 for a 5-V and 3.3-V switchover, respectively. The position of the switch is opposite of the pins shorted.

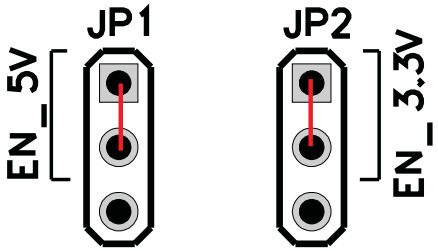

Figure 3. 5-V and 3.3-V Enable Configuration

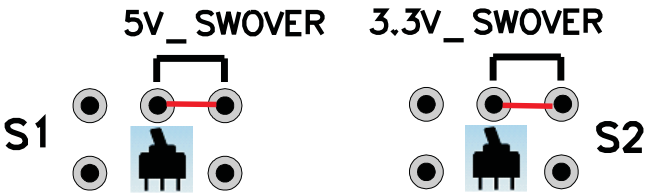

Figure 4. Switchover Function Enabled

4.5 Test Points

Several test points are located around the board. Table 3 lists these various test points and the respective uses of each.

Table 3. Test Points

TEST POINT LABEL	DESCRIPTION
VIN	Input voltage positive sense point
GND_VIN	Input voltage negative sense point
VIN5	5-V input voltage for switch over
VIN3.3	3.3-V input voltage for switch over
5V_OUT	5-V LDO output positive sense point
GND_5V	5-V LDO output negative sense point
3.3V_OUT	3.3-V LDO output positive sense point
GND_3.3V	3.3-V LDO output negative sense point
15V_OUT	Charge pump output positive sense point
3.3V_RTC	3.3-V LDO output for real time clock
CLOCK	250-kHz clock for charge pump

4.6 Equipment Shutdown

Follow these procedures to properly shut down the EVM.

Step 1. Shut down LOAD.

Step 2. Shut down all input voltage sources.

Step 3. Restore the default positions of all switches.

5 Typical Characteristics

5.1 Load Regulation

Figure 5 through Figure 16 present typical performance graphs for the TPS51103EVM. Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference only and may differ from actual field measurements.

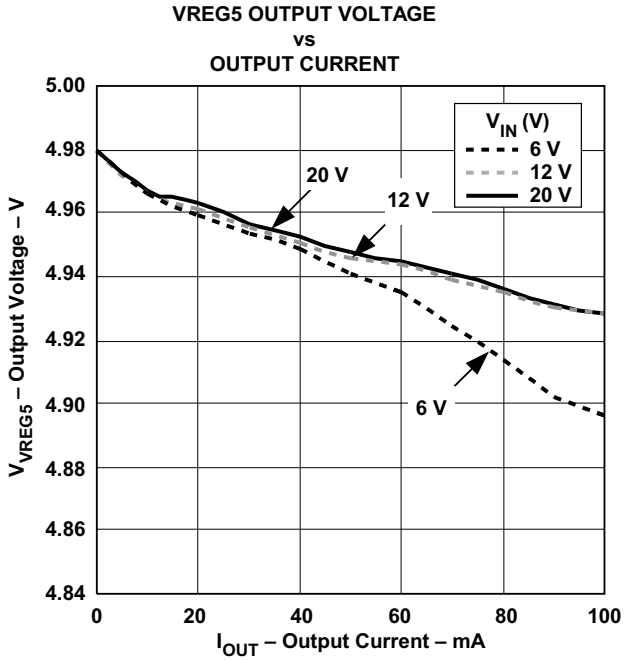

Figure 5. VREG5 Load Regulation

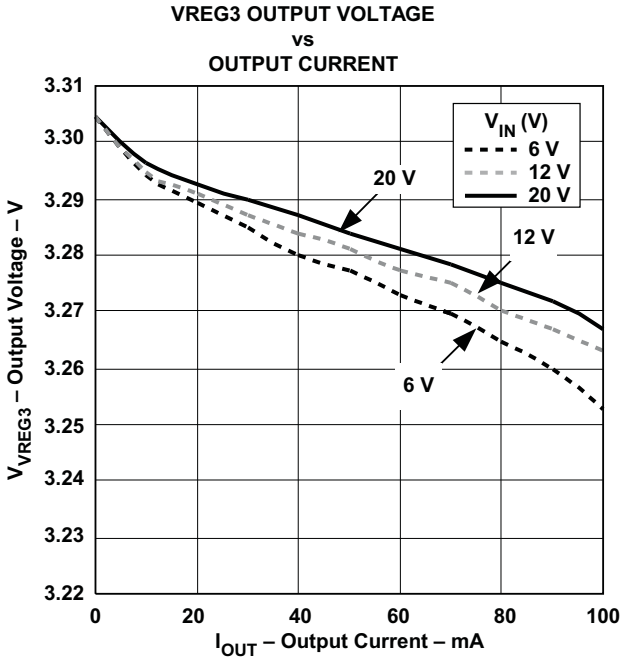

Figure 6. VREG3 Load Regulation

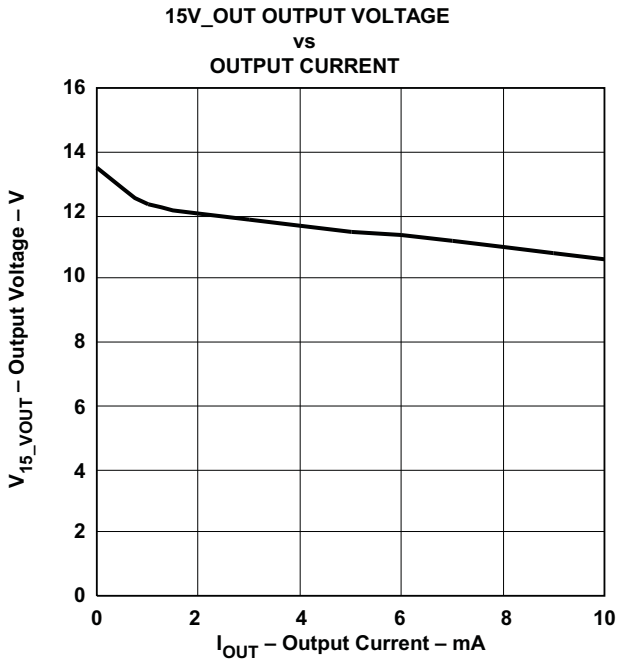

Figure 7. 15V_OUT Load Regulation

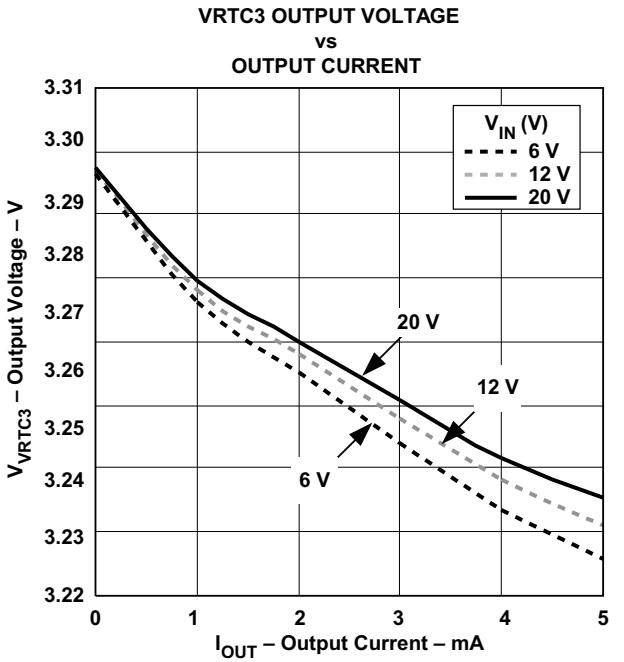

Figure 8. VRTC3 Load Regulation

5.2 Transient Response

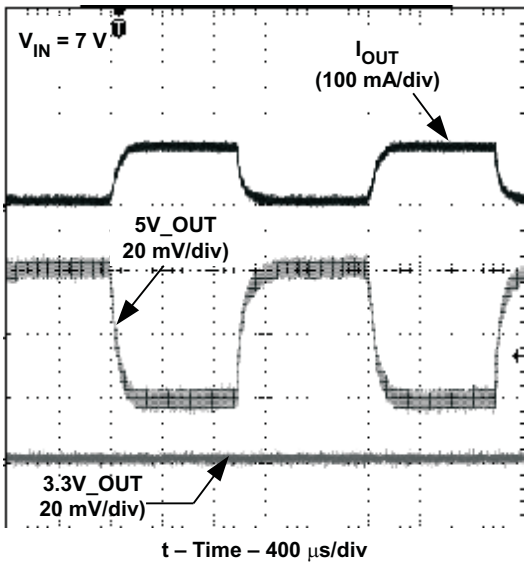

Figure 9. 0-mA to 100-mA Load Step on 5-V Output

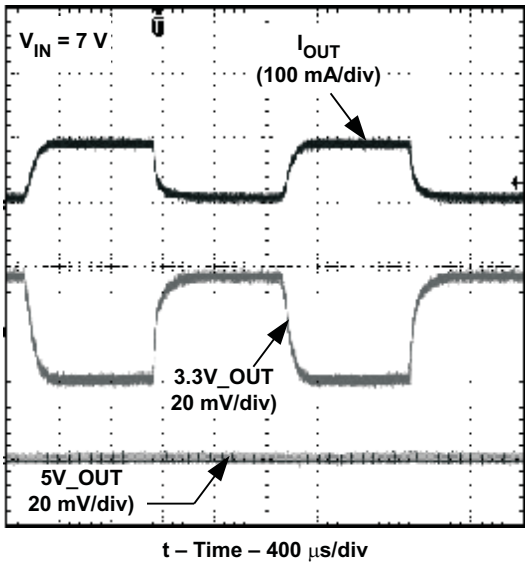

Figure 10. 0-mA to 100-mA Load Step on 3.3-V Output

5.3 Switchover Function

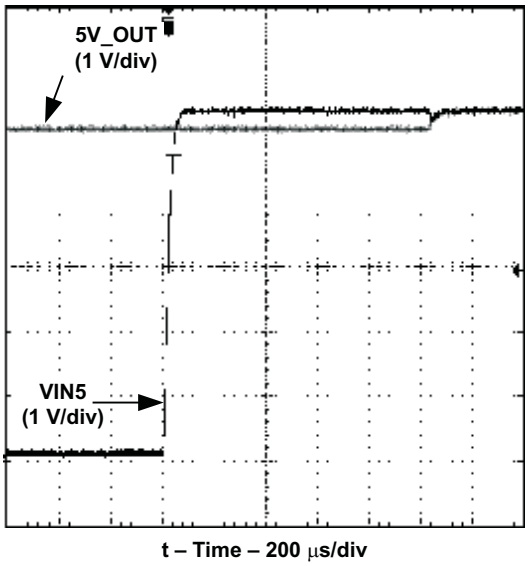

Figure 11. 5.0-V Switch Over

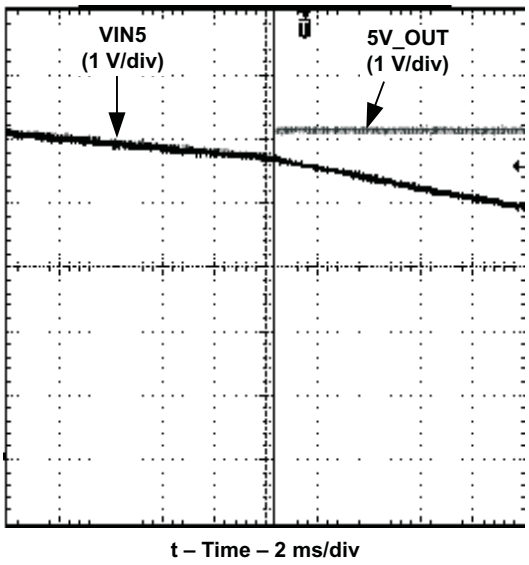

Figure 12. 5.0-V Switch Over

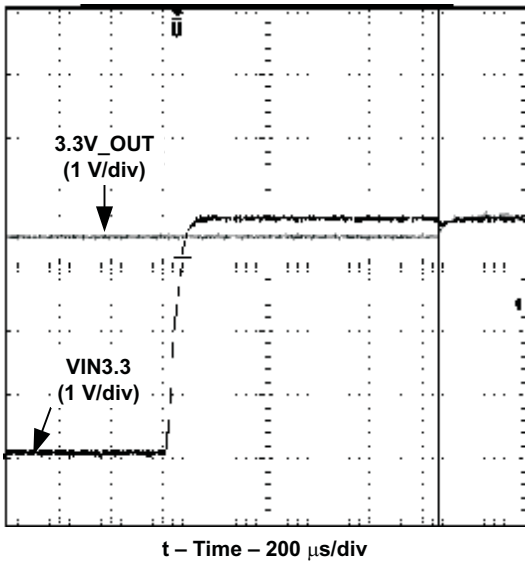

Figure 13. 3.3-V Switch Over

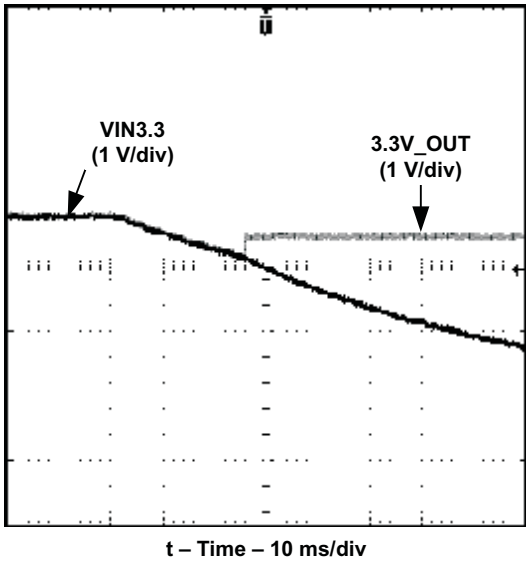

Figure 14. 3.3-V Switch Over

5.4 Clock and 15V_OUT

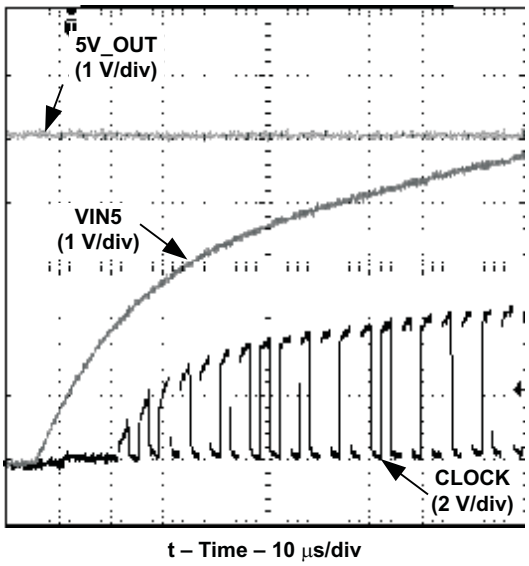

Figure 15. Clock Startup

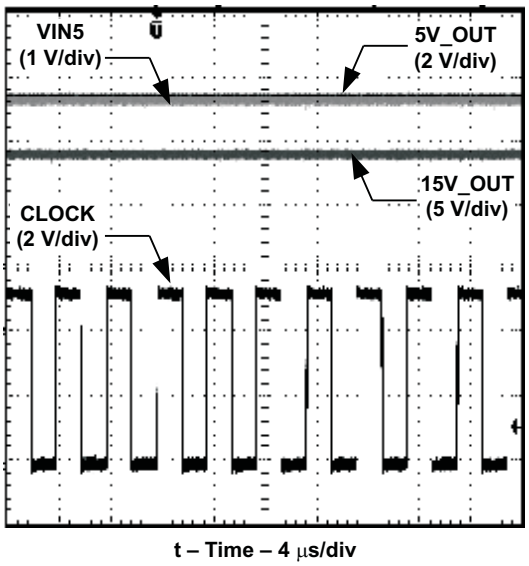

Figure 16. Clock Steady

6 EVM Assembly Drawings and Layout

Figure 17 through Figure 19 show the design of the TPS51103EVM printed circuit board (PCB). This EVM was designed using a two-layer, 2-oz. copper-clad PCB with all components on the top side to allow the user to easily view, probe, and evaluate the TPS51103 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space constrained systems.

Note: Board layouts are not to scale. These drawings are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS51103EVM PCBs.

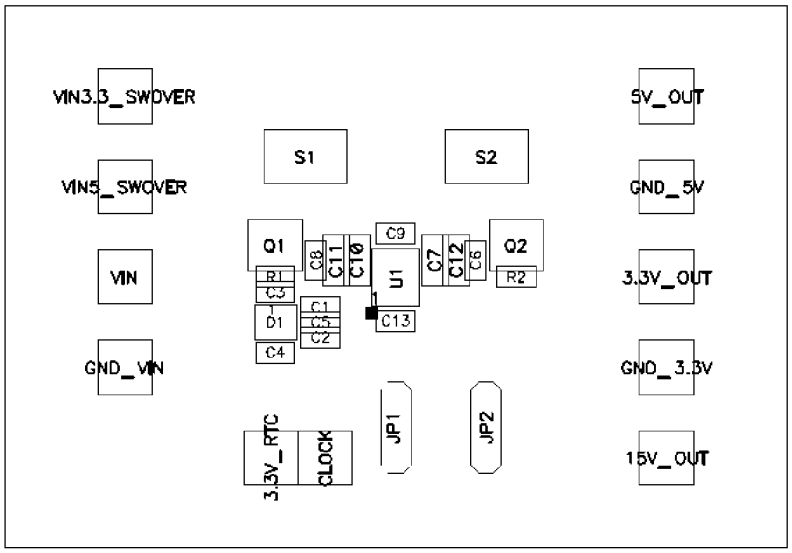

Figure 17. TPS51103EVM Component Placement (Top View)

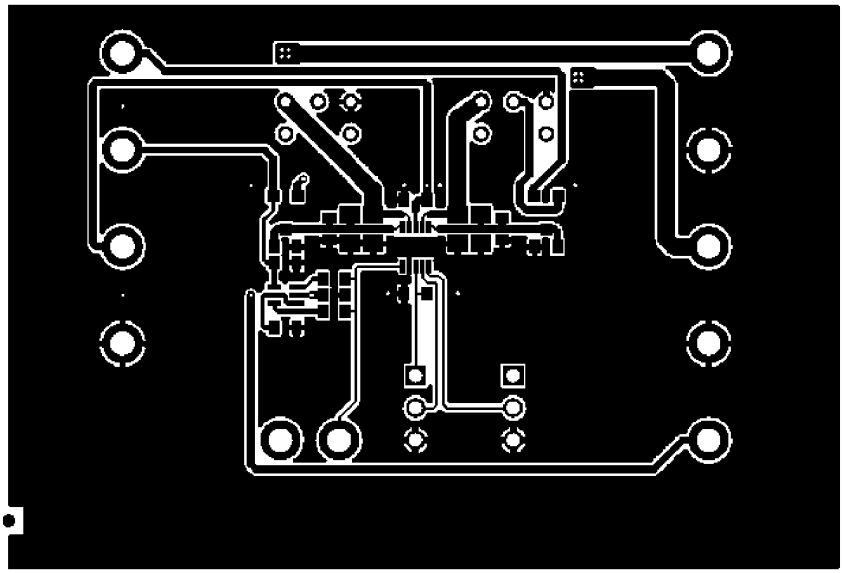

Figure 18. TPS51103EVM Top Copper (Top View)

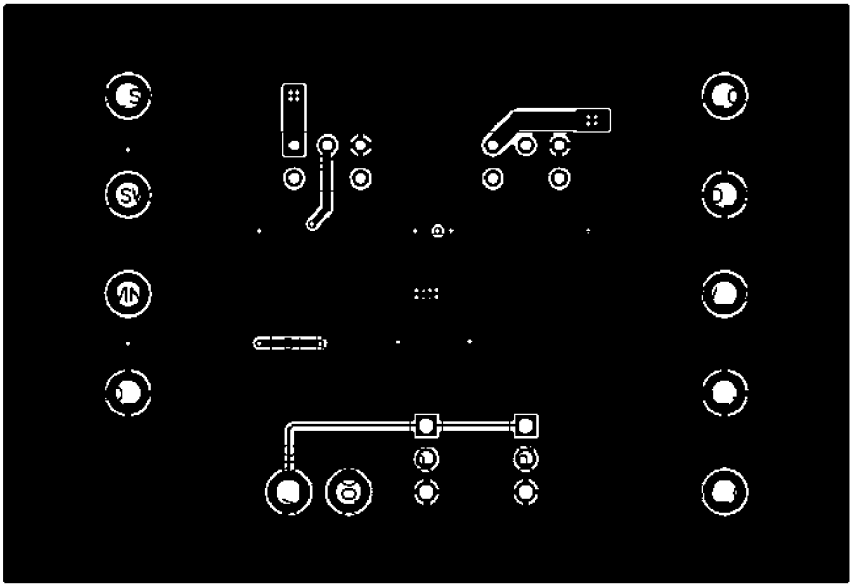

Figure 19. TPS51103EVM Bottom Copper (X-Ray View from Top)

7 Bill of Materials

Table 8. TPS51103EVM Bill of Materials

REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
R1, R2	10 kΩ	Resistor, Chip, 1/16w, 1%	603	std	std
	3138-2	Pin, Wiring Terminal	0.09(D) X 0.31 inch	3138-2-00-15-00-00-080	Mill Max
C1, C2, C4	0.22 µF	Capacitor, Ceramic, 50 V, X7R, ±10%	0603	std	std
C3, C5, C9, C13	1 µF	Capacitor, Ceramic, 25 V, X5R, ±10%	0603	std	std
C6, C8	0.1 µF	Capacitor, Ceramic, 50 V, X7R, ±10%	0603	std	std
C7, C10, C11, C12	10 µF	Capacitor, Ceramic, 10 V, X5R, ±20%	0805	std	std
D1	BAV199DW	Diode, Quad Low Leakage, 160-mA, 85-V	SOT363	BAV199DW	Diodes
JP1, JP2		Header, 3-pin, 100-mil spacing, (36-pin strip)	0.100 x 3 inch	PTC36SAAN	Sullins
Q1, Q2		MOSFET, P-channel, -60 V, -0.33 A, 2 Ω	SOT23	BSS83P	Infineon
		MOSFET, P-channel, -12 V, -0.75 A, 0.18 Ω	SOT23	BSH205	NXP
S1, S2	G12AP	Switch, ON-ON Mini Toggle	0.28 x 0.18 inch	G12AP	NKK
U1		IC, Integrated Power LDO	DGS10	TPS51103DRC	TI
	2-382811-1	Jumper, 0.1-in, 2 contacts		2-382811-1	Tyco/AMP

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of xxx V to xxx V and the output voltage range of xxx V to xxx V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than xxx C. The EVM is designed to operate properly with certain components above xxx C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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