UCC5870QDWJEVM-026 Evaluation Module User's Guide

The evaluation module is designed for evaluation of TI's functional safety compliant 15-A isolated single-channel gate driver UCC5870-Q1 with advanced protection functions. This EVM is targeted to drive high power SiC MOSFETs or Si IGBTs in EV/HEV applications. Protection functions such as DESAT short circuit protection, shunt current sensing support, soft turn-off, VCE overvoltage clamping, UVLO and OVLO of gate driver power supplies, temperature monitoring and thermal shutdown, and gate monitoring are included to support system's demanding high reliability. This driver also incorporates sophisticated diagnostic, protection, and monitoring features through a serial peripheral interface (SPI).

The UCC5870-Q1 evaluation module also includes a MCU daughter board to support SPI communication and program the UCC5870-Q1, a dedicated GUI is developed for configuring and evaluating UCC5870-Q1. This evaluation module has pin outputs that support the 820A 750V IGBT module FS820R08A6P2B connection for high power double pulses test and short circuit test.

Contents

List of Figures

List of Tables

Trademarks

1 General TI High Voltage Evaluation User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you must immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area .
  - Qualified observer(s) must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50 V_{RMS}/75 VDC must be electrically located within a protected Emergency Power Off (EPO) protected power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**

  As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
  - De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

  WARNING: While the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.
- **Personal Safety:**
  - Wear personal protective equipment, for example, latex gloves and/or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training, and is designed to operate from an AC power supply or a high-voltage DC supply. Please read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

⚠

Do not leave the EVM powered when unattended.

WARNING

⚠

High Voltage! Electric shock is possible when connecting board to live wire. Board must be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

2 Description

The UCC5870-Q1 evaluation kit can be used standalone to test the UCC5870-Q1 driver with 100-nF capacitor dummy load soldered on the board, it can also be used to drive IGBT module directly for high power test. The MCU daughter board is populated with 3-position headers for flexibility in configuring different SPI communication methods. The EVM PCB layout is optimized with minimal loop area in the input and output paths for the best performance of high power test.

2.1 Features

- 15-A peak split sink/source drive current for fast turn ON and turn OFF time
- Driver output voltages by default are +15V/-8V with 12-V input supply
- 3750-V_{RMS} one minute isolation per UL 1577 for UCC5870-Q1
- 3000-V_{RMS} one minute isolation for the flyback transformer
- > 8-mm creepage distance between primary and secondary
- Desat short-circuit protection and active Vce clamp
- Active miller clamp using internal or external FET
- Fault feedback and reset
- ADC for temperature sensing and DC bus voltage sensing
- Primary and secondary ASC
- SPI based device reconfiguration, verification, supervision and diagnosis
- Compatible with 820A 750V IGBT module FS820R08A6P2B

2.2 I/O Description

Table 1. I/O Description

PINS	DESCRIPTION
TP–1	+12V supply
TP–2	Primary GND1 input
TP–3	+4.5V supply
TP–4	Primary GND1 input
TP–5	Test point for gate (use for low voltage test only)
TP–6	Test point for source (use for low voltage test only)
TP–7	Driver VCC2 input (use for low voltage test only)
TP–8	Driver secondary GND2 input (use for low voltage test only)
TP–9	Driver VEE2 input (use for low voltage test only)
J1	C2 of the IGBT module (use for high voltage test only)
J2	G2 of the IGBT module (use for high voltage test only)
J3	T11 of the IGBT module (use for high voltage test only)
J4	T12 of the IGBT module (use for high voltage test only)
J5	E2 of the IGBT module (use for high voltage test only)
J6	C1 of the IGBT module (use for high voltage test only)
J7	G1 of the IGBT module (use for high voltage test only)
J8	E1 of the IGBT module (use for high voltage test only)
J9	Connector for MCU daughter card
J17	Test pin (use for low voltage test only)
J18	Test pin (use for low voltage test only)
J19	Test pin (use for low voltage test only)
J20	Test pin (use for low voltage test only)
J21	Secondary ASC (use for low voltage test only)
J22	Test pin (use for low voltage test only)

Table 1. I/O Description (continued)

PINS	DESCRIPTION
J23	Test pin (use for low voltage test only)
J24	Primary ASC (use for low voltage test only)

2.3 Jumpers (Shunt) Options

Table 2. Jumpers Setting

JACK	Jumper Setting Options		FACTORY SETTING
J10	Option A:	Jumper on J10-1 and J10-2 set single input IN+ for the driver	Option A
	Option B:	Jumper on J10-2 and J10-3 set differential input IN+ /IN-for the driver	
J11	Option A:	Jumper on J11-1 and J11-2 set single input IN+ for the driver	Option A
	Option B:	Jumper on J11-2 and J11-3 set differential input IN+ /IN-for the driver	
J12	Option A:	Jumper on J12-1 and J12-2, connect 100-nF dummy load for the driver U4	Option A
	Option B:	Jumper not installed, without connecting 100-nF dummy load for the driver U4	
J13	Option A:	Jumper on J13-1 and J13-2, connect Vcc2 to the flyback supply output for the driver U4	Option A
	Option B:	Jumper not installed, use external supply from TP7 for Vcc2 of the driver U4	
J14	Option A:	Jumper on J14-1 and J14-2, connect Vee2 to the flyback supply output for the driver U4	Option A
	Option B:	Jumper not installed, use external supply from TP7 for Vee2 of the driver U4	
J15	Option A:	Jumper on J14-1 and J14-2, connect Vcc1 to 3.3V for the driver U4	Option A
	Option B:	Jumper not installed, insert current sensor then connect with J15-1 and J15-2 to measure Icc1	
J16	Option A:	Jumper on J12-1 and J12-2, connect 100nF dummy load for the driver U5	Option A
	Option B:	Jumper not installed, without connecting 100nF dummy load for the driver U5	

3 Electrical Specifications

Table 3. UCC5870 EVM Electrical Specifications

DESCRIPTION		MIN	TYP	MAX	UNIT
V_{cc}	Primary-side power supply (TP1)	4.0		5.5	V
V_{supply}	Input for driver auxiliary power supply (TP3)	10	12	15	V
F_S	Switching frequency	0		50 (1)	kHz
V_{C1} ,V_{C2}	Voltage on C1 and C2 pins for high voltage test (J1, J6)		400	750	V
T_J	Operating junction temperature range	-40		150	°C

(1) 30kHz if ADC is used

4 Test Summary

In this section, the UCC5870-Q1 EVM is tested in its default configuration. Different jumper settings, PWM signal input options, and voltage source settings can be found in Section 2.3 Electrical Specifications.

4.1 Equipment

4.1.1 Power Supplies

Two DC power supply with voltage/current above 5-V/0.1-A and 35-V/0.5-A (for example: Agilent E3634A)

4.1.2 Computer

One computer with Windows system and UCC5870 EVM GUI installed

4.2 Equipment Setup

4.2.1 DC Power Supply Settings

- DC power supply #1
  - Voltage setting: 4.5-V, there is LDO circuit on the board which will regulate voltage to 3.3V for the driver VCC1
  - Current limit: 0.2-A
- DC power supply #2
  - Voltage setting: 12-V, as the input of the flyback power supply on the board
  - Current limit: 0.2 A

4.2.2 EVM GUI Program Installation

- UCC5870-Q1 EVM GUI program should be downloaded and installed. This software requires GUI Composer runtime v7.4.1. You can download it during the installation of this GUI software. Alternatively, you can get the runtime here: https://software-dl.ti.com/ccs/non-esd/gui_composer/runtime.

4.2.3 Jumper (Shunt) Settings

The are four jumpers need to be configured on the MCU board for different SPI communication methods which include regular SPI, daisy chain SPI and address mode SPI. Default setting as in Figure 1 is for regular SPI communication.

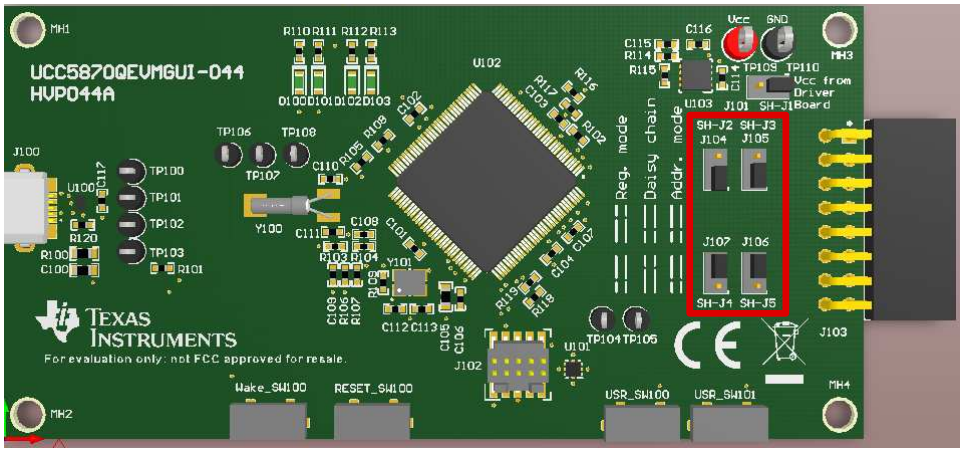

Figure 1. Default Jumper Settings for EVM MCU Daughter Board (Regular Mode SPI)

For testing with address mode or daisy chain mode SPI, the four jumper should be set as in Figure 2 left graph or right graph.

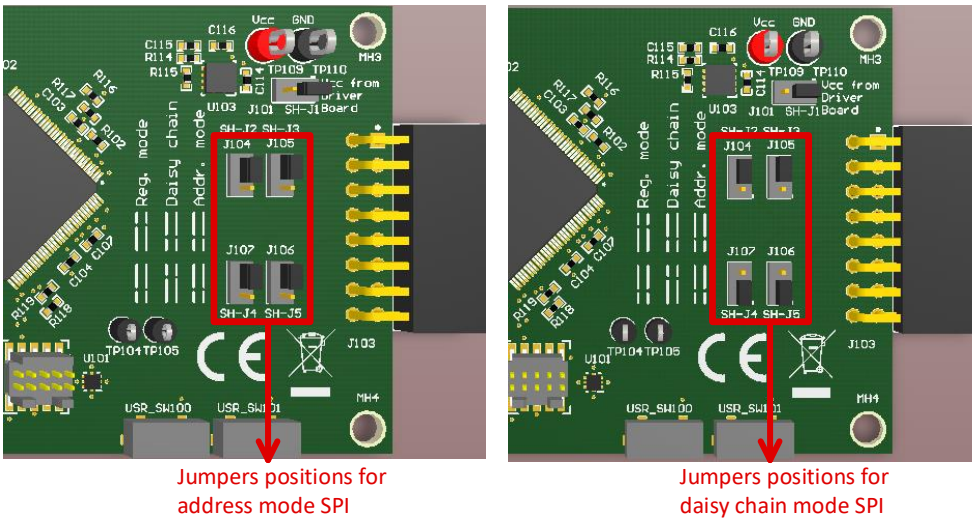

Figure 2. Jumper Settings for EVM MCU Daughter Board (Address Mode SPI and Daisy Chain Mode SPI)

For the EVM board, default jumper configuration as in Figure 3 should be adequate for this test. Shunt 12 and shunt 16 are connecting the driver outputs with 100-nF load separately. Shunt 10 and shunt 11 in the figure are setting up the driver with non-differential input, IN- pins are connected to GND1. The purpose of shunt 13, 14 and 15 is for measuring U4 (UCC5870) Vcc1, Vcc2 and Vee2 quiescent current if current meter can be inserted.

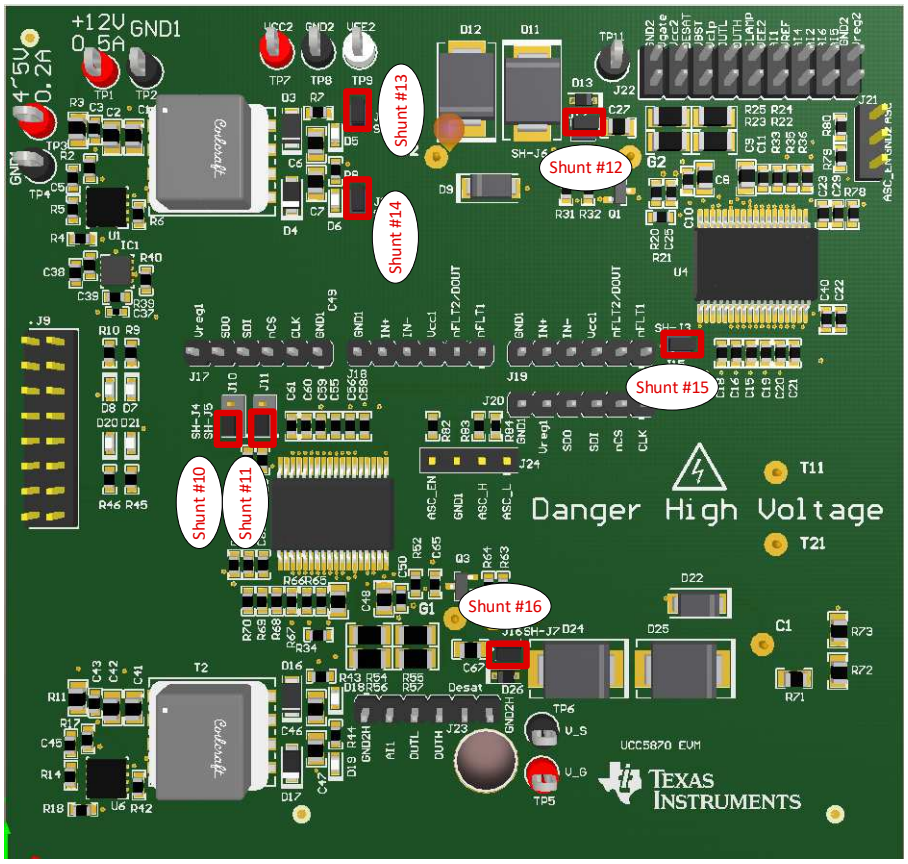

Figure 3. Default Jumper Settings for EVM Driver Board

4.2.4 Bench Setup For Low Voltage Test

The current bench setup includes power supplies, oscilloscope and GUI USB connections.

Follow the connection procedure below. Figure 4 can be used as a reference.

- Make sure the outputs of DC voltage power supplies are OFF before connection.
- Connect 4.5V power supply to TP3 for primary VCC1
- There are two options for the DC power supply connection for secondary power: 1) Option 1: connect +12V to TP1 as the input of the flyback power supply on the board; 2) Option 2: If only testing low side driver, connect +15V directly to VCC2, and 0V or -5V to VEE2; this gives the flexibility and driver voltage can be adjusted easily.
- Connect oscilloscope probes to corresponded test pins.
- Connect MCU daughter board to computer through USB cable.

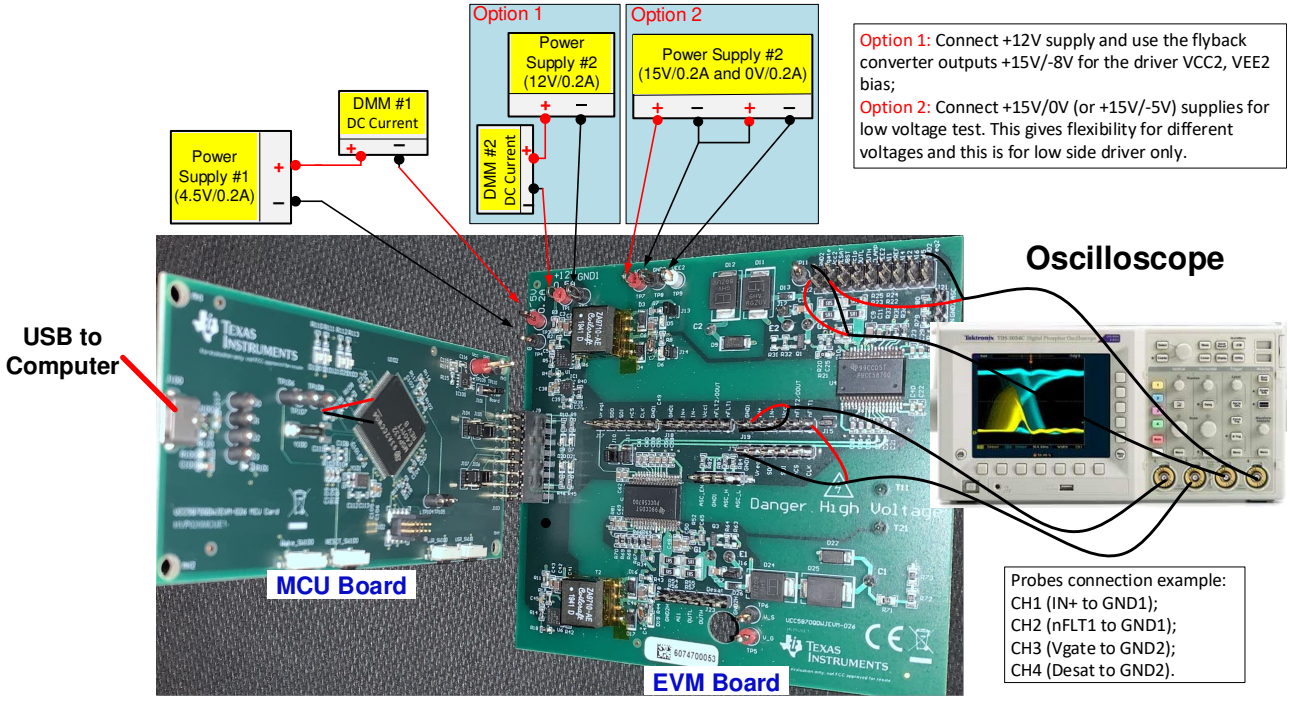

Figure 4. Low Voltage Bench Setup Configuration

The test points labels are all on the upside of the J22 due to the space limitation for the bottom side, the measured signal for each pin of J22 is illustrated as in Figure 5

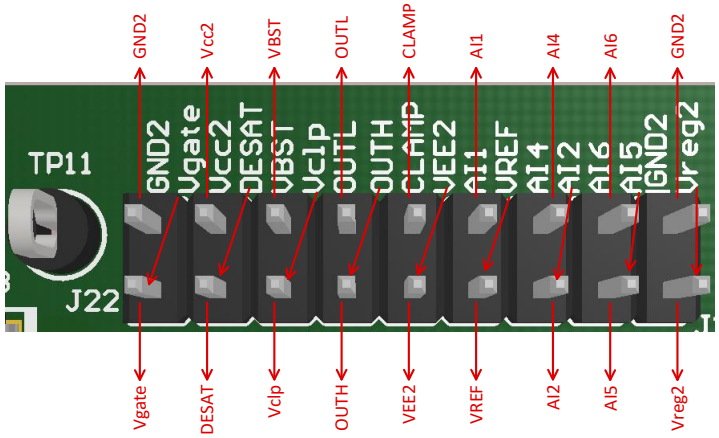

Figure 5. Test Points Labels for J22

5 Low Voltage Test Procedure Example

5.1 Power Up (C_L = 100 nF)

1. Before proceeding to the power up procedure, make sure that Section 4.2.4 is implemented for setting up all the equipment.
2. Enable all power supplies
3. Open the GUI, The home page should look like as Figure 6,The bottom pane should show 'Hardware Connected' after few seconds. In case it is not connected, Click 'Options' -> 'Serial port' and choose the appropriate serial port from the list of available ports.

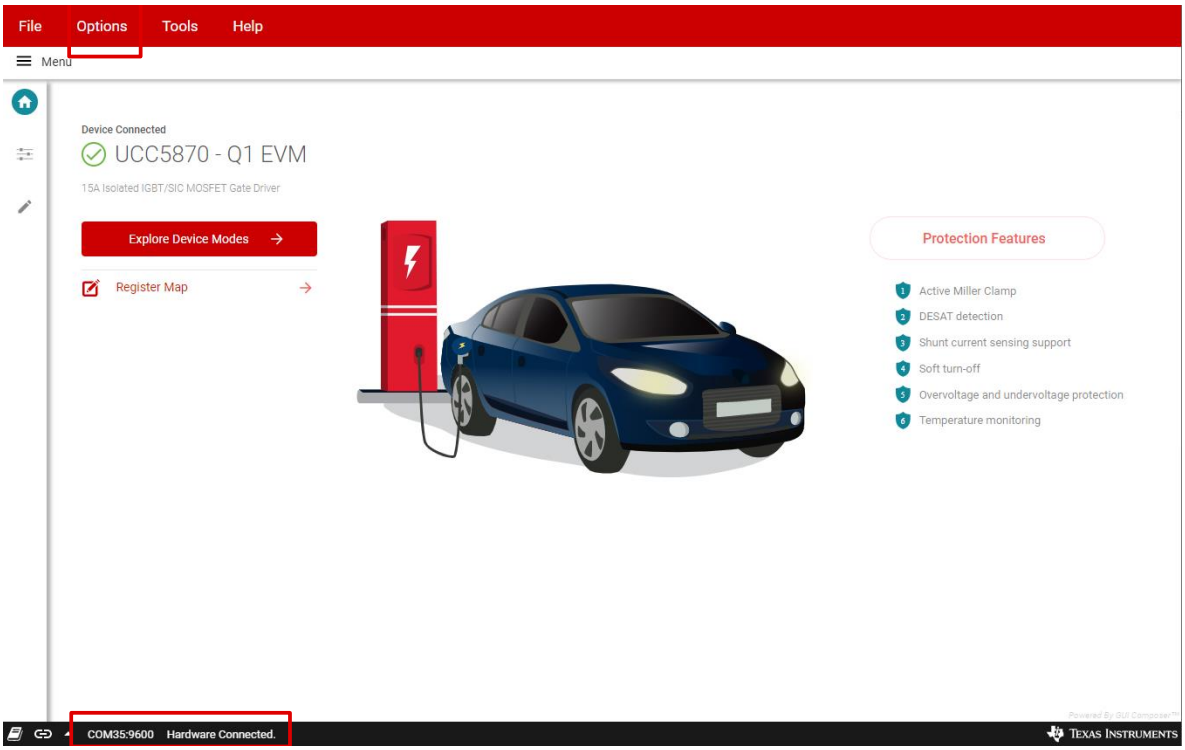

Figure 6. GUI First Page

4. Click "Explore the Device Modes", page as Figure 7 should appear, EVM number will be detected automatically, select SPI type: Regular SPI (Address base SPI can be selected if MCU board is configured for this mode) then click finish.

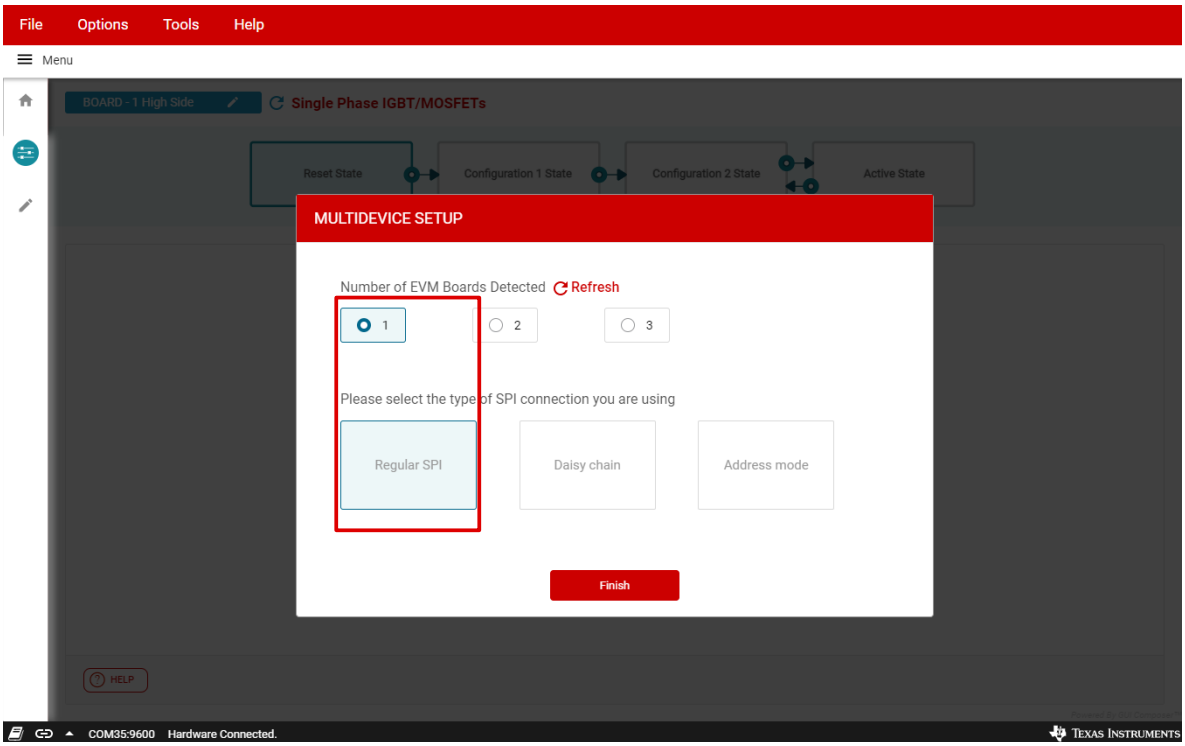

Figure 7. GUI EVM Number and SPI Mode Select

5. Select which driver (high side or low side) to program as in Figure 8

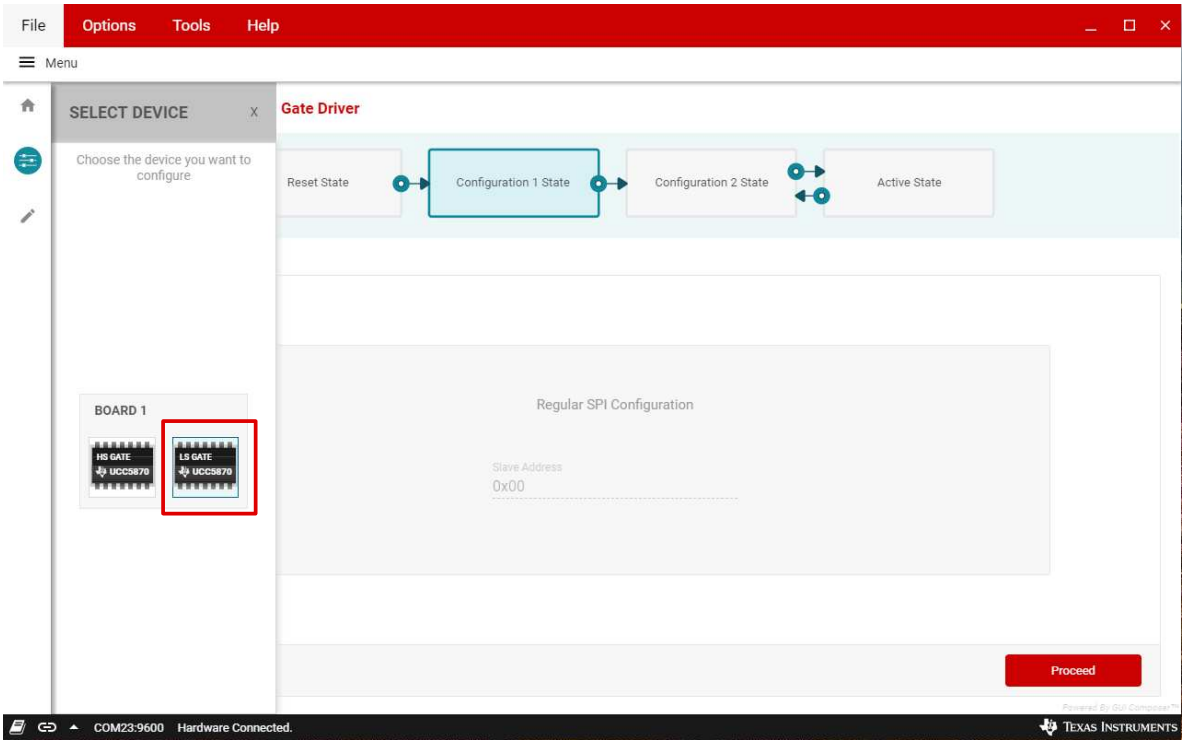

Figure 8. GUI High Side or Low Side Driver Selection

6. Then move to Configuration 1 State, GUI will assign address for each driver during this state if address based SPI mode is selected for the previous step, otherwise GUI has no action.

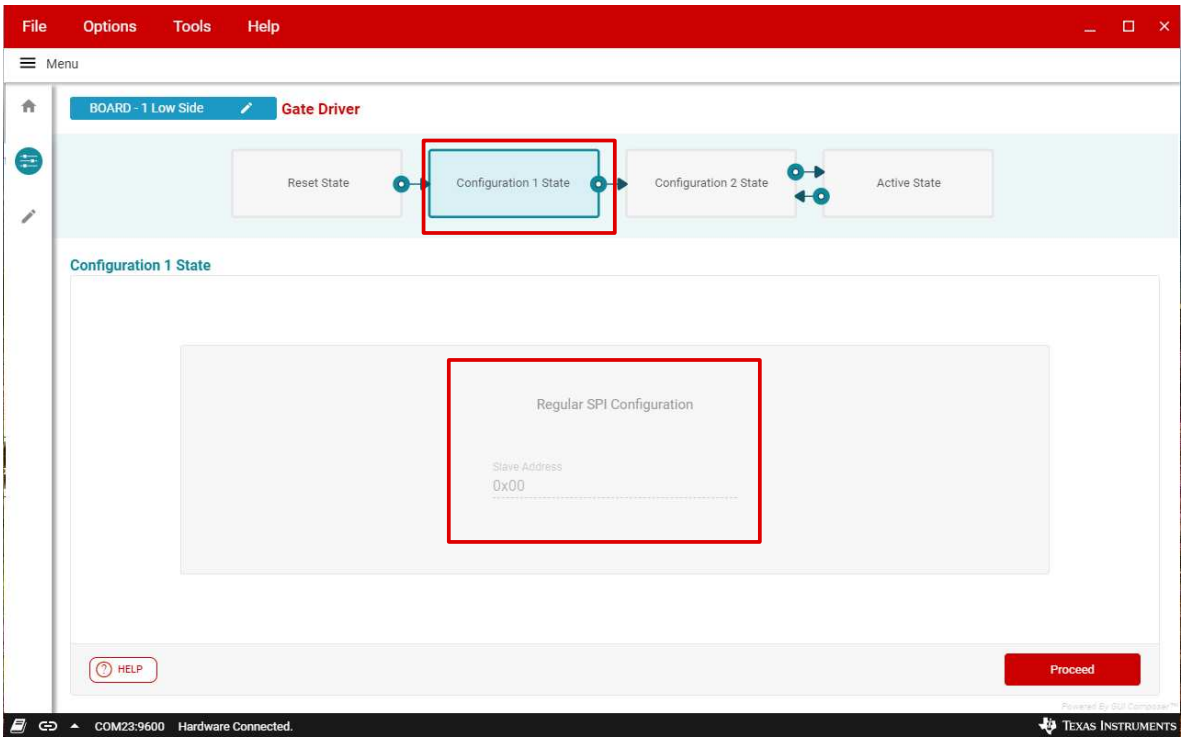

Figure 9. GUI Configuration 1

7. Move to Configuration 2 State in which the registers can be programmed.

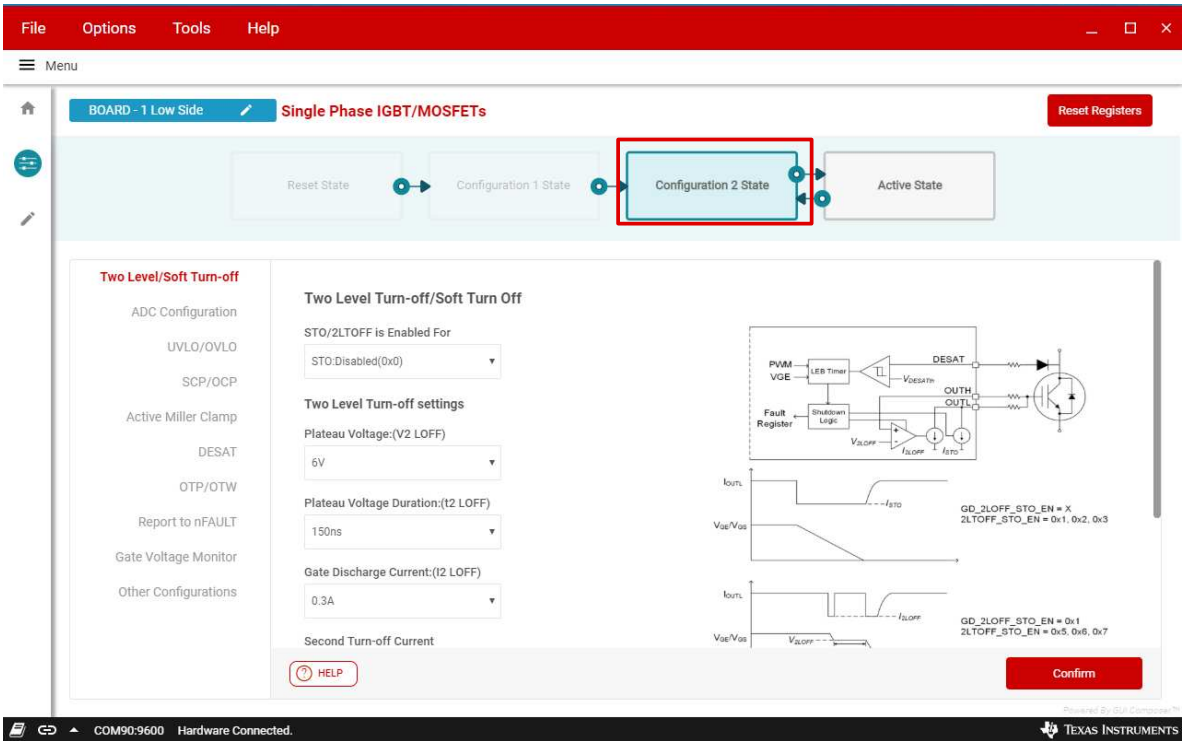

Figure 10. GUI Configuration 2

8. Before making any changes, go to "Register Map" and click " READ ALL REGISTERS".

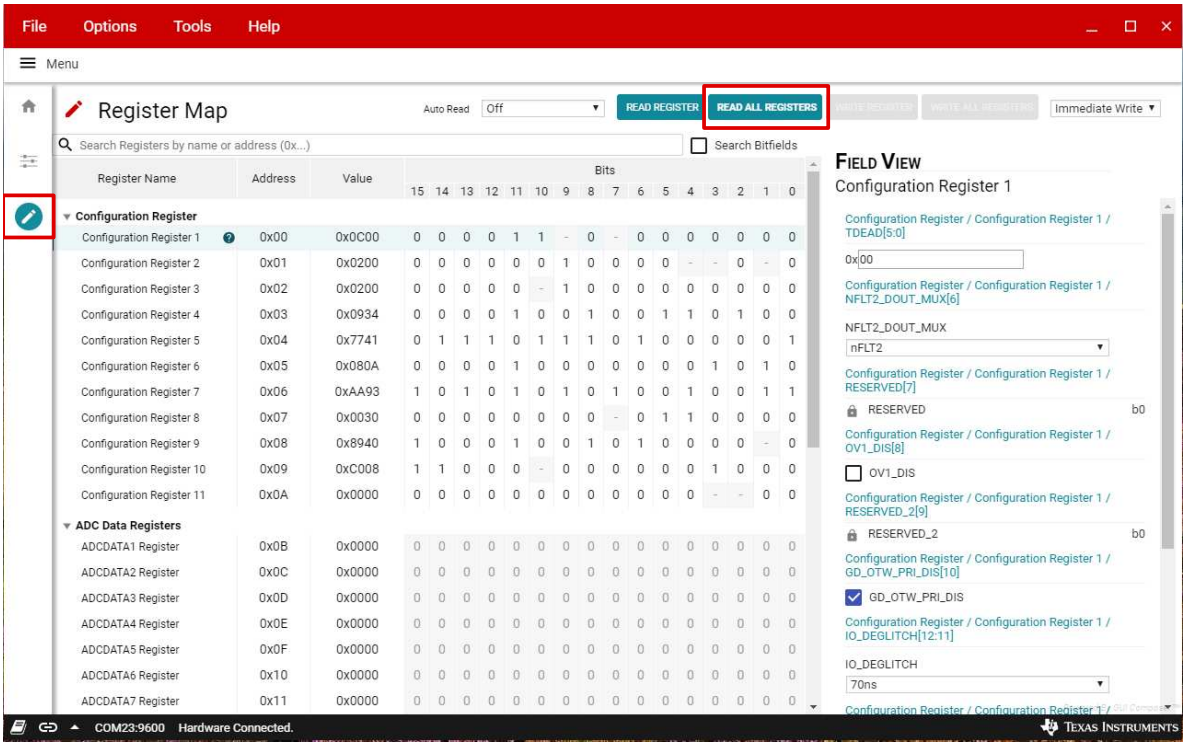

Figure 11. GUI Configuration 2 Read All Registers

9. Then previously saved register file can be loaded by clicking "File" then load saved register, or each register can be programmed separately with this GUI. In this example, let's disable DESAT protection first. Otherwise Desat fault will trig as there is no IGBT connected

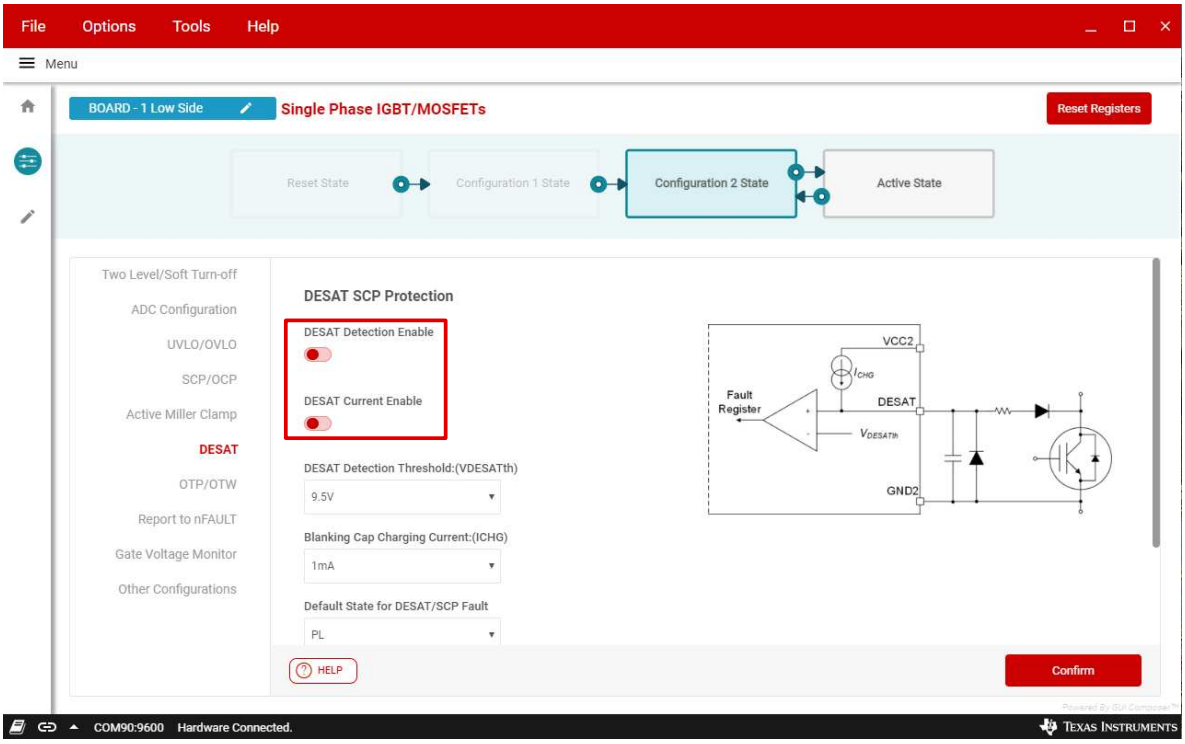

Figure 12. GUI Configuration 2 Disable DESAT Protection

10. Move to "Gate Voltage Monitor" section, disable the gate voltage monitor function or change gate voltage monitor blanking time to 2500-ns and then change default state from "HiZ" to "PL", as this fault may be triggered with 100-nF load and 5.1-Ω gate resistor if tGMBLK = 1000ns.

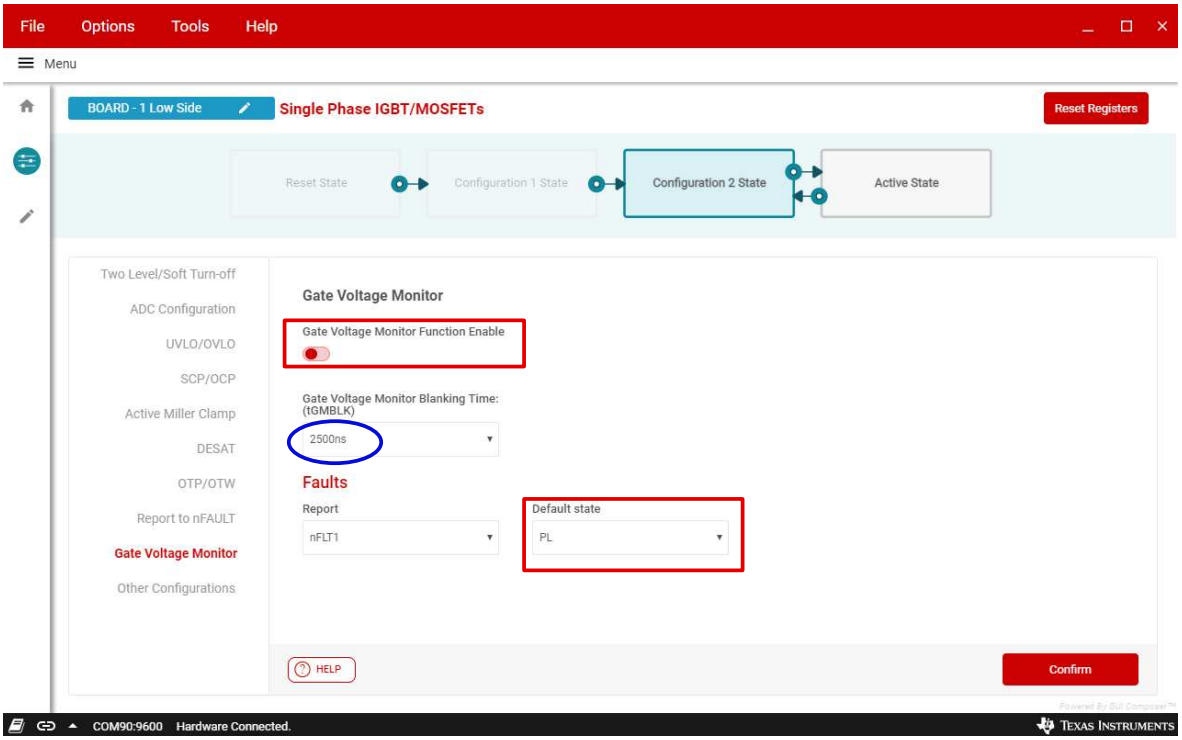

Figure 13. GUI Configuration 2 Disable Gate Voltage Monitor Function

11. Now move to Active State, setup PWM duty cycle for 50% and PWM frequency for 10kHz

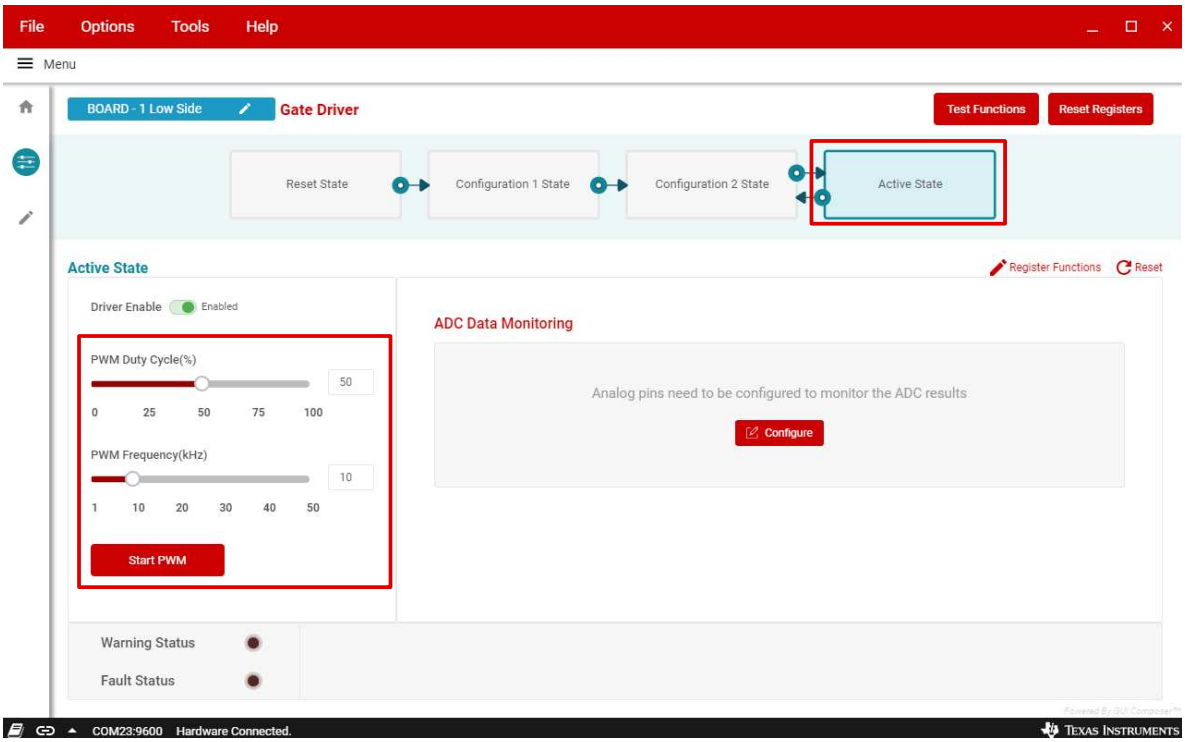

Figure 14. GUI Active State Enable Continuous PWM

12. After click "Stark PWM", PWM waveforms in Figure 15 will be generated.

Figure 15. Continuous PWM Waveforms

13. Stop PWM, click "Test Functions", double pulse test parameters can be set up.

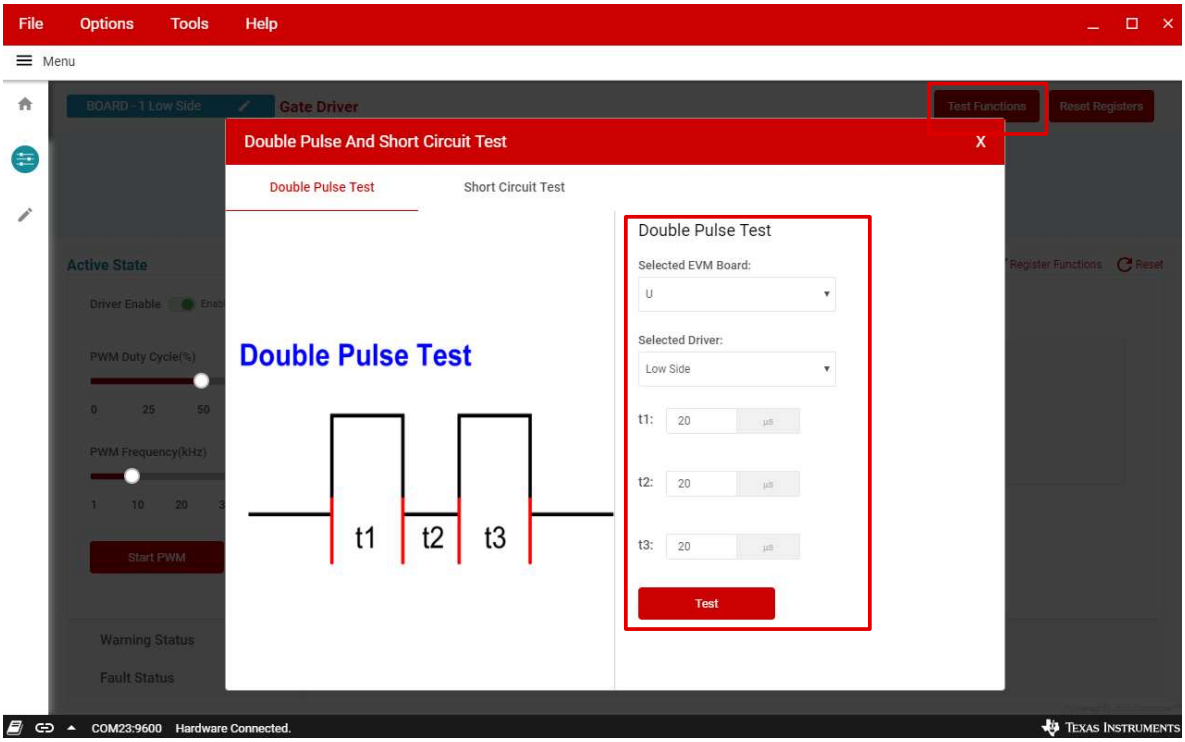

Figure 16. GUI Active State Double Pulses Test

14. Click "Test", double pulses waveforms in Figure 17 will be generated.

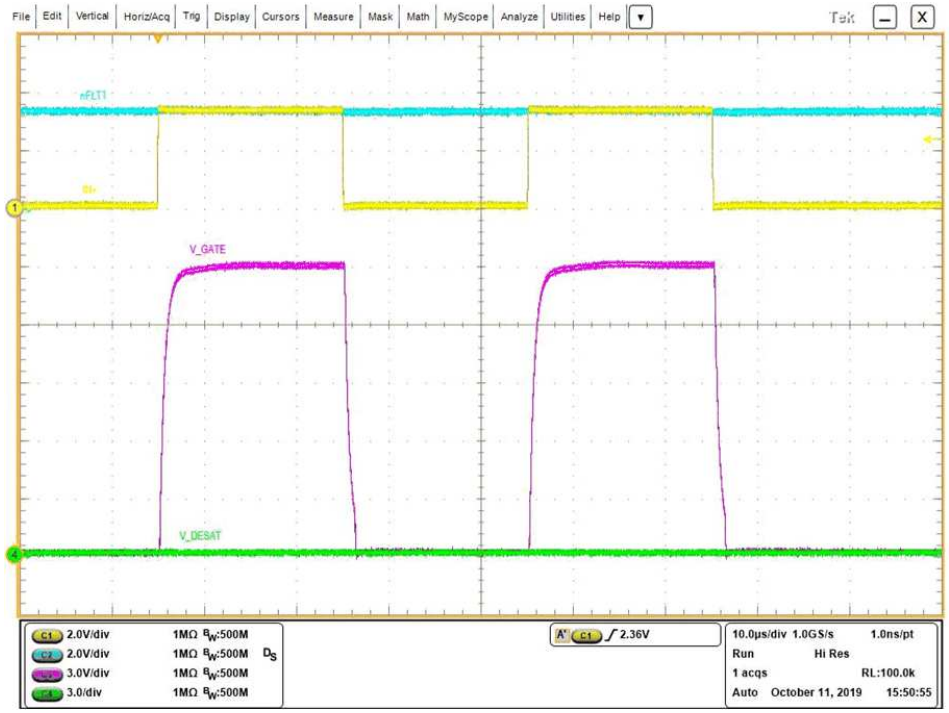

Figure 17. Double Pulses Test Waveforms

15. Next step go back to configuration 2 state and enable the DESAT protection.

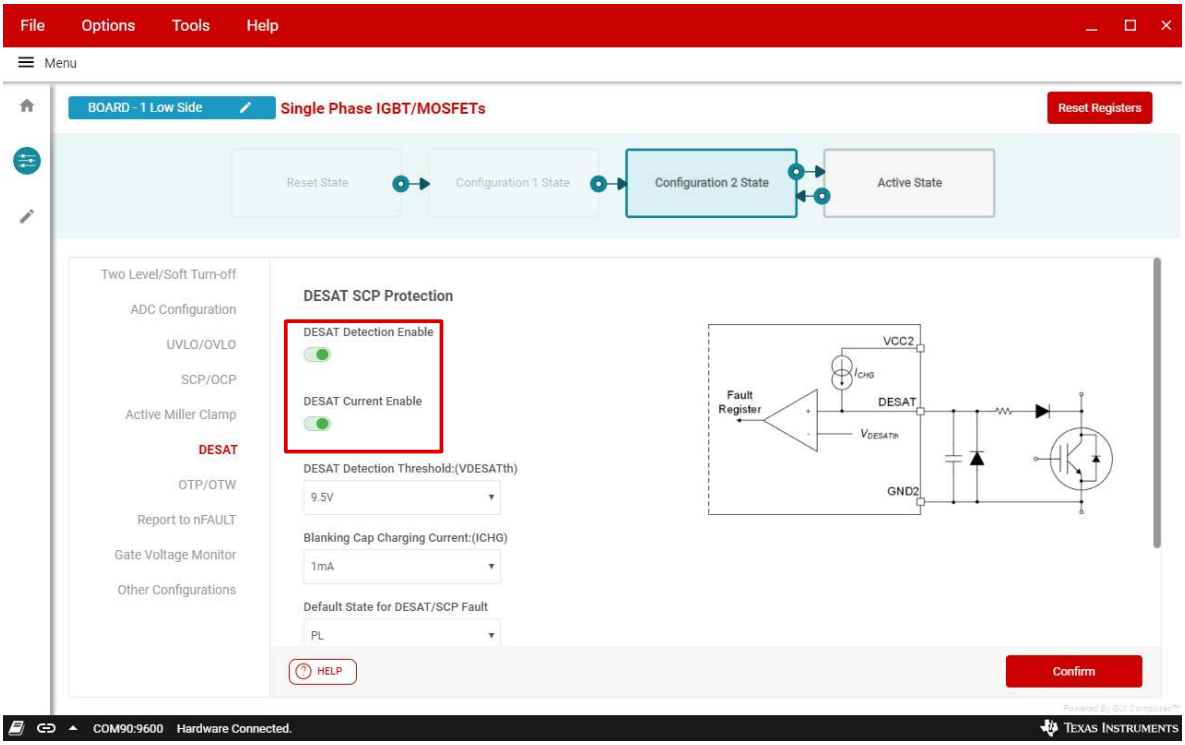

Figure 18. GUI Configuration 2 Enable DESAT Protection

16. In active state, generate a double pulse test, faults status will become red since no IGBT is connected and connector for IGBT collector terminal is floating.

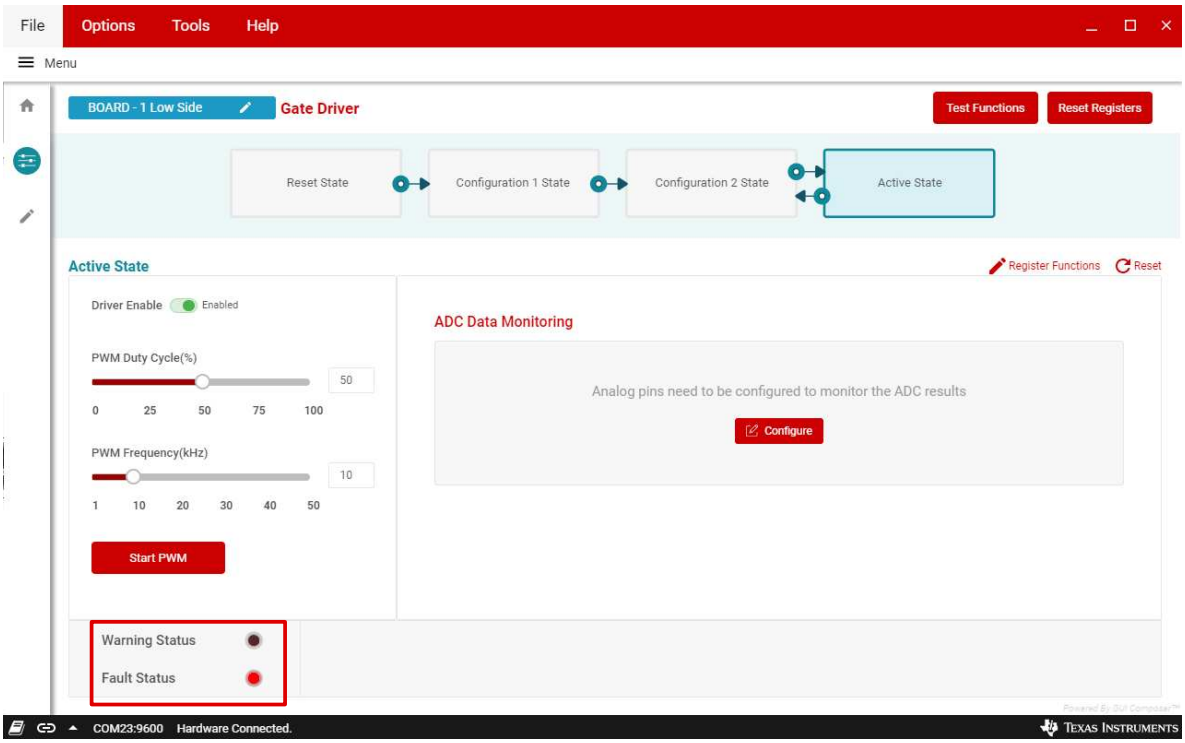

Figure 19. GUI Active Stage Fault Indicator

17. Figure 20 shows the waveforms of the Desat fault, CH4 is the desat pin voltage, when it reaches about 9.5V, the fault is triggered and nFLT1 pin is pulled low.

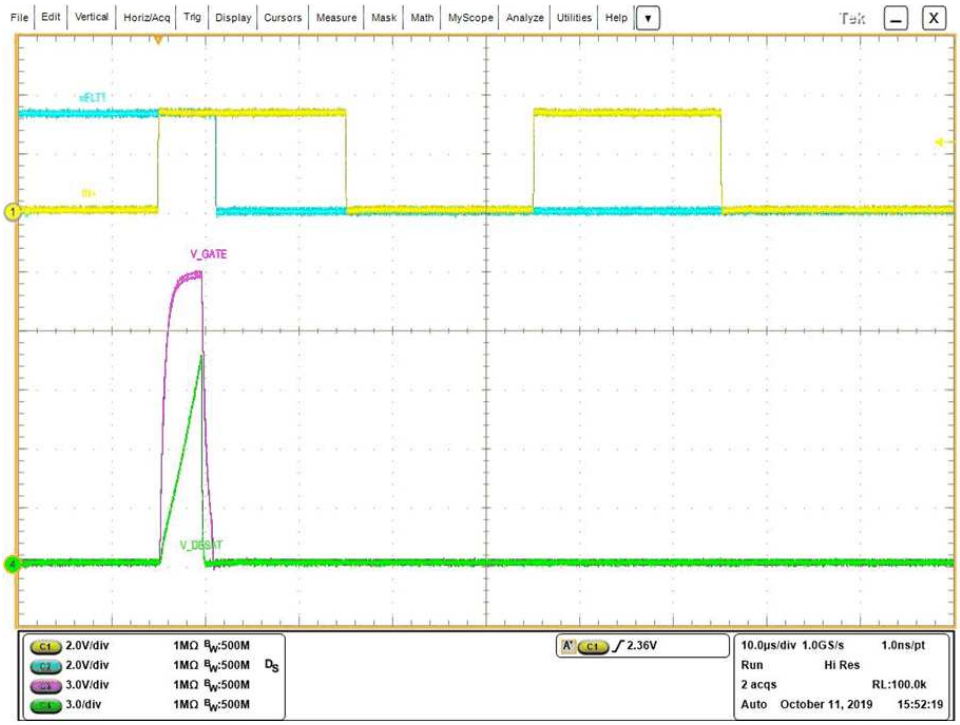

Figure 20. DESAT Fault Test Waveforms

18. When there is a fault, read all status register and find out which fault was triggered in register map. In the above example, it can be found that DESAT_FAULT is triggered.

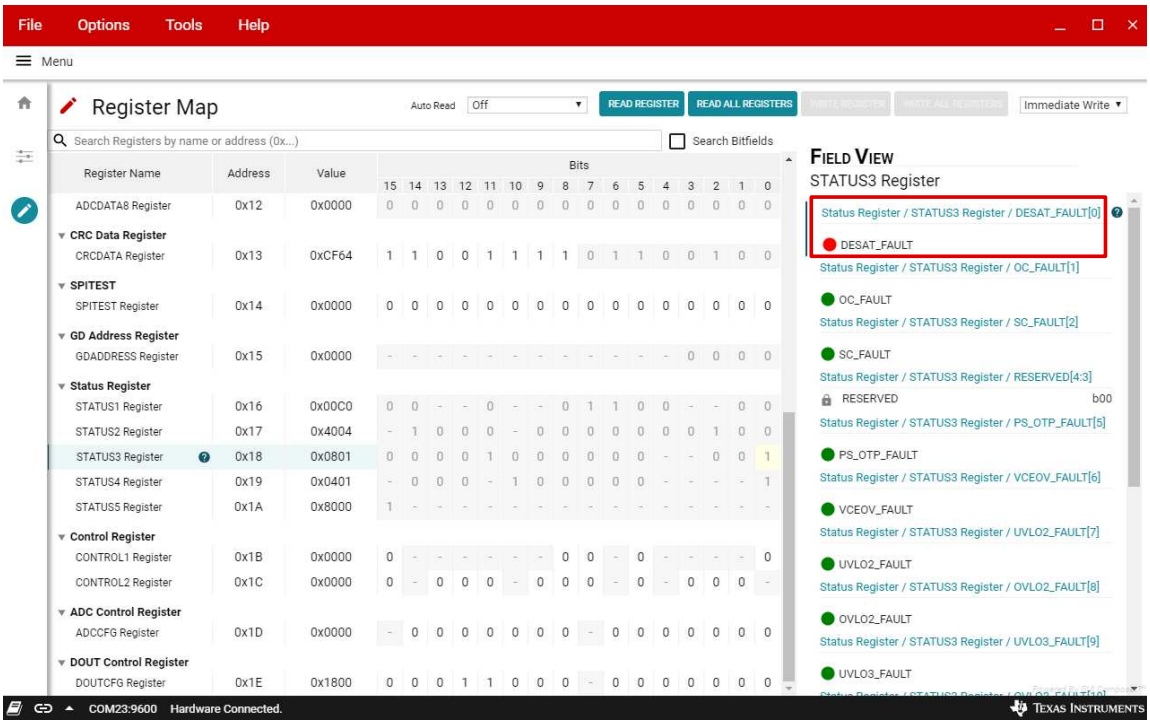

Figure 21. Status Register Shows DESAT Fault

19. The fault can be reset by clicking "Clear fault" which writes 1 to CONTROL2 register bit[15]. Please note ADC fault (Status 5 Register bit[15]) is on with default setting which selects external Vref for ADC but the EVM board doesn't have external Vref, this fault can be cleared by selecting internal Vref.

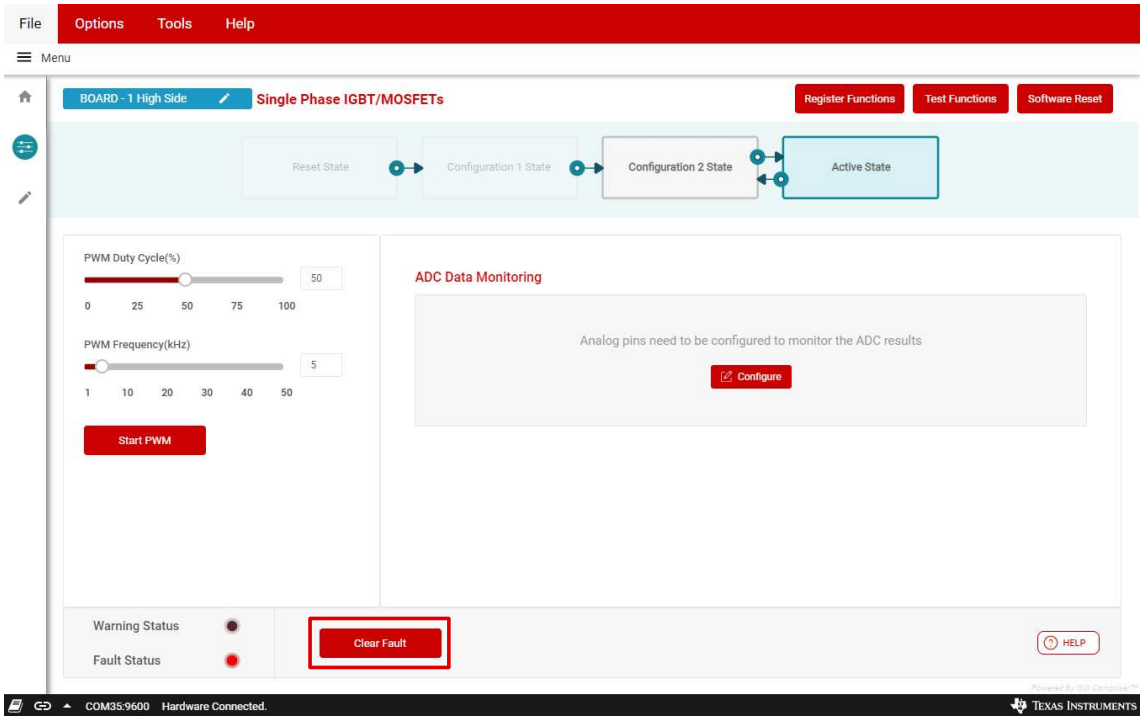

Figure 22. Clear Fault Option

5.2 Daisy Chain Mode SPI

1. If using daisy chain mode SPI, the MCU board jumpers need to be configured as in Figure 2 right graph, then power up the supplies and the GUI should detect one EVM board, select "Daisy chain" and click "Finish"

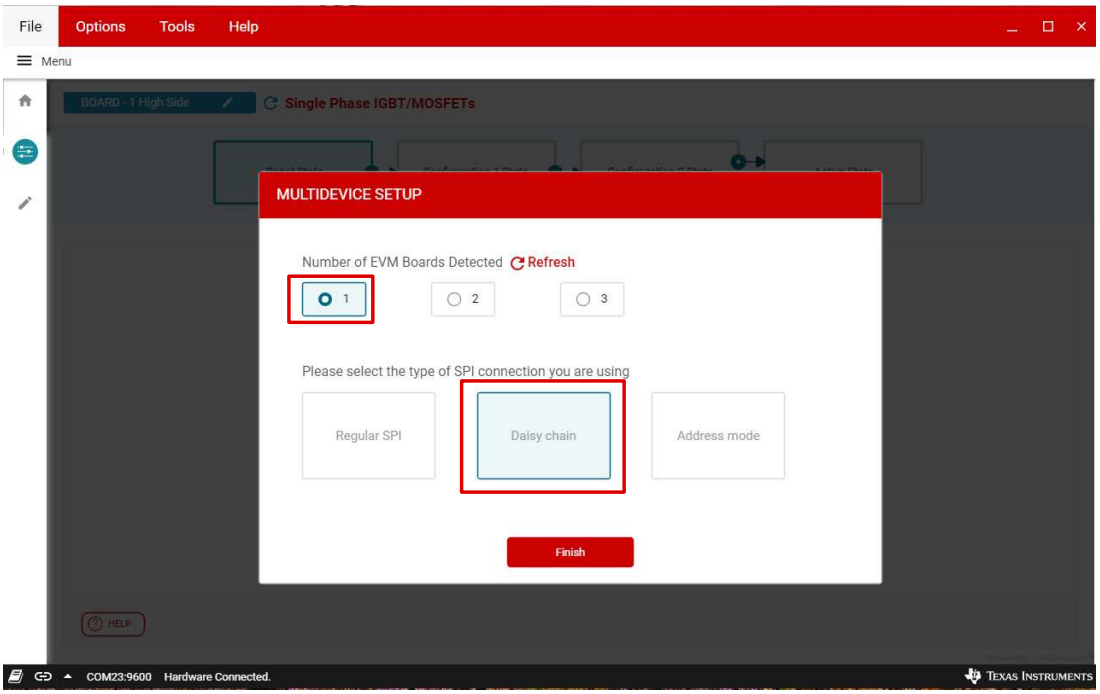

Figure 23. Daisy Chain SPI Mode Selection

2. Then for HS GATE in Configuration 1 State, click "Proceed", at this moment, the driver will not move to configuration 2 stage.

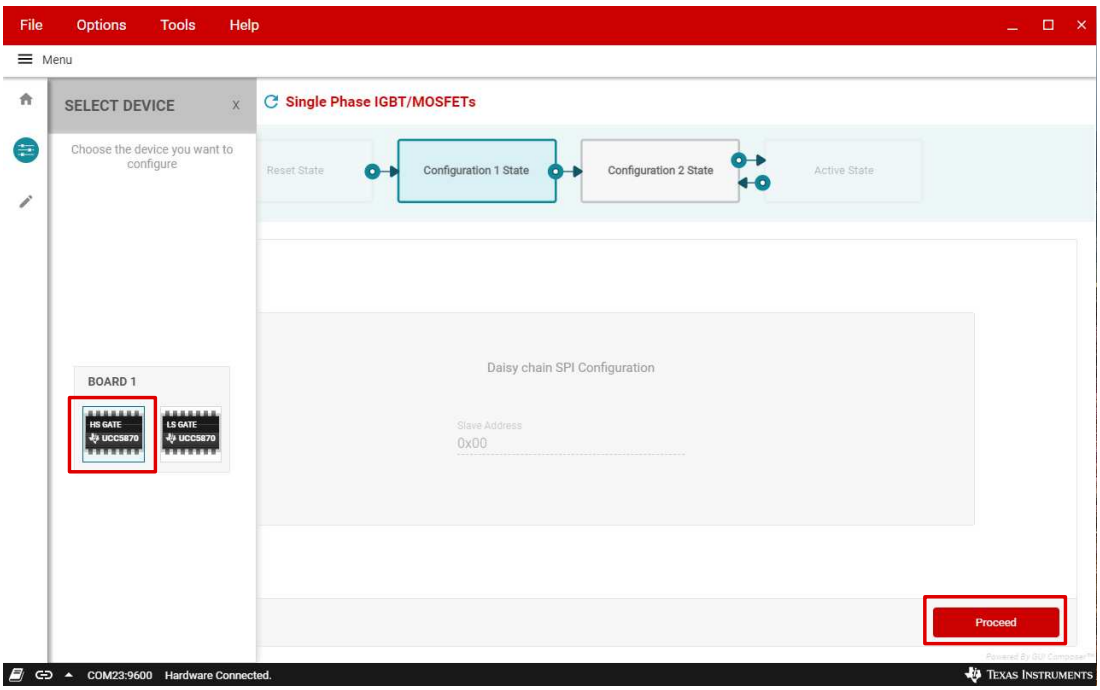

Figure 24. Daisy Chain SPI Mode High Side CF1 State

3. Select LS GATE in Configuration 1 State, click "Proceed", then both high side and low side driver will move to configuration 2 state at the same time.

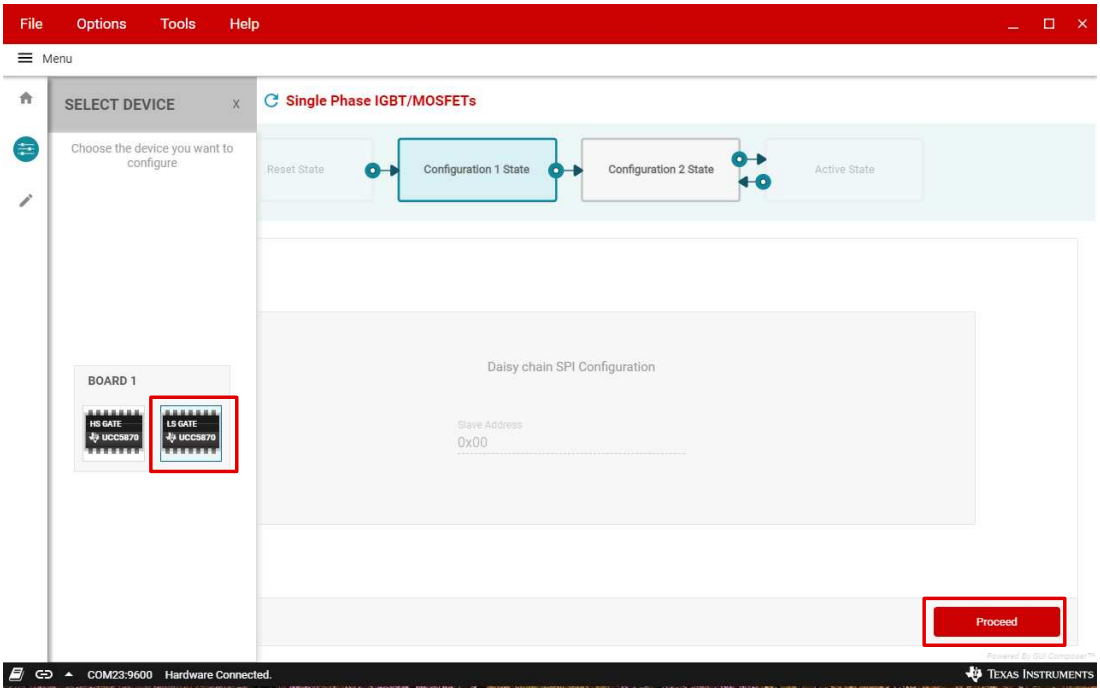

Figure 25. Daisy Chain SPI Mode Low Side CF1 State

4. Below Figure 26 shows the GUI page of the above step when both high side and low side driver are in configuration 2 state.

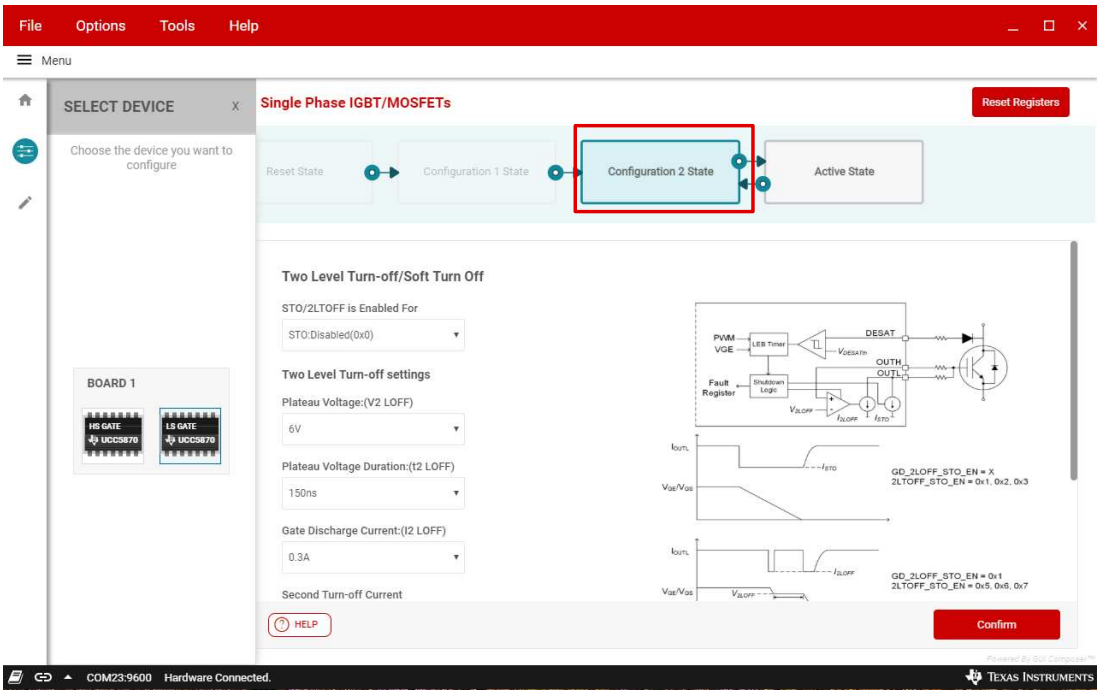

Figure 26. Daisy Chain SPI Mode High Side and Low Side CF2 State

5.3 Address Mode SPI

1. If using address mode SPI, the MCU board jumpers need to be configured as in Figure 2 left graph, then power up the supplies and the GUI should detect one EVM board, select "Address mode" and click "Finish"

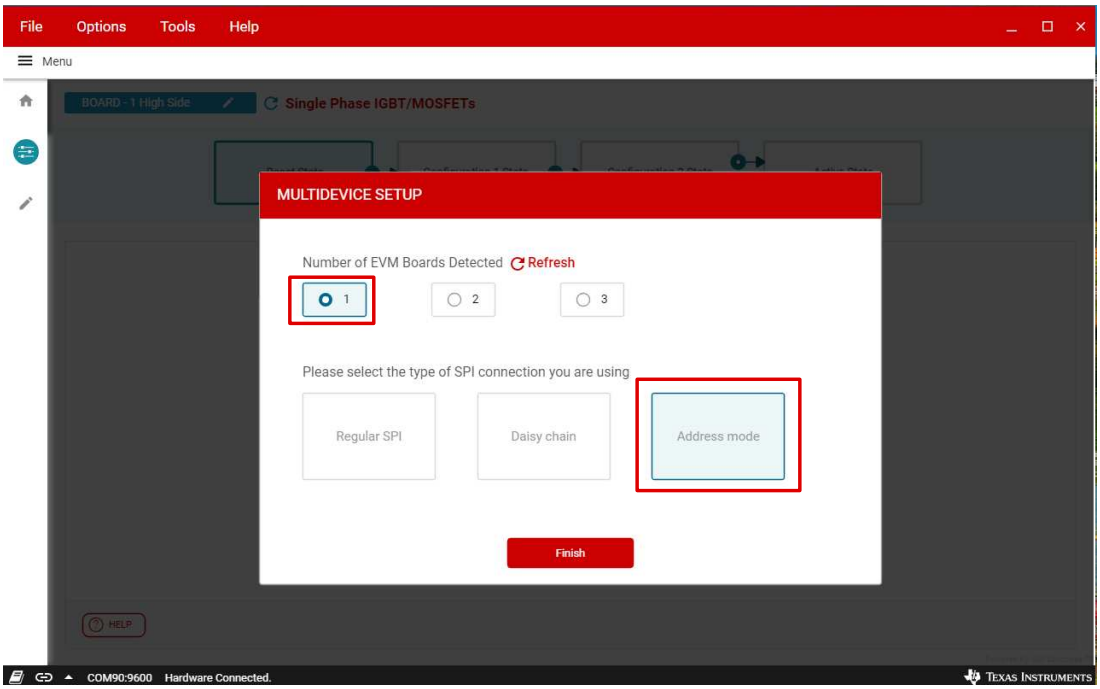

Figure 27. Address SPI Mode Selection

2. Then for HS GATE in Configuration 1 State, click "Proceed", GUI will write chip address 0x01 to the high side gate driver, then it moves to configuration 2 state.

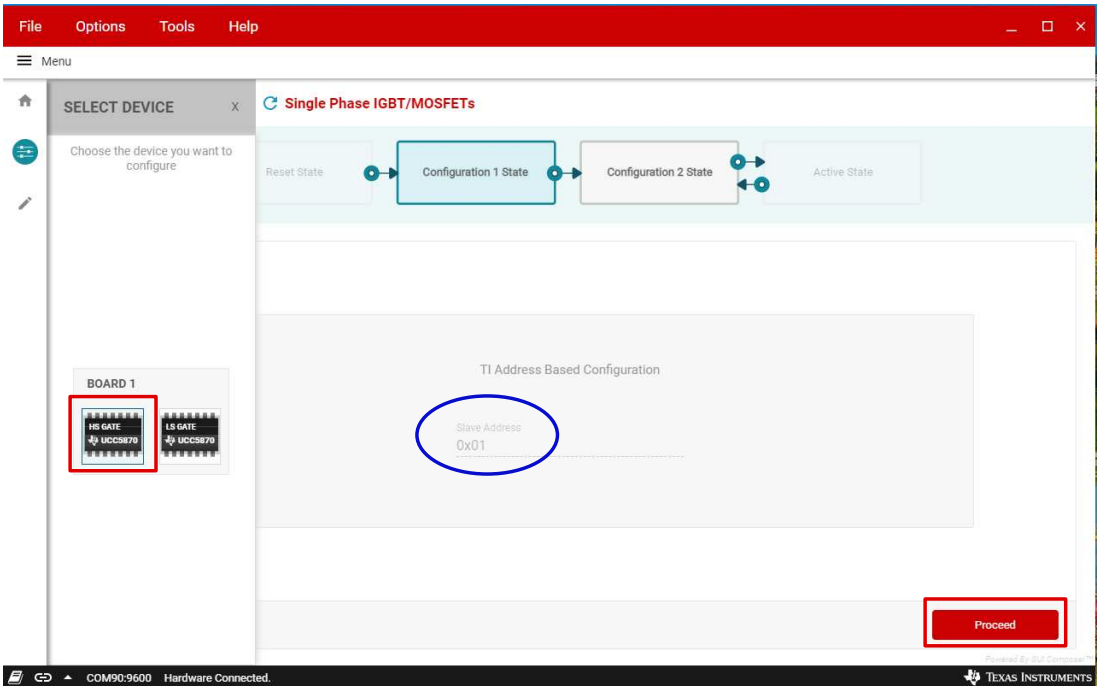

Figure 28. Address SPI Mode High Side CF1 State: Writing Address 0x01

3. Below Figure 29 shows the GUI page of the above step when high side driver is in configuration 2 state.

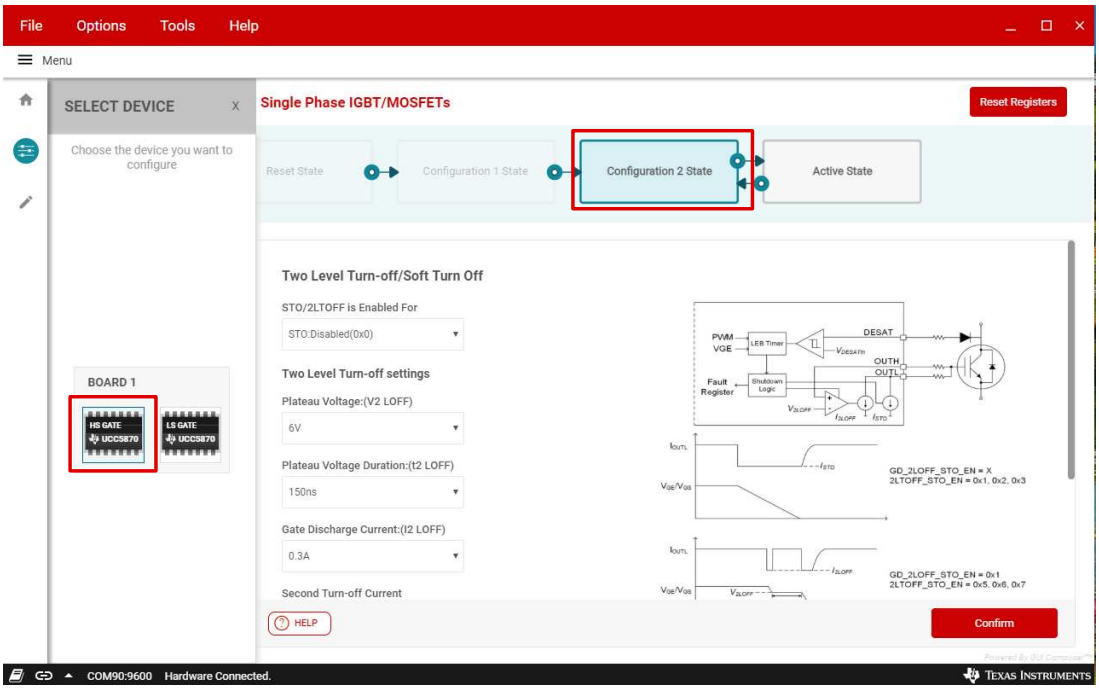

Figure 29. Address SPI Mode High Side CF2 State

4. Repeat the same step for the low side driver, chip address 0x02 will be written to the low side driver.

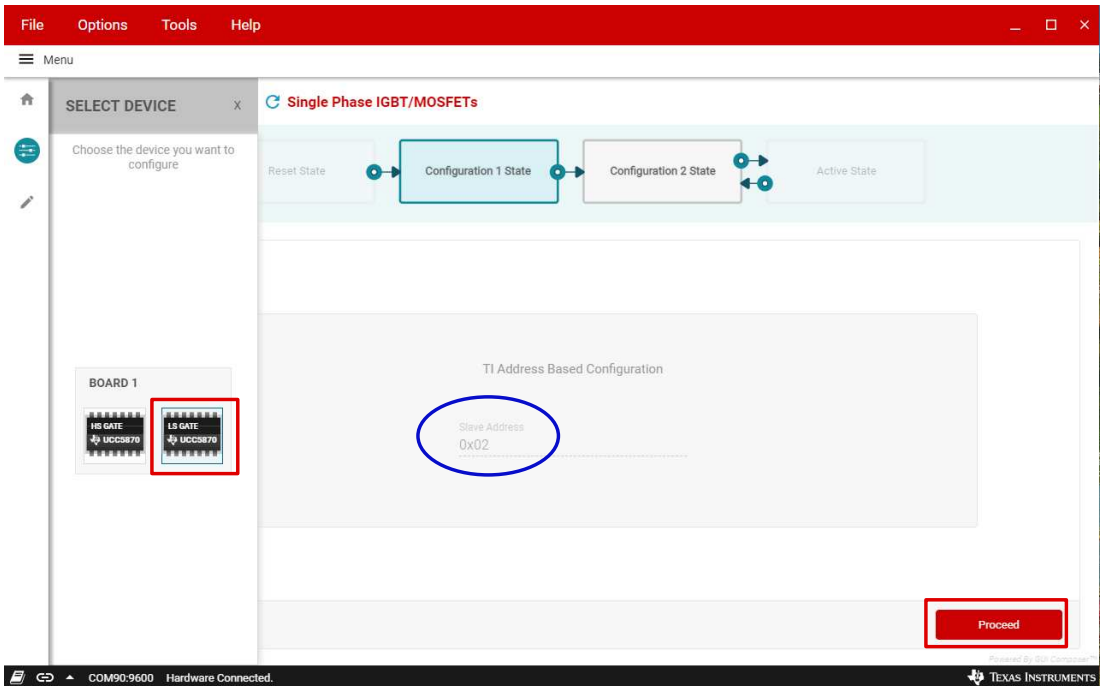

Figure 30. Address SPI Mode Low Side CF1 State: Writing Address 0x02

6 High Voltage Test Example

6.1 EVM isolation

The board view is shown in Figure 31, it can be divided as three sections: 1) primary side of the driver, 2) secondary side for low side IGBT, 3) secondary side for high side IGBT. The both secondary sides have high voltage present when the EVM is connected to the IGBT module with high voltage DC bus. The isolation components between primary and secondary are two flyback transformer and two UCC5870 gate drivers. UCC5870 isolation capability is 3750 Vrms and flyback transformer ZA9710-AE (not exactly the one shown in Figure 31) isolation capability is 3000 Vrms.

To minimize risk of electric shock hazard always follow safety practices normally followed in a development laboratory. Refer to TI's EVM High Voltage guideline accompanying this EVM.

The J22, J23 and other test pins are mainly designed for the convenience of low voltage test, please be extremely cautious if measuring any of these pins during high voltage test.

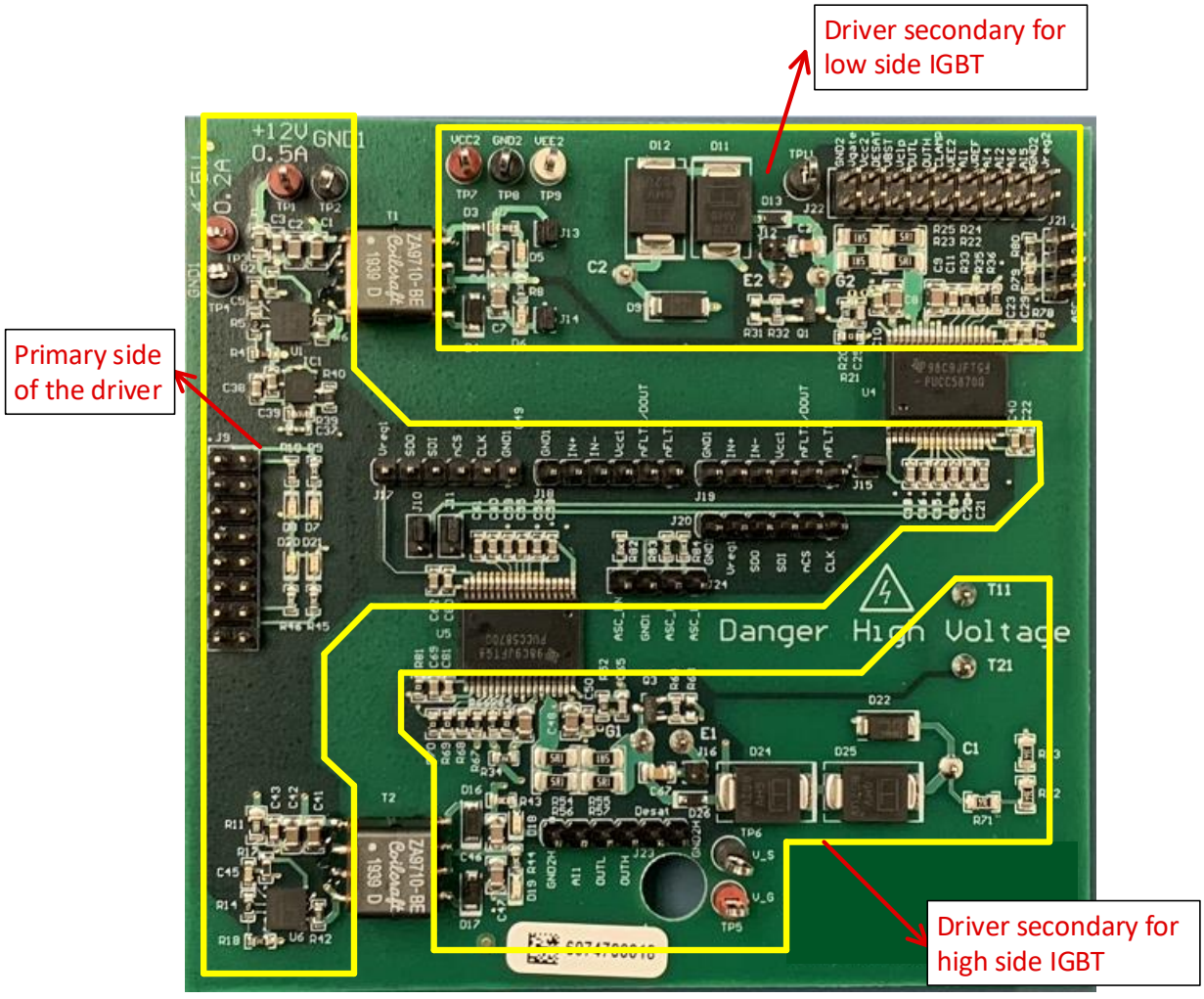

Figure 31. EVM Primary and Secondary

6.2 Bench Setup For High Voltage Test

This EVM is designed to fit a bridge leg of IGBT module FS820R08A6P2B. Figure 32 shows how the EVM and MUC daughter card are connected with the IGBT module. Additional DC bus capacitors and load inductor are needed for performance double pulses and short circuit test. Please make sure all the connections are reliable and the test environment is safe before conducting any test.

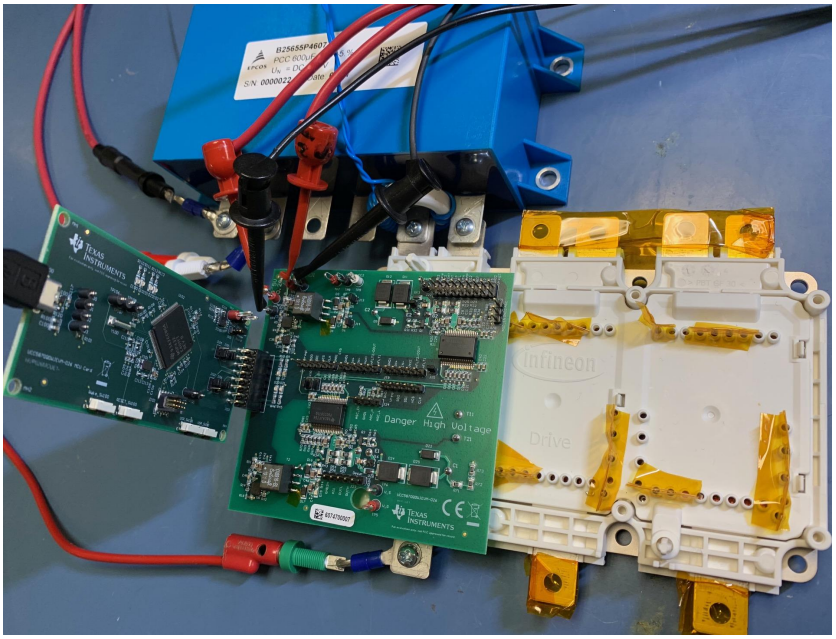

Figure 32. EVM Connected with IGBT Module

6.3 Double Pulses Test Example Waveforms

Figure 33 shows an example double test waveform at for 400V, 100A switching.

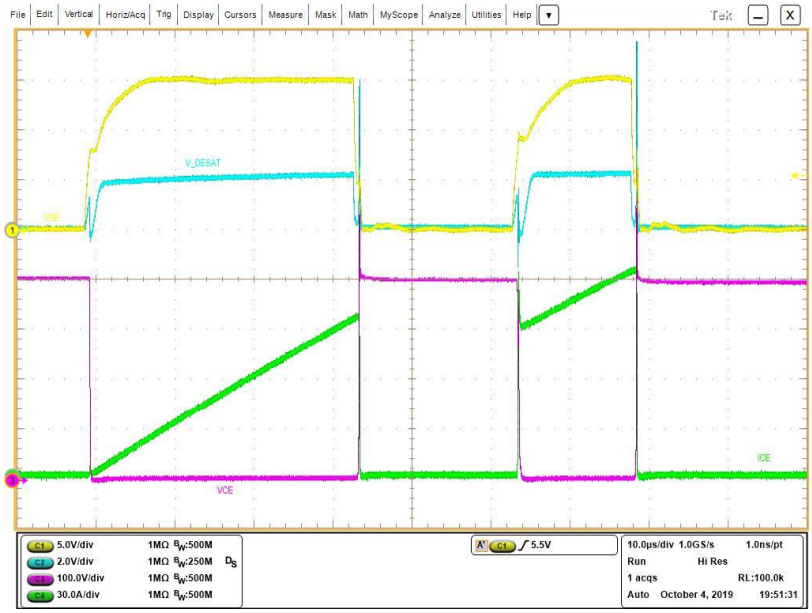

Figure 33. Double Pulses Test Waveforms at 400V 100A

7 Schematic

Figure 34 and Figure 35 show the schematic diagram for the UCC5870 EVM.

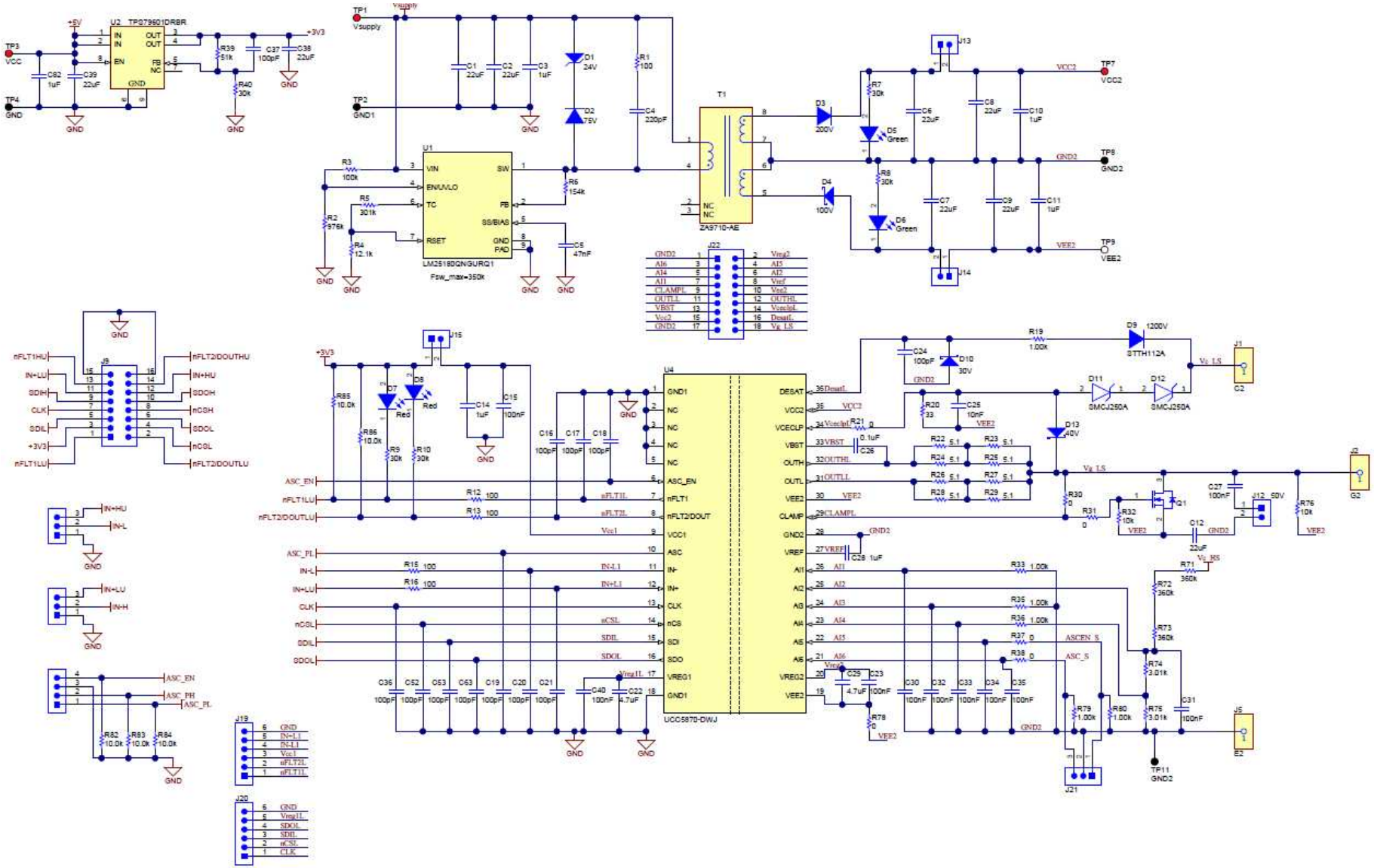

Figure 34. UCC5870 EVM Low Side Driver Schematic

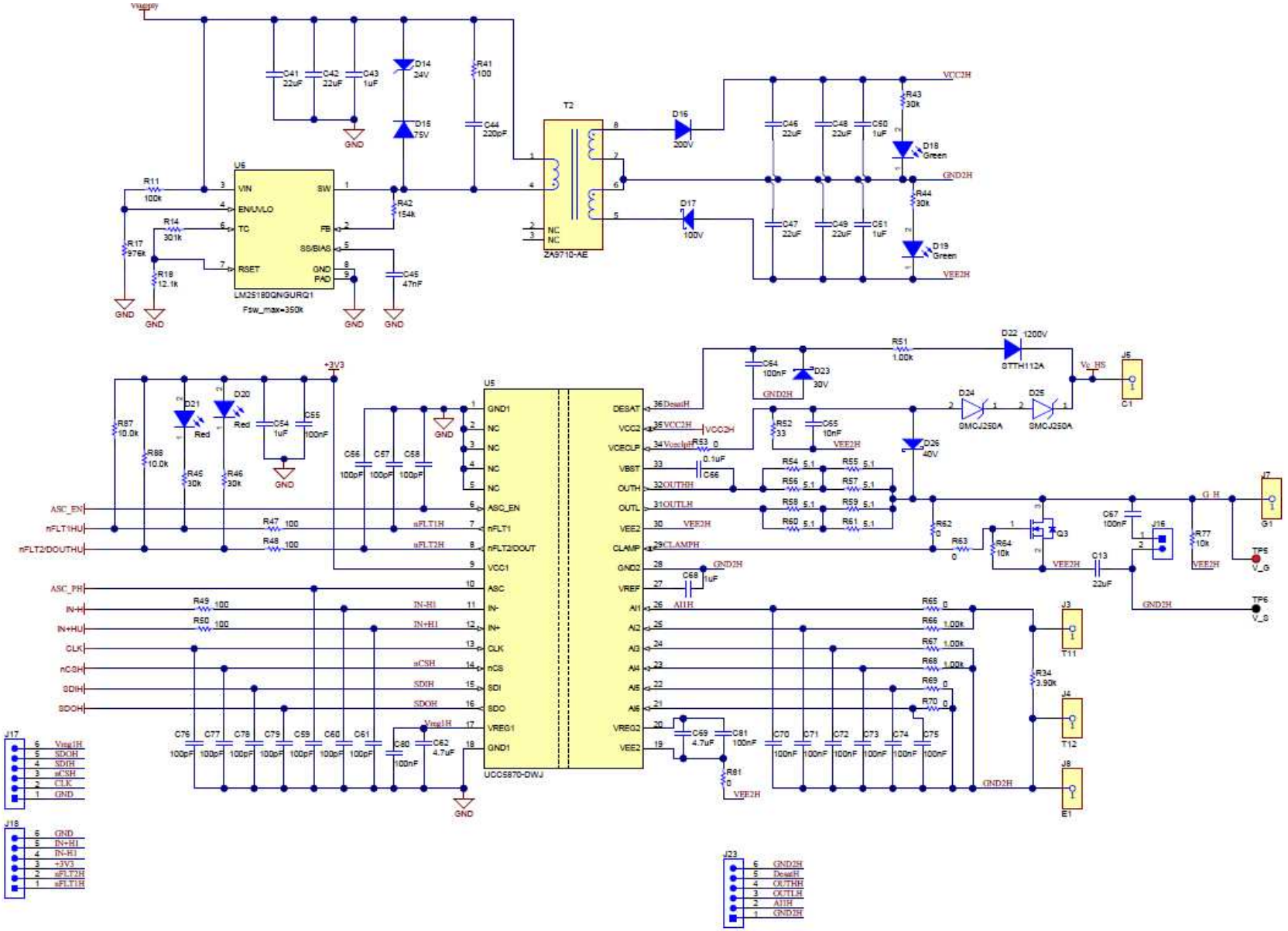

Figure 35. UCC5870 EVM High Side Driver Schematic

8 Layout Diagrams

Figure 36 to Figure 43 show the PCB layout information for the UCC5870 EVM.

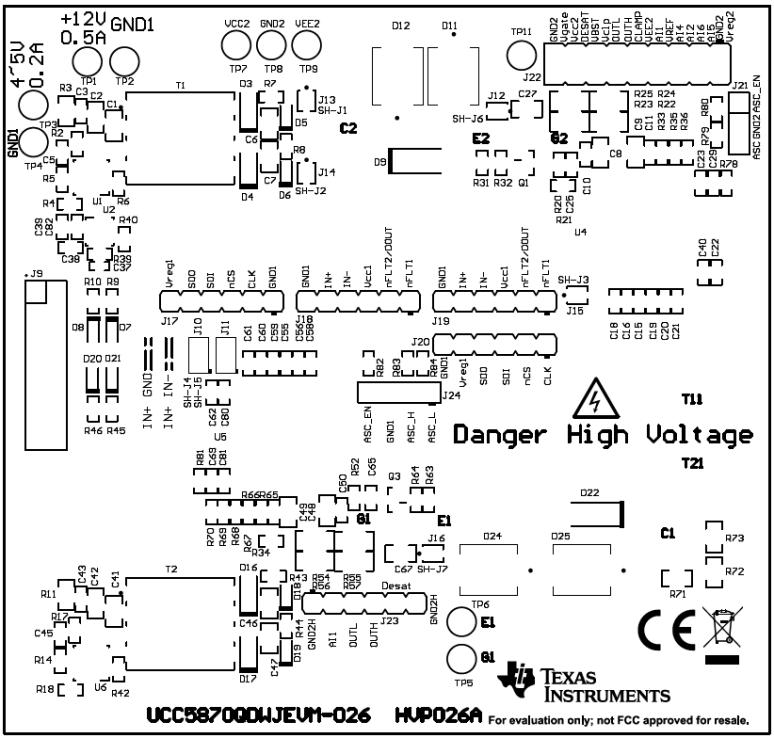

Figure 36. PCB Layout Top Overlay

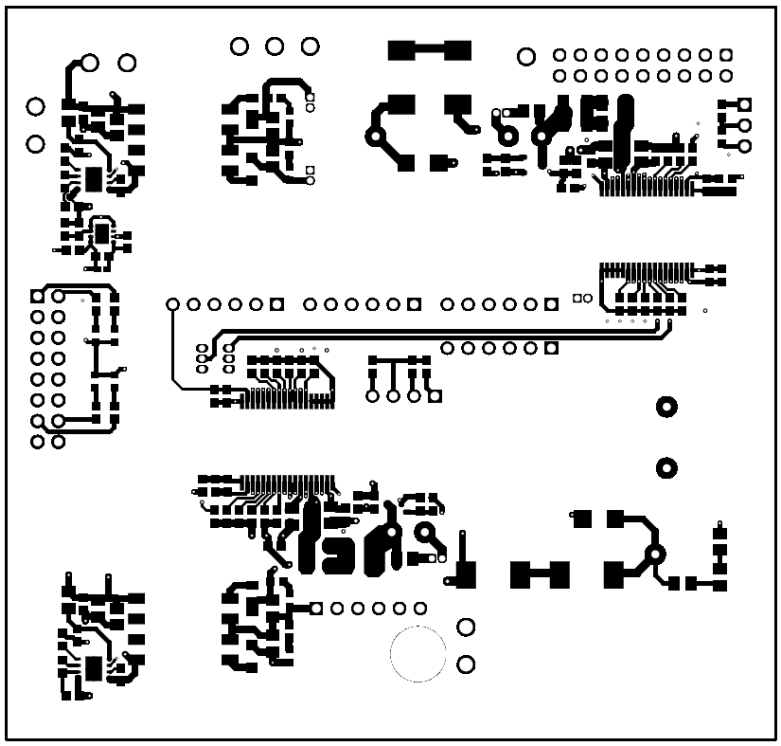

Figure 37. PCB Layout Top Layer

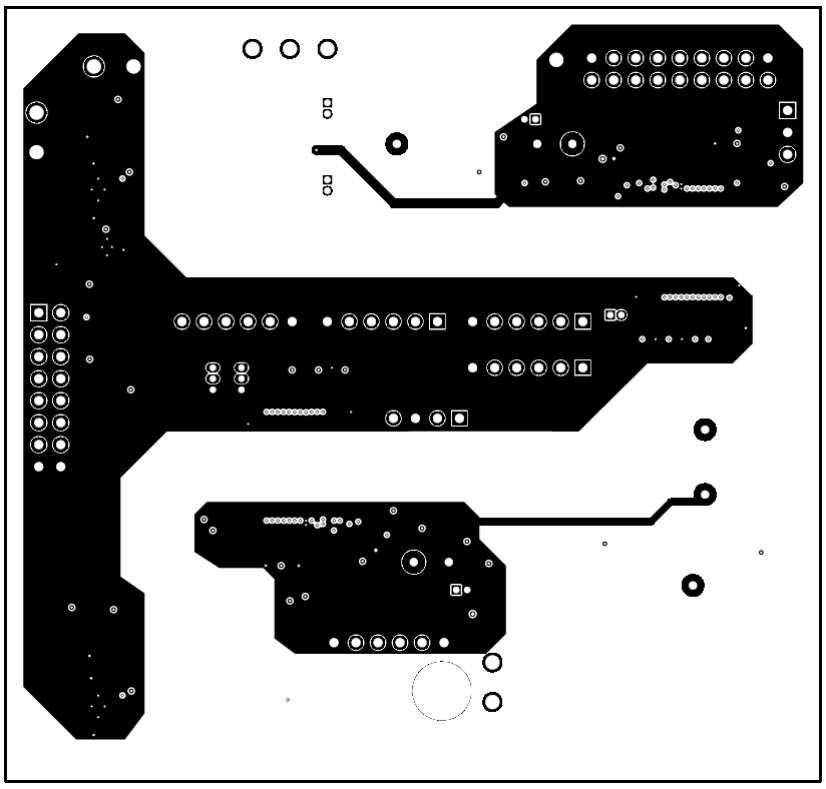

Figure 38. PCB Layout Inter Layer 1

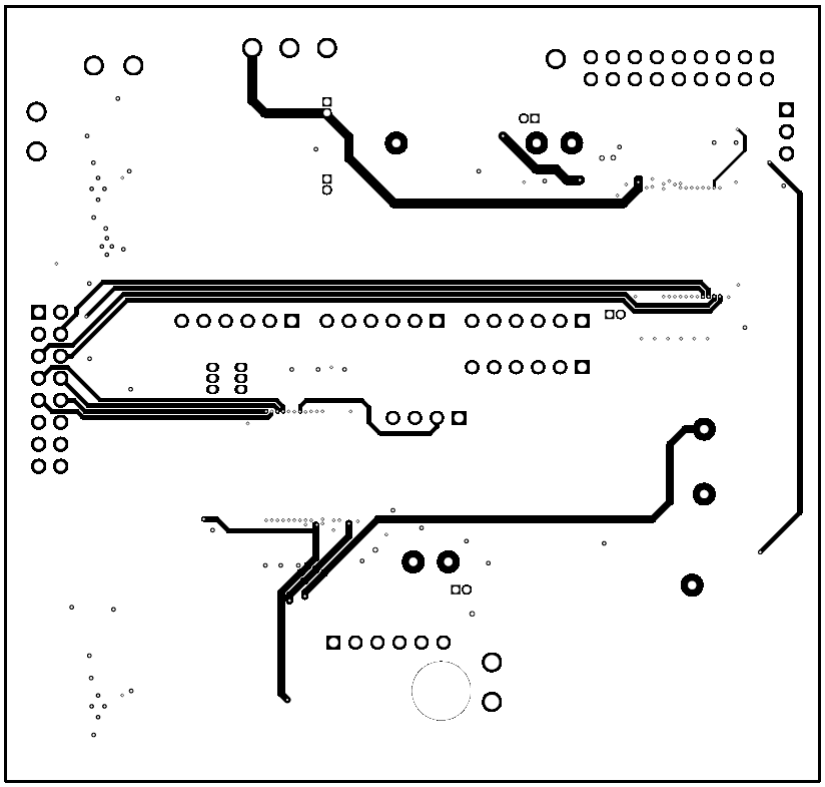

Figure 39. PCB Layout Inter Layer 2

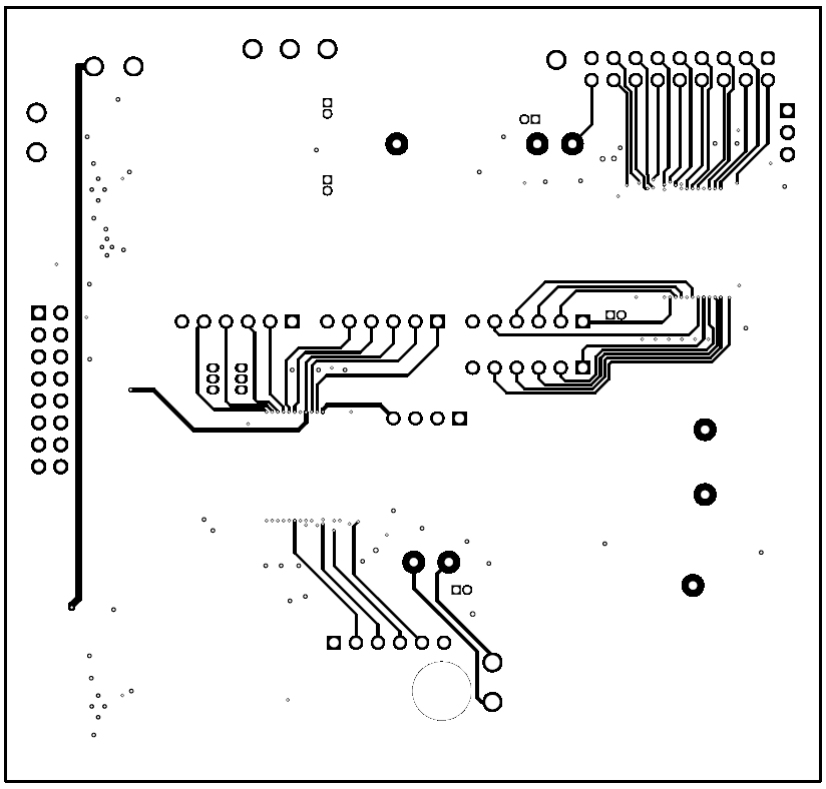

Figure 40. PCB Layout Inter Layer 3

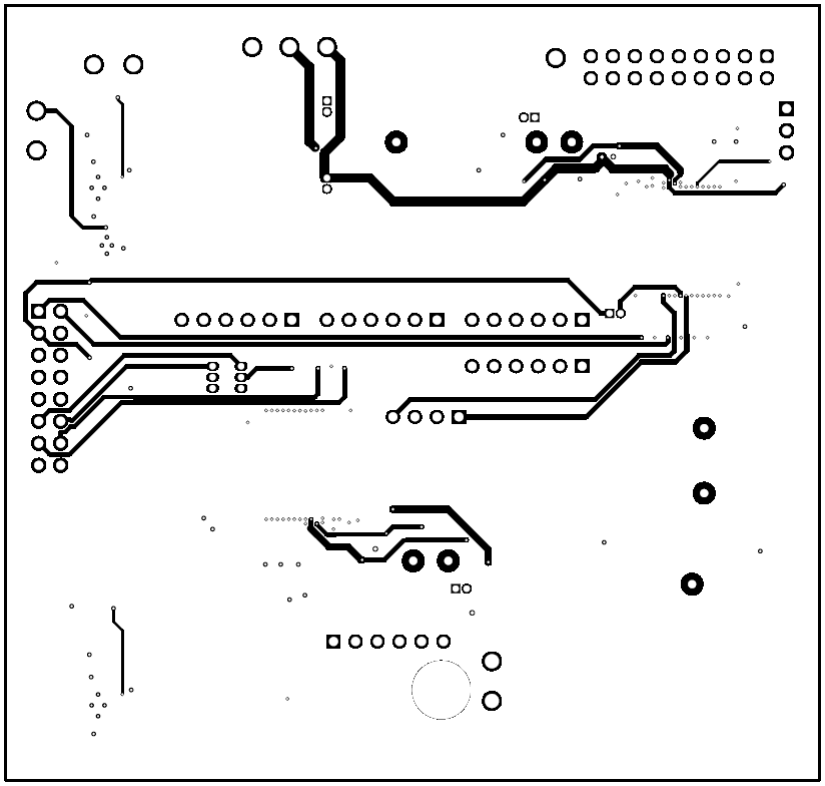

Figure 41. PCB Layout Inter Layer 4

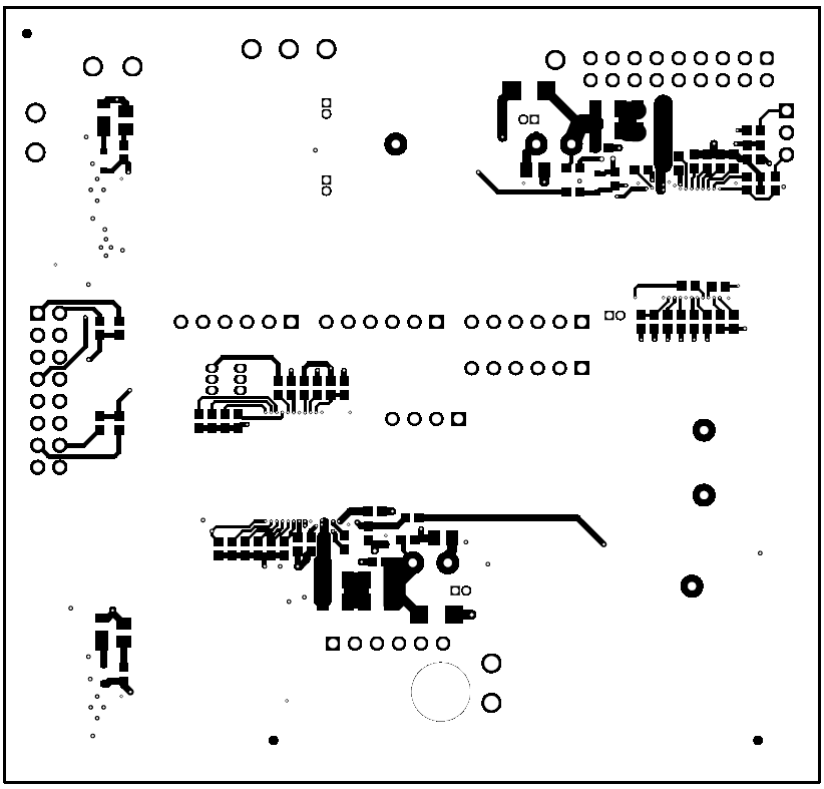

Figure 42. PCB Layout Bottom Layer

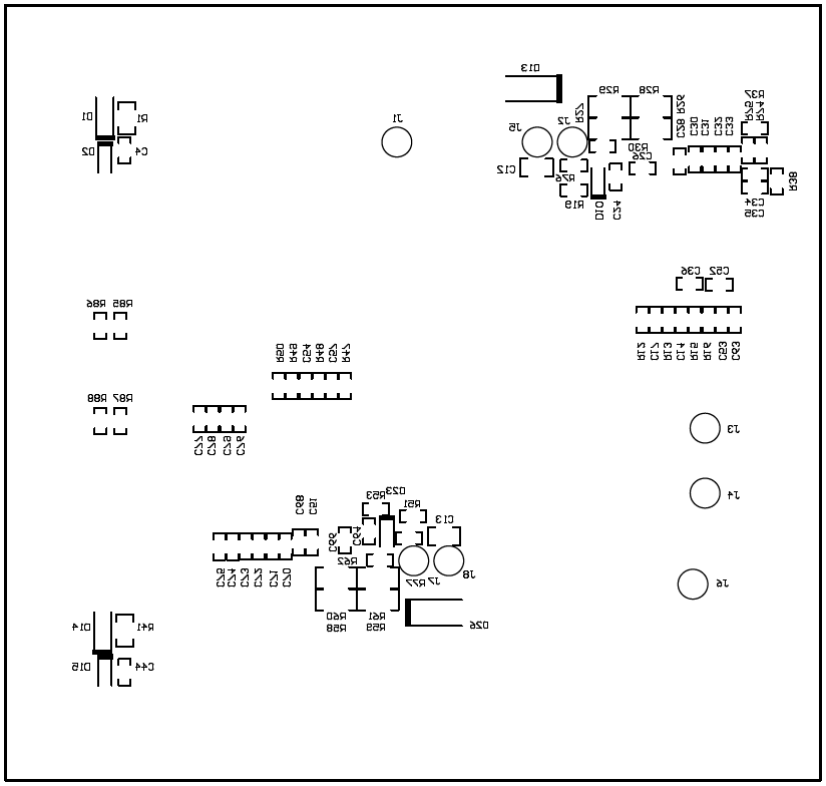

Figure 43. PCB Layout Bottom Overlay

9 Bill of Materials

Table 4. List of Materials

DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C2, C6, C7, C8, C9, C12, C13, C41, C42, C46, C47, C48, C49	14	CAP, CERM, 22 uF, 25 V, +/- 20%, X5R, 0805	MuRata	GRM21BR61E226ME44L
C3, C10, C11, C14, C28, C43, C50, C51, C54, C68, C82	11	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E1X7R1V105K080AC
C4, C44	2	CAP, CERM, 220 pF, 100 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C2A221JA01D
C5, C45	2	CAP, CERM, 0.047 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	MuRata	GCM188R71E473KA37D
C15, C23, C30, C31, C32, C33, C34, C35, C40, C55, C64, C70, C71, C72, C73, C74, C75, C80, C81	19	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E2X7R1E104K080AA
C16, C17, C18, C19, C20, C21, C56, C57, C58, C59, C60, C61	12	CAP, CERM, 100 pF, 100 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	MuRata	GCM1885C2A101JA16D
C22, C29, C62, C69	4	CAP, CERM, 4.7 uF, 10 V, +/- 10%, X5R, 0603	Kemet	C0603C475K8PACTU
C24	1	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 0, 0603	TDK	CGA3E2NP01H101J080AA
C25, C65	2	CAP, CERM, 0.01 uF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E2X7R2A103K080AA
C26, C66	2	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X5R, 0603	TDK	C1608X5R1H104K080AA
C27, C67	2	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 0, 0805	Kemet	C0805C104K5RACAUTO
C37	1	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	Yageo America	CC0402JRNPO9BN101
C38, C39	2	CAP, CERM, 22 uF, 6.3 V, +/- 20%, X5R, 0603	MuRata	GRM188R60J226MEA0D
D1, D14	2	Diode, Zener, 24 V, 1 W, PowerDI123	Diodes Inc.	DFLZ24-7
D2, D15	2	Diode, Ultrafast, 75 V, 0.25 A, SOD-323	Central Semiconductor	CMDD4448
D3, D16	2	Diode, Superfast Rectifier, 200 V, 1 A, AEC-Q101, PowerDI123	Diodes Inc.	DFLU1200-7
D4, D17	2	Diode, Schottky, 100 V, 1 A, AEC-Q101, SOD-123W	Nexperia	PMEG10010ELRX
D5, D6, D18, D19	4	LED, Green, SMD	Wurth Elektronik	150060VS75000
D7, D8, D20, D21	4	LED, Red, SMD	Wurth Elektronik	150060RS75000
D9, D22	2	Diode, Ultrafast, 1200 V, 1 A, SMA	STMicroelectronics	STTH112A
D10, D23	2	Diode, Schottky, 30 V, 0.2 A, SOD-323	Diodes Inc.	BAT54WS-7-F
D11, D12, D24, D25	4	405V Clamp 3.7A Ipp Tvs Diode Surface Mount DO-214AB (SMCJ)	Littelfuse Inc	SMCJ250A
D13, D26	2	Diode, Schottky, 40 V, 3 A, SMA	ON Semiconductor	MBRA340T3G
J1, J2, J3, J4, J5, J6, J7, J8	8	CONN PIN RCPT .032-.046 PRESSFIT	Mill-Max	0405-0-15-15-34-27-04-0
J9	1	Header, 100mil, 8x2, Gold, TH	Sullins Connector Solutions	PBC08DAAN
J10, J11	2	Header, 50mil, 3x1, Gold, TH	Sullins Connector Solutions	GRPB031VWVN-RC

Table 4. List of Materials (continued)

DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
J12, J13, J14, J15, J16	5	Header, 50mil, 2x1, Gold, TH	Sullins Connector Solutions	GRPB021VWVN-RC
J17, J18, J19, J20, J23	5	Header, 2.54mm, 6x1, Gold, TH	Sullins Connector Solutions	PBC06SAAN
J21	1	Header, 100mil, 3x1, Gold, TH	Sullins Connector Solutions	PBC03SAAN
J22	1	Header, 2.54mm, 9x2, Tin, TH	Sullins Connector Solutions	PEC09DAAN
J24	1	Header, 2.54 mm, 4x1, Gold, TH	Sullins Connector Solutions	PBC04SAAN
Q1, Q3	2	MOSFET, N-CH, 40 V, 5.6 A, SOT-23	Vishay-Siliconix	SI2318CDS-T1-GE3
R1, R41	2	RES, 100, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW0805100RFKEA
R2, R17	2	RES, 976 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603976KFKEA
R3, R11	2	RES, 100 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	Vishay-Dale	CRCW0805100KFKEA
R4, R18	2	RES, 12.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060312K1FKEA
R5, R14	2	RES, 301 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603301KFKEA
R6, R42	2	RES, 154 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603154KFKEA
R7, R8, R9, R10, R40, R43, R44, R45, R46	9	RES, 30 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060330K0JNEA
R12, R13, R15, R16, R47, R48, R49, R50	8	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100RJNEA
R19, R33, R35, R36, R51, R66, R67, R68, R79, R80	10	RES, 1.00 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031K00FKEA
R20, R52	2	RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060333R0JNEA
R21, R30, R37, R38, R53, R62, R65, R69, R70, R78, R81	11	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA
R22, R23, R24, R25, R26, R27, R28, R29, R54, R55, R56, R57, R58, R59, R60, R61	16	RES, 5.1, 5%, 0.25 W, AEC-Q200 Grade 0, 1206	Vishay-Dale	CRCW12065R10JNEA
R32, R64, R76, R77	4	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060310K0JNEA
R39	1	RES, 51 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060351K0JNEA
R71, R72, R73	3	RES, 360 k, 0.1%, 0.125 W, 0805	Susumu Co Ltd	RG2012P-364-B-T5
R74, R75	2	RES, 3.01 k, 0.1%, 0.1 W, 0603	Yageo America	RT0603BRD073K01L
R82, R83, R84, R85, R86, R87, R88	7	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060310K0FKEA
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7	7	Mini Shunt, Closed Top, 650 V AC, -45 to 85 degC, Pitch 1.27 mm, Height 3 mm, RoHS	Sullins Connector Solutions	NPB02SVAN-RC
T1, T2	2	Flyback Transformer	Coilcraft	ZA9710-AE
TP1, TP3, TP5, TP7	4	Test Point, Multipurpose, Red, TH	Keystone	5010
TP2, TP4, TP6, TP8, TP11	5	Test Point, Multipurpose, Black, TH	Keystone	5011
TP9	1	Test Point, Multipurpose, White, TH	Keystone	5012
U1, U6	2	LM25180-Q1 42-VIN PSR Flyback DC/DC Converter With 65-V, 1.5-A Integrated MOSFET, NGU0008C (WSON-8)	Texas Instruments	LM25180QNGURQ1

Table 4. List of Materials (continued)

DES	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
U2	1	Single Output High PSRR LDO, 1 A, Adjustable 1.2 to 5.5 V Output, 2.7 to 5.5 V Input, 8-pin SON (DRB), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS79601DRBR
U4, U5	2	Isolated IGBT, SiC MOSFET Gate Driver With Real-Time Programmability, DWJ0036A (SOIC-36)	Texas Instruments	UCC5870-DWJ
C36, C52, C53, C63, C76, C77, C78, C79	0	CAP, CERM, 100 pF, 100 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	MuRata	GCM1885C2A101JA16D
FID1, FID2, FID3	0	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
R31, R63	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA
R34	0	RES, 3.90 k, 0.1%, 0.1 W, 0603	Susumu Co Ltd	RG1608P-392-B-T5

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