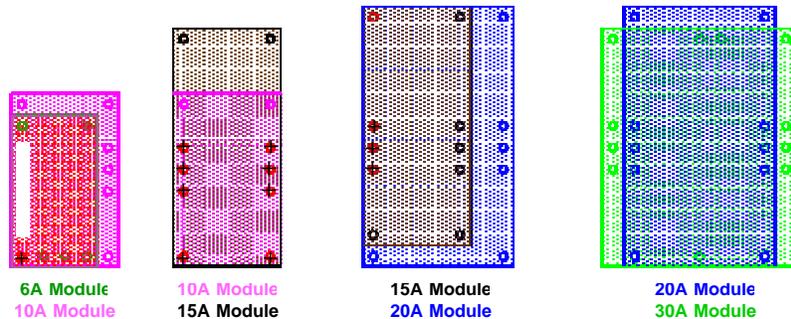


PR252
Virtex-II Pro™ Design 3
Module-based (PTHxxx series) Power Management Solution Providing $I_{CCINT} = 15\text{ A}$
from $V_{IN} = 5.0\text{ V}$ and Featuring Simultaneous Sequencing

FEATURES:

- Simple to use plug-in modules enables fast time-to-market
- High efficiency minimizes heat
- Interchange modules to power one or more FPGAs
 - o 6A to 30A load currents
 - o If current requirements decrease, easy to use dual footprints allow cost reduction without redesign



- o 3.3V, 5V, or 12V input supply
- In-rush current (for charging decoupling caps and FPGA start-up) that places a demand on the input power supply is minimized by the use of optional
 - o Integrated soft-start provides 5 ms rise time for V_{CCINT} and V_{CCO}
 - o Simultaneous sequencing of V_{CCINT} , V_{CCAUX} , then V_{CCO} using the integrated AutoTrack™ feature and a TPS3828 SVS
- High UVLO trip point and integrated soft-start of the PTH series modules eliminates the need for an external Supply Voltage Supervisor (SVS) to monitor the input rail.
- RocketIO™ powered by ultra-low noise, high PSRR (for rejecting noise at the input from translating to the output) low dropout linear regulators (LDOs), TPS79xxx and TPS786xx. This series has been qualified by Xilinx to replace LT1963.
- The design meets Xilinx's V_{CCINT} and V_{CCO} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at <http://www.ti.com/xilinfpga> for more information and other reference designs.

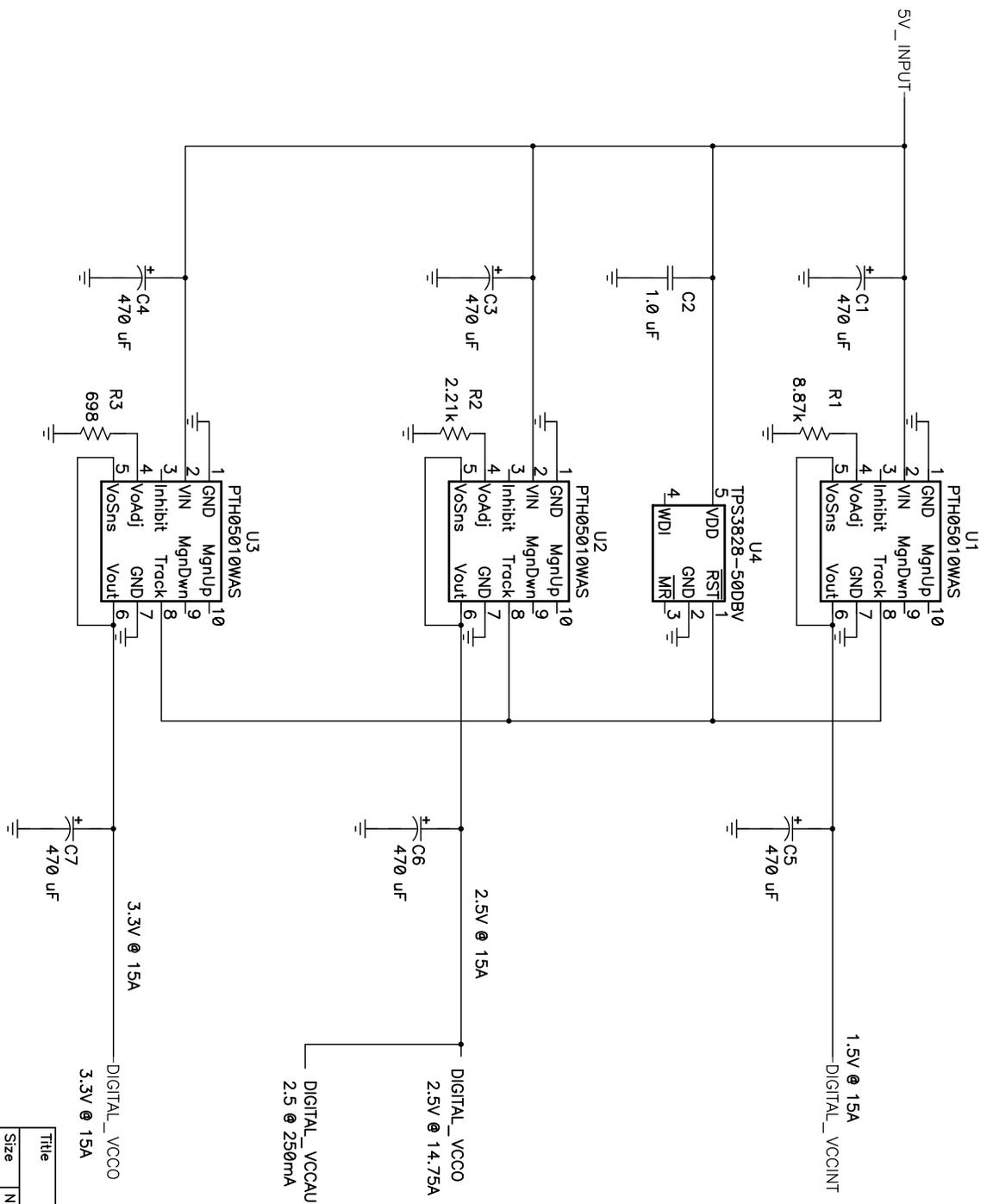
- Link to datasheet at <http://focus.ti.com/lit/ds/symlink/pth05010w.pdf> and <http://focus.ti.com/lit/ds/symlink/tps3828-50.pdf>.

IMPLEMENTATION NOTES:

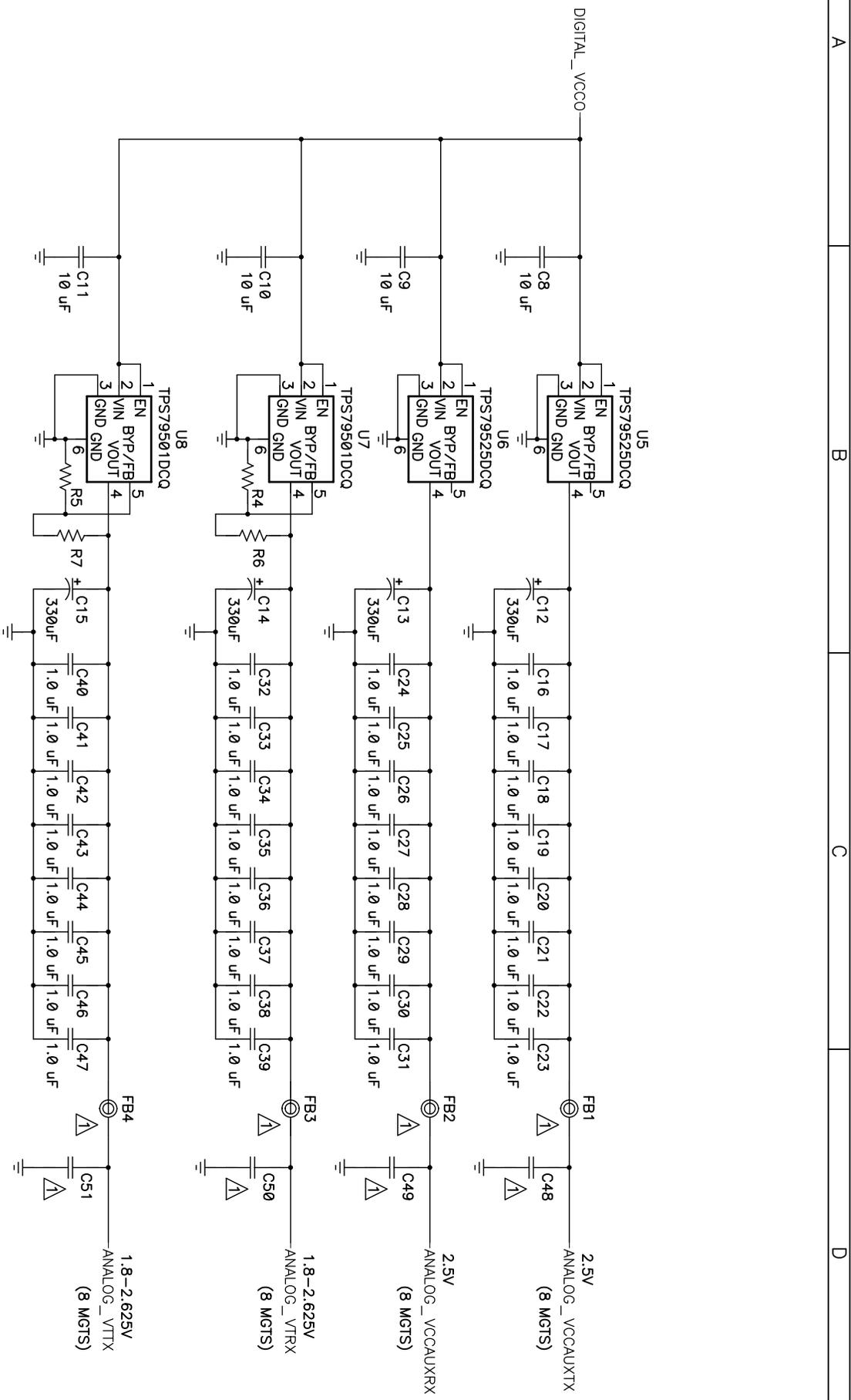
- **Sequencing:** Although sequencing is **not** required by Xilinx FPGAs, simultaneous Sequencing using the AutoTrack feature of the PTH series is useful when the core and I/O voltage difference needs to be minimized during power up. If Sequential Sequencing (there is a short, on the order of milliseconds, time interval between the core and I/O power up, in any order, in order to minimize demand on the input supply) is preferred, please see PR221. If sequencing is not desired, please see PR217.
- **Additional Capacitance:**
 - o The PTH05010 input capacitance requirement may change depending on the application. See the minimum input capacitance required at the bottom of page 3, the computation for determining input capacitance on page 5 as well as recommended capacitors on page 6 of the datasheet.
 - o The PTH05010 device has a limitation to the amount and type of additional capacitance that can be added to its output. See the specifications for external output capacitance and associated ESR at the bottom of page 3 as well as the application note (including recommended output caps) on page 6 of the datasheet.
- **V_{CCAUX} :** V_{CCAUX} powers time-critical resources in the FPGA, including the Digital Clock Managers (DCMs). Therefore, this supply voltage is especially susceptible to power supply noise. V_{CCAUX} can share a power plane with V_{CCO}, but only if V_{CCO} does not have excessive noise. Changes in V_{CCAUX} voltage beyond 200 mV peak-to-peak should take place no faster than 10 mV per millisecond.
- **RocketIO:** When powering the RocketIO:
 - o A_{VCCAUTX}, V_{CCAUXRX}, A_{VTRX}, and A_{VTTX} may each be powered by their own linear regulator or by the same regulator if their voltages are the same. Keep power dissipation capability of the linear regulator package in mind.
 - o Select the appropriate TPS79xxx based on the load current requirement, and the power dissipation capability of the package. In general, the lower the current rating, the lower the price of the linear regulator. Power dissipation of linear regulators is explained in TI Application Note SLVA118.
 - o For the TPS79x01 adjustable devices, size the feedback resistors according to the datasheet. These resistors are not populated in the schematic.
 - o All unused RocketIO transceivers must be connected to power (2.5V) and ground.

QUESTIONS?

- Send an email to <mailto:fpgasupport@list.ti.com>



Title			
Virtex-II Pro Module			
Size	Number	Rev	
B	PR252		
Date	10/13/04	Drawn by	
Filename	pr252.sch	Sheet	1 of 2



Refer to Xilinx's Rocket IO Transceiver User Guide (UG024) for component values

Title	Virtex-II Pro Module		
Size	Number	PR252	Rev
B			
Date	10/13/04		
Filename	pr252.sch		
	Sheet	2	of 2

Filename: PR252_bom.xls					
Date: 04/22/2004					
PR252 BOM					
COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
6	C1, C3, C4, C5, C6, C7	Capacitor, Tantalum, 470-uF, 10-V, 120-milliohm, 20%	7343(D)	Vishay	595D477X0010R2T35
1	C2	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
8	C8, C9, C10, C11, C12, C13, C14, C15	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J225KC01
1	R1	Resistor, Chip, 8.87k-Ohms, 1/16-W, 1%	603	Std	Std
1	R2	Resistor, Chip, 2.21k-Ohms, 1/16-W, 1%	603	Std	Std
1	R3	Resistor, Chip, 698-Ohms, 1/16-W, 1%	603	Std	Std
0	R4, R5, R6, R7	Resistor, Chip, xx-Ohms, 1/16-W, yy%	603		
3	U1, U2, U3	Module, Wide Output Adj, 15A, 0.8V to 3.6V, 5V Input	1.370 X 0.620	TI	PTH05010WAS
1	U4	IC, Processor Supervisory Circuits	SOT23-5	TI	TPS3828-50DBV
2	U5, U6	IC, LDO Linear Regulator Ultralow-Noise High PSRR Fast RF, 500mA, 2.5V	SOT223-6	TI	TPS79525DCQ
2	U7, U8	IC, Utralow-Noise, High PSRR, Fast RF 250 mA, LDO Linear Regulators, AdjV	SOT223-6	TI	TPS79401DCQ

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