User's Guide

TPS54A24 SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS54A24EVM-058 evaluation module (BSR058) as well as for the TPS54A24 dc/dc converter. Also included are the performance characteristics, the schematic, and the bill of materials for the TPS54A24EVM-058.

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1 Introduction

1.1 Background

The TPS54A24 dc/dc converter is a synchronous buck converter designed to provide up to an 10-A output. The input (VIN) is rated for 4.5 V to 17 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54A24 regulator. The RT/CLK pin is configured for 500-kHz switching frequency. The high-side and low-side MOSFETs are incorporated inside the TPS54A24 package along with the gate-drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS54A24 to achieve high efficiencies and helps keep the junction temperature low at high output currents. An external divider allows for an adjustable output voltage. Additionally, the TPS54A24 provides adjustable soft start and undervoltage lockout inputs and a power good output.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54A24EVM-058	V_{IN} = 4.5 V to 17 V	0 A to 10 A

1.2 Performance Characteristics Summary

A summary of the TPS54A24EVM-058 performance characteristics is provided in Table 1-2. Characteristics are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.8 V, unless otherwise specified. The TPS54A24EVM-058 is designed and tested for V_{IN} = 4.5 V to 17 V. The ambient temperature is room temperature (20 to 25°C) for all measurements, unless otherwise noted.

Table 1-2. TPS54A24EVM-058 Performance Characteristics Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			4.5	12	17	V
Input current	V_{IN} = 12 V, I_O = 0 A			18.5		mA
	V_{IN} = 4.5 V, I_O = 10 A			4.57		A
V_{IN} start voltage				4.5		V
V_{IN} stop voltage				4		V
Output voltage setpoint				1.8		V
Output current range	V_{IN} = 4.5 V to 17 V		0		10	A
Load regulation	V_{IN} = 4.5 V to 17 V, I_O = 10 A			–0.1%		
Load transient response	I_O = 2.5 A to 7.5 A	Voltage change		–70		mV
		Recovery time		80		µs
	I_O = 7.5 A to 2.5 A	Voltage change		70		mV
		Recovery time		80		µs
Loop bandwidth	V_{IN} = 12 V, R_O = 0.3 Ω			76		kHz
Phase margin				56		degrees
Input ripple voltage	I_O = 10 A			240		mVPP
Output ripple voltage				7		mVPP
Output rise time				1.3		ms
Operating frequency (f_{SW})				500		kHz
Peak efficiency	TPS54A24EVM-058, V_{IN} = 5 V, I_O = 2 A			94.7%		
	TPS54A24EVM-058, V_{IN} = 12 V, I_O = 3.5 A			91.6%		
IC case temperature	TPS54A24EVM-058, V_{IN} = 12 V, I_O = 10 A, 15-minute soak			62.7		°C

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54A24. Some modifications can be made to this module. When modifications are made to the components on the EVM, the compensation components connected to the COMP pin may need to be changed. Changes to the f_{SW}, output voltage, output

inductor, and output capacitors may require a change in the external compensation. Ensure all components have sufficient voltage and current ratings. Table 1-3 gives some example values for different applications.

1.3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R8 (R_{FBT}) and R6 (R_{FBB}). R6 is fixed at 6.04 kΩ to set the FB divider current at ~100 µA. To change the output voltage of the EVM, the value of resistor R8 must change. Changing the value of R6 can change the output voltage above the 0.6-V reference voltage (V_{REF}). The value of R8 for a specific output voltage can be calculated using Equation 1.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

1.3.2 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R2 (R_{ENT}) and R9 (R_{ENB}). See the TPS54A24 datasheet for detailed instructions for setting the external UVLO.

1.3.3 Component Values to Evaluate Common Output Voltages

Table 1-3 shows recommended modifications to the EVM for evaluating other common output voltages. These recommended component values were selected to keep the output capacitors at the default EVM components to minimize the number of changes. Depending on the load step response requirements in the application, the output capacitors may need to be different from the default EVM components. More or less output capacitance may be used. If the output capacitors are changed, the compensation may also need to be adjusted. Additionally if the f_{SW} is changed, the inductance value (L) may also need to be changed. The TPS54A24 datasheet equations or WEBENCH can be used to calculate the output capacitor value, compensation, f_{SW} and inductance. Ensure all components have sufficient voltage and current ratings.

Table 1-3. Component Values to Evaluate Common Output Voltages

V_{OUT} (V)	f_{SW} (kHz)	R_T (R7) (kΩ)	L (µH)	C_{OUT} (µF)	R_{FBT} (R8) (kΩ)	R_C (R5) (kΩ)	C_C (C18) (nF)	C_P (C17) (pF)	C_{FF} (C19) (pF)
1	500	100	0.68	3x 100	4.02	6.65	4.7	82	330
1.2	500	100	0.82	3x 100	6.04	6.65	4.7	82	220
3.3	500	100	1.8	3x 100	27.4	12.1	2.7	39	47
5	500	100	2.2	3x 100	44.2	12.1	2.7	39	33

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54A24EVM-058 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start-up, and current limit modes. Measurements are taken at room temperature (20 to 25°C) unless otherwise noted.

2.1 Input/Output Connections

The TPS54A24EVM-058 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying greater than 7.5 A must be connected to J1 through a pair of 20-AWG wires or better. Banana jacks J5 and J6 provide an alternative connection to input power supply. The load must be connected to J2 through a pair of 20-AWG wires or better. The maximum load current capability is nearly 15 A before the TPS54A24 goes into current limit. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP7 providing a convenient ground reference. TP4 is used to monitor the output voltage with TP11 as the ground reference.

If modifications are made to the TPS54A24EVM-058 the input current may change. The input power supply and wires connecting the EVM to the power supply must be rated for the input current.

Table 2-1. TPS54A24EVM-058 EVM Connectors and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	VIN screw terminal to connect input voltage (see Table 1-1 for V_{IN} range)
J2	VOUT screw terminal to connect load
J3	2-pin header for enable. Add shunt to connect EN to ground and disable device.
J4	2-pin header for power good resistor pull-up connection. Add a shunt to pull up to VOUT. Populate resistor R3 if VOUT is greater than 5 V to keep the PGOOD pin voltage below its 6.5 V abs max rating.
J5	Banana jack for positive terminal of input power supply
J6	Banana jack for negative terminal of input power supply
TP1	VIN test point
TP2	EN test point. If applying an external voltage, it must be kept below the EN pin's abs max voltage of 6.5 V.
TP3	SW node test point
TP4	Output voltage test point
TP5	PGOOD test point
TP6	PGOOD pull-up test point. Remove the shunt on J4 to provide an external pull-up voltage. The external pull-up voltage must keep the PGOOD pin voltage below its 6.5 V abs max rating.
TP7, TP9, TP11	PGND test point
TP8	SS/TRK test point
TP10	Test point between voltage divider network and output voltage. Used for loop response measurements.
TP12, TP13, TP14	AGND test point
TP15	SMB connector to measure SW node. When using this test point the scope should be set for 50 Ω termination. The combination of 50 Ω termination and R12||R13 creates a 20:1 attenuation.
TP16	SMB connector to measure output voltage. When using this test point the scope should be set for 1 MΩ termination.
TP17	Test point for supplying external CLK for synchronization. C2 and R10 should be populated to use this test point.

2.2 Efficiency

Figure 2-1 shows the efficiency for the TPS54A24EVM-058.

Figure 2-2 shows the efficiency for the TPS54A24EVM-058 using a semi-log scale to more easily show efficiency at lower output currents. The TPS54A24 operates in forced continuous conduction mode at light loads.

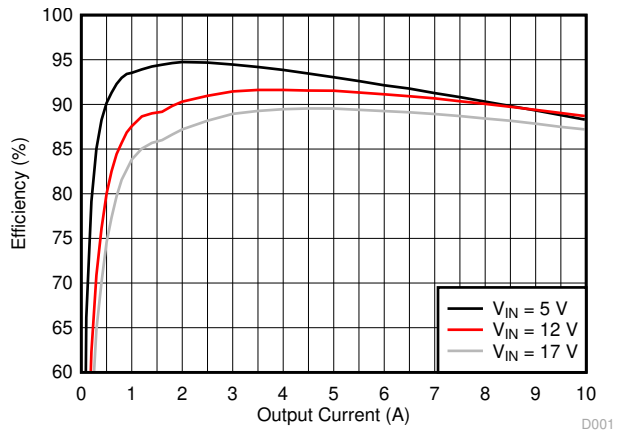

Figure 2-1. TPS54A24EVM-058 Efficiency

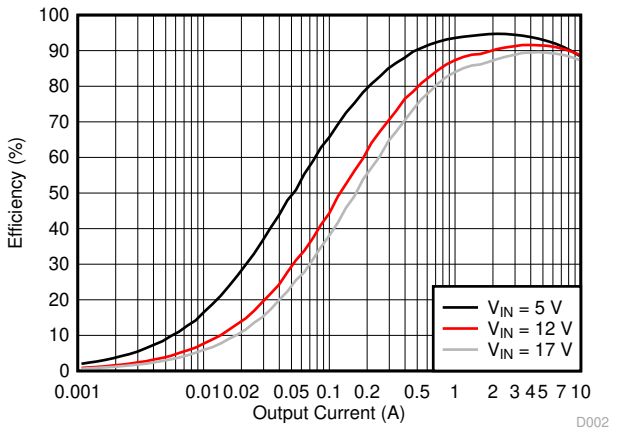

Figure 2-2. TPS54A24EVM-058 Low Current Efficiency

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54A24EVM-058.

Figure 2-4 shows the line regulation for the TPS54A24EVM-058.

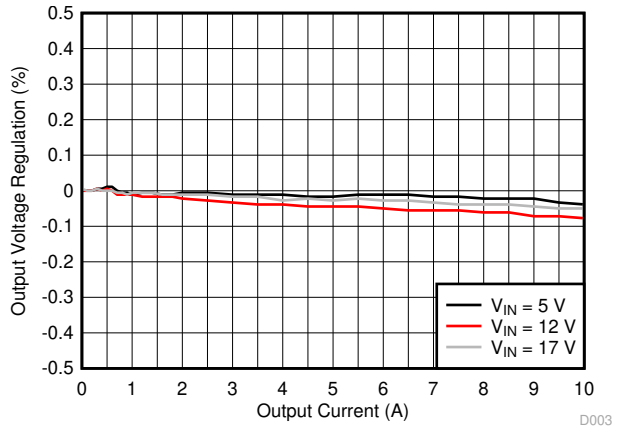

Figure 2-3. TPS54A24EVM-058 Load Regulation

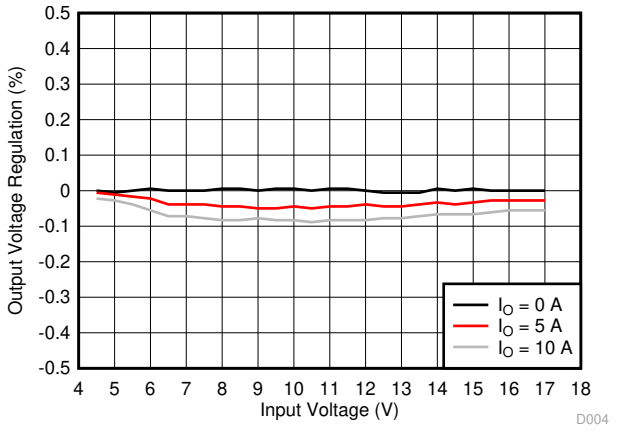

Figure 2-4. TPS54A24EVM-058 Line Regulation

2.4 Load Transient and Loop Response

Figure 2-5 shows the TPS54A24EVM-058 response to load transients. The current step is from 2.5 A to 7.5 A and the current step slew rate is 1 A/µs. The VOUT voltage is measured using TP16.

Figure 2-6 shows the TPS54A24EVM-058 loop response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V and a 0.3 Ω resistive load.

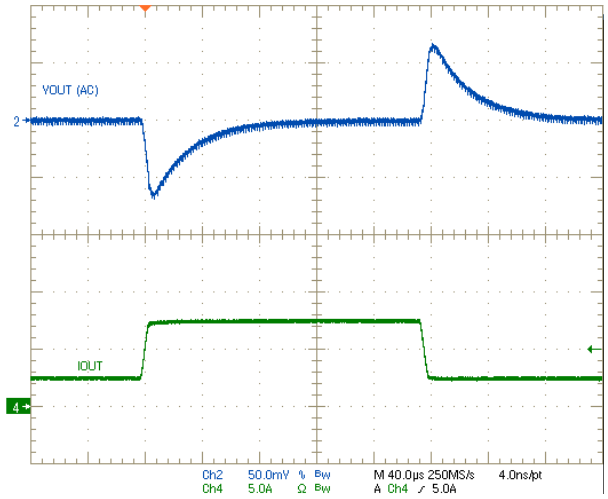

Figure 2-5. TPS54A24EVM-058 Transient Response

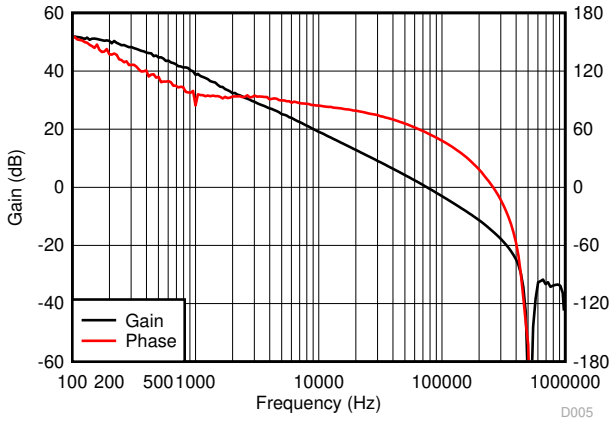

Figure 2-6. TPS54A24EVM-058 Loop Response

2.5 Output Voltage Ripple

Figure 2-7 and Figure 2-8 show the TPS54A24EVM-058 output voltage ripple. The load currents are no load and 10 A. V_{IN} = 12 V. The VOUT voltage is measured using TP16 and the SW voltage is measured using TP15.

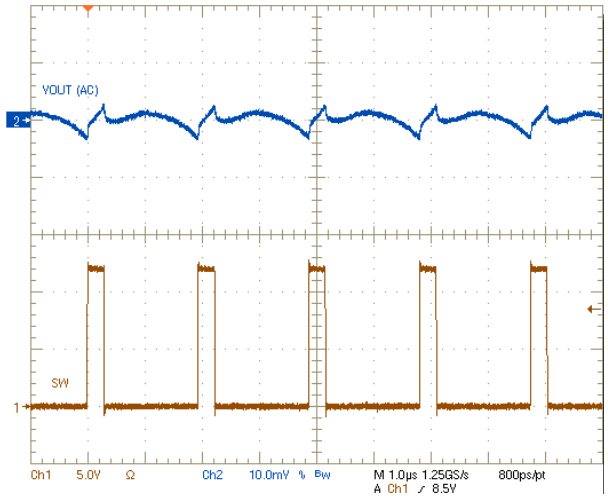

Figure 2-7. TPS54A24EVM-058 Output Ripple, No Load

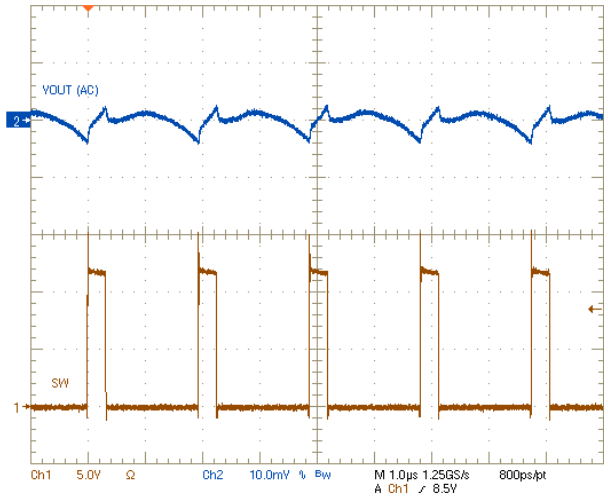

Figure 2-8. TPS54A24EVM-058 Output Ripple, 10-A Load

2.6 Input Voltage Ripple

Figure 2-9 and Figure 2-10 show the TPS54A24EVM-058 input voltage ripple. The load currents are no load and 10 A. V_{IN} = 12 V. The ripple voltage is measured directly across TP1 and TP7.

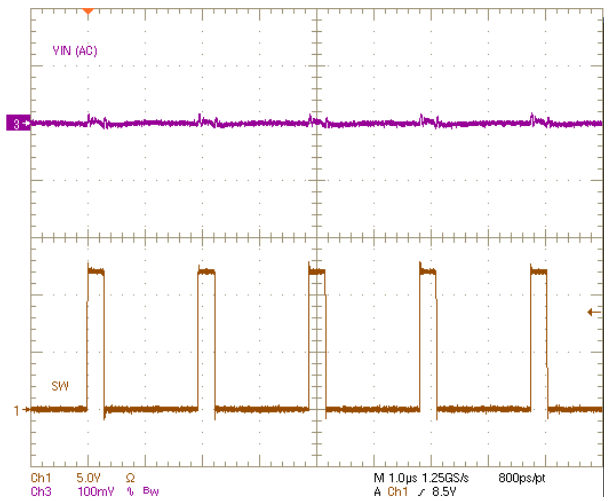

Figure 2-9. TPS54A24EVM-058 Input Ripple, No Load

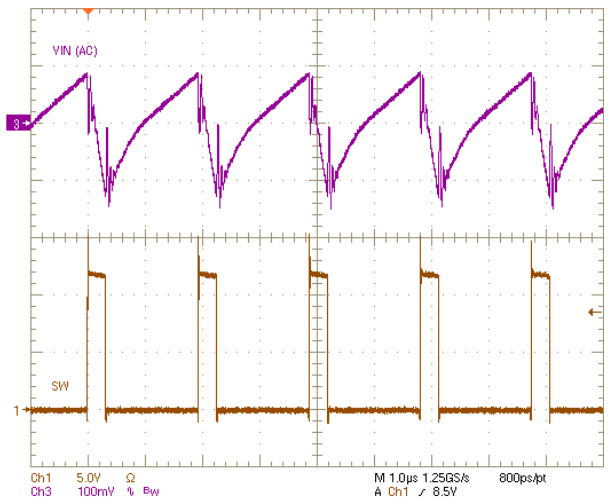

Figure 2-10. TPS54A24EVM-058 Input Ripple, 10-A Load

2.7 Powering Up

Figure 2-11 and Figure 2-12 show the start-up waveforms for the TPS54A24EVM-058. In Figure 2-11, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold. In Figure 2-12, the input voltage is initially applied and the output is inhibited by pulling EN to GND using an external function generator. When the EN voltage is increased above the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.8 V. The input voltage for these plots is 12 V and the load is 1.8 Ω. Alternatively, a jumper at J3 to tie EN to GND can also be used. When the jumper is removed, EN is released and the start-up sequence begins.

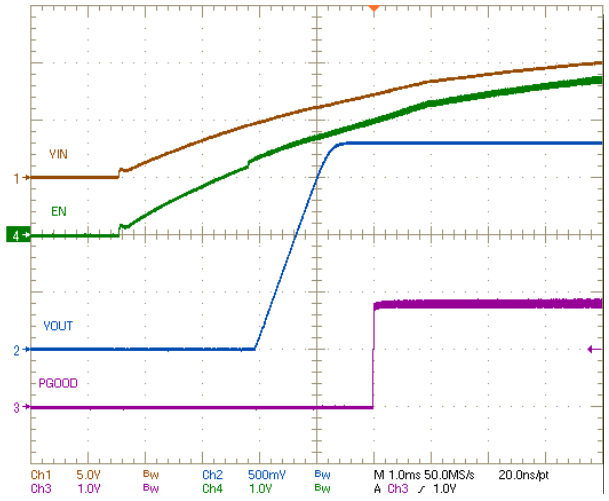

Figure 2-11. TPS54A24EVM-058 Start-Up Relative to V_{IN}

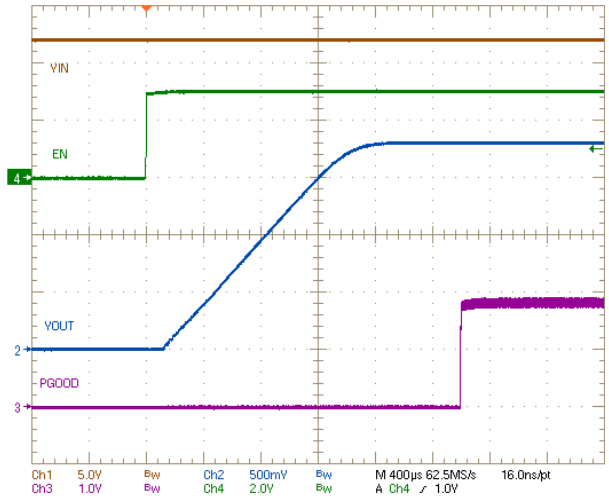

Figure 2-12. TPS54A24EVM-058 Start-Up Relative to Enable

2.8 Powering Down

Figure 2-13 and Figure 2-14 show the TPS54A24EVM-058 shutdown. The input voltage for these plots is 12 V and the load is 1.8 Ω.

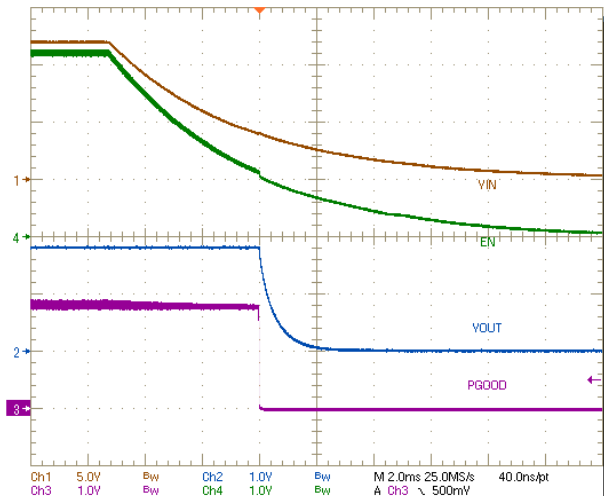

Figure 2-13. TPS54A24EVM-058 Shutdown Relative to V_{IN}

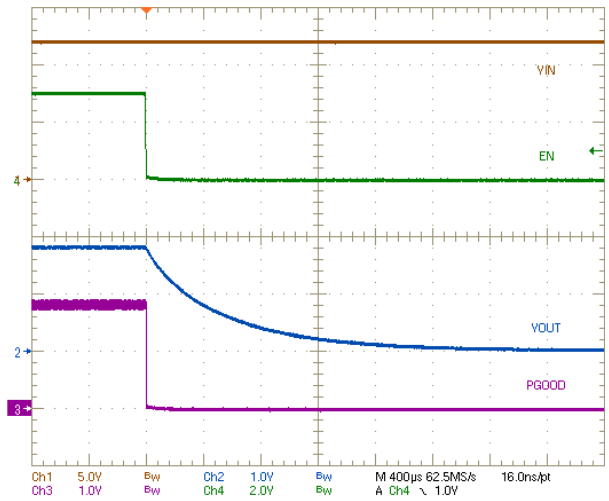

Figure 2-14. TPS54A24EVM-058 Shutdown Relative to Enable

2.9 Start-Up Into Pre-Bias

Figure 2-15 shows the TPS54A24EVM-058 start up into a pre-biased output. The output voltage is pre-biased to 1 V through a 100-Ω resistor.

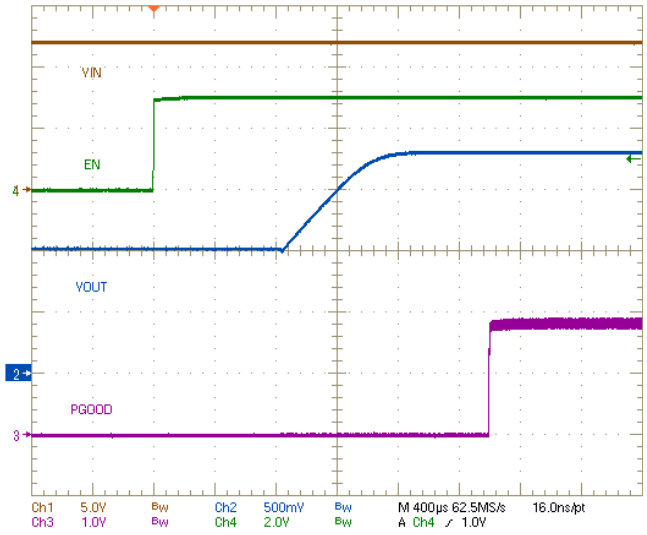

Figure 2-15. TPS54A24EVM-058 Start-Up Into Pre-Bias

2.10 Hiccup Mode Current Limit

Figure 2-16, Figure 2-17, and Figure 2-18 show the TPS54A24 hiccup current limit feature. If a current limit event persists for the wait-time before hiccup, the TPS54A24 shuts down. The TPS54A24 restarts after the hiccup time.

Figure 2-16 shows the TPS54A24EVM-058 entering hiccup with a short circuit on the output. The initial overshoot in the output current is the output capacitors discharging. Figure 2-17 shows the TPS54A24EVM-058 entering hiccup with a longer timescale to show the hiccup period. Figure 2-18 shows the TPS54A24EVM-058 exiting hiccup after the short circuit was removed.

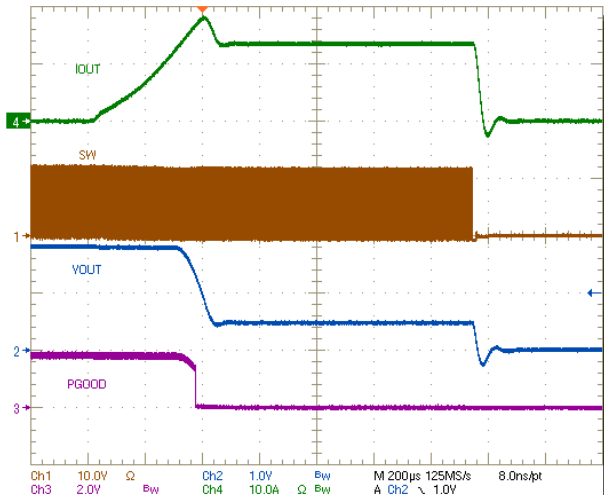

Figure 2-16. TPS54A24EVM-058 Hiccup Current Limit

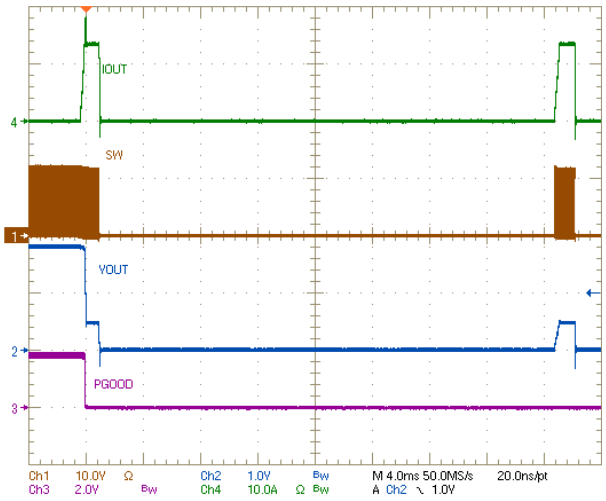

Figure 2-17. TPS54A24EVM-058 Hiccup Start

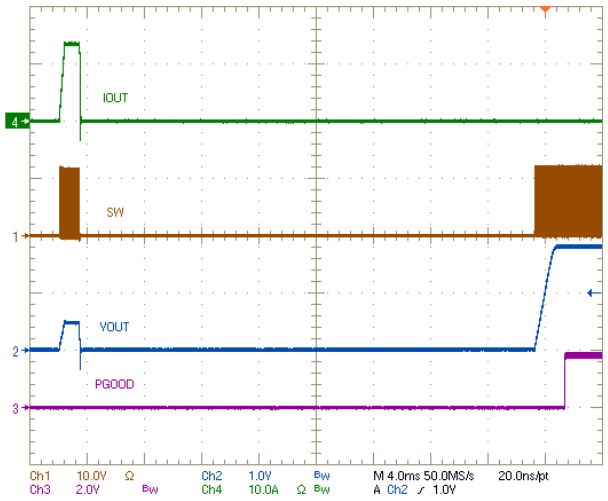

Figure 2-18. TPS54A24EVM-058 Hiccup Stop

2.11 Thermal Performance

Figure 2-19 shows the temperature rise of the TPS54A24 IC and the inductor versus load current. A 15 minute soak time was used before taking each measurement..

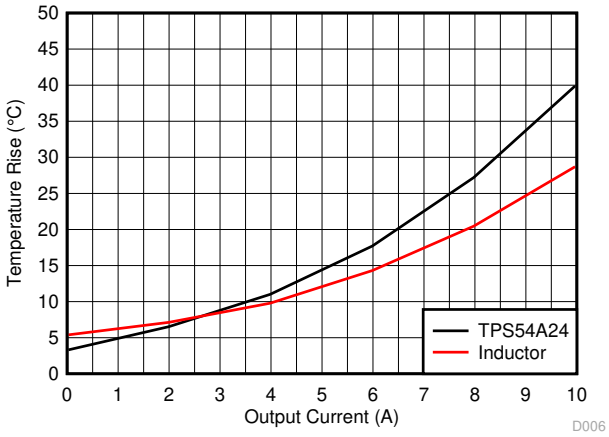

Figure 2-19. TPS54A24EVM-058 Thermal Performance

3 Board Layout

This section provides a description of the TPS54A24EVM-058 board layout and layer illustrations.

3.1 Layout

The board layout for the TPS54A24EVM-058 is shown in Figure 3-1 through Figure 3-6. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for VIN, VOUT, and SW. Also on the top layer are connections for the remaining pins of the TPS54A24 and the majority of the signal traces. The top layer has dedicated ground plane for quiet analog ground that is connected to the main power ground plane at a single point. The mid layer 1 is a large ground plane and also routes signals to test points. The mid layer 2 contains an additional large ground copper area with the BOOT trace and an additional VIN and VOUT copper fill. The bottom layer is another ground plane with the trace for the output voltage feedback and traces from signals to test points. The top-side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the TP4 test point. An additional input bulk capacitor is used to limit the noise entering the converter from the input supply. Critical analog circuits such as the voltage set point divider, EN resistor, SS/TRK capacitor, RT/CLK resistor, and COMP pin are terminated to the quiet analog ground (AGND) island on the top layer.

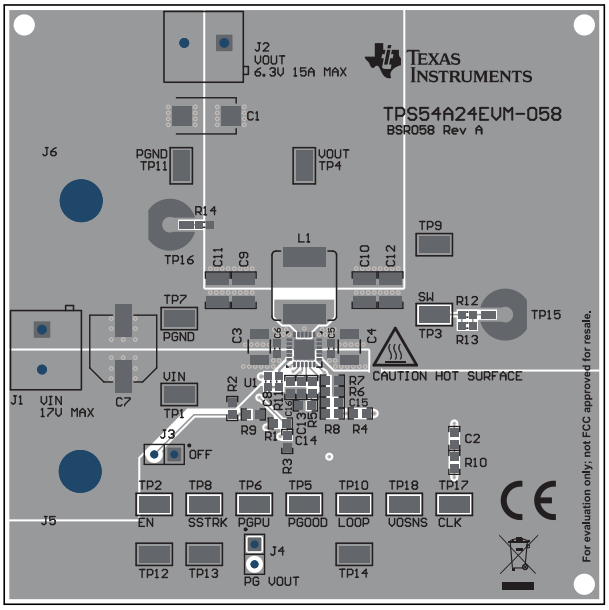

Figure 3-1. Top-Side Composite View

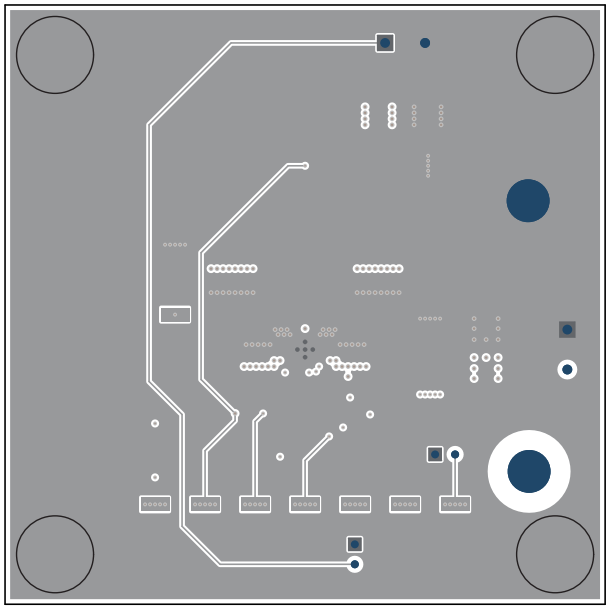

Figure 3-2. Bottom-Side Composite View (Viewed From Bottom)

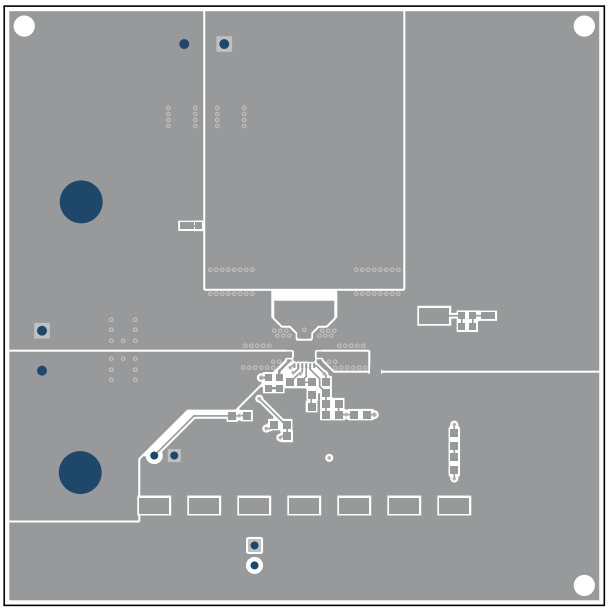

Figure 3-3. Top Layer Layout

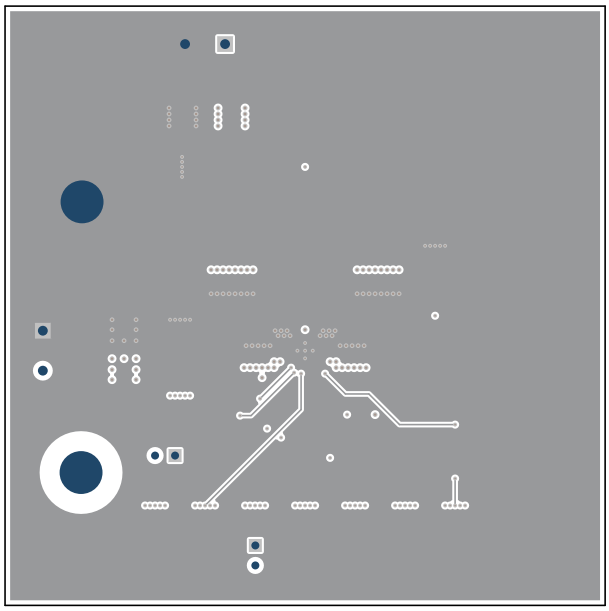

Figure 3-4. Mid Layer 1 Layout

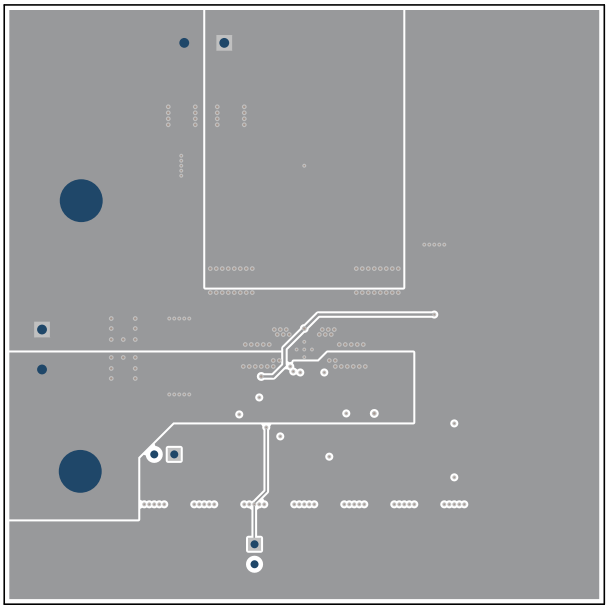

Figure 3-5. Mid Layer 2 Layout

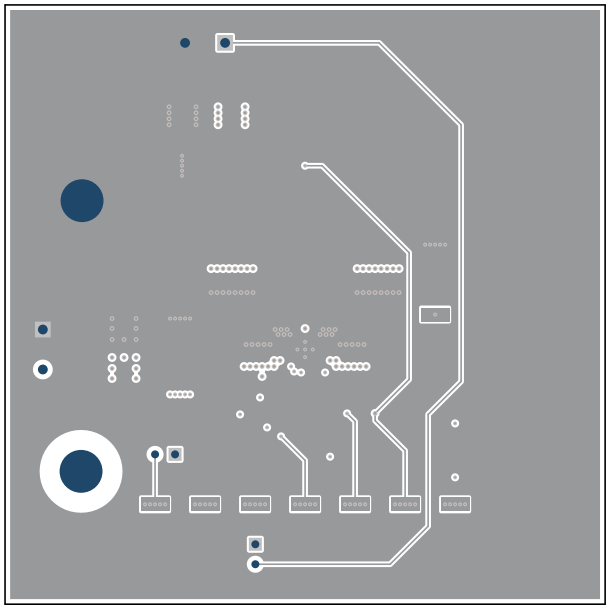

Figure 3-6. Bottom Layer Layout

4 Schematic and Bill of Materials

This section presents the TPS54A24EVM-058 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54A24EVM-058.

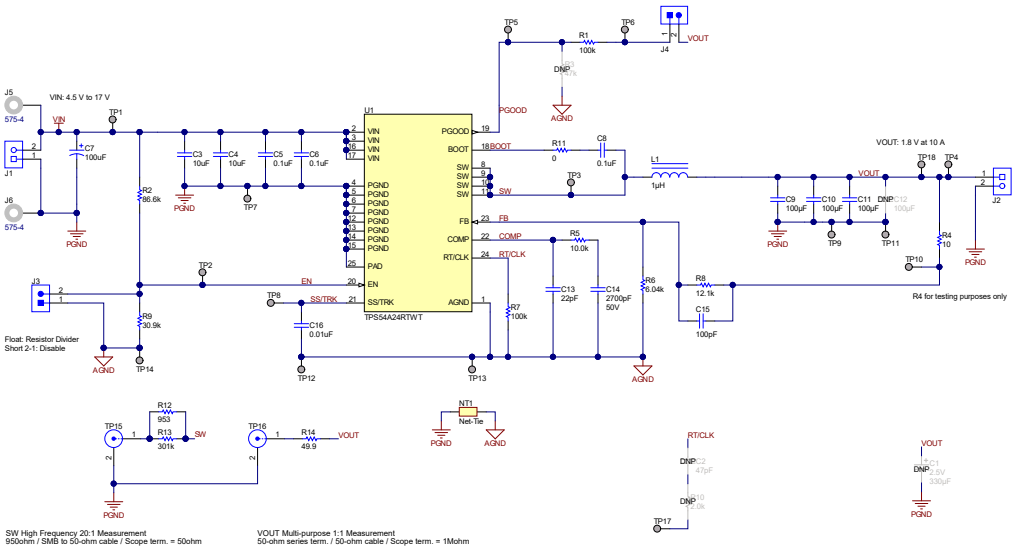

Figure 4-1. TPS54A24EVM-058 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54A24EVM-058.

Table 4-1. TPS54A24EVM-058 Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		BSR058	Any
BO1, BO2, BO3, BO4	4		Bumpon, Hemisphere, 0.375 X 0.235, Black	Black Bumpon	SJ61A2	3M
C3, C4	2	10uF	CAP, CERM, 10 uF, 25 V, +/- 20%, X7R, 1210	1210	C3225X7R1E106M250AC	TDK
C5, C6, C8	3	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	0603	06033C104KAT2A	AVX
C7	1	100uF	CAP, AL, 100 uF, 35 V, +/- 20%, 0.16 ohm, AEC-Q200 Grade 2, SMD	SMT Radial F	EEE-FK1V101P	Panasonic
C9, C10, C11	3	100uF	CAP, CERM, 100 µF, 6.3 V,+/- 20%, X7S, 1210	1210	GRM32EC70J107ME15L	MuRata
C13	1	22pF	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	C0603C220J5GACTU	Kemet
C14	1	2700pF	CAP, CERM, 2700 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H272JA01D	MuRata
C15	1	100pF	CAP, CERM, 100 pF, 10 V, +/- 10%, X7R, 0603	0603	0603ZC101KAT2A	AVX
C16	1	0.01uF	CAP, CERM, 0.01 uF, 100 V, +/- 10%, X7R, 0603	0603	C0603C103K1RACTU	Kemet
J1, J2	2		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J3, J4	2		Header, 100mil, 2x1, Gold, TH	Header, 100mil, 2x1, TH	HTSW-102-07-G-S	Samtec
J5, J6	2		Standard Banana Jack, Uninsulated, 5.5mm	Keystone_575-4	575-4	Keystone
L1	1	1uH	Inductor, Shielded, Powdered Iron, 1 µH, 14 A, 0.00463 ohm, SMD	9.2x8.5mm	74437358010	Wurth Elektronik
R1, R7	2	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	RC0603FR-07100KL	Yageo
R2	1	86.6k	RES, 86.6 k, 1%, 0.1 W, 0603	0603	RC0603FR-0786K6L	Yageo
R4	1	10	RES, 10, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0JNEA	Vishay-Dale
R5	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic
R6	1	6.04k	RES, 6.04 k, 1%, 0.1 W, 0603	0603	RC0603FR-076K04L	Yageo
R8	1	12.1k	RES, 12.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0712K1L	Yageo
R9	1	30.9k	RES, 30.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060330K9FKEA	Vishay-Dale
R11	1	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3GEY0R00V	Panasonic
R12	1	953	RES, 953, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603953RFKEA	Vishay-Dale
R13	1	301k	RES, 301 k, 1%, 0.1 W, 0603	0603	RC0603FR-07301KL	Yageo
R14	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo
SH-J1, SH-J2	2	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP17, TP18	16		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
TP15, TP16	2		Connector, Receptacle, 50 ohm, TH	SMB Connector	SMBR004D00	JAE Electronics
U1	1		4.5-V to 17-V Input, Current Mode, 10-A Synchronous SWIFT(TM) Step-Down Converter, RTW0024B (WQFN-24)	RTW0024B	TPS54A24RTWT	Texas Instruments

Table 4-1. TPS54A24EVM-058 Bill of Materials (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1	0	330uF	CAP, Aluminum Polymer, 330 µF, 2.5 V,+/- 20%, 0.006 ohm, 7343-20, SMD	7343-20	EEFSX0E331XE	Panasonic
C2	0	47pF	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A470JAT2A	AVX
C12	0	100uF	CAP, CERM, 100 µF, 6.3 V,+/- 20%, X7S, 1210	1210	GRM32EC70J107ME15L	MuRata
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R3	0	47k	RES, 47 k, 5%, 0.1 W, 0603	0603	RC0603JR-0747KL	Yageo
R10	0	2.0k	RES, 2.0 k, 5%, 0.1 W, 0603	0603	RC0603JR-072KL	Yageo

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2019) to Revision A (August 2021)	Page
• Updated user's guide title	3
• Updated the numbering format for tables, figures, and cross-references throughout the document.	3

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