*User's Guide*

# *TPS6594x-Q1 Evaluation Module*


**ABSTRACT**

The TPS6594x-Q1 and TPS6593x-Q1 evaluation modules (EVM) highlight the performance and flexibility of the TPS6594x-Q1 and TPS6593x-Q1 power management ICs (PMICs). The modular design allows the EVMs to be stacked, which provides a multi-PMIC solution and increases the scalability of these EVMs to develop and evaluate a wide range of power applications. The scalability of the products supports up to six devices, with one primary and up to five secondary PMICs. This document enumerates the features and interfaces provided to develop and evaluate the PMIC.


| | Warning | Warning Hot surface.<br>Contact may cause burns.<br>Do not touch! |
|---|---|---|

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# 1 Introduction

The TPS65941x-Q1 PMIC family is extremely flexible and scalable, providing configurability at the device and system level. At the device level, a single PMIC can provide up to five separate step down converters (BUCK regulators) and four LDOs. Four of these BUCK regulators can be used in multi-phase mode to provide a single 14 A source. At the system level, several PMICs can be configured to work in a master-slave topology with one master and up to five slave PMICs. The TPS65941x-Q1 EVM is both an evaluation and development tool. With the EVM both device level and system level configurability are available through an easy to use graphical user interface (GUI) tool.

Table 1-1 shows the available master and slave EVMs, the silicon associated with those EVMs, the initial non-volatile memory (NVM) configuration, and the hardware components associated with the configurations. Any EVM can be configured as a master or slave device because of the configurable nature of both the part and the EVM. Master and slave configurations are provided to facilitate getting started and to accelerate development.

**Table 1-1. EVM Descriptions**

| PMIC Device Part Number | Mode | NVM Phase Configuration | Components on the Back Side of the EVM | | EVM Part Number |
|---|---|---|---|---|---|
| | | | R1-R7 | J23,J24,J25 | |
| PTPS65940400RWERQ1 | Single PMIC | 1+1+1+1 | R1, R3,R5, R7 | None | TPS6594EVM |
| PTPS65930400RWERQ1 | Single PMIC | 1+1+1+1 | R1, R3,R5, R7 | None | TPS6593EVM |

# 2 Getting Started

The USB must be connected to a host PC in order to evaluate the EVM, because the default configuration does not enable the regulators. A type-A to type-C cable is provided with the EVM to connect to the host computer. The EVM will enumerate as two COM ports and one additional port for the devices firmware updates. The Scalable PMIC GUI will provide an interface to configure the regulators for evaluation. Please refer to the SLVUBT8 for more information.

The USB can also be used to provide power to the PMIC but it is not recommended when evaluating the regulators. The remainder of this document describes the different connectors and jumpers available on the EVMs.

Figure 2-1 and Figure 2-2 shows the TPS6594EVM and the TPS6593EVM respectively.

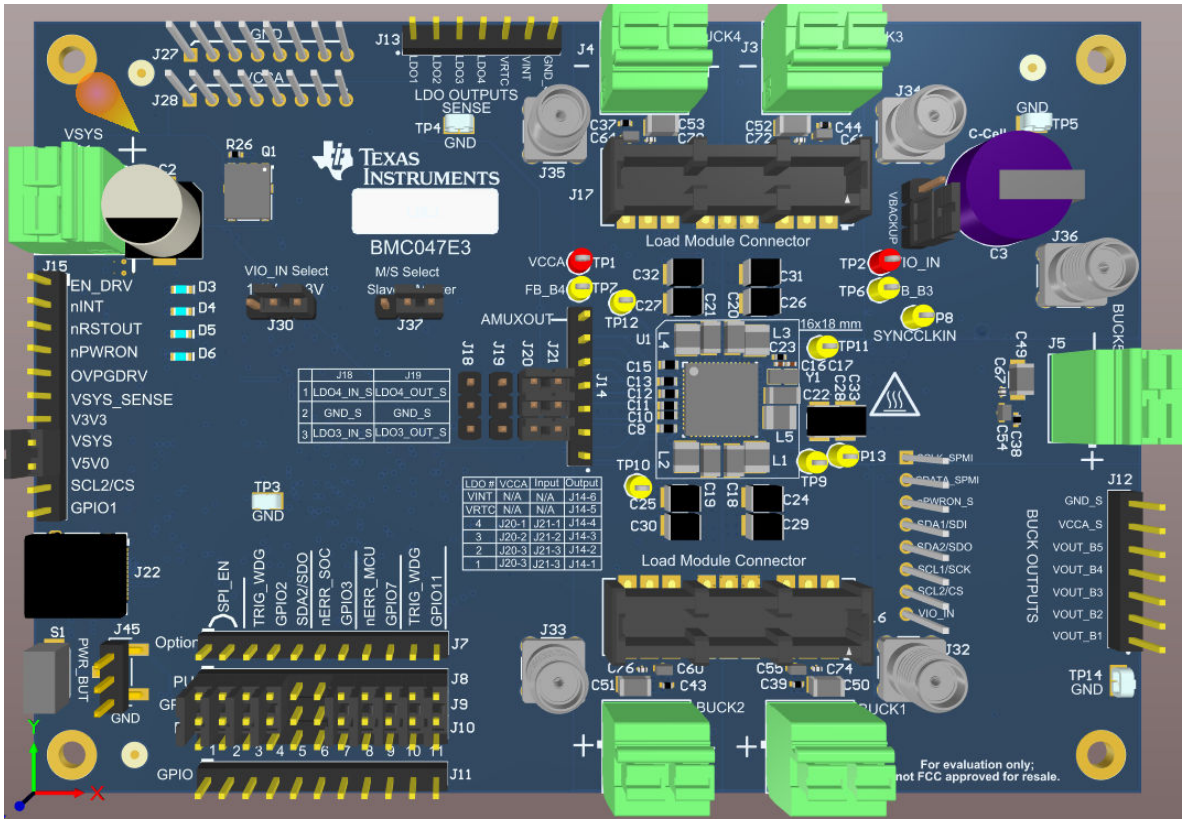


**Figure 2-1. TPS6594EVM Top View**

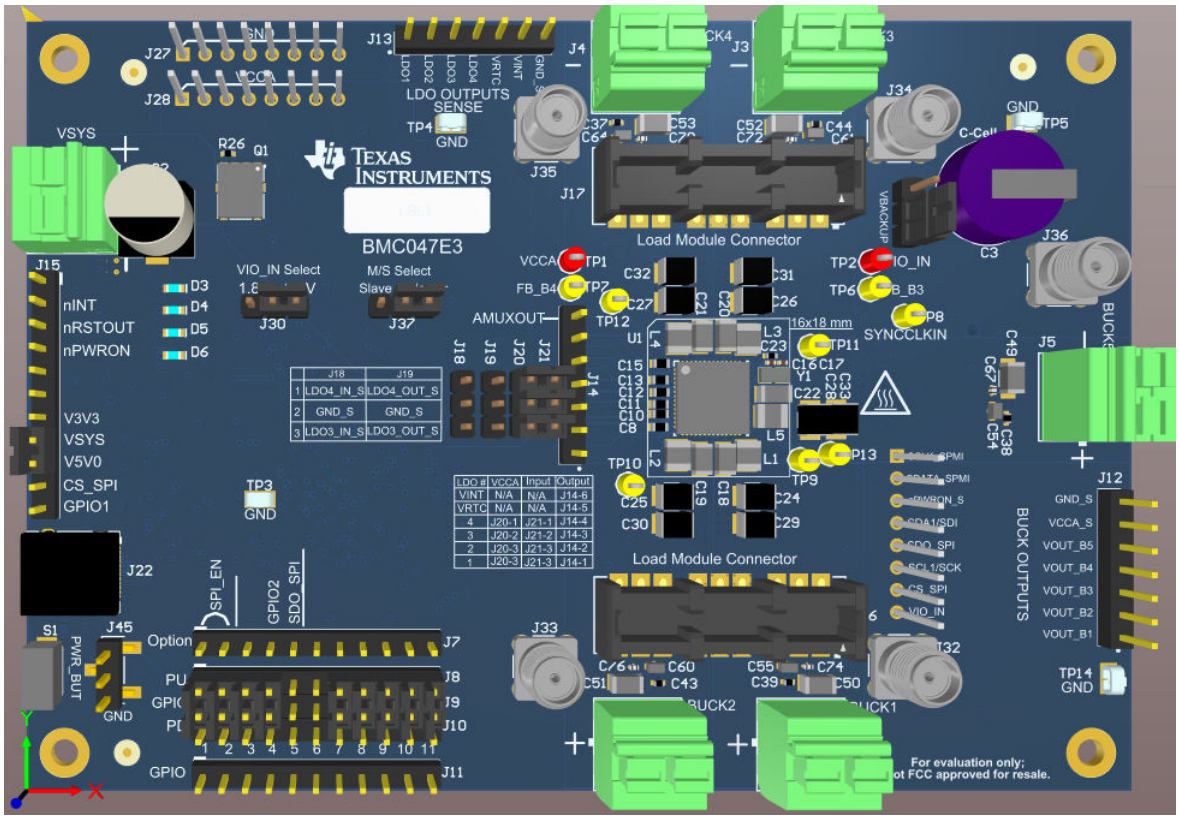


**Figure 2-2. TPS6593EVM Top View**

### 2.1 Getting Started: Single EVM

1. Connect Power to the EVM.
2. Connect the EVM to the Host PC through the USB. In the event that the power is provided by the USB cable, apply the appropriate jumper connection to connect VBUS and VSYS see Table 3-7.
3. Launch the GUI and evaluate.

Terminal J6, labeled VSYS_IN in Figure 2-1 and Figure 2-2, can accept wire gauges up to 14 AWG. The voltage supplied must be within the input range of the device, 2.7 V to 5.5 V. The power supply providing the input to VSYS_IN is required to supply 120% of the output power. Once power has been supplied to VSYS_IN, the pullup on nPWRON/ENABLE pin will enable the device and the power output rails will activate. The default ON Request for the master device is the ENABLE pin which is a level sensitive input. Please refer to SLVSEA7 for more details.

### 2.2 Getting Started: Multiple EVM Evaluation

1. Connect Power to one EVM and remove the jumpers on all EVMs shorting VBUS and VSYS. All VCCA and GND power pins are shared between the stacked EVMs.
2. Connect one EVM to the Host PC through the USB. In the event that the power is provided by the USB cable, apply the appropriate jumper connection to connect VBUS and VSYS see Table 3-7.
3. Stack Master EVM and one or more Slave EVMs. For convenience it is recommended to place the Master on the top of the stack.
4. Launch the GUI and evaluate.

The EVM can be powered solely from the 5 V USB connection (either 5V VUSB or 3.3V USB_3V3), provided that the total load does not exceed the USB. This removes the requirement for a separate supply when evaluating a number of the digital features of the PMIC with the EVM.

The three distinguishing characteristics of the slave EVM are the PMIC, the backside components described in Figure 4-3, and the jumper position on J37. With the jumper on J37 placed in the slave position, the ENABLE pin of the slave PMIC is connected to the VOUT_LDOINT output pin of the master PMIC through the J29 Stack-up header. Once the master and slave devices are stacked, supplying power on J6 is the only requirement for getting started. VSYS_IN is connected to VCCA and distributed across all stacked boards through J28. The power supply can be applied to any of the available J6 terminals.

### 2.3 The GUI Tool

Texas Instruments provides a GUI tool to enable, configure, and evaluate the various features of the TPS6594x-Q1 with the EVM. Please refer to the GUI User's Guide SLVUBT8 for a more detailed description of this tool.

The GUI will run on most PC platforms and requires an available USB port. The EVM USB connector is type-C and a type-A to type-C cable is provided with the EVM to connect to the host computer. The EVM will enumerate as two COM ports and one additional port for the devices firmware updates. The port the GUI should use is the ACCtrl COM port (and not the ACCtrl Console).

## 3 EVM Details

The following sections describe the various interfaces for measuring and controlling the configuration. Note: the configurations are in coordination with the settings of the PMIC. It is important to understand that both the EVM configuration and the settings of the PMIC must match. For example, if the GUI is used to change the PMIC interface to SPI from $I^2C$, then the appropriate SPI related jumpers should be in place on J7 and J15. Refer to the GUI User's Guide SLVUBT8 on how to update the PMIC communication protocol.

## 3.1 Differences Between the TPS6594EVM and the TPS6593EVM

The TPS6593EVM does not provide the functional safety features which are found on the TPS6594EVM. Table 3-1 lists the component differences between the EVMs which are related to functional safety.

**Table 3-1. Differences Between TPS6594EVM and TPS6593EVM**

| Part | TPS6594EVM | TPS6593EVM | Description(1) |
|---|---|---|---|
| D1 | Fitted | Not Fitted | Protection Diode for VSYS_SENSE |
| Q1 | Fitted | Not Fitted | Protection FET controlled by OVPGDRV |
| R20 | Fitted | Not Fitted | Current Limiting resistor for VSYS_SENSE |
| R21 | Fitted | Not Fitted | Current Limiting resistor for VSYS_SENSE |
| R25 | Not Fitted | Fitted | Connect VSYS and VCCA |
| R26 | Fitted | Not Fitted | Connect OVPGDRV to Q1 |
| R39 | Fitted | Not Fitted | Connect VSYS_SENSE to VSYS |
| R35 | Fitted | Not Fitted | Connect EN_DRV to LED indicator D5 through U2 |

(1) Unless specifically described the features are the same between the TPS6594EVM and the TPS6593EVM.

## 3.2 Terminal Blocks

The terminal blocks are simple push and release terminals which can accommodate wire sizes up to 14 AWG. Table 3-2 lists the terminal blocks found around the perimeter of the EVM. J6, VSYS, is the input voltage for all regulators (BUCK and LDO).[1] The remaining 5 terminal blocks are the BUCK outputs.

**Table 3-2. Terminal Blocks**

| Terminal | Designator | Description |
|---|---|---|
| VSYS | J6 | All Regulator Input (PVIN_LDOx, PVIN_Bx), 2.7 V to 5.5 V Range |
| BUCK1 | J1 | Buck 1 Output, 3.5 A Capable |
| BUCK2 | J2 | Buck 2 Output, 3.5 A Capable |
| BUCK3 | J3 | Buck 3 Output, 3.5 A Capable |
| BUCK4 | J4 | Buck 4 Output, 4 A (single phase) or 3.5 A Capable |
| BUCK5 | J5 | Buck 5 Output, 2 A Capable |

[1] See Section 3.5 for applying input voltages other than VSYS to the LDO regulators through J21

## 3.3 Test Point Descriptions

Numerous test points are provided to access voltages and signals. All test points are designed for sensing voltages only and are not designed to carry large DC currents.

**Table 3-3. Test Point Descriptions**

| Test Point | Device Pin | Description |
|---|---|---|
| TP1 | VCCA | This point can be used to measure IDDQ, when resistor R58 is removed. |
| TP2 | VIO_IN | This point can be used to measure IDDQ when resistor R65 is removed. |
| TP3, TP4, TP5 | GND | NA |
| TP6 | FB_B3 | External voltage monitor connection. |
| TP7 | FB_B4 | |
| TP8 | GPIO10 (SYNCCLKIN) | Sync Clock input, up to 4.4 Mhz |
| TP9 | SW_B1 | Test Point for the switch node. Not populated to reduce EMI. |
| TP10 | SW_B2 | |
| TP11 | SW_B3 | |
| TP12 | SW_B4 | |
| TP13 | SW_B5 | |
| TP14 | GND | NA |

## 3.4 Configuration Headers

There are six headers available to configure the EVM function. Headers J26 and J37 configure the backup power supply and master and slave mode of operation respectively. J45 is connected to J37, which can pull the nPWRON/ENABLE pin of the PMIC to a logic high or low. Header J7, as shown in the silk screen picture in Figure 3-1 and Figure 3-2, is used to configure the EVM to match the feature setting written to the device configuration registers. J30 is used to select the PMIC IO voltage, either 1.8 V or 3.3 V. The sixth header is a portion of J15, which allows VSYS to be powered from the USB connection and the configuration of GPIO1.

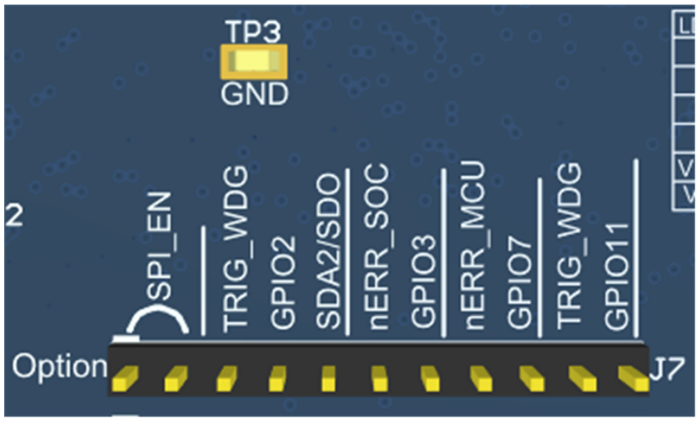


**Figure 3-1. TPS6594EVM Header J7**

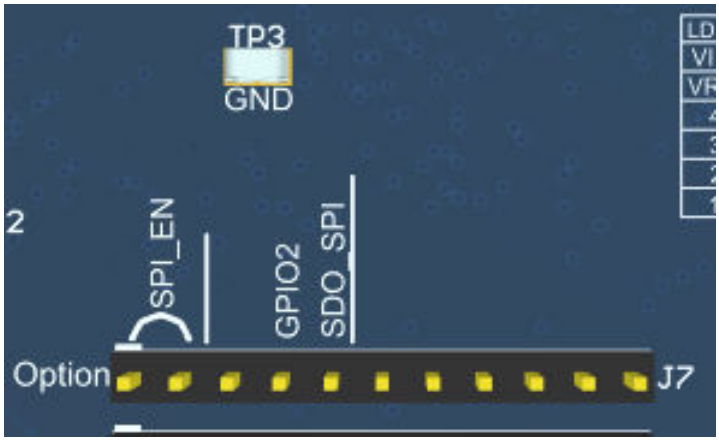


**Figure 3-2. TPS6593EVM Header J7**

**Table 3-4. TPS6594EVM Header J7 Description**

| Option Pins | Configuration | Description | |
|---|---|---|---|
| SPI_EN | Open (Default) | $I^2C$ Mode. The signal path for $I^2C$ communication between the MCU and the PMIC is enabled. | |
| | Closed | SPI mode. The signal path for SPI communication between the MCU and the PMIC is enabled. | |
| TRIG_WDG, GPIO2, SDA2/SDO | Open | GPIO mode. GPIO2 from PMIC is connected to PM7 of the MCU through a level translator. | |
| | TRIG_WDG, GPIO2: Closed | Trigger Watchdog mode. GPIO2 of the PMIC should be in the Alternative function to support the watchdog trigger input signal. GPIO2 from the PMIC is connected to the MCU output and TRIG_WDG. | |
| | GPIO2,SDA2/SDO: Closed (Default) | $I^2C$ Mode (J7 VIO_IN, I2C/SPI: Open) | Q&A Watchdog mode. GPIO2 of the PMIC should be in the Alternative function to support the Q&A Watchdog and the $I^2C$ mode is selected. This setting is done in conjunction with J15, GPIO1,SCL2/CS: Closed. |
| | | SPI mode (J7 VIO_IN, I2C/SPI: Closed) | SPI mode, Chip Select. GPIO2 of the PMIC should be in the Alternative function to support SPI communication. This setting is done in conjunction with J15, GPIO1, SCL2/CS: Closed. |
| ERR_SoC, GPIO3 | Open (Default) | GPIO mode. GPIO3 of the PMIC is connected to PP5 of the through a level translator. | |
| | Closed | SoC Error Count Down mode. GPIO3 of the PMIC should be in the Alternative function to support the system error count down from the SoC. GPIO is connected to alternative MCU output, nERR_SoC. | |
| ERR_MCU, GPIO7 | Open (Default) | GPIO mode. GPIO7 of the PMIC is connected to POH of the through a level translator. | |
| | Closed | MCU Error Count Down mode. GPIO7 of the PMIC should be in the Alternative function to support the system error count down from the MCU. GPIO7 is connected to MCU output PK5, nERR_MCU. | |
| TRIG_WDG, GPIO11 | Open (Default) | GPIO mode. GPIO11 from PMIC is connected to PP4 of the MCU through a level translator. | |
| | Closed | Trigger Watchdog mode. GPIO11 of the PMIC should be in the Alternative function to support the watchdog trigger input signal. GPIO11 from the PMIC is connected to the MCU output PK4, TRIG_WDG. | |

**Table 3-5. Header J26, VBACKUP**

| Configuration | Description |
|---|---|
| Open | VBACKUP is not connected. |
| Pin1, Pin2: Closed (Default) | VCCA is connected to the PMIC Battery Backup and VBACKUP. |
| Pin2, Pin3: Closed | Cell C3 is connected to the PMIC Battery Backup and VBACKUP.(1) |

(1) C3 is not populated on the EVM, but left to the end user to populate with either a coin cell or super cap, depending upon the desired use case.

**Table 3-6. Header J30 VIO_IN Voltage Select**

| Configuration | Description1 |
|---|---|
| Open | Not Allowed, 1.8 V or 3.3 V must be selected. |
| VIO Select, 3.3 V: Closed (Default) | VIO_IN is 3.3 V. |
| VIO Select, 1.8 V: Closed | VIO_IN is 1.8 V. |

1. In addition to J7 and J26, the lower portion of J15 is also used for the selection of VSYS and GPIO1.

**Table 3-7. Header J15, V3V3/VSYS/V5V0, GPIO1/I2C/SPI**

| Configuration | Description1 | |
|---|---|---|
| V3V3, VSYS: Closed (Default) | 3.3 V from U13 is connected to VSYS (VCCA). U13 is supplied with the 5 V from the USB connection (VBUS) through J47. VBUS is not intended to support heavy load conditions of greater than 3 W. This is the default state of the EVM | |
| VSYS, V5V0, and V3V3: Open | VSYS, VBUS, and USB_3V3 are isolated. VSYS should be powered from J6. | |
| VSYS, V5V0: Closed | 5 V from U14 is connected to VSYS (VCCA). U14 is supplied with the 5 V from the USB connection (VBUS) through J47. VBUS is not intended to support heavy load conditions of greater than 3 W. | |
| SCL2/CS, GPIO1: Open | GPIO mode. GPIO1 of the PMIC is connected to IO1 of the MCU. | |
| SCL2/CS, GPIO1: Closed (Default) | I2C mode (J7 SPI_EN: Open) | Q&A Watchdog mode. GPIO1 of the PMIC should be in the Alternative function to support the Q&A Watchdog and the I2C mode selected. This setting is done in conjunction with J7, GPIO2, SDA2/SDO: Closed |
| | SPI mode (J7 SPI_EN: Closed) | SPI mode, Chip Select. GPIO1 of the PMIC should be in the Alternative function to support SPI communication. This setting is done in conjunction with J7, GPIO2, SDA2/SDO: Closed |

1. The PMIC device can be configured for a power good level of 3.3 V or 5.0 V for the VCCA pin. Align the V3V3/VSYS/VBUS jumper with the PMIC configuration. The default PMIC configuration is 3.3 V.

## 3.5 Signal Headers

Signal headers are provided for the LDOs, BUCK regulators, and GPIO signals. Headers J13 (LDOs), J12 (BUCKs), and J11 (GPIOs) are placed on the perimeter of the board to enable probing of these signals even when in a stacked configuration.

There are 6 signal headers associated with the LDO; five are shown in the EVM silk screen capture, Figure 3-3. These include J20 and J21, the power inputs to the LDOs, J14 and J13, the LDO outputs, and J18 and J19 which can be used to measure Power Supply Rejection Ratio (PSRR) on LDO3 and LDO4. All pins of J20 are connected to the VCCA, and J20 is placed next to J21 to easily connect all the LDO power inputs to the VCCA; this is the default jumper configuration. An external power supply for the LDOs can also be applied directly to J21.

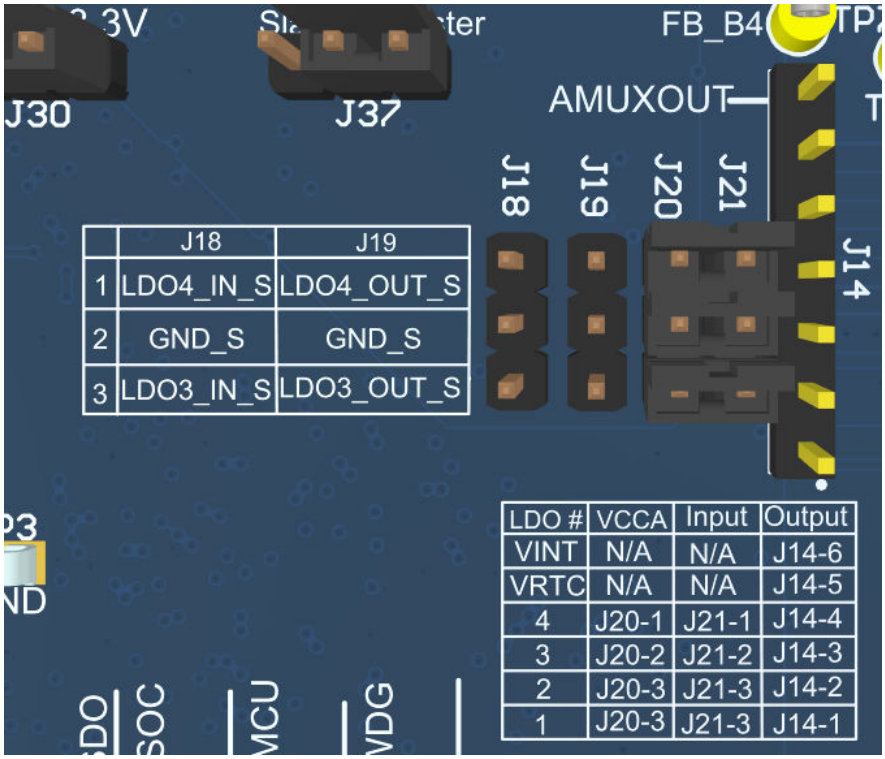


**Figure 3-3. LDO_Headers_v2**

**Note**

J13 and J14 provide the same LDO outputs; however, J13 should only be used for probing. J14 provides a shorter and wider trace, lowering the impedance and supporting maximum loads of 500 mA. Also, pin 7 is a different signal for J13 and J14; GND_S and AMUXOUT, respectively.

Signal Header J12 provides access to all of the buck regulator outputs, GND_S and VCCA_S.

**Note**

Header J12 should only be used for voltage probing and not for power delivery.

GPIO signals are provided on both J9 and J11. J8 (PU) is located directly above J9 enabling each GPIO to be pulled to the voltage defined in table Table 3-8 through a 10 kΩ resistor pullup. J10 (PD) is located directly below J9 to enable shorting each GPIO directly to GND.

**Table 3-8. Header J8 Pullup Voltages**

| J8, Pin(s) | Pullup Voltage | Description |
|---|---|---|
| 1,2,7-11 | VIO_IN | GPIO1, GPIO2, GPIO7-11: Output Type Selection; Power Domain is VIO |
| 3,4 | VOUT_LDOVRTC | GPIO3 and GPIO4: Input Type Selection; Power Domain is VRTC |
| 5,6 | VOUT_LDOVINT | GPIO5 and GPIO6: Output Type Selection; Power Domain is VINT |

## 3.6 Stack-Up Headers

As shown in Figure 3-4, multiple boards can be configured into a master-slave relationship (1 master and up to 5 slaves) and physically stacked upon each other. VCCA and GND are shared between boards on headers J27 and J28. Communication between the boards is shared on header J29. This header, J29, is marked on the bottom silkscreen, as shown in Figure 3-5.

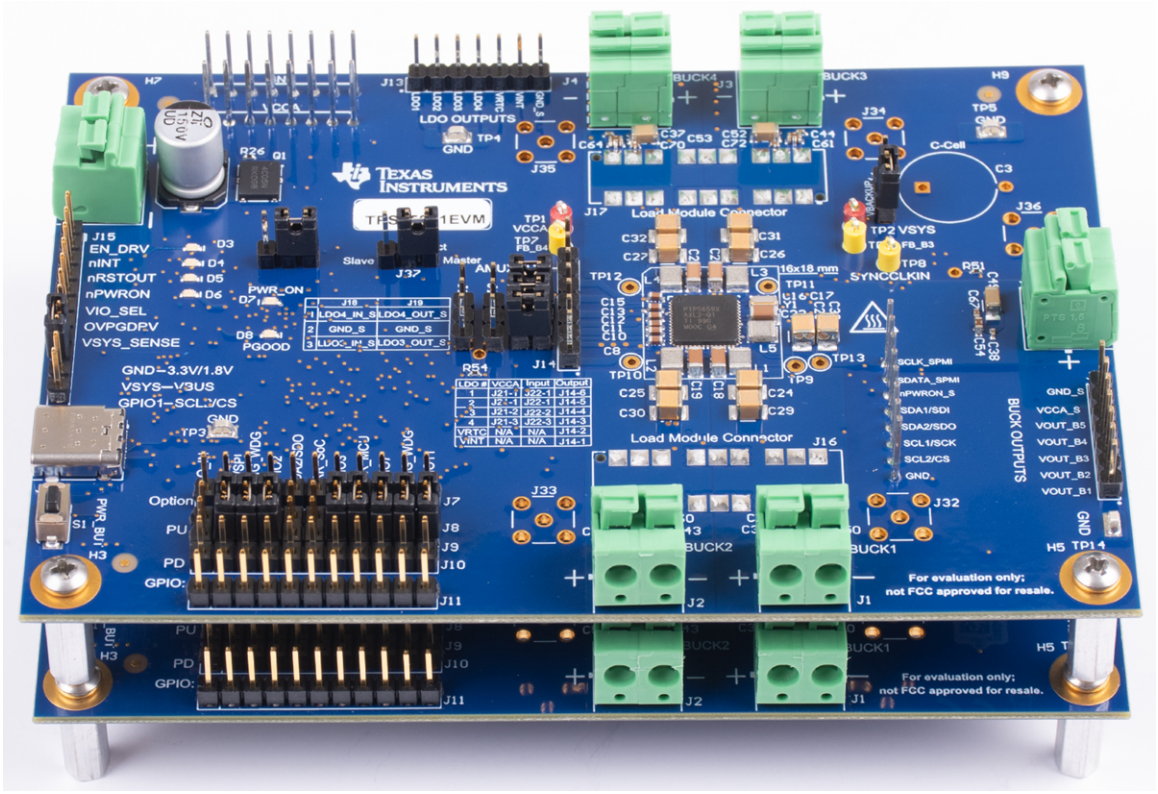


**Figure 3-4. EVM Masters Slave Configuration**

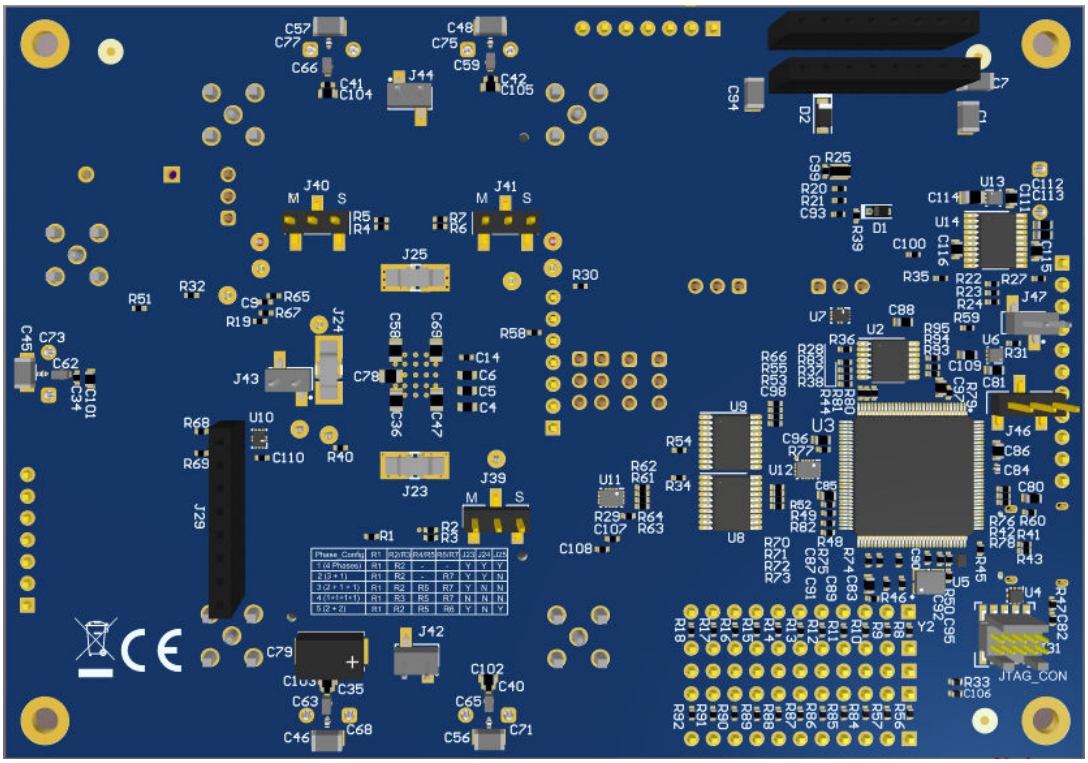


**Figure 3-5. EVM Bottom View Version 2**

The J29 signal, nPWRON_S, and the nPWRON/ENABLE or VOUT_LDOVINT signals of the PMIC are connected through J37. When multiple PMICs are stacked, as shown in Figure 3-6, the expectation is that the master is placed in master mode, connecting the stackable signal nPWRON_S, and the VOUT_LDOVINT. By using this stackup configuration, one or more of the slaves power up sequence will always follow the master. When in master mode or when the header J37 is left open the nPWRON/ENABLE pin can be controlled with the EVM push button, S1, or the jumper J45.[2]

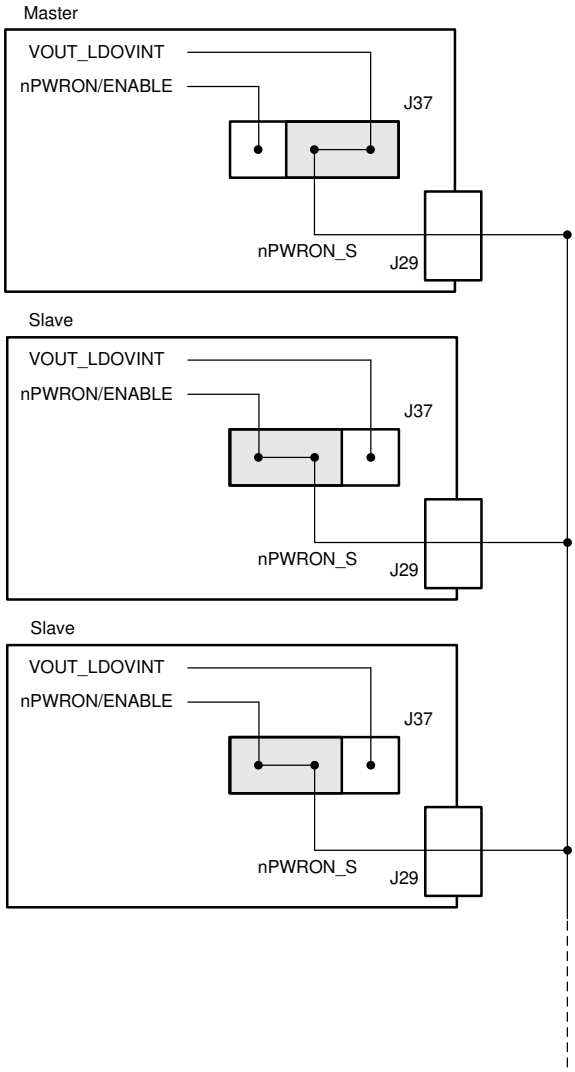


**Figure 3-6. Header J37 Master and Slave Select Table Description for 'OPEN' configuration**

**Table 3-9. Header J37 Master and Slave Select**

| Configuration | Description |
|---|---|
| Open | When used as a single PMIC (no stacking). ENABLE is connected to a pullup and therefore automatically enabled. S1 can be used to generate edges or J45 at any level.[3] |
| Slave, M/S Select: Closed | Slave Mode. The PMIC signal ENABLE is connected to the nPWRON_S signal which is from the master's VOUT_LDOVINT. |
| M/S Select, Master: Closed | Master Mode. The PMIC signal, VOUT_LDOVINT, is connected to the nPWRON_S which will be the ENABLE signal on the PMICs connected as slaves. |

[2] The default position for J45 is with pins 1-2 closed so that the pullup is applied to nPWRON/ENABLE.
[3] The default position for J45 is with pins 1-2 closed so that the pullup is applied to nPWRON/ENABLE. J45 is provided so that the signal nPWRON/ENABLE can be pulled low or sourced from an off board signal.

### 3.7 Connectors

In addition to J12 and the terminal connections, J1-J6, SMA connectors, J32-J36 are provided for testing the buck regulator outputs. These connectors are not populated.

Two load module connector footprints are provided, J16 and J17. The connector components are not populated.

### 3.8 EVM Control, GPIO, and Additional Regulators

The EVM has a built-in USB interface based upon the MSP432E401Y (U3) to allow the GUI, from the host computer, to communicate with the PMIC. The supply voltage required by the MSP432E401Y is generated automatically by the TLV7103318 (U6) device which provides 3.3 V and 1.8 V from USB power, VBUS. These voltages are available for supplying VIO_IN for the PMIC (selectable from J30). Two SN74GTL2003 level shifters (U8, U9) are used in order to support the use case of the PMIC VIO_IN of 1.8 V (the MCU IO will always be 3.3 V). It is important to note that the 3.3 V used for the MCU and the VIO_IN, MCUVCC, is different from the 3.3 V, 3V3V, provided to the PMIC through U13.

The TS3A5018RSVR switch is used to apply the pullup resistors for I2C communication with the MSP432E401Y. If the EVM is not a master (J37) or if SPI communication is used (J7, SPI_EN) then the pullups are not applied. The application of the pullup resistors is for I2C mode only and is only intended for one board in a stack-up application. Note: in the stack-up configuration only one board can have a valid VBUS voltage on the board. This means that the master board can have a connected USB cable supplying VBUS or that VSYS can be connected to VBUS through J15, see Table 3-6.

The EVM has 4 LEDs to indicate board power, on or off, and some select PMIC GPOs status. The signals are listed in Table 3-10.

**Table 3-10. EVM LED Indicators**

| LED Designator | Indication |
|---|---|
| D3 | LED is on when nINT is low. |
| D4 | LED is on when EN_DRV is high. |
| D5 | LED is on when nRSTOUT is low. |
| D6 | LED indicating that MCUVCC is present. |

## 4 Customization

The EVM, in conjunction with GUI tool, provides various degrees of customization. A couple of examples are provided here which can be generalized to a number of functions.

### 4.1 Changing the Communication Interface

The default setting for communication with the PMIC is I2C. In some devices a second I2C channel is available on GPIO1 and GPIO2. In order to support the second I2C channel the GPIO1 and GPIO2 must be configured appropriately and pullups applied through J8 and J9, as shown in Figure 4-1 and Figure 4-2. Alternatively these GPIOs can be used to support SPI communication.

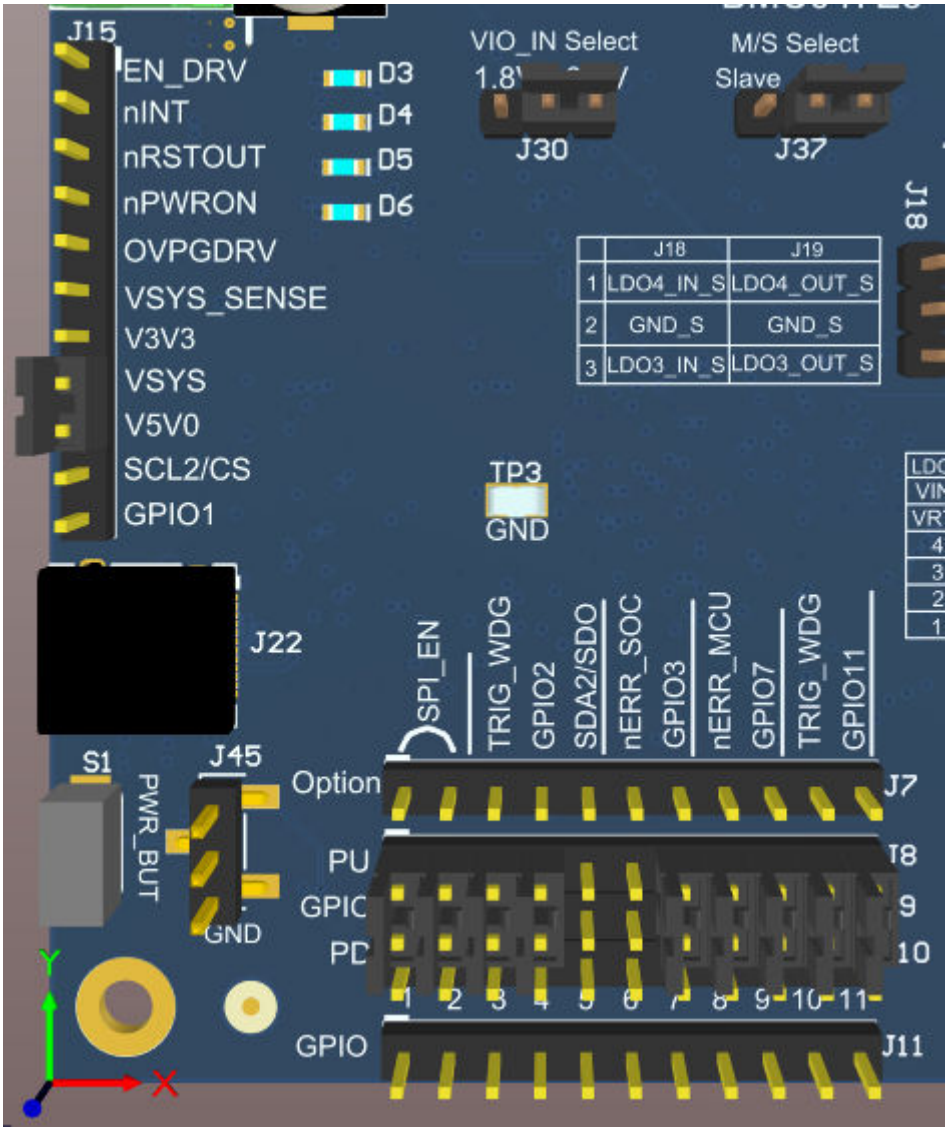


**Figure 4-1. TPS6594EVM Interface Settings for Communication**

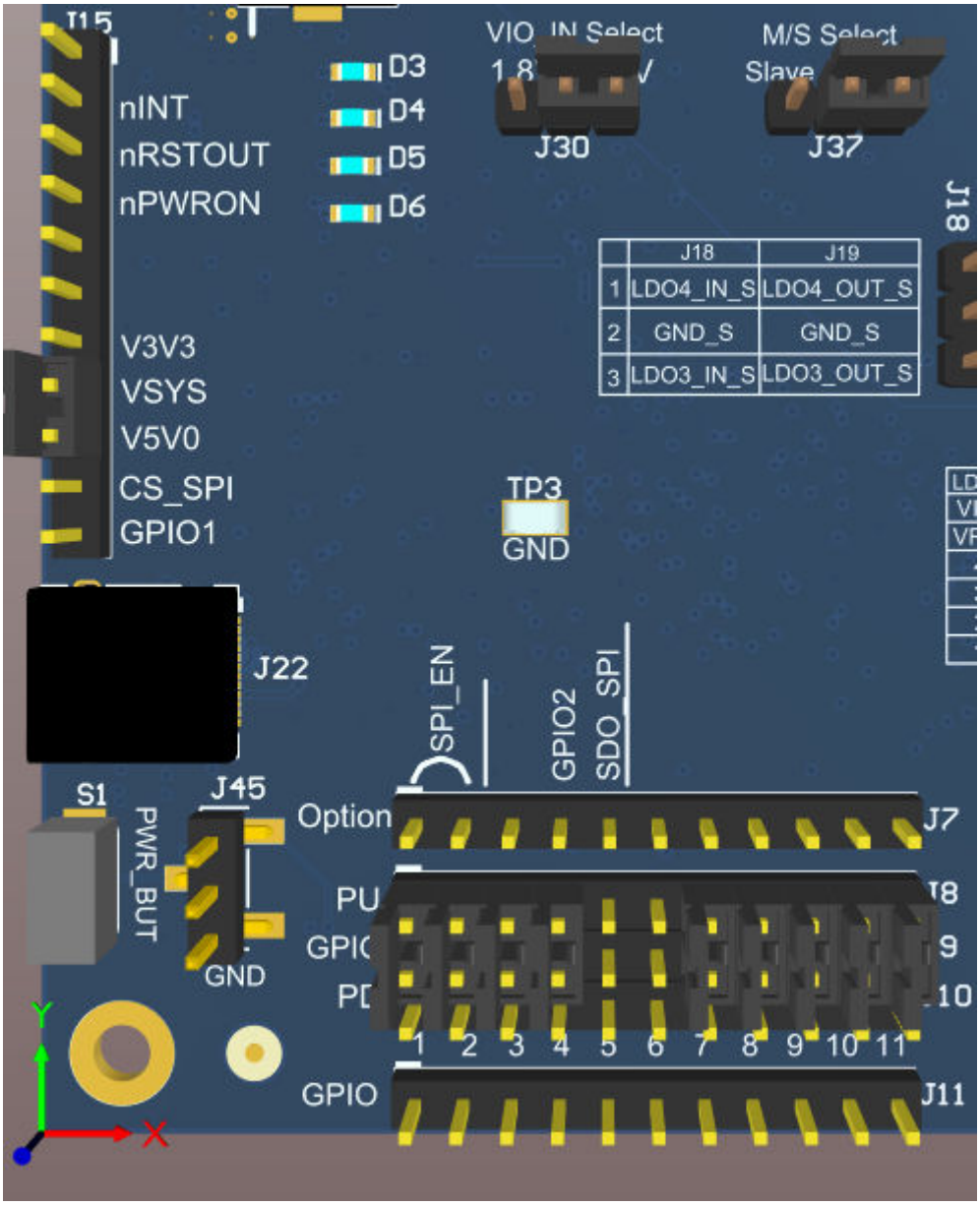


**Figure 4-2. TPS6593EVM Interface Settings for Communication**

Changing to SPI requires a minor change to the jumper settings. The first jumper to place is on the SPI_EN option on connector J7, as shown in Figure 4-1 and Figure 4-2. Placing this jumper will connect the micro controller to the SPI bus which is connected to all available PMICs through the EVM stack connection through J29. In a multiple EVM stackup, this jumper should only be placed on the EVM with the USB connection to the host computer. The SPI does not have a device ID and therefore the chip select is used to determine which PMIC will receive and respond to commands on the SPI bus. The signals SCL2/CS and GPIO1 on J15 should only be jumpered on the EVM which is intended to communicate with the GUI (through the micro controller). All other EVMs which are stacked should pull GPIO1 high, so that the PMIC does not respond or interfere with the SPI communication.

**Note**

For SPI communication it is recommended to remove the pullups or pulldowns on GPIO1 and GPIO2. Remove any jumpers between J8, J9, and J10 for GPIO1 and GPIO2.

## 4.2 Changing the Phase Configuration

As shown in Figure 4-3, there are five possible phase configurations. It is important that the phase configuration of the EVM matches the phase configuration of the PMIC. Specific consideration should be given to BUCK3 and BUCK4 in phase configurations 1 and 2, since these regulators have independent feedback circuits which can be configured to measure external supplies. FB_B3 and FB_B4 are made available on test points TP6 and TP7 respectively. If the voltage monitors associated with BUCK3 and BUCK4 are disabled, then it is recommended to connect the FB_Bn pins to reference ground, using R4 and R6.

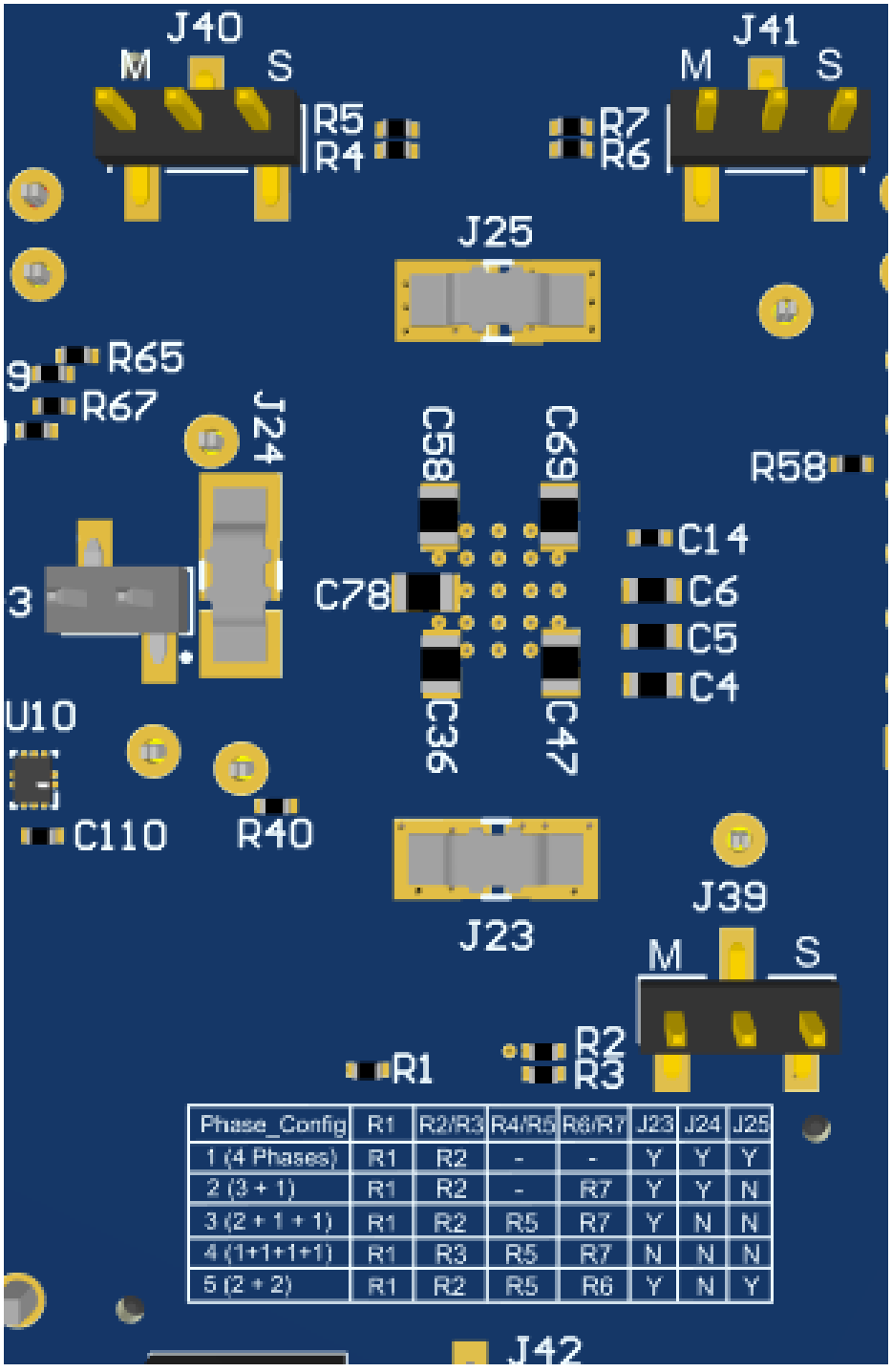


**Figure 4-3. Phase Configuration Components**

# 5 Schematic, Layout, and Bill of Materials

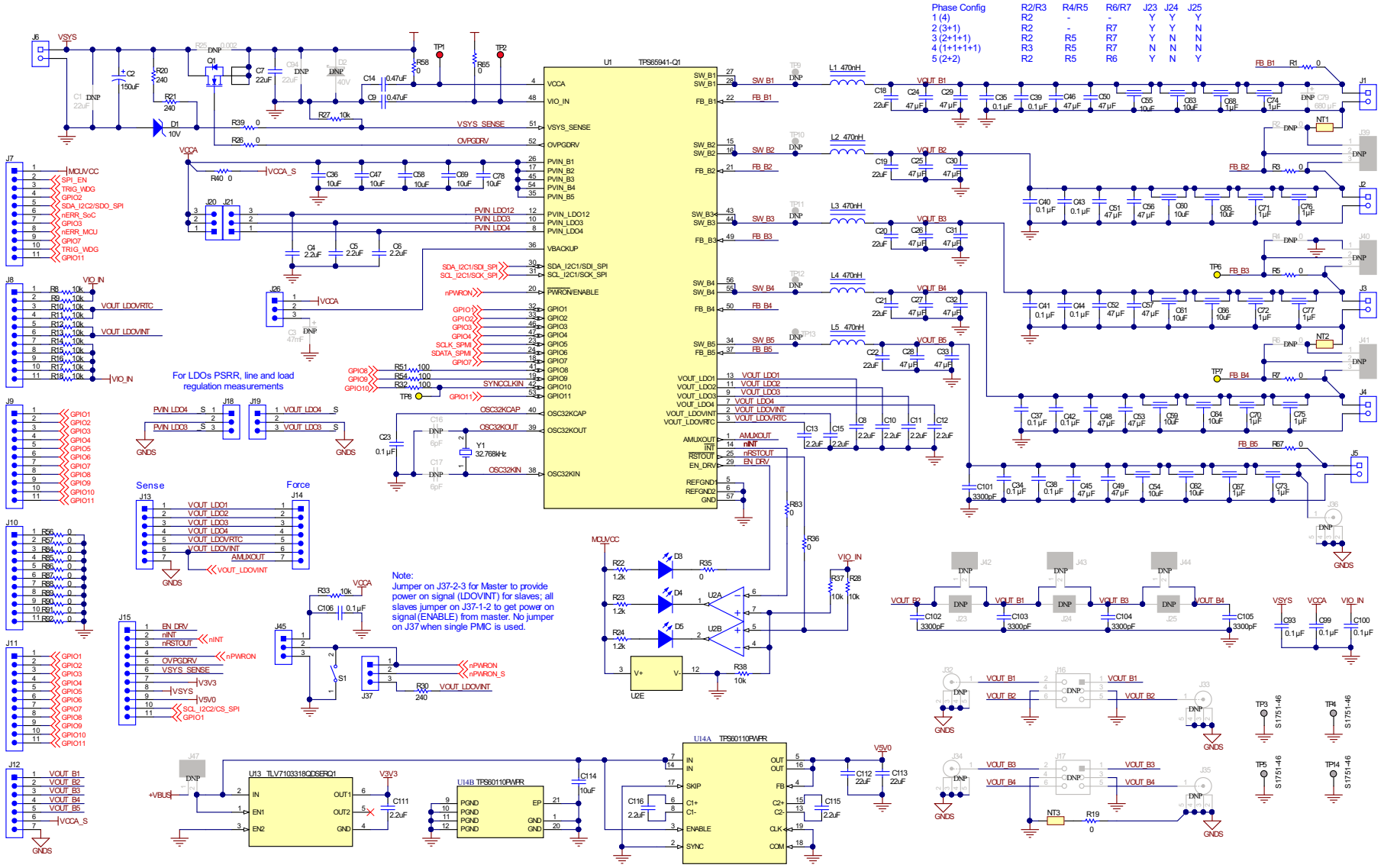


**Figure 5-1. TPS6594EVM 1+1+1+1+1 Configuration, Schematic Page 1**

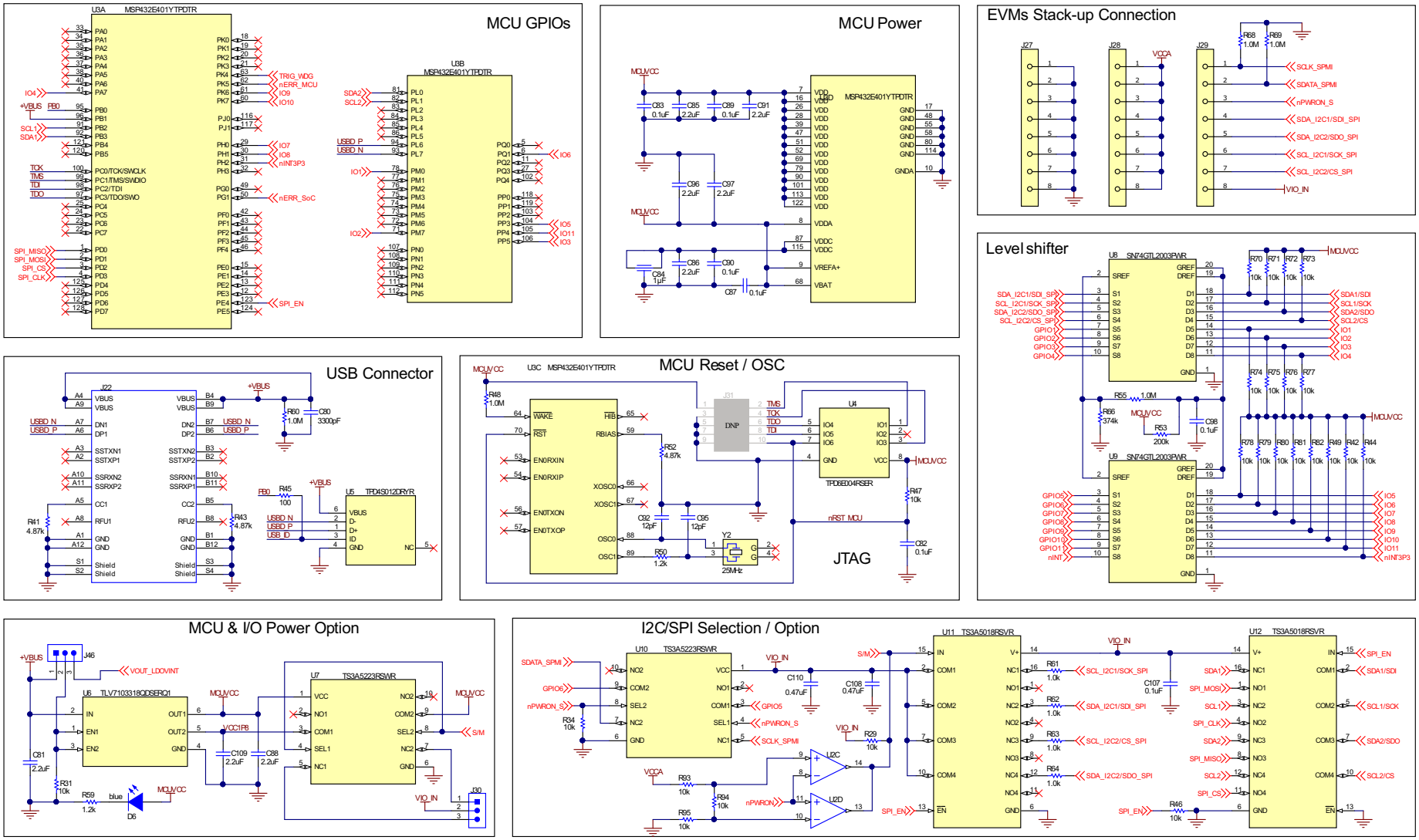


**Figure 5-2. TPS6594EVM 1+1+1+1+1 Configuration, Schematic Page 2**

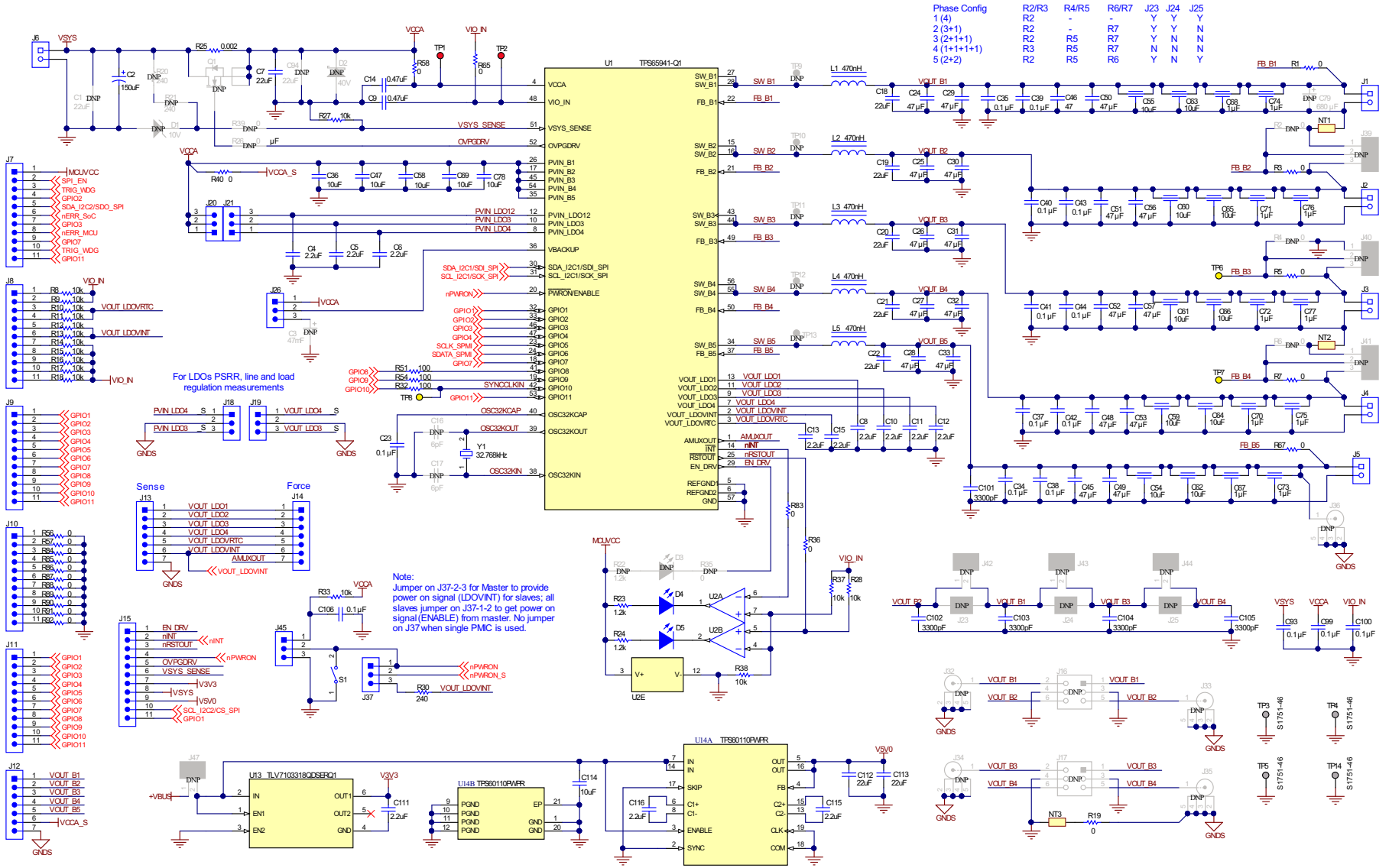


**Figure 5-3. TPS6593EVM 1+1+1+1+1 Configuration, Schematic Page 1**

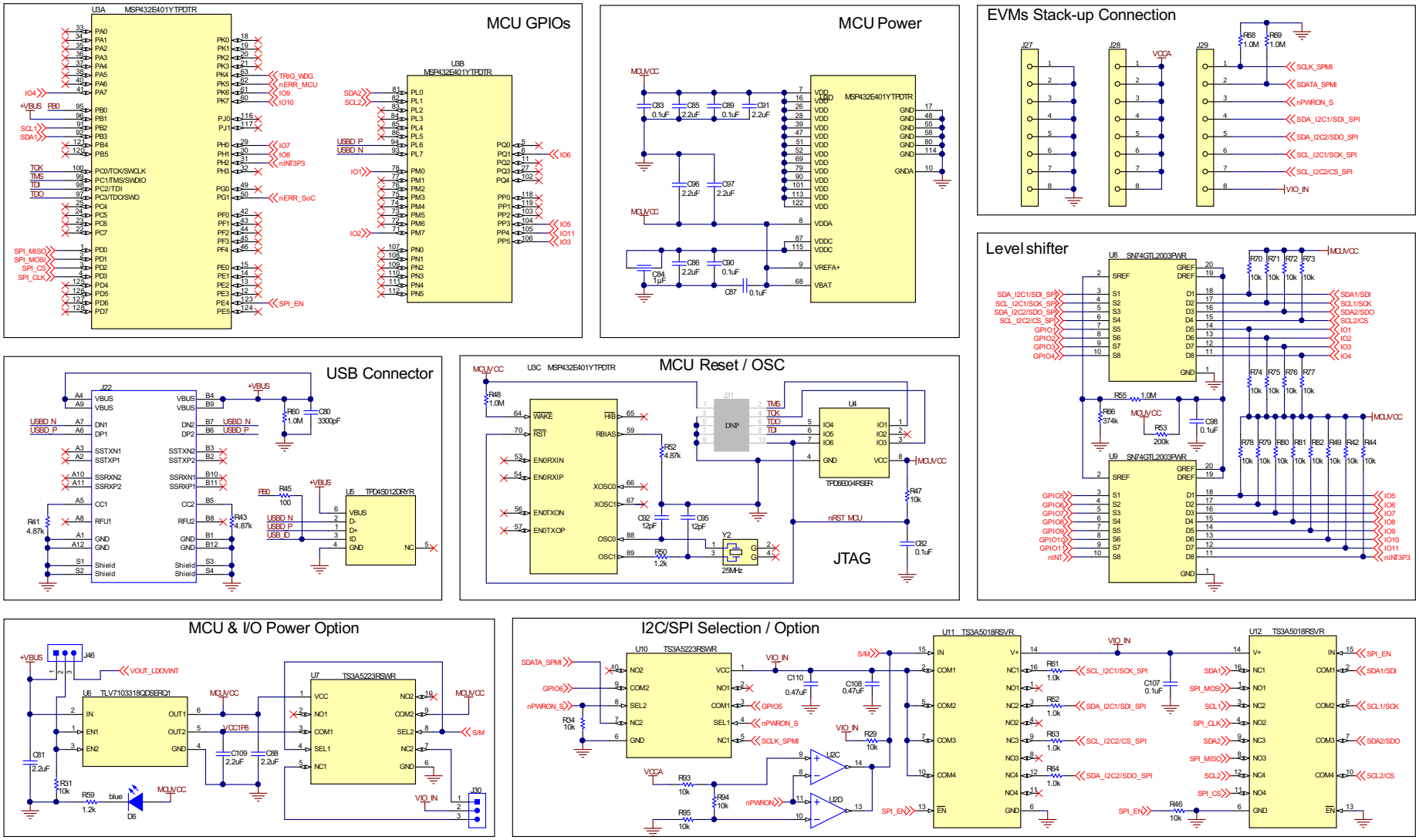


**Figure 5-4. TPS6593EVM 1+1+1+1+1 Configuration, Schematic Page 2**

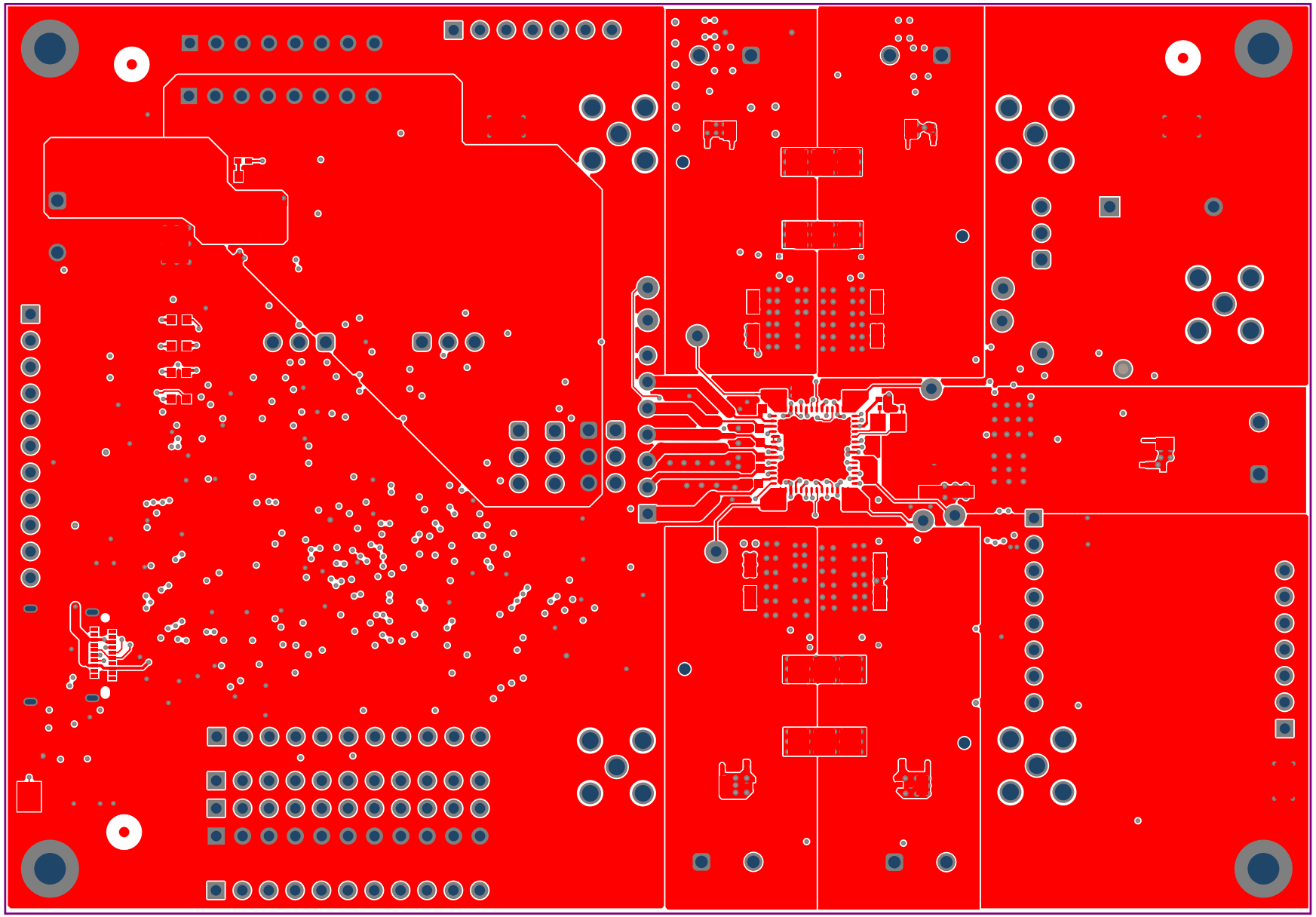

**Figure 5-5. Layout Top, Layer 1**

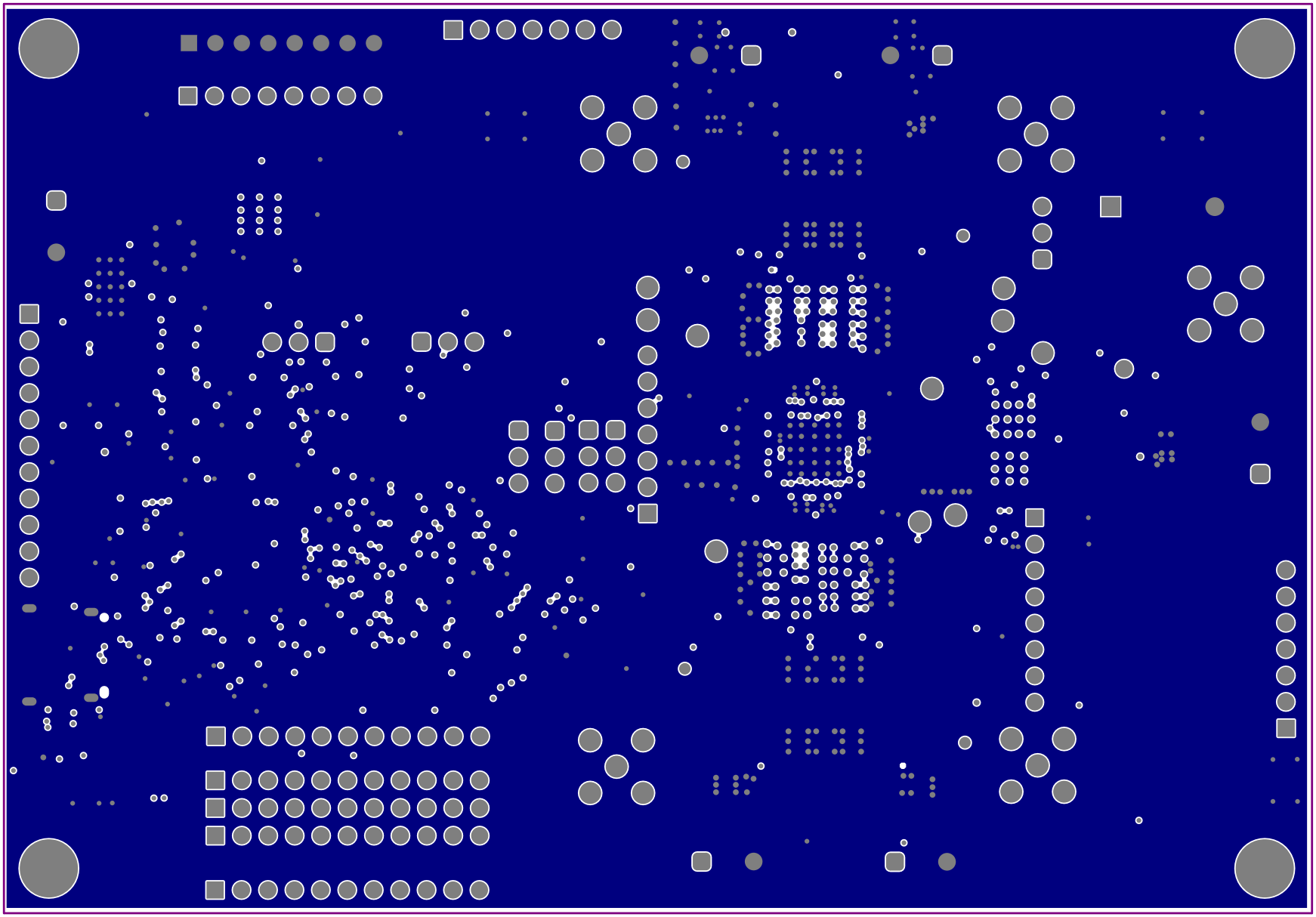

**Figure 5-6. Layout Ground, Layer 2**

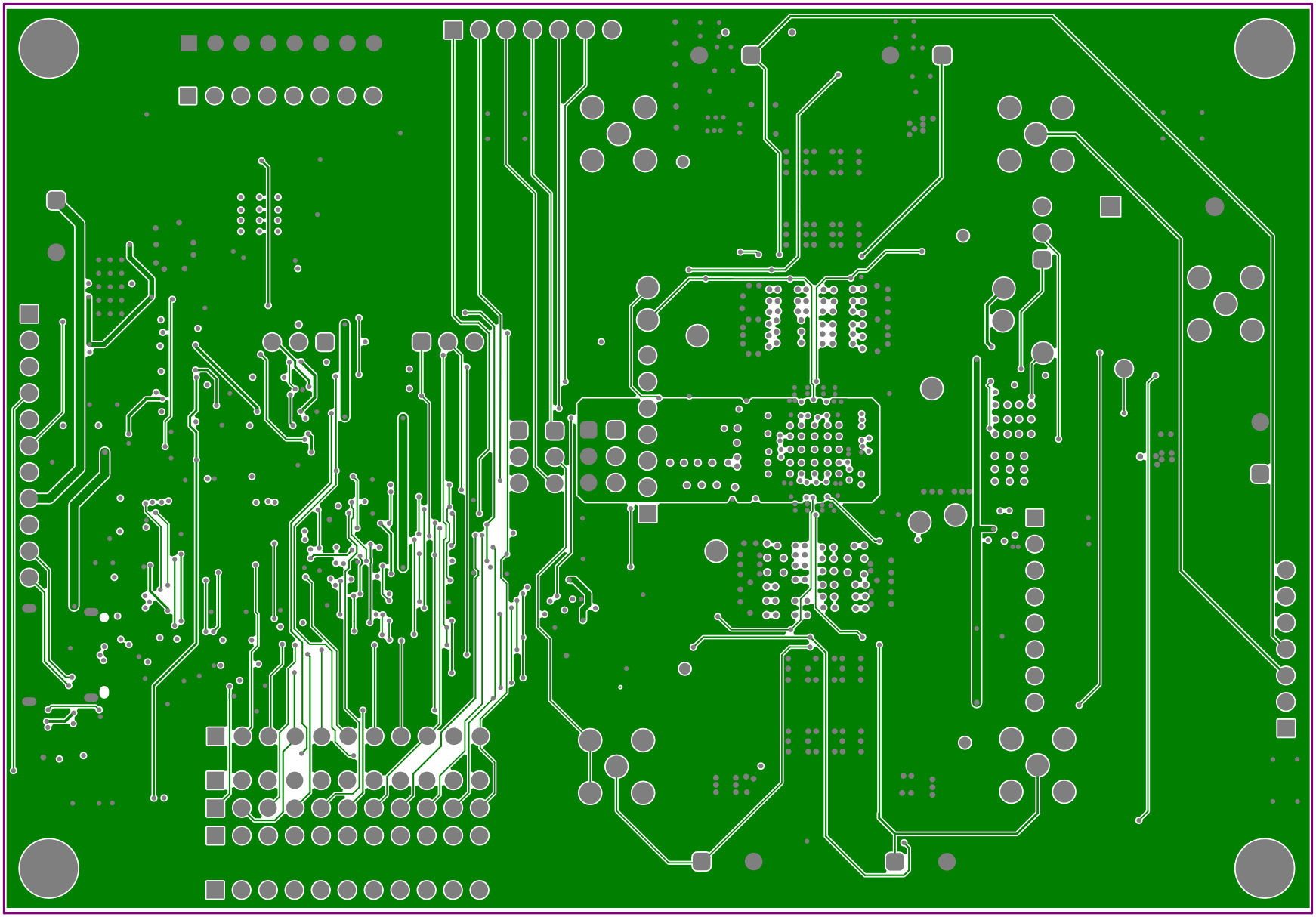

**Figure 5-7. Layout Signal, Layer 3**

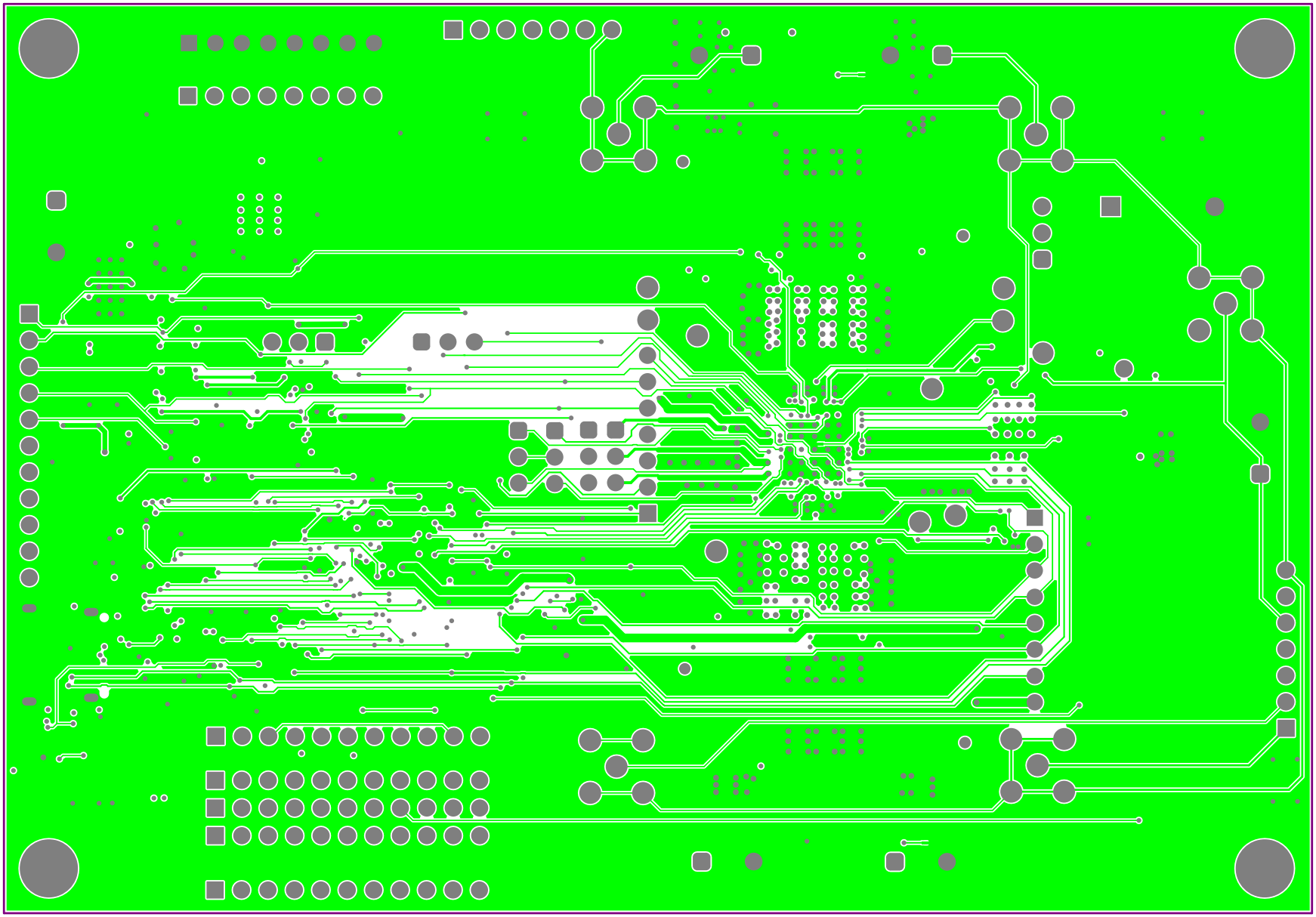

**Figure 5-8. Layout Signal, Layer 4**

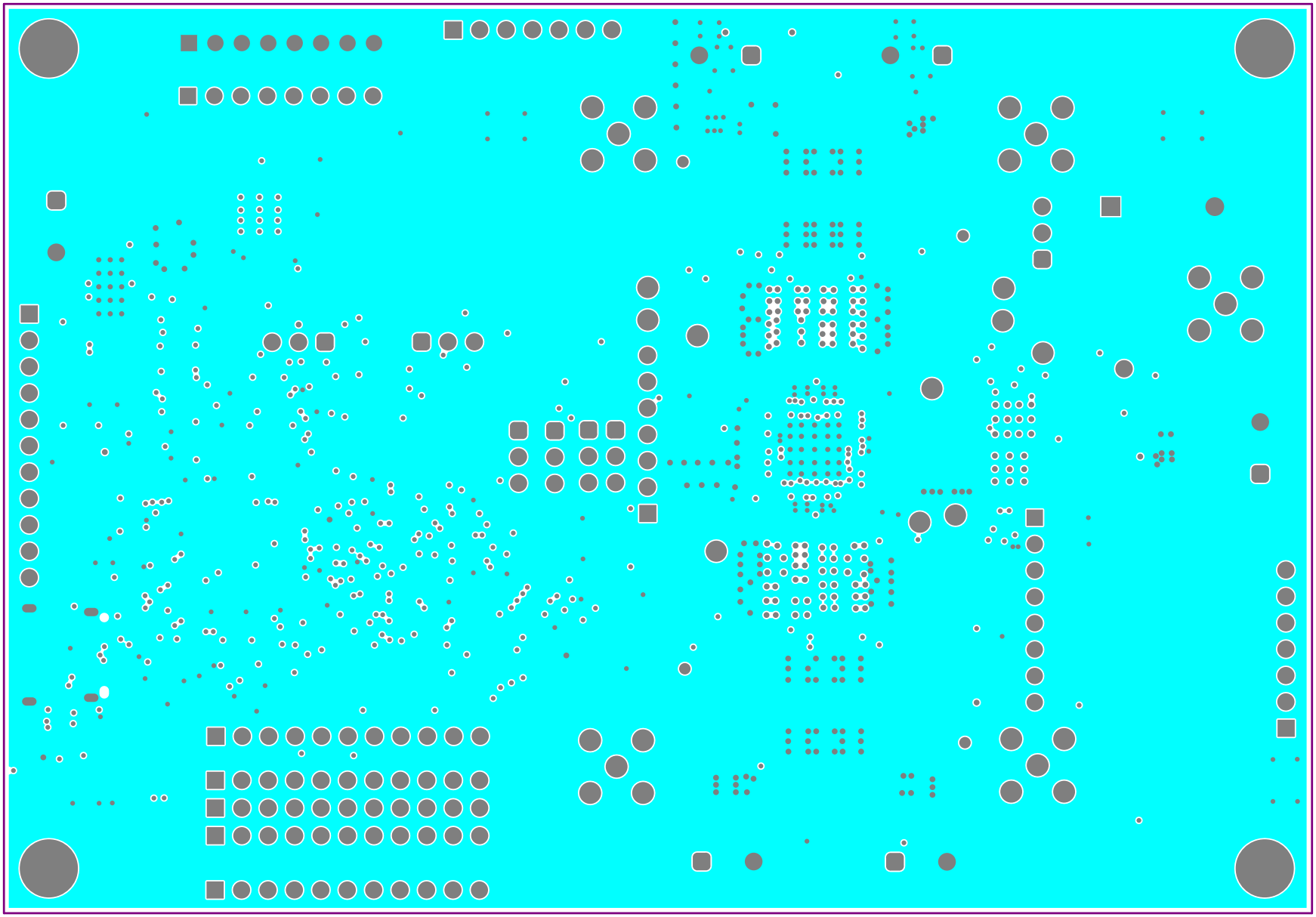

**Figure 5-9. Layout Ground, Layer 5**

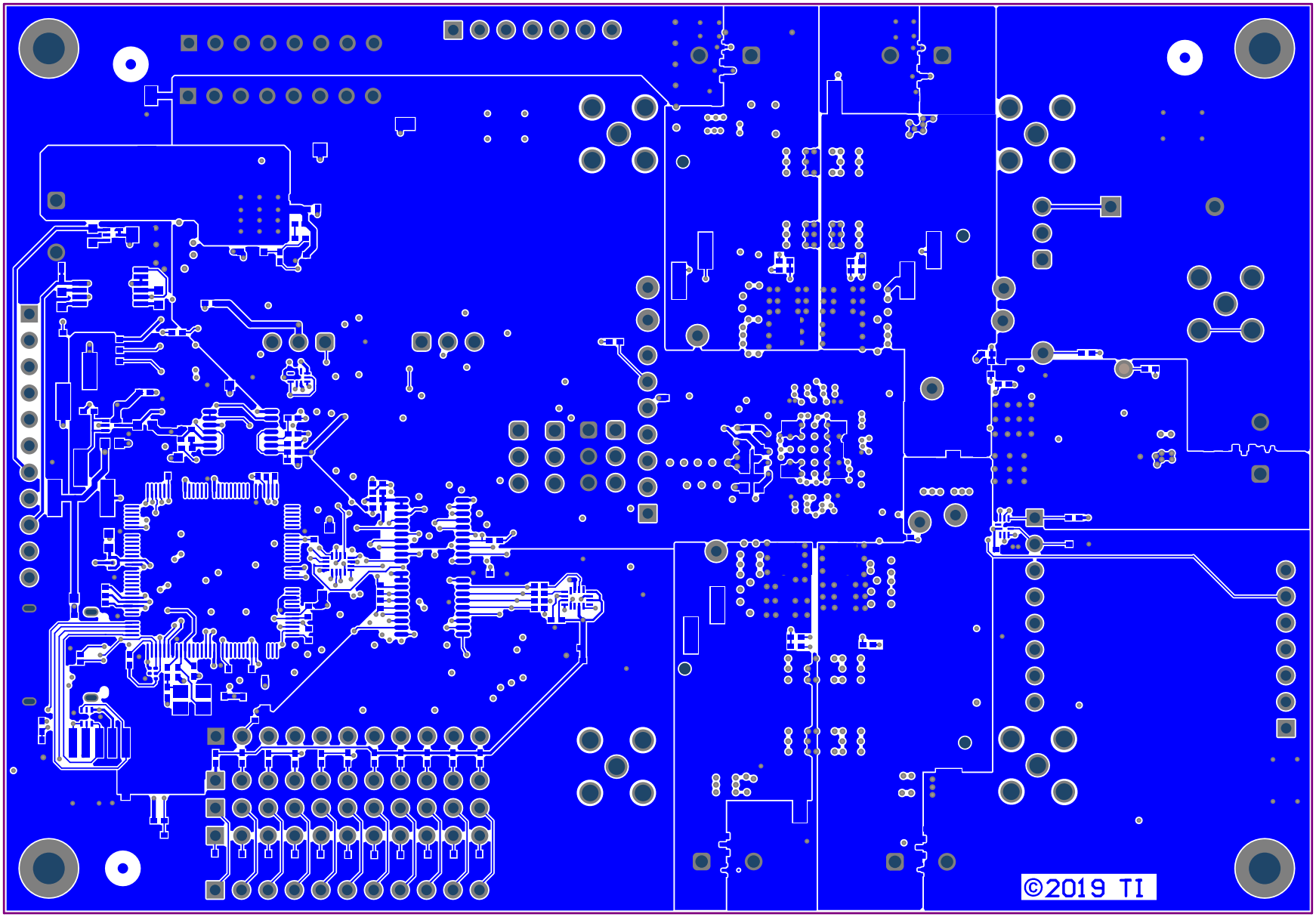


**Figure 5-10. Layout Bottom**

**Table 5-1. TPS6594EVM Bill of Materials of Balance of Components**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| C2 | 1 | 150 µF | CAP, AL, 150 µF, 35 V, ± 20%, 0.17 Ω, SMD | 8x10 | UUD1V151MNL1GS |
| C4, C5, C6, C8, C10, C11, C12, C13, C15, C81, C85, C86, C88, C91, C96, C97, C109, C111, C115, C116 | 20 | 2.2 µF | CAP, CERM, 2.2 µF, 16 V, ± 20%, X7S, AEC-Q200 Grade 1, 0603 | 0603 | CGA3E1X7S1C225M080AC |
| C7, C18, C19, C20, C21, C22 | 6 | 22 µF | CAP, CERM, 22 µF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206 | 1206 | CGA5L1X7R0J226M160AC |
| C9, C14, C108, C110 | 4 | 0.47 µF | CAP, CERM, 0.47 µF, 10 V,± 10%, X7S, 0402 | 0402 | GCM155C71A474KE36D |
| C23, C34, C35, C37, C38, C39, C40, C41, C42, C43, C44, C93, C99, C100, C106 | 15 | 0.1 µF | CAP, CERM, 0.1 µF, 16 V,± 5%, X7R, AEC-Q200 Grade 1, 0402 | 0402 | GCM155R71C104JA55D |
| C24, C25, C26, C27, C28, C29, C30, C31, C32, C33 | 10 | 47 µF | CAP, CERM, 47 µF, 6.3 V, ± 20%, X7R, 1210 | 1210 | GCM32ER70J476ME19L |
| C36, C47, C58, C69, C78, C114 | 6 | 10 µF | CAP, CERM, 10 µF, 16 V, ± 10%, X7S, AEC-Q200 Grade 1, 0805 | 0805 | CGA4J1X7S1C106K125AC |
| C45, C46, C48, C49, C50, C51, C52, C53, C56, C57 | 10 | | Chip Multilayer Ceramic Capacitors for Automotive | 1206 (3216 Metric) | GCM31CD70G476ME |
| C54, C55, C59, C60, C61, C62, C63, C64, C65, C66 | 10 | 10 µF | CAP, CERM, 10 µF, 4 V,± 20%, 1.6x0.8mm | 1.6x0.8mm | NFM18HC106D0G3 |
| C67, C68, C70, C71, C72, C73, C74, C75, C76, C77, C84 | 11 | | 3 Terminals Chip Multilayer Ceramic Capacitor (EMIFIL) | 0402 | NFM15HC105D0G3 |
| C80, C101, C102, C103, C104, C105 | 6 | 3300pF | CAP, CERM, 3300 pF, 50 V, ± 10%, X7R, 0603 | 0603 | C0603C332K5RACTU |
| C82, C83, C87, C89, C90, C98, C107 | 7 | 0.1 µF | CAP, CERM, 0.1 µF, 16 V, ± 10%, X7R, 0402 | 0402 | GCM155R71C104KA55D |
| C92, C95 | 2 | 12pF | CAP, CERM, 12 pF, 50 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0402 | 0402 | GCM1555C1H120JA16J |
| C112, C113 | 2 | 22 µF | CAP, CERM, 22 µF, 6.3 V, ± 20%, X5R, 0603 | 0603 | GRM188R60J226MEA0D |
| D1 | 1 | 10V | Diode, Zener, 10 V, 300 mW, SOD-323 | SOD-323 | MM3Z10VST1G |
| D3, D4, D5, D6 | 4 | Blue | LED, Blue, SMD | BLUE 0603 LED | LB Q39G-L2N2-35-1 |
| H1, H2, H3, H4 | 4 | | MACHINE SCREW PAN PHILLIPS 4-40 | | 9900 |
| H5 | 1 | | USB A MALE TO USB C Male | | 3021090-01M |

**Table 5-1. TPS6594EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| H6, H7, H8, H9 | 4 | | | SPACER | FC2058-440-A |
| J1, J2, J3, J4, J5, J6 | 6 | | Terminal Block, 5mm, 2x1, R/A, TH | Terminal Block, 5mm, 2x1, R/A, TH | 1792863 |
| J7, J8, J9, J10, J11, J15 | 6 | | Header, 100mil, 11x1, Gold, TH | 11x1 Header | TSW-111-07-G-S |
| J12, J13, J14 | 3 | | Header, 100mil, 7x1, Gold, TH | 7x1 Header | TSW-107-07-G-S |
| J18, J19, J20, J21, J26, J30, J37 | 7 | | Header, 2.54 mm, 3x1, Gold, TH | Header, 2.54mm, 3x1, TH | 61300311121 |
| J22 | 1 | | Receptacle, 0.5mm, USB TYPE C, R/A, SMT | Receptacle, 0.5mm, USB TYPE C, R/A, SMT | 12401610E4#2A |
| J27, J28, J29 | 3 | | Board-To-Board Connector, Vertical, ESQ Series, 8 Contacts, Receptacle, 2.54 mm, Through Hole | HDR8 | ESQ-108-14-T-S |
| J45, J46 | 2 | | Header, 100mil, 3x1, Gold, SMT | Samtec_TSM-103-01-X-SV | TSM-103-01-L-SV |
| L1, L2, L3, L4, L5 | 5 | 470nH | Inductor, Thin Film, 470 nH, 5.3 A, 0.021 Ω, AEC-Q200 Grade 0, SMD | TDK Inductor | TFM322512ALMAR47MTAA |
| LBL1 | 1 | | | PCB Label 0.650 x 0.200 inch | THT-14-423-10 |
| Q1 | 1 | 30V | MOSFET, N-CH, 30 V, 27.2 A, AEC-Q101, SO-8FL | SO-8FL | NVMFS4C05NT1G |
| R1, R3, R5, R7, R19, R26, R35, R36, R39, R40, R56, R57, R58, R65, R67, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92 | 25 | 0 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | RK73Z1ETTP |
| R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R27, R28, R29, R31, R33, R34, R37, R38, R42, R44, R46, R47, R49, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R93, R94, R95 | 40 | 10k | RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040210K0JNED |
| R20, R21, R30 | 3 | 240 | RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW0402240RJNED |
| R22, R23, R24, R50, R59 | 5 | 1.2k | RES, 1.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021K20JNED |
| R32, R45, R51, R54 | 4 | 100 | RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW0402100RJNED |

**Table 5-1. TPS6594EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| R41, R43, R52 | 3 | 4.87k | RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04024K87FKED |
| R48, R55, R60, R68, R69 | 5 | 1.0Meg | RES, 1.0 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021M00JNED |
| R53 | 1 | 200k | RES, 200 k, 5%, 0.063 W, 0402 | 0402 | CRCW0402200KJNED |
| R61, R62, R63, R64 | 4 | 1.0k | RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021K00JNED |
| R66 | 1 | 374k | RES, 374 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW0402374KFKED |
| S1 | 1 | | Switch, SPST, Off-On, 50 mA,24V, SMD | 6x3.5mm | 147873-1 |
| SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16 | 16 | | Shunt, 100mil, Gold plated, Black | Shunt 2 pos. 100 mil | 881545-2 |
| TP1, TP2 | 2 | | Test Point, Miniature, Red, TH | Red Miniature Testpoint | 5000 |
| TP3, TP4, TP5, TP14 | 4 | | Test Lead clips and hooks, SMT | Test Point, Body 3.25x1.65mm | S1751-46 |
| TP6, TP7, TP8 | 3 | | Test Point, Miniature, Yellow, TH | Yellow Miniature Testpoint | 5004 |
| U1 | 1 | | Power Management IC (PMIC) With 4-Phase 14-A Buck for Processors, RVJ0056A (VQFN-56) | RVJ0056A | TPS65941-Q1 |
| U2 | 1 | | AEC-Q100 Quad Comparator, PW0014A (TSSOP-14) | PW0014A | LM2901AVQPWRQ1 |
| U3 | 1 | | MSP432E401YTPDT, PDT0128A (TQFP-128) | PDT0128A | MSP432E401YTPDTR |
| U4 | 1 | | Low-Capacitance 6-Channel ±15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8) | RSE0008A | TPD6E004RSER |
| U5 | 1 | | 4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6) | DRY0006A | TPD4S012DRYR |

**Table 5-1. TPS6594EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| U6, U13 | 2 | | Automotive Catalog, Dual, 200mA, Low-IQ Low-Dropout Regulator for Portable Devices, DSE0006A (WSON-6) | DSE0006A | TLV7103318QDSERQ1 |
| U7, U10 | 2 | | 0.5Ω Dual SPDT Bidirectional Analog Switch, RSW0010A (UQFN-10) | RSW0010A | TS3A5223RSWR |
| U8, U9 | 2 | | 8-BIT BIDIRECTIONAL LOW-VOLTAGE TRANSLATOR, PW0020A (TSSOP-20) | PW0020A | SN74GTL2003PWR |
| U11, U12 | 2 | | 10-Ω Quad SPDT Analog Switch, RSV0016A (UQFN-16) | RSV0016A | TS3A5018RSVR |
| U14 | 1 | | 5 V, Boost Charge Pump, 300 mA, 2.7 to 5.4 V Input with Synchonrization pin, -40 to 85 °C, 20-pin SOP (PWP20), Green (RoHS & no Sb/Br) | PWP0020C | TPS60110PWPR |
| Y1 | 1 | | Crystal, 32.768 KHz, 9 pF, AEC-Q200 Grade 1, SMD | 1.5x3.2mm | NX3215SD-STD-MUS-6 |
| Y2 | 1 | | Crystal, 25 MHz, 8pF, SMD | 3.2x0.75x2.5mm | NX3225GA-25.000M-STD-CRG-2 |
| C1, C94 | 0 | 22 µF | CAP, CERM, 22 µF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206 | 1206 | CGA5L1X7R0J226M160AC |
| C3 | 0 | 47000 µF | CAP, Electric Double Layer, 47000 µF, 5.5 V, +80/-20%, TH | Horizontal D11.5x5mm | DX-5R5H473U |
| C16, C17 | 0 | | CAP CER 6PF 50V C0G 0402 | 0402 | GCM1555C1H6R0CA16 |
| C79 | 0 | 680 µF | CAP, TA, 680 µF, 6.3 V, ± 10%, 0.023 Ω, AEC-Q200 Grade 1, SMD | 7343-40 | T510X687K006AGA023 |
| D2 | 0 | 40V | Diode, Schottky, 40 V, 2 A, SOD-123F | SOD-123F | DB2W40200L |
| FID6 | 0 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A |
| J16, J17 | 0 | | Receptacle, 2.5mm, 3x2, Gold, SMT | Receptacle, 2.5mm, 3x2, SMT | 6651712-1 |
| J23, J24, J25 | 0 | | JUMPER TIN SMD | 6.85x0.97x2.51 mm | S1911-46R |
| J31 | 0 | | Header (Shrouded), 1.27mm, 5x2, Gold, SMT | Header(Shrouded), 1.27mm, 5x2, SMT | FTSH-105-01-F-DV-K |

**Table 5-1. TPS6594EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| J32, J33, J34, J35, J36 | 0 | | SMA Jack, Straight, 50 Ω, Gold, TH | TH, 5-Leads, Body 7x7mm | SMA-J-P-H-ST-TH1 |
| J39, J40, J41 | 0 | | Header, 100mil, 3x1, Gold, SMT | Samtec_TSM-103-01-X-SV | TSM-103-01-L-SV |
| J42, J43, J44, J47 | 0 | | Header, 100mil, 2x1, Tin, SMD | SMD, 2-Leads, Body 200x100mil | TSM-102-01-T-SV-P-TR |
| R2, R4, R6 | 0 | 0 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | RK73Z1ETTP |
| R25 | 0 | 0.002 | RES, 0.002, 2%, 1 W, 0508 | 0508 | KRL2012E-M-R002-G-T5 |
| TP9, TP10, TP11, TP12, TP13 | 0 | | Test Point, Miniature, Yellow, TH | Yellow Miniature Testpoint | 5004 |

**Table 5-2. TPS6593EVM Bill of Materials of Balance of Components**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| C2 | 1 | 150 µF | CAP, AL, 150 µF, 35 V, ± 20%, 0.17 Ω, SMD | 8 × 10 | UUD1V151MNL1GS |
| C4, C5, C6, C8, C10, C11, C12, C13, C15, C81, C85, C86, C88, C91, C96, C97, C109, C111, C115, C116 | 20 | 2.2 µF | CAP, CERM, 2.2 µF, 16 V, ± 20%, X7S, AEC-Q200 Grade 1, 0603 | 0603 | CGA3E1X7S1C225M080AC |
| C7, C18, C19, C20, C21, C22 | 6 | 22 µF | CAP, CERM, 22 µF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206 | 1206 | CGA5L1X7R0J226M160AC |
| C9, C14, C108, C110 | 4 | 0.47 µF | CAP, CERM, 0.47 µF, 10 V,± 10%, X7S, 0402 | 0402 | GCM155C71A474KE36D |
| C23, C34, C35, C37, C38, C39, C40, C41, C42, C43, C44, C93, C99, C100, C106 | 15 | 0.1 µF | CAP, CERM, 0.1 µF, 16 V,± 5%, X7R, AEC-Q200 Grade 1, 0402 | 0402 | GCM155R71C104JA55D |
| C24, C25, C26, C27, C28, C29, C30, C31, C32, C33 | 10 | 47 µF | CAP, CERM, 47 µF, 6.3 V, ± 20%, X7R, 1210 | 1210 | GCM32ER70J476ME19L |
| C36, C47, C58, C69, C78, C114 | 6 | 10 µF | CAP, CERM, 10 µF, 16 V, ± 10%, X7S, AEC-Q200 Grade 1, 0805 | 0805 | CGA4J1X7S1C106K125AC |
| C45, C46, C48, C49, C50, C51, C52, C53, C56, C57 | 10 | | Chip Multilayer Ceramic Capacitors for Automotive | 1206 (3216 Metric) | GCM31CD70G476ME |
| C54, C55, C59, C60, C61, C62, C63, C64, C65, C66 | 10 | 10 µF | CAP, CERM, 10 µF, 4 V, ± 20%, 1.6x × 0.8 mm | 1.6 × 0.8 mm | NFM18HC106D0G3 |
| C67, C68, C70, C71, C72, C73, C74, C75, C76, C77, C84 | 11 | | 3 Terminals Chip Multilayer Ceramic Capacitor (EMIFIL) | 0402 | NFM15HC105D0G3 |
| C80, C101, C102, C103, C104, C105 | 6 | 3300pF | CAP, CERM, 3300 pF, 50 V, ± 10%, X7R, 0603 | 0603 | C0603C332K5RACTU |
| C82, C83, C87, C89, C90, C98, C107 | 7 | 0.1 µF | CAP, CERM, 0.1 µF, 16 V, ± 10%, X7R, 0402 | 0402 | GCM155R71C104KA55D |
| C92, C95 | 2 | 12pF | CAP, CERM, 12 pF, 50 V,± 5%, C0G/NP0, AEC-Q200 Grade 1, 0402 | 0402 | GCM1555C1H120JA16J |
| C112, C113 | 2 | 22 µF | CAP, CERM, 22 µF, 6.3 V, ± 20%, X5R, 0603 | 0603 | GRM188R60J226MEA0D |
| D4, D5, D6 | 3 | Blue | LED, Blue, SMD | BLUE 0603 LED | LB Q39G-L2N2-35-1 |
| H1, H2, H3, H4 | 4 | | MACHINE SCREW PAN PHILLIPS 4-40 | | 9900 |
| H5 | 1 | | USB A MALE TO USB C Male | | 3021090-01M |
| H6, H7, H8, H9 | 4 | | | SPACER | FC2058-440-A |

**Table 5-2. TPS6593EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| J1, J2, J3, J4, J5, J6 | 6 | | Terminal Block, 5 mm, 2 × 1, R/A, TH | Terminal Block, 5 mm, 2 × 1, R/A, TH | 1792863 |
| J7, J8, J9, J10, J11, J15 | 6 | | Header, 100 mil, 11 × 1, Gold, TH | 11x1 Header | TSW-111-07-G-S |
| J12, J13, J14 | 3 | | Header, 100 mil, 7 × 1, Gold, TH | 7 × 1 Header | TSW-107-07-G-S |
| J18, J19, J20, J21, J26, J30, J37 | 7 | | Header, 2.54 mm, 3 × 1, Gold, TH | Header, 2.54 mm, 3 × 1, TH | 61300311121 |
| J22 | 1 | | Receptacle, 0.5 mm, USB TYPE C, R/A, SMT | Receptacle, 0.5 mm, USB TYPE C, R/A, SMT | 12401610E4#2A |
| J27, J28, J29 | 3 | | Board-To-Board Connector, Vertical, ESQ Series, 8 Contacts, Receptacle, 2.54 mm, Through Hole | HDR8 | ESQ-108-14-T-S |
| J45, J46 | 2 | | Header, 100mil, 3x1, Gold, SMT | Samtec_TSM-103-01-X-SV | TSM-103-01-L-SV |
| L1, L2, L3, L4, L5 | 5 | 470 nH | Inductor, Thin Film, 470 nH, 5.3 A, 0.021 Ω, AEC-Q200 Grade 0, SMD | TDK Inductor | TFM322512ALMAR47MTAA |
| LBL1 | 1 | | | PCB Label 0.650 × 0.200 inch | THT-14-423-10 |
| R1, R3, R5, R7, R19, R36, R40, R56, R57, R58, R65, R67, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92 | 22 | 0 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | RK73Z1ETTP |
| R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R27, R28, R29, R31, R33, R34, R37, R38, R42, R44, R46, R47, R49, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R93, R94, R95 | 40 | 10 k | RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW040210K0JNED |
| R23, R24, R50, R59 | 4 | 1.2 k | RES, 1.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021K20JNED |
| R25 | 1 | 0.002 | RES, 0.002, 2%, 1 W, 0508 | 0508 | KRL2012E-M-R002-G-T5 |
| R30 | 1 | 240 | RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW0402240RJNED |
| R32, R45, R51, R54 | 4 | 100 | RES, 100, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW0402100RJNED |
| R41, R43, R52 | 3 | 4.87 k | RES, 4.87 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04024K87FKED |

**Table 5-2. TPS6593EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| R48, R55, R60, R68, R69 | 5 | 1.0 Meg | RES, 1.0 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021M00JNED |
| R53 | 1 | 200 k | RES, 200 k, 5%, 0.063 W, 0402 | 0402 | CRCW0402200KJNED |
| R61, R62, R63, R64 | 4 | 1.0 k | RES, 1.0 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021K00JNED |
| R66 | 1 | 374 k | RES, 374 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW0402374KFKED |
| S1 | 1 | | Switch, SPST, Off-On, 50 mA,24V, SMD | 6 × 3.5 mm | 147873-1 |
| SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16 | 16 | | Shunt, 100mil, Gold plated, Black | Shunt 2 pos. 100 mil | 881545-2 |
| TP1, TP2 | 2 | | Test Point, Miniature, Red, TH | Red Miniature Testpoint | 5000 |
| TP3, TP4, TP5, TP14 | 4 | | Test Lead clips and hooks, SMT | Test Point, Body 3.25 × 1.65 mm | S1751-46 |
| TP6, TP7, TP8 | 3 | | Test Point, Miniature, Yellow, TH | Yellow Miniature Testpoint | 5004 |
| U1 | 1 | | Power Management IC (PMIC) With 4-Phase 14-A Buck for Processors, RVJ0056A (VQFN-56) | RVJ0056A | TPS65941-Q1 |
| U2 | 1 | | AEC-Q100 Quad Comparator, PW0014A (TSSOP-14) | PW0014A | LM2901AVQPWRQ1 |
| U3 | 1 | | MSP432E401YTPDT, PDT0128A (TQFP-128) | PDT0128A | MSP432E401YTPDTR |
| U4 | 1 | | Low-Capacitance 6-Channel ±15 kV ESD Protection Array for High-Speed Data Interfaces, RSE0008A (UQFN-8) | RSE0008A | TPD6E004RSER |
| U5 | 1 | | 4-Channel USB ESD Solution with Power Clamp, DRY0006A (USON-6) | DRY0006A | TPD4S012DRYR |
| U6, U13 | 2 | | Automotive Catalog, Dual, 200 mA, Low-IQ Low-Dropout Regulator for Portable Devices, DSE0006A (WSON-6) | DSE0006A | TLV7103318QDSERQ1 |

**Table 5-2. TPS6593EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| U7, U10 | 2 | | 0.5Ω Dual SPDT Bidirectional Analog Switch, RSW0010A (UQFN-10) | RSW0010A | TS3A5223RSWR |
| U8, U9 | 2 | | 8-BIT BIDIRECTIONAL LOW-VOLTAGE TRANSLATOR, PW0020A (TSSOP-20) | PW0020A | SN74GTL2003PWR |
| U11, U12 | 2 | | 10 Ω Quad SPDT Analog Switch, RSV0016A (UQFN-16) | RSV0016A | TS3A5018RSVR |
| U14 | 1 | | 5 V, Boost Charge Pump, 300 mA, 2.7 to 5.4 V Input with Synchonrization pin, -40 to 85°C, 20-pin SOP (PWP20), Green (RoHS & no Sb/Br) | PWP0020C | TPS60110PWPR |
| Y1 | 1 | | Crystal, 32.768 KHz, 9 pF, AEC-Q200 Grade 1, SMD | 1.5 × 3.2 mm | NX3215SD-STD-MUS-6 |
| Y2 | 1 | | Crystal, 25 MHz, 8 pF, SMD | 3.2 × 0.75 × 2.5 mm | NX3225GA-25.000M-STD-CRG-2 |
| C1, C94 | 0 | 22 µF | CAP, CERM, 22 µF, 6.3 V, ± 10%, X7R, AEC-Q200 Grade 1, 1206 | 1206 | CGA5L1X7R0J226M160AC |
| C3 | 0 | 47000 µF | CAP, Electric Double Layer, 47000 µF, 5.5 V, +80/-20%, TH | Horizontal D11.5 × 5 mm | DX-5R5H473U |
| C16, C17 | 0 | | CAP CER 6PF 50 V C0G 0402 | 0402 | GCM1555C1H6R0CA16 |
| C79 | 0 | 680 µF | CAP, TA, 680 µF, 6.3 V, ± 10%, 0.023 Ω, AEC-Q200 Grade 1, SMD | 7343-40 | T510X687K006AGA023 |
| D1 | 0 | 10V | Diode, Zener, 10 V, 300 mW, SOD-323 | SOD-323 | MM3Z10VST1G |
| D2 | 0 | 40V | Diode, Schottky, 40 V, 2 A, SOD-123F | SOD-123F | DB2W40200L |
| D3 | 0 | Blue | LED, Blue, SMD | BLUE 0603 LED | LB Q39G-L2N2-35-1 |
| FID6 | 0 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A |
| J16, J17 | 0 | | Receptacle, 2.5 mm, 3 × 2, Gold, SMT | Receptacle, 2.5 mm, 3 × 2, SMT | 6651712-1 |
| J23, J24, J25 | 0 | | JUMPER TIN SMD | 6.85 × 0.97 × 2.51 mm | S1911-46R |
| J31 | 0 | | Header (Shrouded), 1.27 mm, 5 × 2, Gold, SMT | Header(Shrouded), 1.27 mm, 5 × 2, SMT | FTSH-105-01-F-DV-K |

**Table 5-2. TPS6593EVM Bill of Materials of Balance of Components (continued)**

| Designator | Quantity | Value | Description | Package Reference | Part Number |
|---|---|---|---|---|---|
| J32, J33, J34, J35, J36 | 0 | | SMA Jack, Straight, 50 Ω, Gold, TH | TH, 5-Leads, Body 7 × 7 mm | SMA-J-P-H-ST-TH1 |
| J39, J40, J41 | 0 | | Header, 100 mil, 3 × 1, Gold, SMT | Samtec_TSM-103-01-X-SV | TSM-103-01-L-SV |
| J42, J43, J44, J47 | 0 | | Header, 100 mil, 2 × 1, Tin, SMD | SMD, 2-Leads, Body 200 × 100 mil | TSM-102-01-T-SV-P-TR |
| Q1 | 0 | 30 V | MOSFET, N-CH, 30 V, 27.2 A, AEC-Q101, SO-8FL | SO-8FL | NVMFS4C05NT1G |
| R2, R4, R6, R26, R35, R39 | 0 | 0 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | RK73Z1ETTP |
| R20, R21 | 0 | 240 | RES, 240, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW0402240RJNED |
| R22 | 0 | 1.2 k | RES, 1.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | 0402 | CRCW04021K20JNED |
| TP9, TP10, TP11, TP12, TP13 | 0 | | Test Point, Miniature, Yellow, TH | Yellow Miniature Testpoint | 5004 |

## 6 Additional Resources

- Texas Instruments, Programmable Processor PMIC's GUI User's Guide
- Texas Insturments, TPS65921-Q1 Power Management IC (PMIC) With 4-Phase 14-A Buck for Processors

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (September 2019) to Revision A (January 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added caution image to the *Abstract* section | 1 |
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 3 |
| • Updated the *Abstract* section | 3 |
| • Updated the *EVM Descriptions* table in the *Introduction* | 3 |
| • Updated the *Getting Started* section | 3 |
| • Updated the *EVM Details* section | 5 |
| • Changed VSYS_IN to VSYS in the *Terminal Blocks* section | 6 |
| • Updated the *Configuration Headers* section | 7 |
| • Updated the *LDO Headers* figure | 9 |
| • Updated the *Stack-Up Headers* section | 10 |
| • Updated the *Connectors* section | 13 |
| • Updated the *EVM Control,GPIO, and Additional Regulators* section | 13 |
| • Updated *Changing the Communcation Interface* section | 13 |
| • Added the *TPS6594EVM and TPS6593EVM Interface Settings for Communication* figure | 13 |
| • Removed the *Interface Settings for SPI Communication* figure | 13 |
| • Updated the *Phase Configuration Components* figure | 16 |

## STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

**WARNING**

**Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.**

**User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.**

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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8. *Limitations on Damages and Liability:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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