TPS7H4001QEVM-CVAL Evaluation Module User's Guide

The TPS7H4001QEVM-CVAL is the evaluation module (EVM) that demonstrates parallel, quadrature phase operation of four TPS7H4001-SP devices. With this parallel configuration, the 4-Channel design is capable of providing up to 72-Amps of load current to a single regulated line. This user's guide provides details about the EVM, its configuration, schematics, and BOM. In addition, links to application reports explaining how to modify this EVM to convert it into a 1-Channel, 2-Channel, or 3-Channel design are provided in the references at the end of the document.

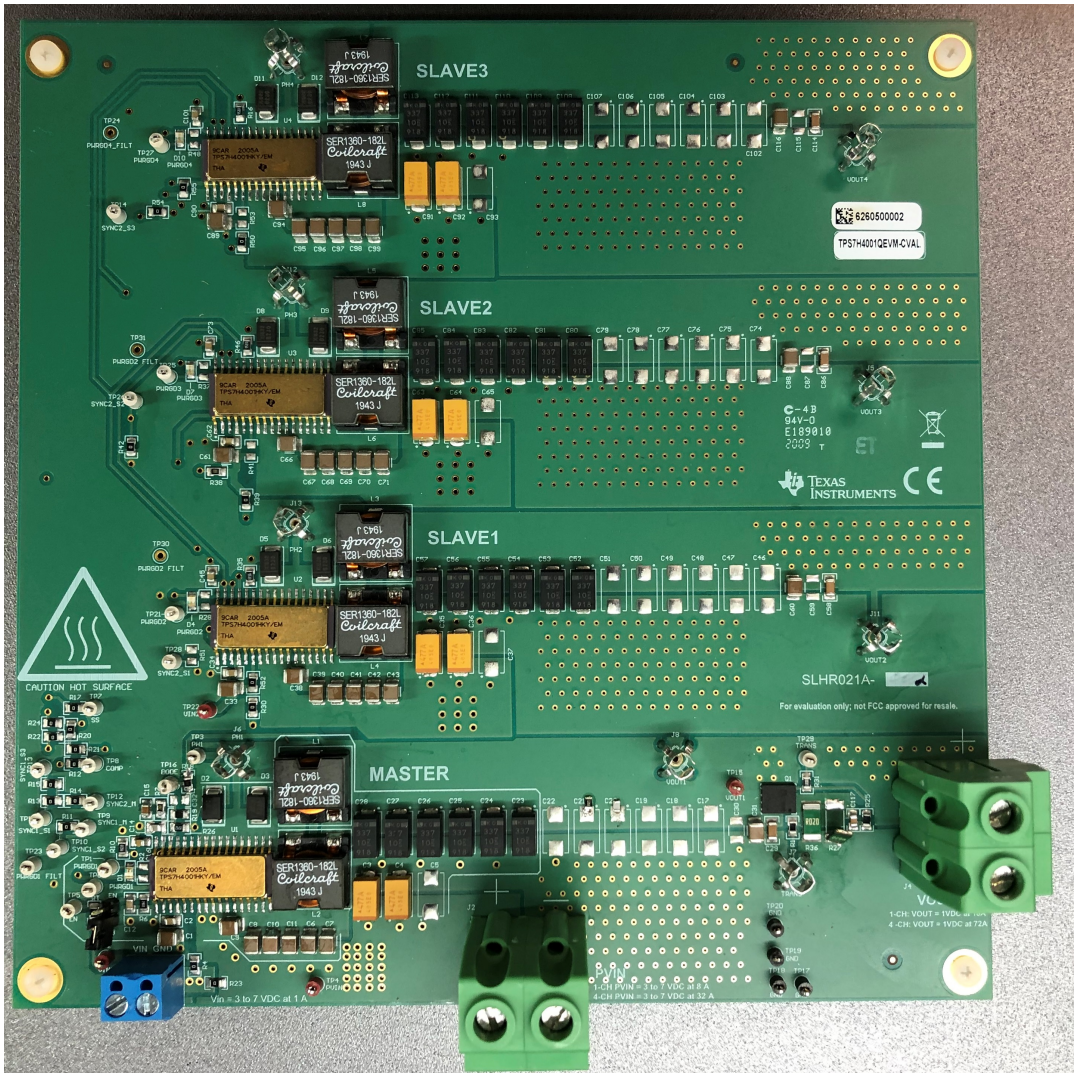

Figure 1. TPS7H4001QEVM-CVAL -002 (Quad Channel)

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1 TPS7H4001QEVM-CVAL Overview

The TPS7H4001-SP is a radiation hardened, 7-V, 18-A synchronous step-down converter with integrated high-side and low-side MOSFETs. High efficiency and efficient usage of space are achieved through low resistance MOSFETs and a current mode control implementation.

The EVM is configured in a default state to accept a 5-V input but can be modified to disable or change the under voltage lock out (UVLO) protection, allowing for any input voltage from 3 V to 7 V. The EVM is also configured for a 1-V output. . The regulated output voltage can be modified by changing one resistor on the board. The TSP7H4001-SP has a dedicated soft start, enable, and adjustable slope compensation pins providing design flexibility to meet specific application requirements.

Finally, as shown in Figure 1, this EVM is populated and configured to support four channel parallel operation. However, users may wish to evaluate 1-channel, 2-channel, or 3-channel operation using this same EVM. Please refer to series of application reports that are available outlining the modifications needed to the BOM to make such conversions.

1.1 Features

- 0.6-V ±1.5% voltage reference over temperature, radiation, and line and load regulation
- Adjustable slope compensation
- Adjustable soft start
- Adjustable input enable and undervoltage lockout (UVLO)
- Maximum output current of 72 A

1.2 Applications

- High current point of load regulation
- Supports harsh environment applications
- Space satellite point of load supply for FPGAs, microcontrollers, data converters, and ASICs
- Space satellite payloads
- Radiation hardened applications

2 TPS7H4001QEVM-CVAL Default Configuration

Table 1 describes the default configuration of the TPS7H4001QEVM-CVAL listing the external components that define the complete parallel converter design.

Table 1. Default EVM Configuration

PARAMETER	SPECIFICATIONS	DESCRIPTION
Input power supply	5 V	Bound by UVLO enable circuit (R5, R6)
Regulated output voltage	1 V	R19 (RTOP) = 10 kΩ, R26 (RBOTTOM) = 15.4 kΩ
L_{OUT} per converter	0.9 µH	Chosen to meet inductor ripple current of 10% (Kind = 0.1)
C_{OUT} per converter	1980 µF	Chosen for (1) ESR = 1 mΩ to set output voltage ripple; (2) value used during single event effects testing ensuring regulation maintained with single event upset to switching
Output current per converter	0 to 18 A	By design
Switching frequency	500 kHz	Set by R9 (RT) = 174 kΩ
Soft start time constant	≈2 ms	Set by C13 (Css) = 39 nF
UVLO enable rising	≈4.249 V	Set by R5 = 10 kΩ and R6 = 3.4 kΩ
UVLO enable falling	≈4.011 V	Set by R5 = 10 kΩ and R6 = 3.4 kΩ
Loop bandwidth	≈25 kHz	Set by operational transconductance amplifier (OTA) compensation circuit: R7 (RCOMP) = 2 kΩ, C15 (CCOMP) = 33 nF, C14 (CHF) = 330 pF
Loop phase margin	≈60°	
Gain margin	≈–25 dB	

3 TPS7H4001QEVM-CVAL Initial Setup

This section provides the test instruments required and the connections to the EVM as shown in Figure 2.

1. Remove Jumper J9 so that enable pins to all devices is no longer grounded.
2. Input DC power supply
   a. Set for 5-V DC, 30-A current limit
   b. Connect positive output of DC supply to pin 1 of connector J2 (PVIN) and negative terminal of supply to pin 2 of connector J2 for ground using 16 AWG wire or larger. [Note: For more precise measurements, eliminating the IR voltage drop in the input cables is achieved by using a power supply source with sensing ports and connecting between TP4 to PVIN and TP18 to GND.]
3. DC electronic load
   a. Connect positive DC input of e-load to pin 2 of connector J4 (VOUT) using 16 AWG wire.
   b. Connect negative DC input of e-load to pin 1 of connector J4 (VOUT) using 16 AWG wire.
   c. Connect voltage monitoring sensing ports of e-load across test points TP15 (VOUT1) and TP20 (GND). A voltage meter can be used to monitor this voltage also.
4. Oscilloscope
   a. CH1 - Connect voltage scope probe to scope probe test point J6 (PH1) to monitor the phase node. DC coupled, Full BW, 2 V/div, Rising Edge Trigger at 0.5 V.
   b. CH2 - Connect voltage scope probe to scope probe test point J13 (PH2) to monitor the phase node. DC coupled, Full BW, 2 V/div, Rising Edge Trigger at 0.5 V.
   c. CH3 - Connect voltage scope probe to scope probe test point J12 (PH3) to monitor the phase node. DC coupled, Full BW, 2 V/div, Rising Edge Trigger at 0.5 V.
   d. CH4 - Connect voltage scope probe to scope probe test point J10 (PH4) to monitor the phase node. DC coupled, Full BW, 2 V/div, Rising Edge Trigger at 0.5 V.

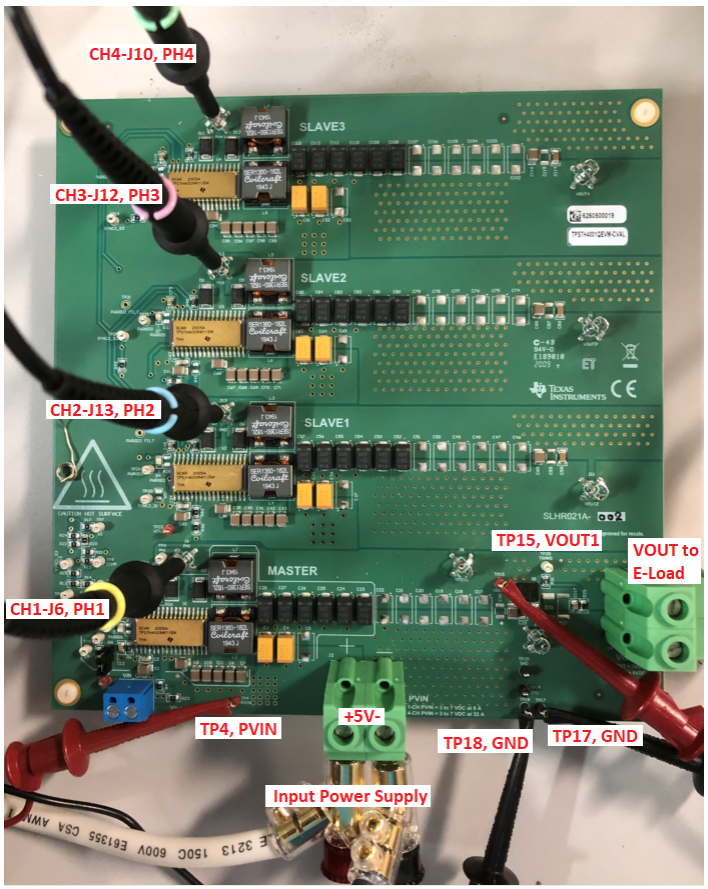

Figure 2. TPS7H4001QEVM-CVAL Initial Setup

Table 2. Summary of Connections

Reference Designator	Silkscreen	Function
J2	PVIN	Input power: pin 1 = 5 V, pin 2 = GND (Vsupply)
J4	VOUT	Output voltage: pin 1 = GND, pin 2 = Vout ≈1 V (e-load)
J6	PH1	Phase switching node scope probe test point (Scope CH-1)
J13	PH2	Phase switching node scope probe test point (Scope CH-2)
J12	PH3	Phase switching node scope probe test point (Scope CH-3)
J10	PH4	Phase switching node scope probe test point (Scope CH-4)
TP15	VOUT1	VOUT1 test point (e-load monitor)
TP4	PVIN	PVIN test point (Vsupply_sense)
TP17, TP18	GND	GND test points (Vsupply_sense, e-load monitor)

4 TPS7H4001QEVM-CVAL Testing

The following tests will be described in subsequent sections.

1. Output voltage regulation
2. Quadrature Phases
3. Output voltage ripple
4. Soft startup
5. Transient response to positive/negative load step (27 A to 67 A to 27 A)
6. Loop frequency response
7. Efficiency
8. Current limiting
9. Current Sharing

4.1 Output Voltage Regulation

- Turn-on input DC source (5 V)
- Turn on the e-load and sweep load current from 0 A to 72 A. The monitored output voltage at TP15 (VOUT1) is at or near 1.0 V across the entire current load sweep as shown in Figure 3.

Figure 3. Line Regulation (VIN = 5 V, VOUT = 1 V, IOUT = 0A to 72 A)

4.2 Quadrature Phases

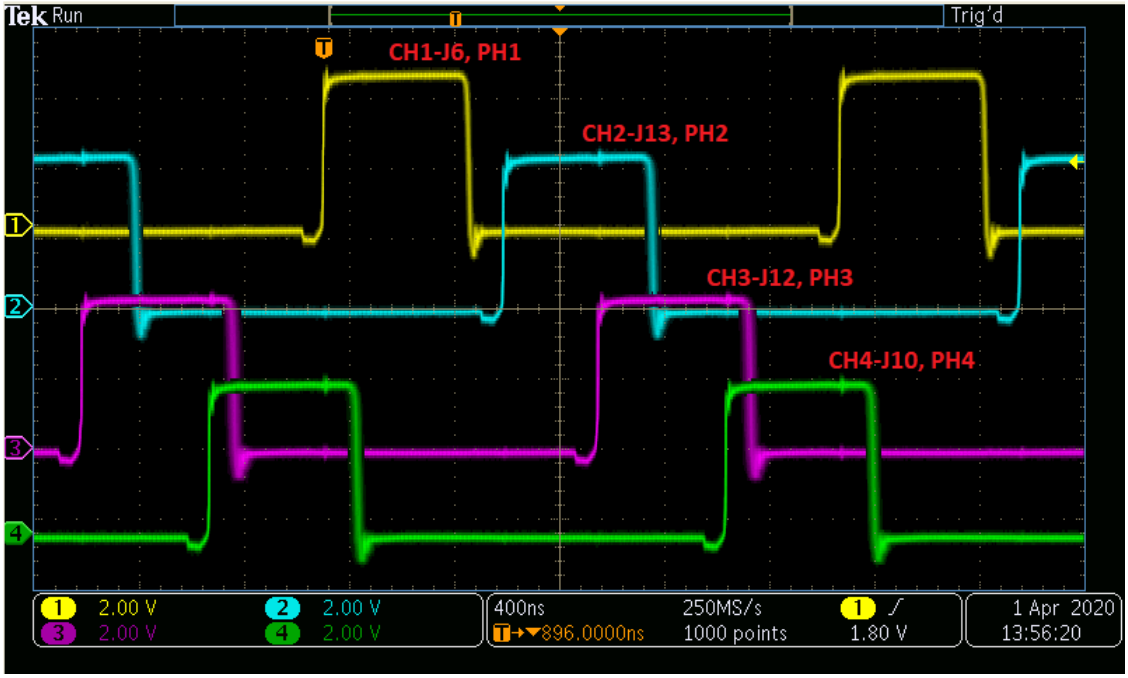

Figure 4. Quadrature Phase Nodes (VIN = 5 V, VOUT = 1 V, IOUT = 72 A)

4.3 Output Voltage Ripple

Display CH1 (PH1) and CH2 (VOUT1) [AC coupled, BW = 20 MHz] on oscilloscope to monitor the switching phase node and the output voltage ripple as shown in Figure 5.

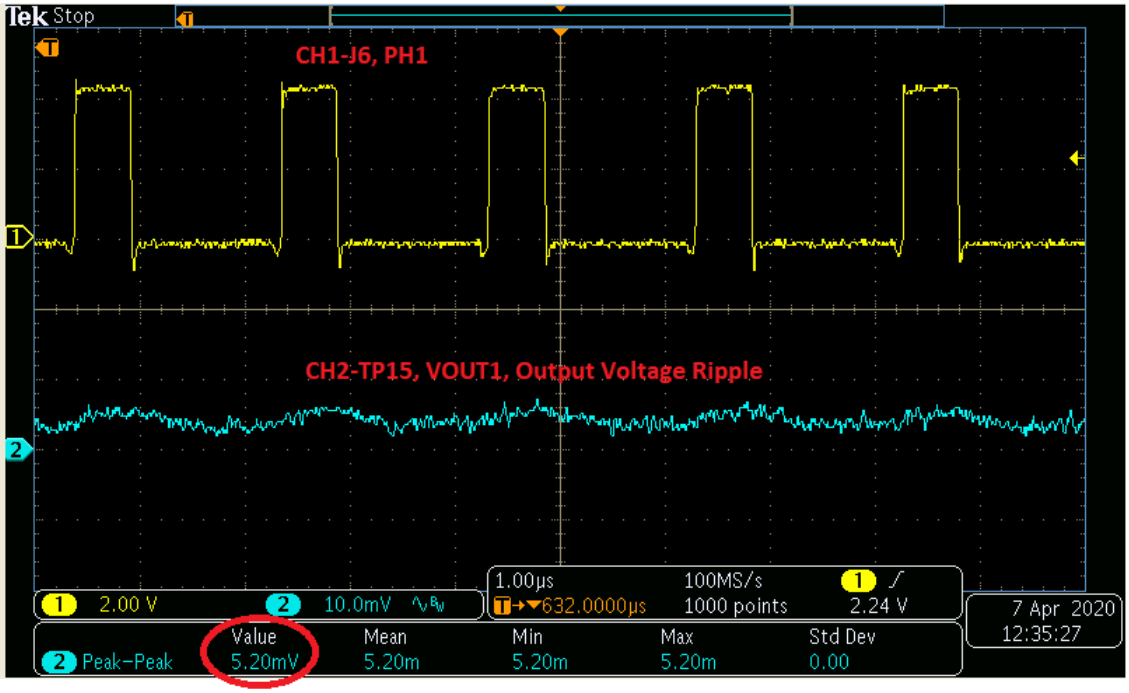

Figure 5. Output Voltage Ripple (VIN = 5 V, VOUT = 1 V, IOUT = 72 A)

4.4 Soft Startup

Display CH1 (PH1) and CH2 (VOUT1) [DC coupled, 500 mV/div] on oscilloscope to monitor the switching phase and the soft start profile of the output voltage as shown in Figure 6.

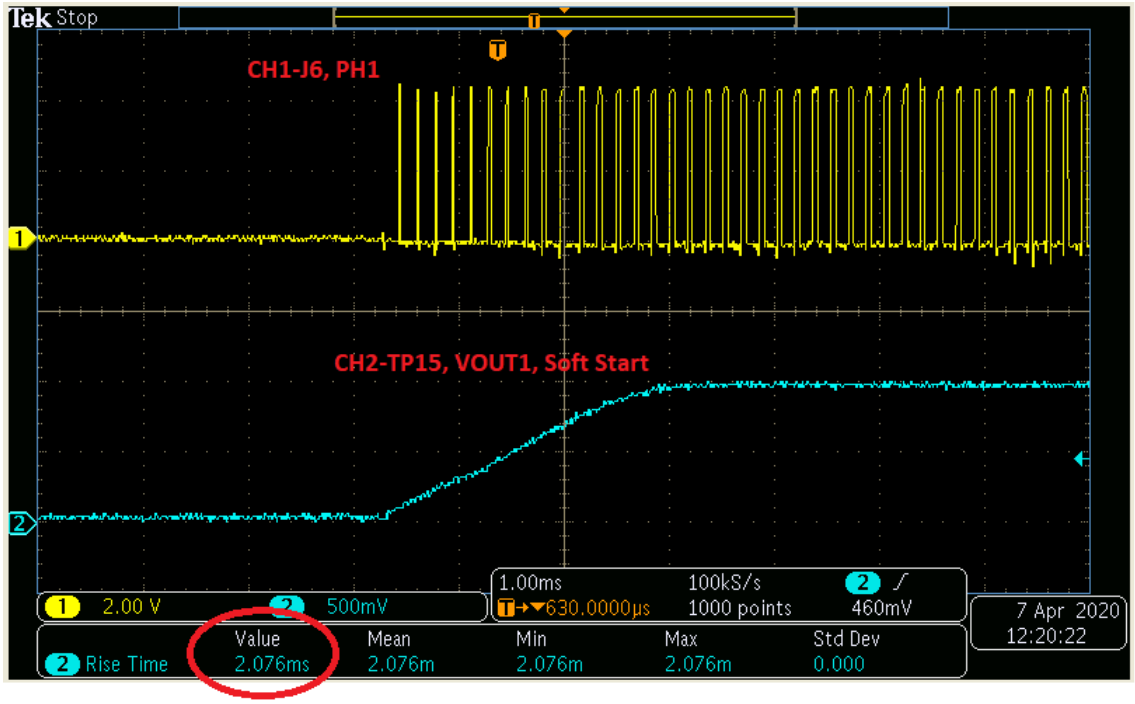

Figure 6. VOUT Soft Start (VIN = 5 V, VOUT = 1 V, IOUT = 72 A)

4.5 Transient Response to Positive/Negative Load Step (27 A to 67 A to 27 A)

The TPS7H4001QEVM-CVAL hardware contains a sub-circuit which is useful for measuring the transient response to a very high current step. See Section 8 for full explanation of how the test is conducted and circuit is used.

Figure 7 shows the response to an estimated 40A load step to be approximately 60mV.

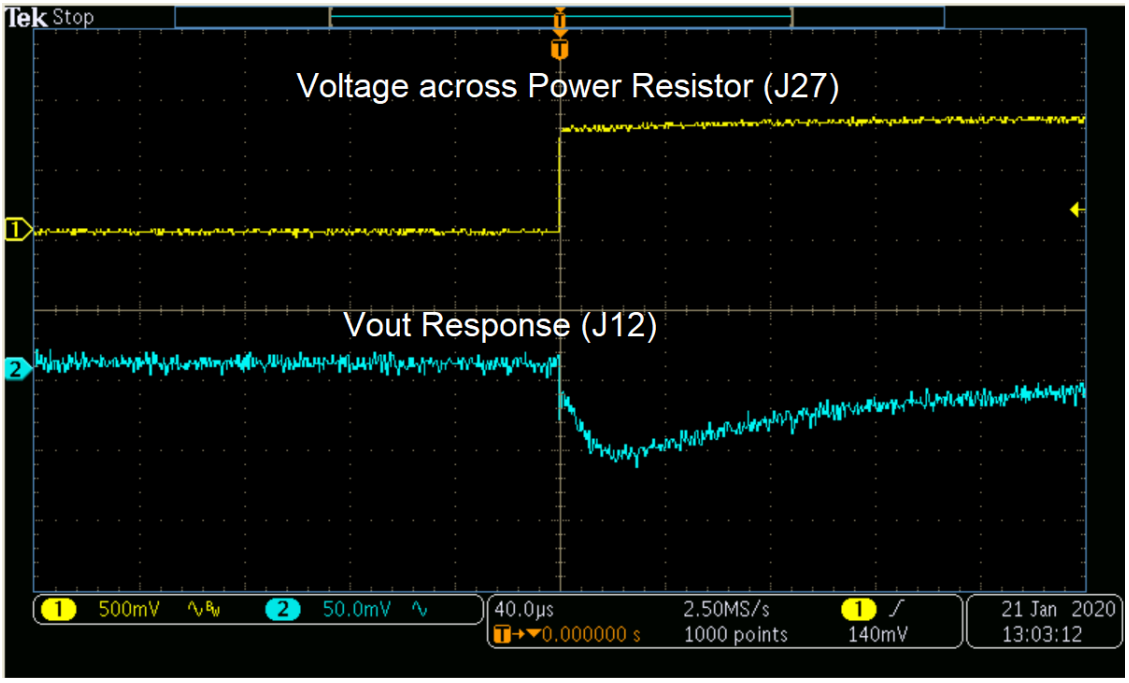

Figure 7. Vout Transient Response to Current Step from 27A to 67A

- Change the trigger on CH1 to falling edge to capture the transient response of VOUT to negative current step from 67 A to 27 A as shown in Figure 8.

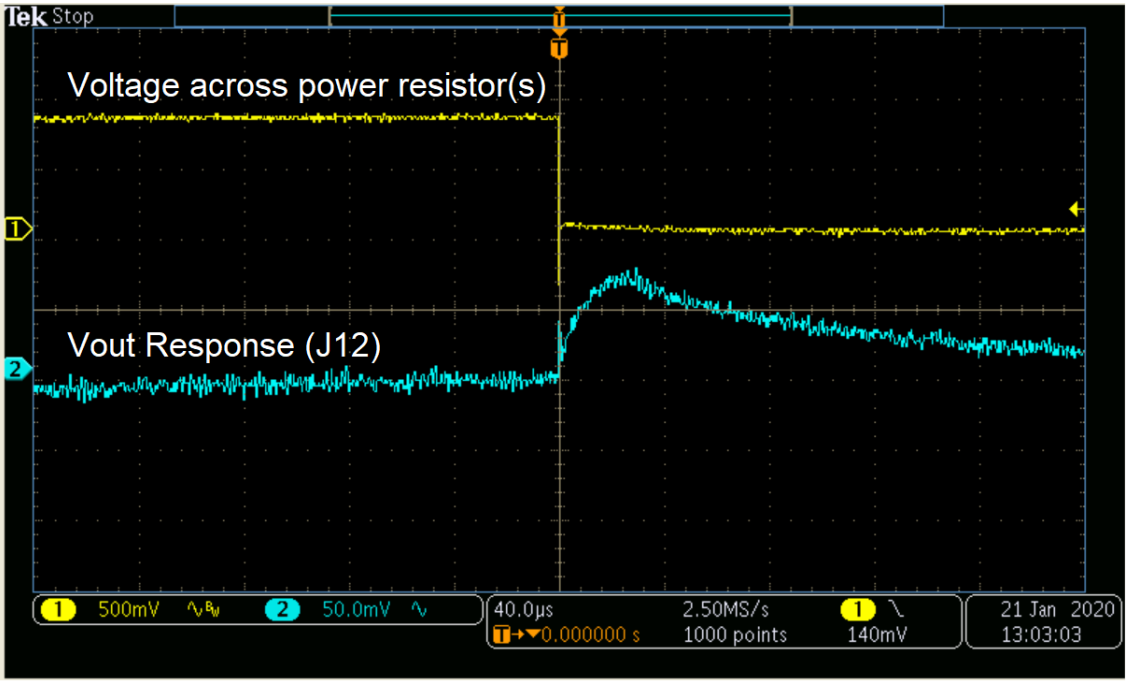

Figure 8. Vout Transient Response to Current Step from 67A to 27A

4.6 Loop Frequency Response

Measuring the frequency response of the feedback loop requires a unique test setup as well as physical changes to the EVM. 0-Ω resistor jumper R18, to the right of TP16 (BODE) test point and circled in yellow in the graphic below, must be lifted in order to break the loop. Both test points TP16 (BODE) and TP15 (VOUT1) will be used for connections to the Bode100 instruments.

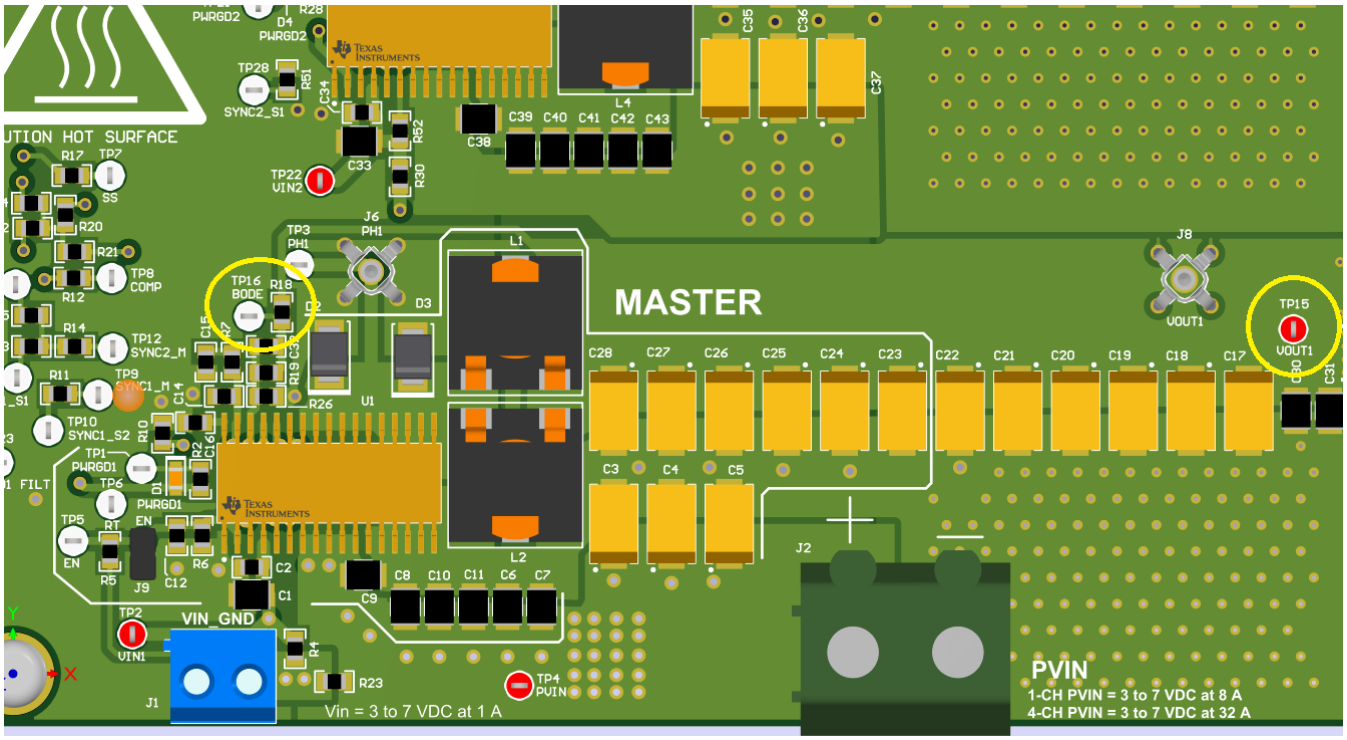

Figure 9. EVM Modification to Measure Frequency Response

The test setup which includes several connections to Picotest Bode100 test instruments is shown in Figure 10 with measurement results shown in Figure 11.

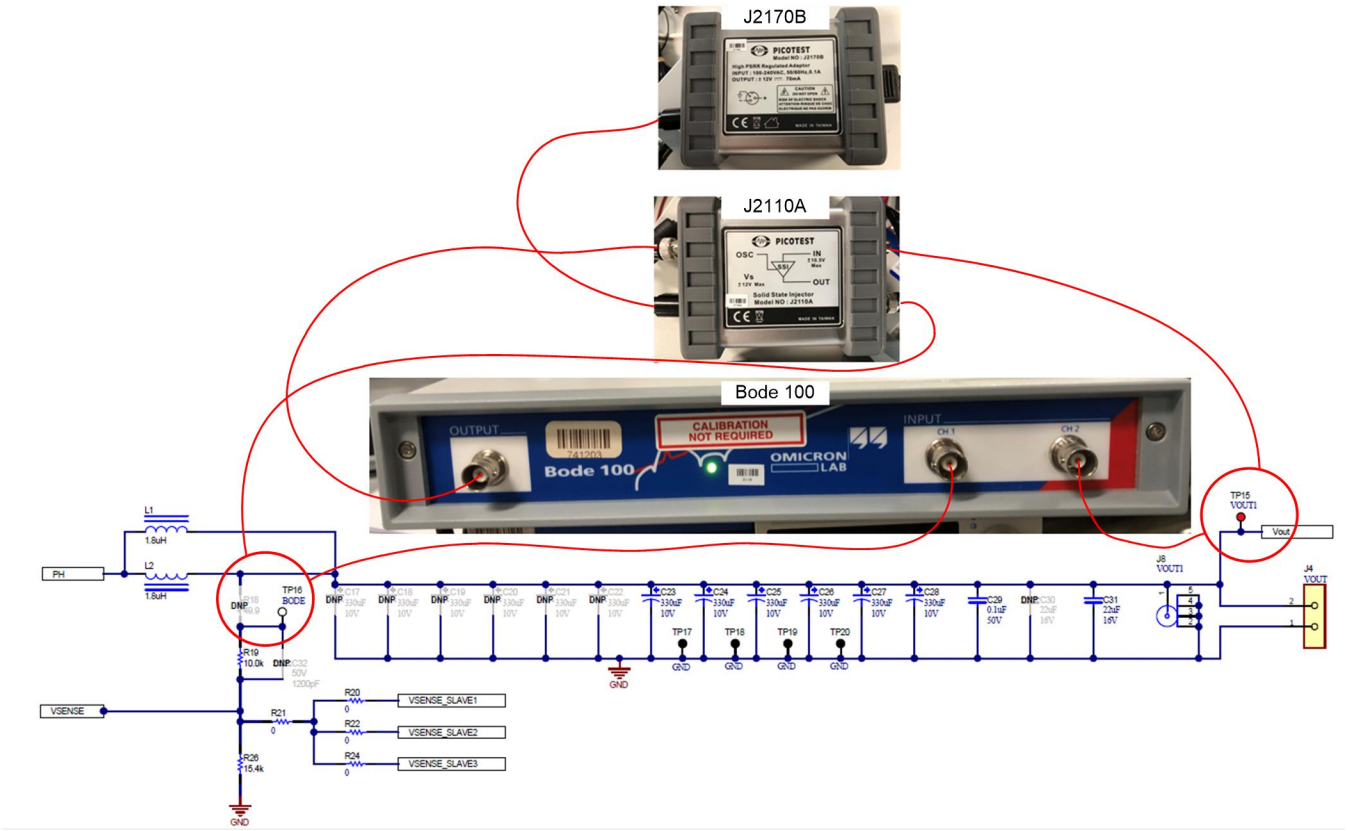

Figure 10. Frequency Response Measurement Setup

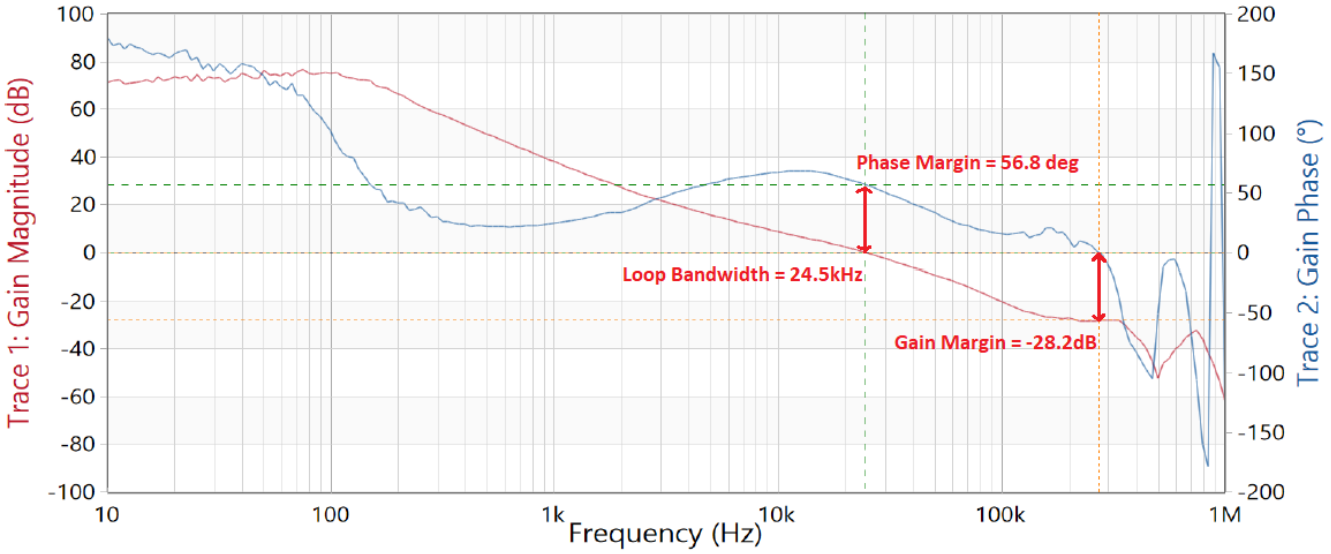

Figure 11. Loop Frequency Response (Rcomp=2kohms, Ccomp=33nF, CHF=330pF)

4.7 Efficiency

The efficiency of the 4-channel design was measured from a 0A to 72A load currents. Figure 12 shows a peak efficiency of Y% at 9A load and X% at 72A load. The measurement recordings for this test were done without instrument automation and without controlled DUT temperature. Therefore, self heating effects of the device are evident in the slight curvature of the plot.

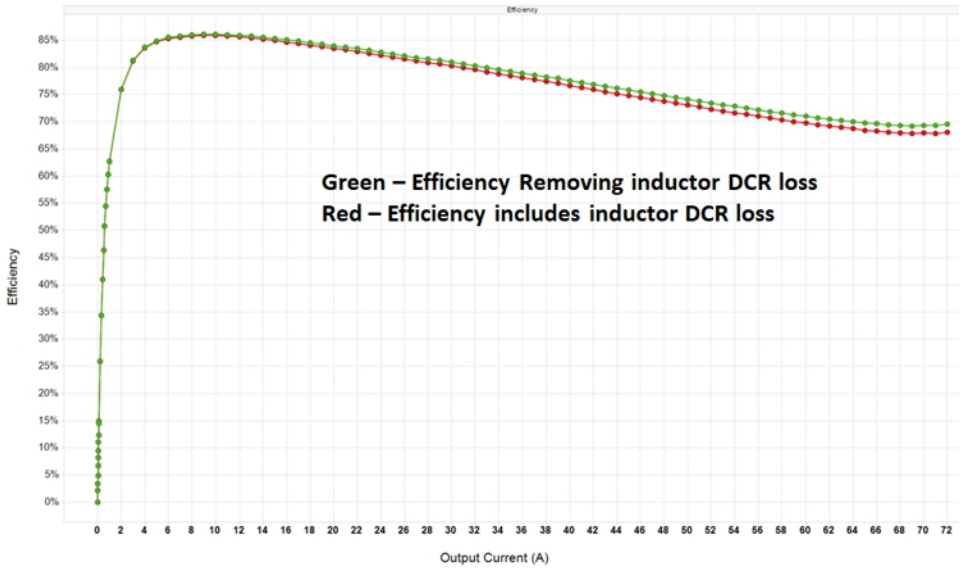

Figure 12. Typical Characteristics Efficiency

4.8 Current Limiting

Finally, it is worth mentioning the behavior of the device with regards to current limiting. Although, the recommended operating condition (ROC) of the device is to never exceed 18-A peak current per converter, the design is robust enough to handle output currents up to the limiting mechanism of the device, which is typically 25 A, without damage to the DUT. This does not mean that external components cannot be damaged so it is imperative that the ratings of these components be in line with intended and, potential, unintended operational conditions.

Figure 13 shows what happens when the high side current limit threshold is exceeded. The soft start pin is pulled low which causes the switching phase node to stop switching. This, in turn, causes the output voltage to drop causing VSENSE (not shown) to drop. Only after the soft start pin re-establishes a voltage level equal to the VSENSE pin (VOUT) does the device start switching again as shown in zoomed out version of Figure 14.

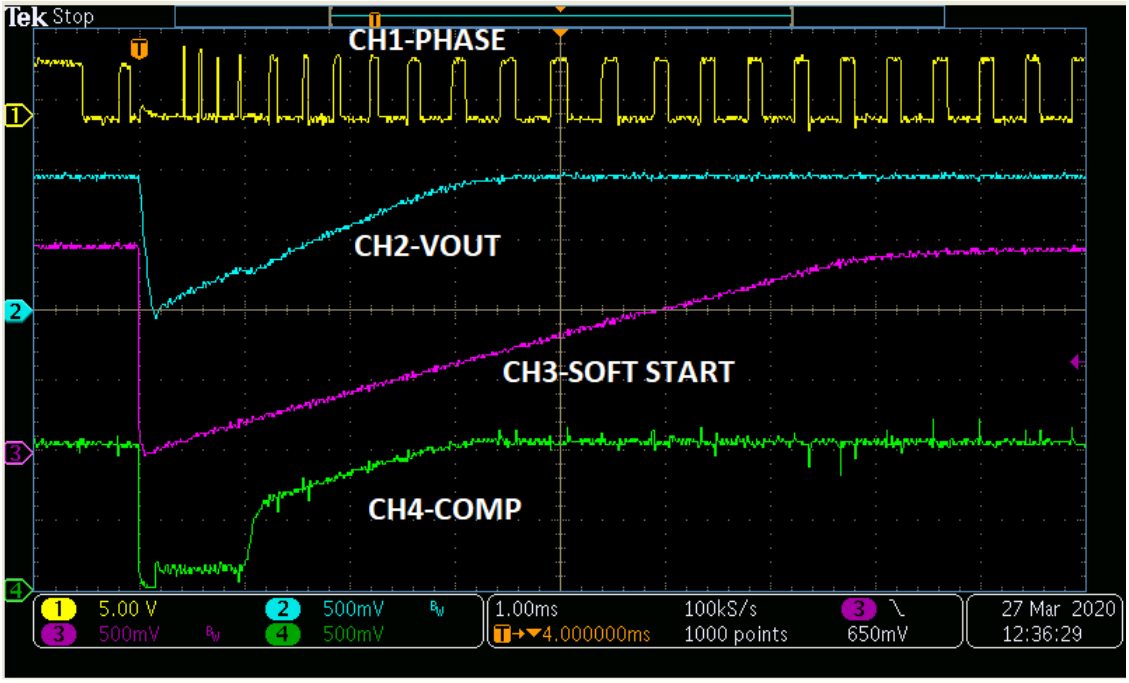

Figure 13. High Side Current Limiting

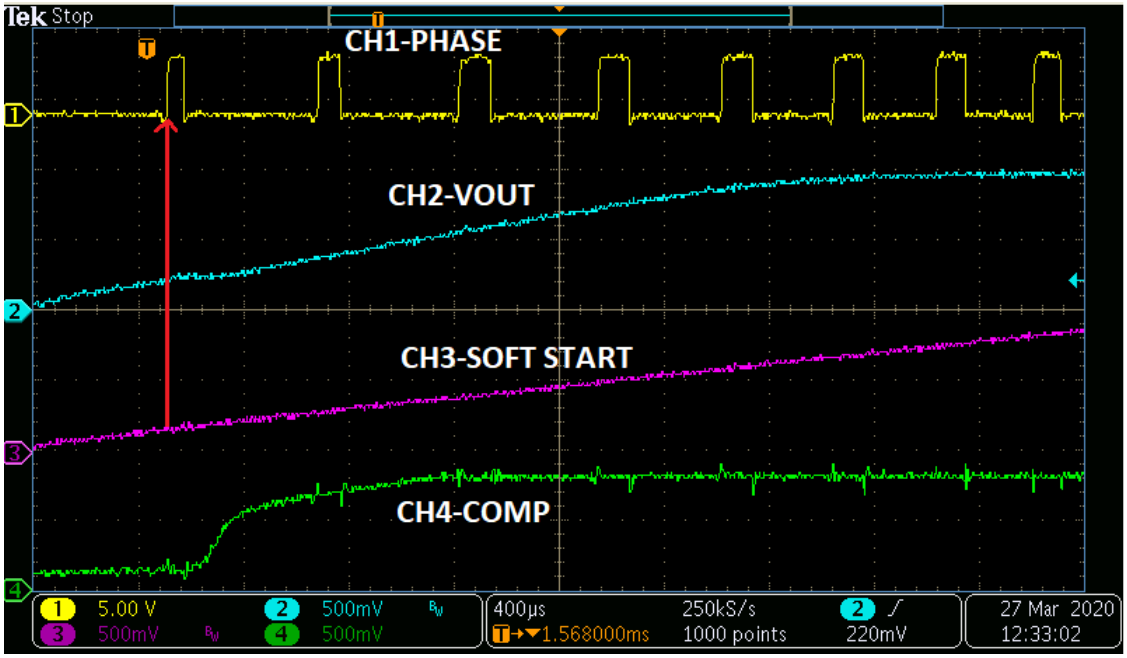

Figure 14. High Side Current Limiting - Zoomed In

4.9 Current Sharing

One important consideration when operating devices in parallel configuration is how the total current is shared among the converters. Designers of such parallel systems want to ensure that each converter remains within the recommended operating conditions of the data sheet while also considering worst case conditions. Ensuring this is not a trivial task but can be achieved through various approaches. The most straight forward approach, and the one resulting in the most conservative design, is to take the worst case condition and apply it to all converters regardless of the statistical improbability of such an occurrence. Another approach is to characterize the devices in a parallel system allowing designers to eliminate a signficant amount of variation by having an understanding of the baseline starting point under nominal conditions.

Regardless of the approach, an assumption is made that the ouput current of each converter will be proportional to that converter's power stage transconductance (gmps, or COMP to Iswitch gm in the data sheet). Looking at the electrical characteristics table of the data sheet, one can see that this parameter is specified with an approximate tolerance of +/- 28% regardless of temperature. Without applying any practical engineering judgement, this specification says that in order to guarantee that no single converter exceeds the ROC peak current of 18A (assuming 10% current peaking), the nominal design would target ~13.5A. Allowing for lowest gmps (-28%), the design would provide 9.8A per converter. Extrapolating this worst case even further by assuming all four parallel converters would have the lowest gmps value, a 4-channel parallel design would provide ~39A of total load current. One can certainly design with such assumptions and create a very conservative design. However, doing so would ignore the fact that realizing such a worst case implementation is highly improbable.

By characterizing a parallel system through measurements, the tolerance window of +/-28% can be greatly reduced allowing for more optimal design. Figure 15 and Figure 16 shows how current sharing on a 4-Channel design was characterized. The EVM was modified to allow for a current probe to measure the current out of each converter by placing a wire between the PHASE node of the DUT and the output inductors.

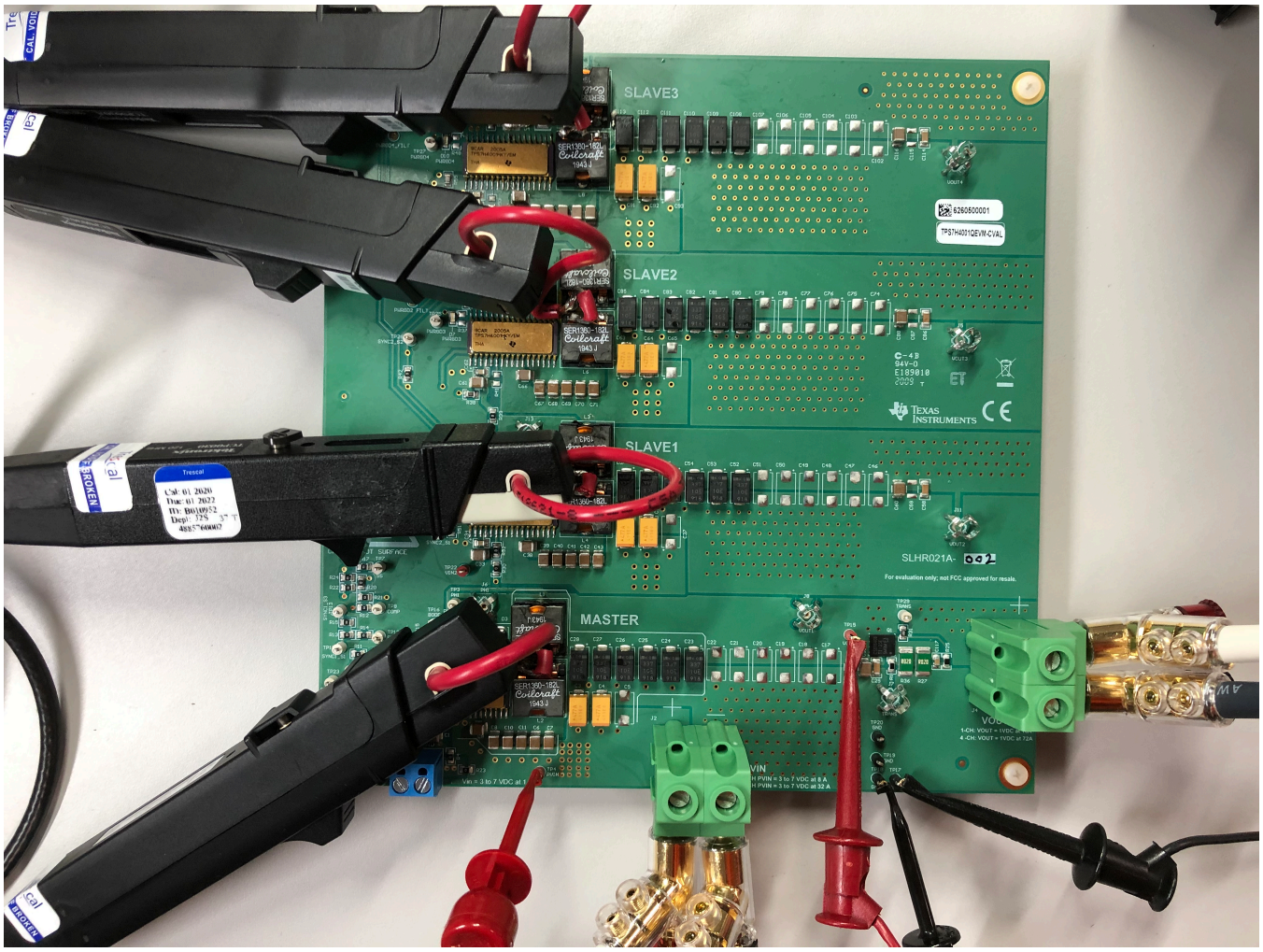

Figure 15. Current Sharing Measurement Setup

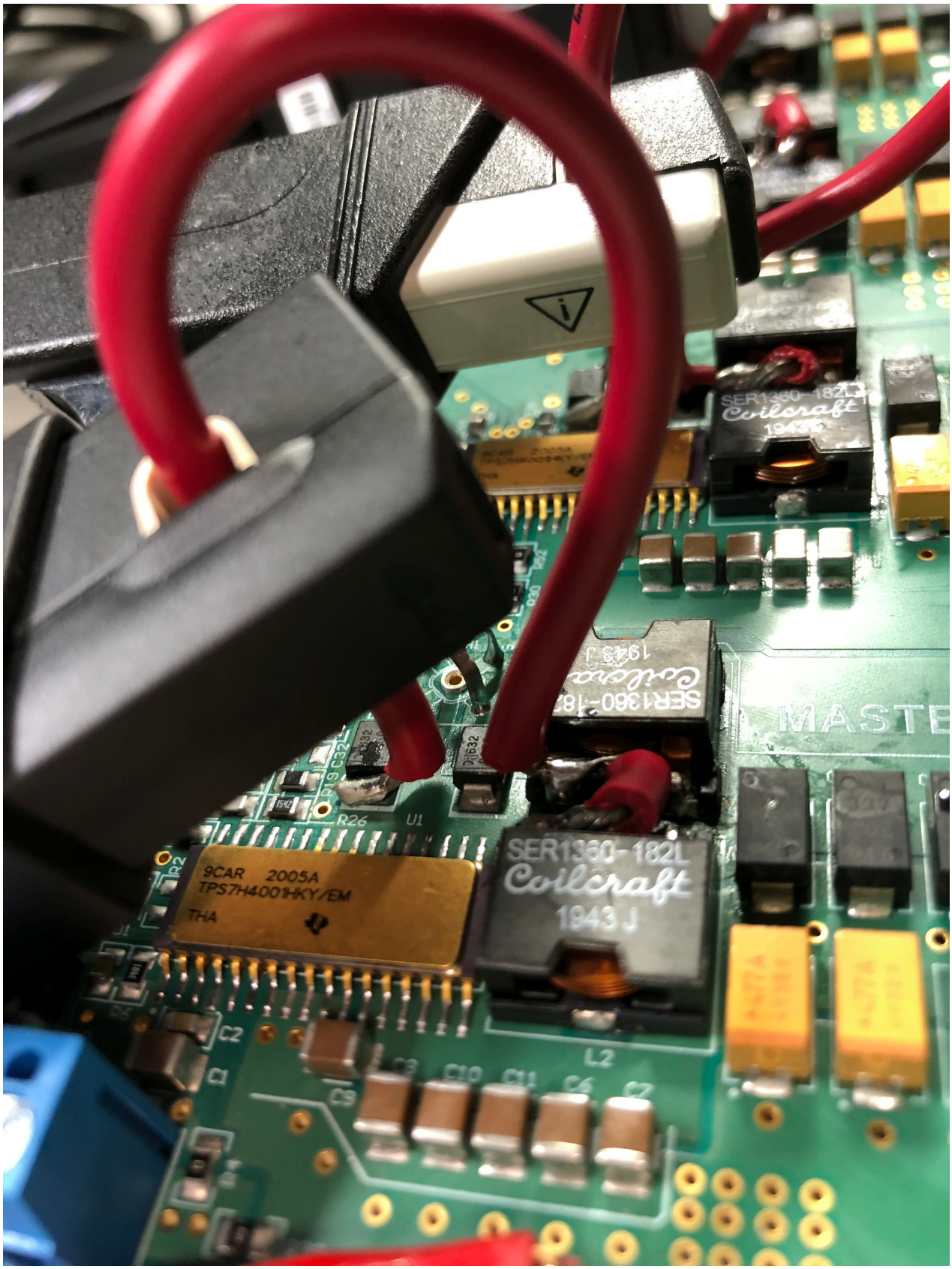

Figure 16. Current Sharing Measurement Setup

The RMS currents of each probe were captured and recorded on the oscilloscope as shown in Figure 17 and Figure 18. Figure 17 shows the individual converter currents when the total e-load current was set to 40A while Figure 18 shows the same for an e-load current of 65A.

Figure 17. Current Sharing 40Amps Total eLoad Current

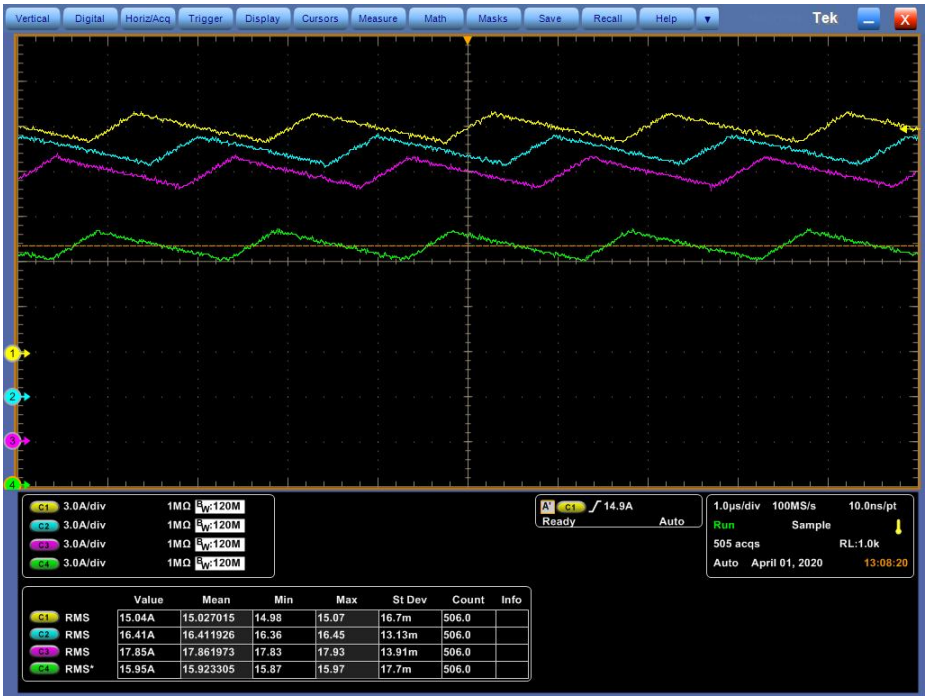

Figure 18. Current Sharing 65Amps Total eLoad Current

Table 3 shows a summary of the measurements for load currents from 15A to 80A. The second column of Table 3 shows the ideal current per converter if matching were perfect. The next four columns show the mean value of current measured for each converter while the last four columns show the deviation from the ideal value as a percentage. It is this data that is invaluable in understanding the true variation within a system. Taking the row in the table for 65A total e-load current as an example, converter SLAVE2 is operating at +9.92% above nominal, while the MASTER converter is operating at -7.53% below nominal current level. With this information, the system can operate at a toal current of 65A while still keeping each converter within the ROC specified, compared to the 39A the design would support assuming worst case for all converters.

Table 3. Current Sharing Data

		Measured Mean Current				Deviation from Ideal (%)			
Total eLoad Current (Amps)	**Perfect match Current per converter (Amps)**	**MASTER (Amps)**	**SLAVE1 (Amps)**	**SLAVE2 (Amps)**	**SLAVE3 (Amps)**	**MASTER**	**SLAVE1**	**SLAVE2**	**SLAVE3**
15	3.75	3.48	4.16	4.47	3.15	-7.17%	10.87%	19.12%	-16.07%
20	5.00	4.66	5.37	5.80	4.44	-6.83%	7.38%	15.93%	-11.17%
25	6.25	5.81	6.60	7.16	5.72	-7.08%	5.52%	14.50%	-8.55%
30	7.50	6.99	7.82	8.50	7.01	-6.81%	4.23%	13.33%	-6.55%
35	8.75	8.14	9.06	9.85	8.33	-7.01%	3.55%	12.62%	-4.76%
40	10.00	9.32	10.26	11.17	9.61	-6.78%	2.57%	11.74%	-3.89%
45	11.25	10.47	11.47	12.51	10.85	-6.91%	1.98%	11.24%	-3.55%
50	12.50	11.65	12.72	13.86	12.14	-6.82%	1.77%	10.91%	-2.84%
55	13.75	12.84	13.96	15.19	13.44	-6.47%	1.56%	10.48%	-2.23%
60	15.00	14.03	15.19	16.50	14.74	-6.47%	1.24%	10.03%	-1.75%
65	16.25	15.03	16.41	17.86	15.92	-7.53%	1.00%	9.92%	-2.01%
70	17.50	16.22	17.61	19.21	17.21	-7.32%	0.63%	9.77%	-1.66%
80	20.00	18.63	20.14	21.69	19.82	-6.83%	0.69%	8.46%	-0.92%

5 TPS7H4001QEVM-CVAL EVM Schematic

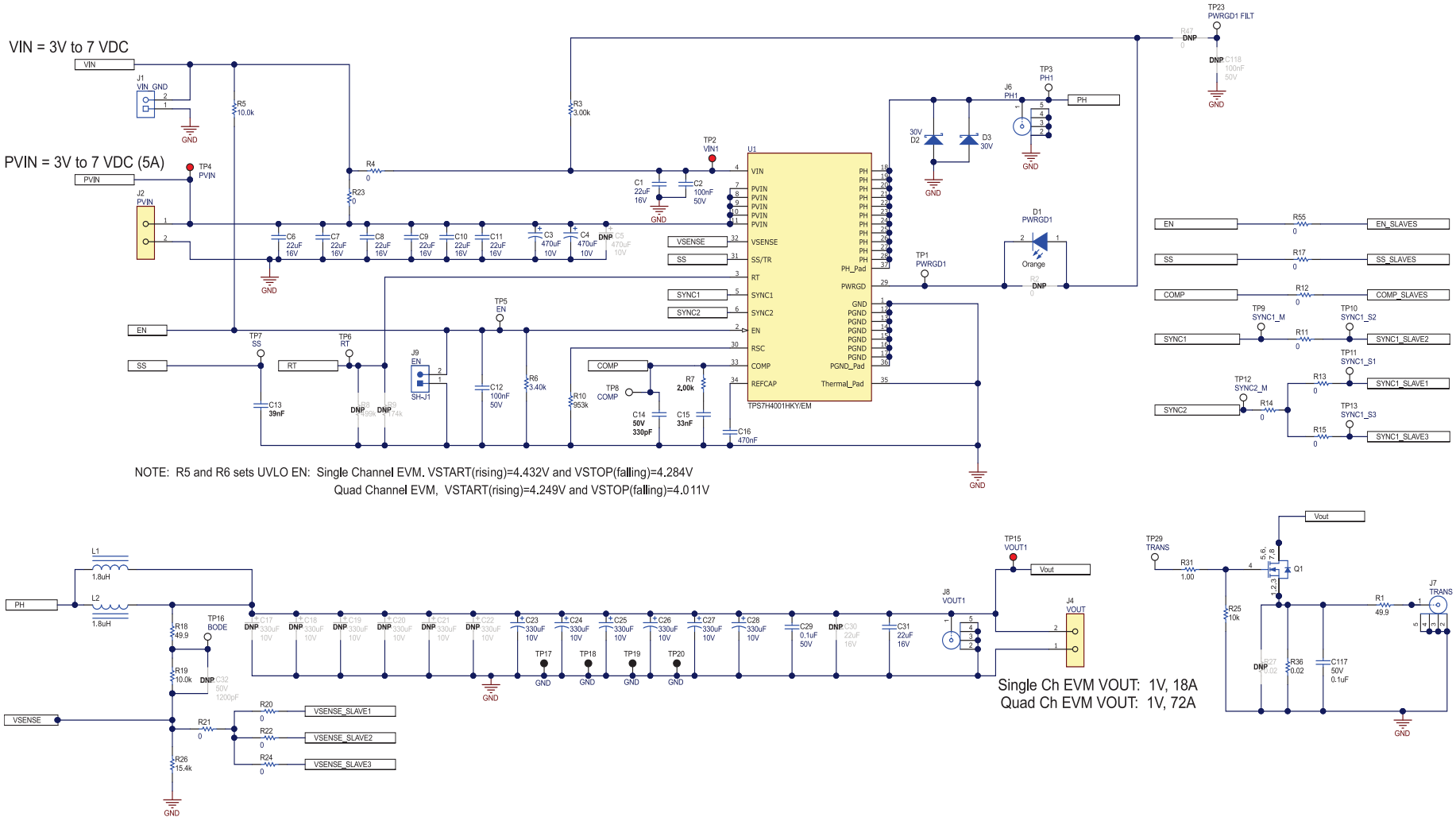

Figure 19. TPS7H4001QEVM-CVAL EVM Master Pol1 at U1 Schematic

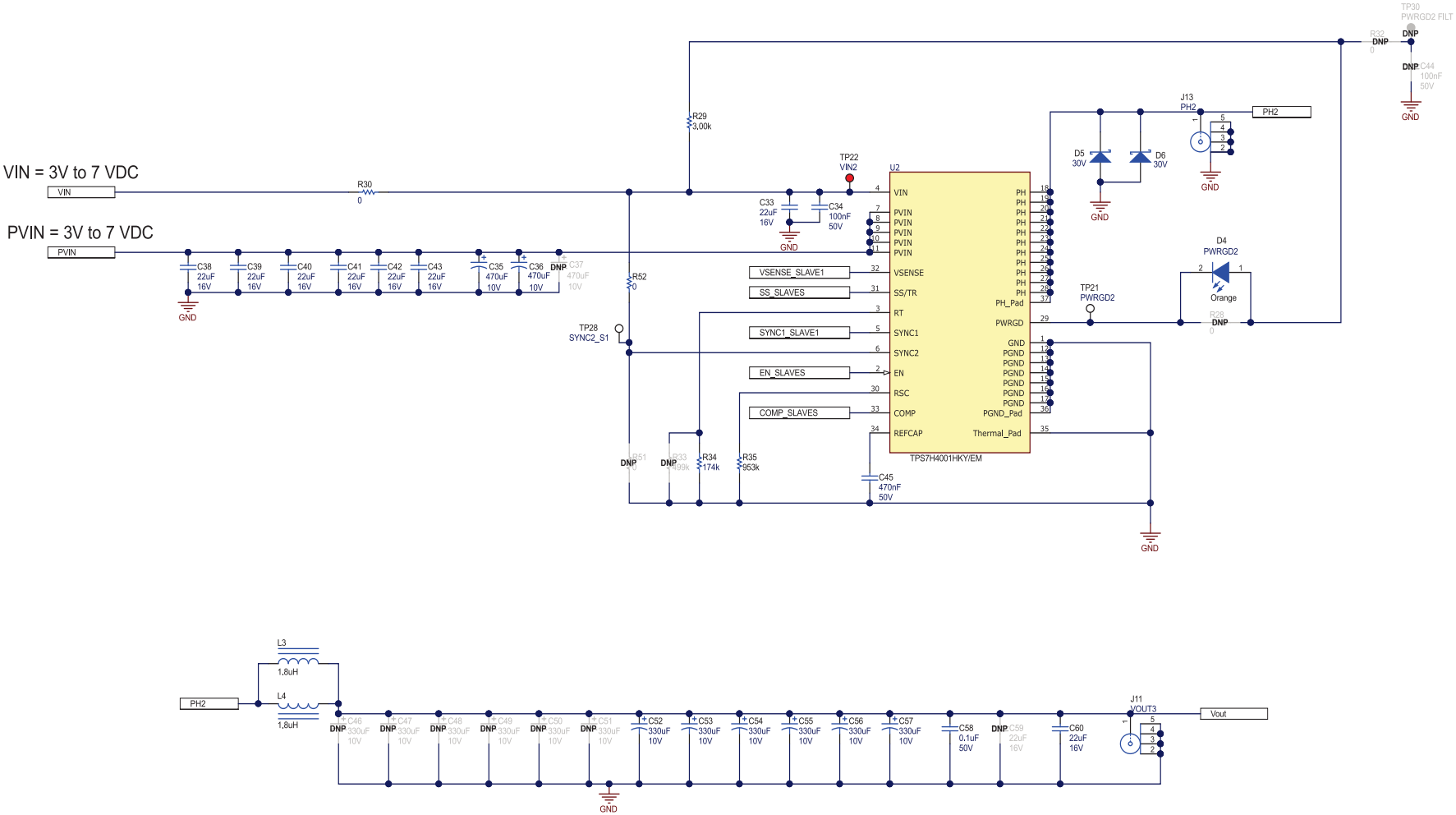

Figure 20. TPS7H4001QEVM-CVAL EVM Slave1 Pol2 at U2 Schematic

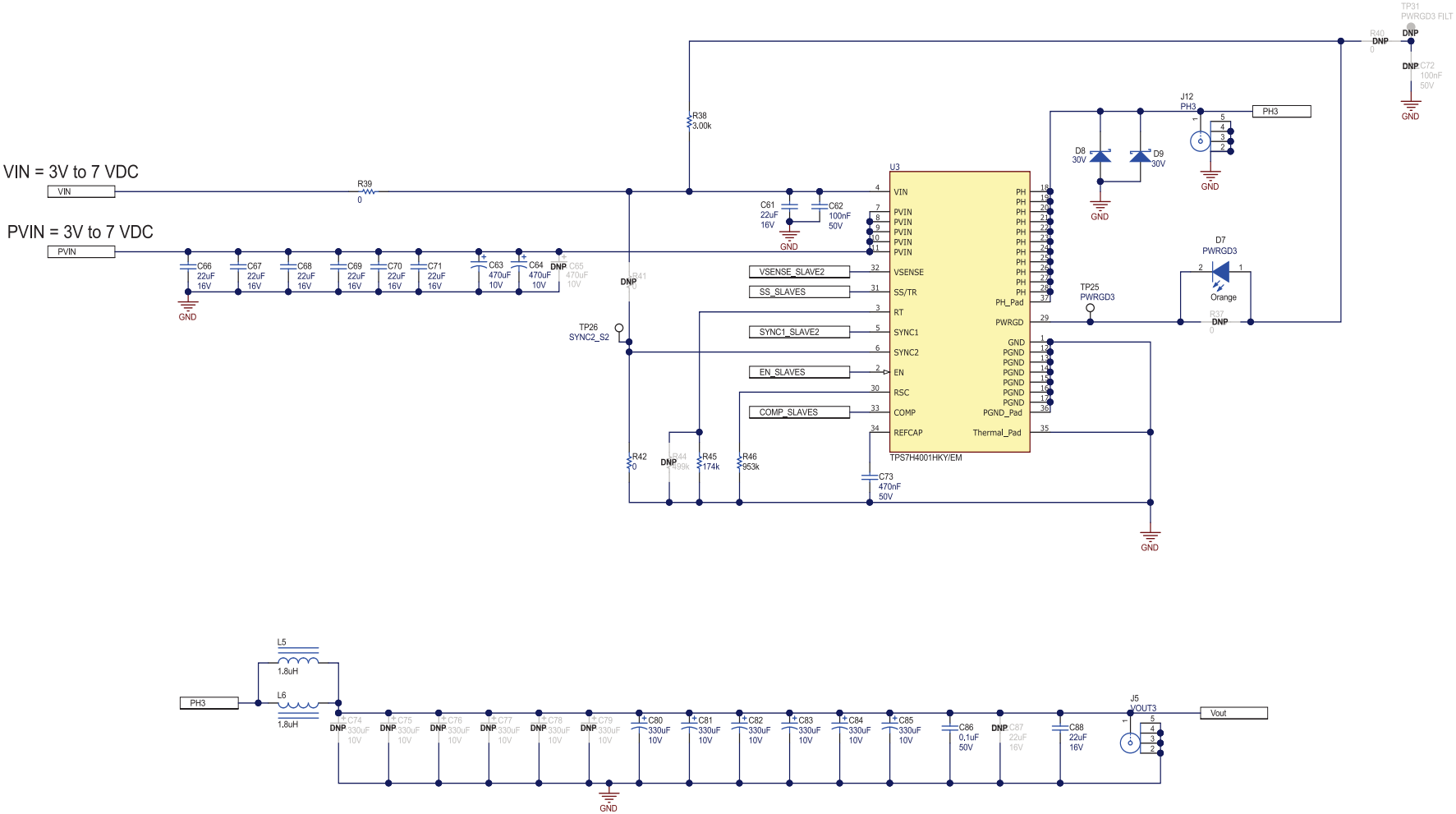

Figure 21. TPS7H4001QEVM-CVAL EVM Slave2 Pol3 at U3 Schematic

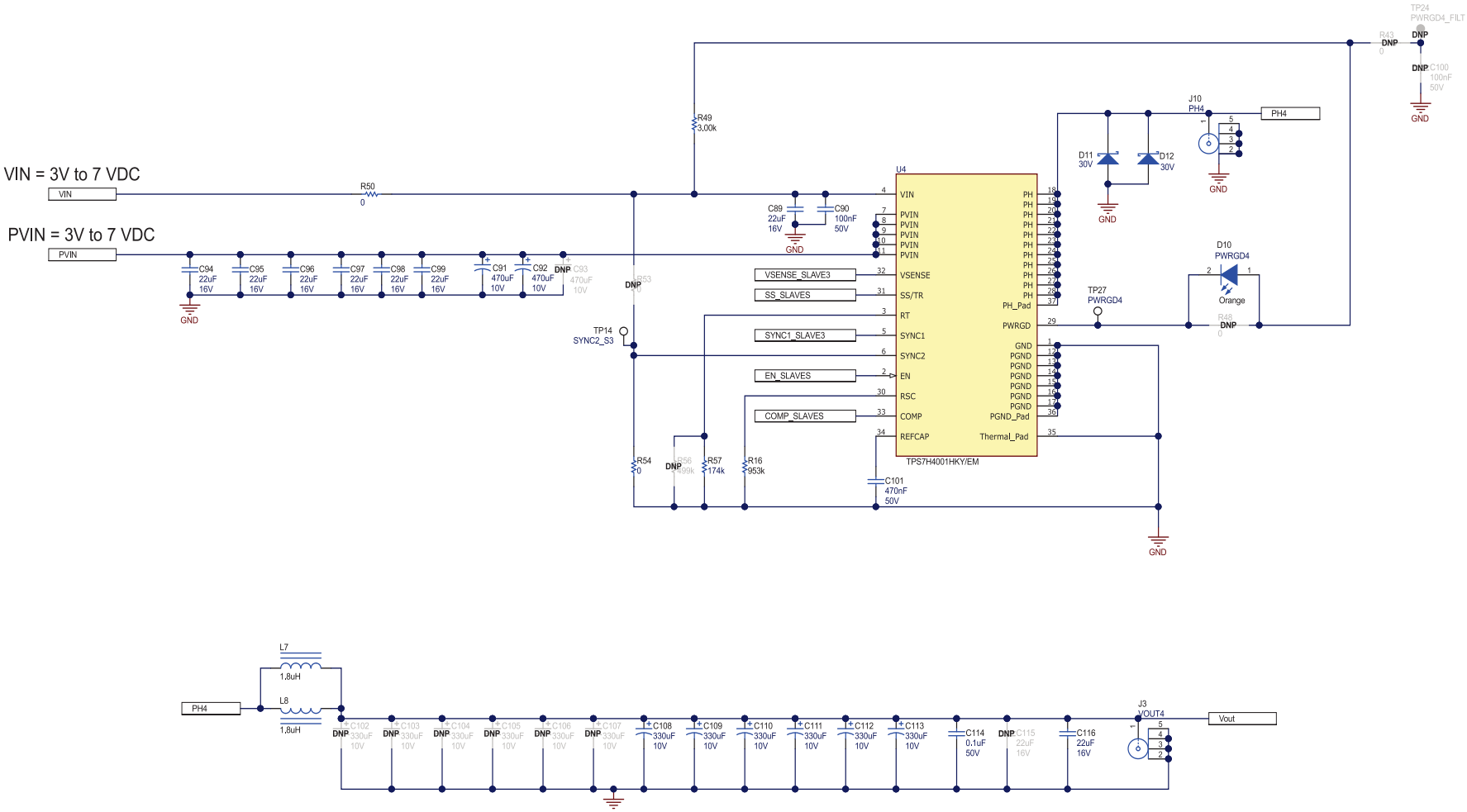

Figure 22. TPS7H4001QEVM-CVAL EVM Slave3 Pol4 at U4 Schematic

6 TPS7H4001QEVM-CVAL Bill of Materials (BOM)

Table 4. TPS7H4001QEVM-CVAL BOM

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		SLHR021	Any
C1, C6, C7, C8, C9, C10, C11, C31, C33, C38, C39, C40, C41, C42, C43, C60, C61, C66, C67, C68, C69, C70, C71, C88, C89, C94, C95, C96, C97, C98, C99, C116	32	22uF	CAP, CERM, 22 uF, 16 V, +/- 10%, X7R, 1210	1210	C3225X7R1C226K250AC	TDK
C2, C12, C34, C62, C90	5	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805	0805	08055C104JAT2A	AVX
C3, C4, C35, C36, C63, C64, C91, C92	8	470uF	CAP, TA, 470 uF, 10 V, +/- 10%, 0.023 ohm, SMD	7343-43	TPME477K010R0023	AVX
C13	1	0.039uF	CAP, CERM, 0.039 uF, 50 V, +/- 10%, X7R, 0805	0805	08055C393KAT2A	AVX
C14	1	330pF	CAP, CERM, 330 pF, 50 V, +/- 5%, C0G/NP0, 0805	0805	08055A331JAT2A	AVX
C15	1	0.033uF	CAP, CERM, 0.033 uF, 50 V, +/- 5%, X7R, 0805	0805	08055C333JAT2A	AVX
C16, C45, C73, C101	4	0.47uF	CAP, CERM, 0.47 uF, 50 V, +/- 10%, X7R, 0805	0805	C2012X7R1H474K125AB	TDK
C23, C24, C25, C26, C27, C28, C52, C53, C54, C55, C56, C57, C80, C81, C82, C83, C84, C85, C108, C109, C110, C111, C112, C113	24	330uF	CAP, Tantalum Polymer, 330 uF, 10 V, +/- 20%, 0.006 ohm, 7343-43 SMD	7343-43	T530X337M010ATE006	Kemet
C29, C58, C86, C114	4	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 1206	1206	C1206C104J5RACTU	Kemet
C117	1	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0805	0805	C0805C104K5RACTU	Kemet
D1, D4, D7, D10	4	Orange	LED, Orange, SMD	LED_0805	LTST-C170KFKT	Lite-On
D2, D3, D5, D6, D8, D9, D11, D12	8	30V	Diode, Schottky, 30 V, 2 A, SMB	SMB	B230-13-F	Diodes Inc.
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B & F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Terminal Block, 5.08 mm, 2x1, Brass, TH	2x1 5.08 mm Terminal Block	ED120/2DS	On-Shore Technology
J2, J4	2		Fixed Terminal Blocks MKDSP 10 HV/ 2-10	HDR2	1929517	Phoenix Contact
J3, J5, J6, J7, J8, J10, J11, J12, J13	9		Compact Probe Tip Circuit Board Test Points, TH, 25 per	TH Scope Probe	131-5031-00	Tektronix
J9	1		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik
L1, L2, L3, L4, L5, L6, L7, L8	8	1.8uH	Inductor, Shielded E Core, Ferrite, 1.8 µH, 13 A, 0.0026 ohm, AEC-Q200 Grade 3, SMD	SER1360	SER1360-182KLB	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1	1	25V	MOSFET, N-CH, 25 V, 113 A, DQH0008A (VSON-CLIP-8)	DQH0008A	CSD16408Q5	Texas Instruments

Table 4. TPS7H4001QEVM-CVAL BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R1, R18	2	49.9	RES, 49.9, 0.1%, 0.125 W, 0805	0805	RT0805BRD0749R9L	Yageo America
R3, R29, R38, R49	1	3.00k	RES, 3.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF3001V	Panasonic
R4, R11, R12, R13, R14, R15, R17, R20, R21, R22, R23, R24, R30, R39, R42, R50, R52, R54, R55	2	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08050000Z0EA	Vishay-Dale
R5, R19	2	10.0k	RES, 10.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080510K0FKEA	Vishay-Dale
R6	1	3.40k	RES, 3.40 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08053K40FKEA	Vishay-Dale
R7	1	2.00k	RES, 2.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF2001V	Panasonic
R10, R16, R35, R46	4	953k	RES, 953 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW0805953KFKEA	Vishay-Dale
R25	1	10k	RES, 10 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	'CRCW080510K0JNEA	Vishay-Dale
R26	1	15.4k	RES, 15.4 k, 0.1%, 0.125 W, 0805	0805	RG2012P-1542-B-T5	Susumo Co Ltd
R31	1	1.00	RES, 1.00, 1%, 0.125 W, 0805	0805	RC0805FR-071RL	Ygeo America
R34, R45, R57	3	174k	RES, 174 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF1743V	Panasonic
R36	1	0.02	RES, 0.02, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	LRMAM2512-R02FT4	TT Electronics/IRC
SH-J1	1	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP3, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP16, TP21, TP23, TP25, TP26, TP27, TP28, TP29	20		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP2, TP4, TP15, TP22	4		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP17, TP18, TP19, TP20	4		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U1, U2, U3, U4	4		Radiation Hardened 3-V to 7-V Input, 18-A Synchronous Buck Converter	CDFP34		Texas Instruments
C5, C37, C65, C93	0	470uF	CAP, TA, 470 uF, 10 V, +/- 10%, 0.023 ohm, SMD	7343-43	TPME477K010R0023	AVX
C17, C18, C19, C20, C21, C22, C46, C47, C48, C49, C50, C51, C74, C75, C76, C77, C78, C79, C102, C103, C104, C105, C106, C107	0	330uF	CAP, Tantalum Polymer, 330 uF, 10 V, +/- 20%, 0.006 ohm, 7343-43 SMD	7343-43	T530X337M010ATE006	Kemet
C30, C59, C87, C115	0	22uF	CAP, CERM, 22 uF, 16 V, +/- 10%, X7R, 1210	1210	C3225X7R1C226K250AC	TDK
C32	0	1200pF	CAP, CERM, 1200 pF, 50 V, +/- 10%, X7R, 0805	0805	08055C122KAT2A	AVX
C44, C72, C100, C118	0	0.1uF	CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805	0805	08055C104JAT2A	AVX
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R2, R28, R32, R37, R40, R41, R43, R47, R48, R51, R53	0	0	RES, 0, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW08050000Z0EA	Vishay-Dale

Table 4. TPS7H4001QEVM-CVAL BOM (continued)

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
R8, R33, R44, R56	0	499k	RES, 499 k, 0.1%, 0.125 W, 0805	0805	RG2012P-4993-B-T5	Susumu co Ltd
R9	0	174k	RES, 174 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	ERJ-6ENF1743V	Panasonic
R27	0	0.02	RES, 0.02, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	LRMAM2512-R02FT4	TT Electronics/IRC
TP24, TP30, TP31	0		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone

7 Board Layout

The following is the layer stack of the TPS7H4001QEVM-CVAL board.

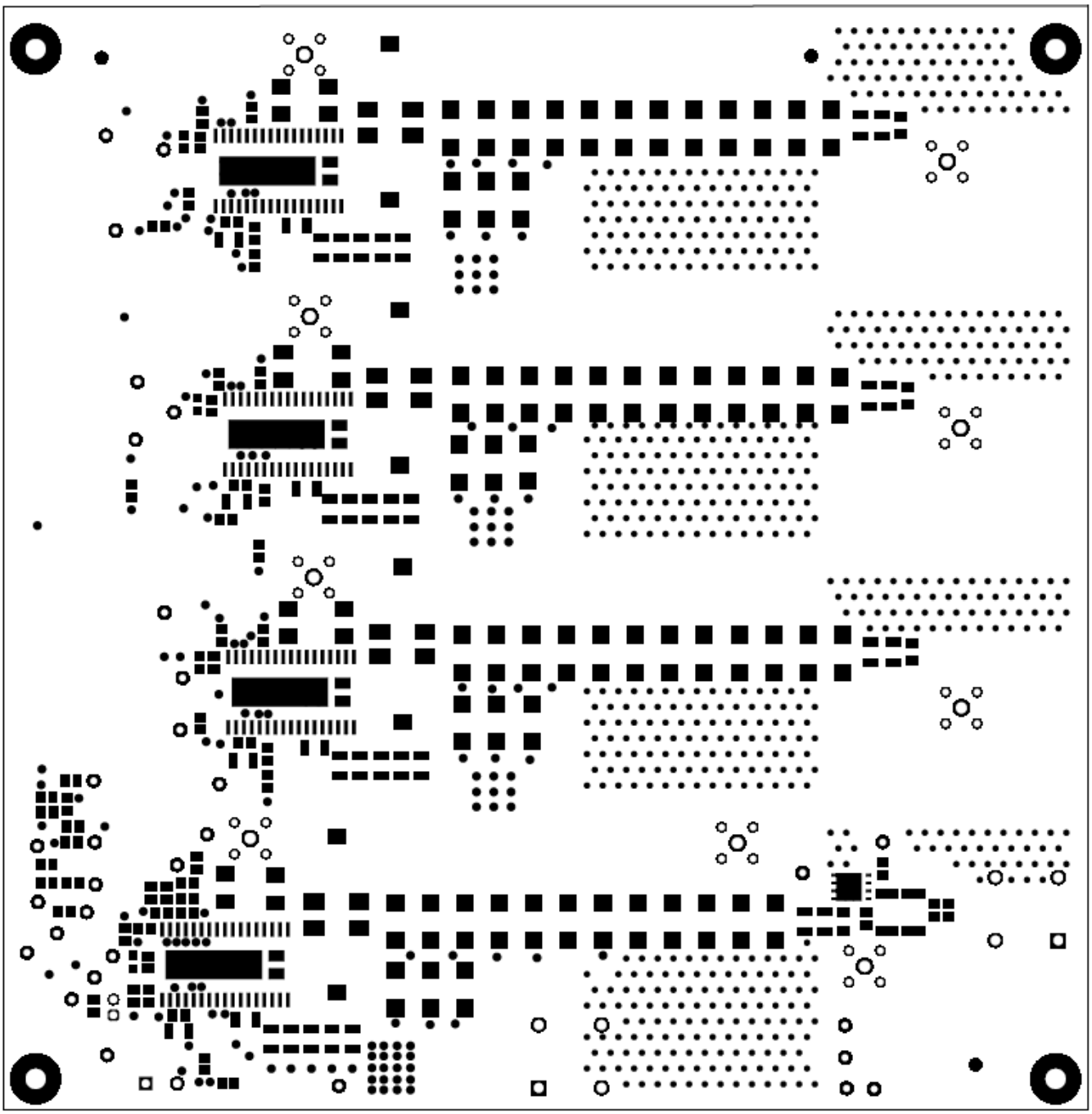

Figure 23. Top Overlay

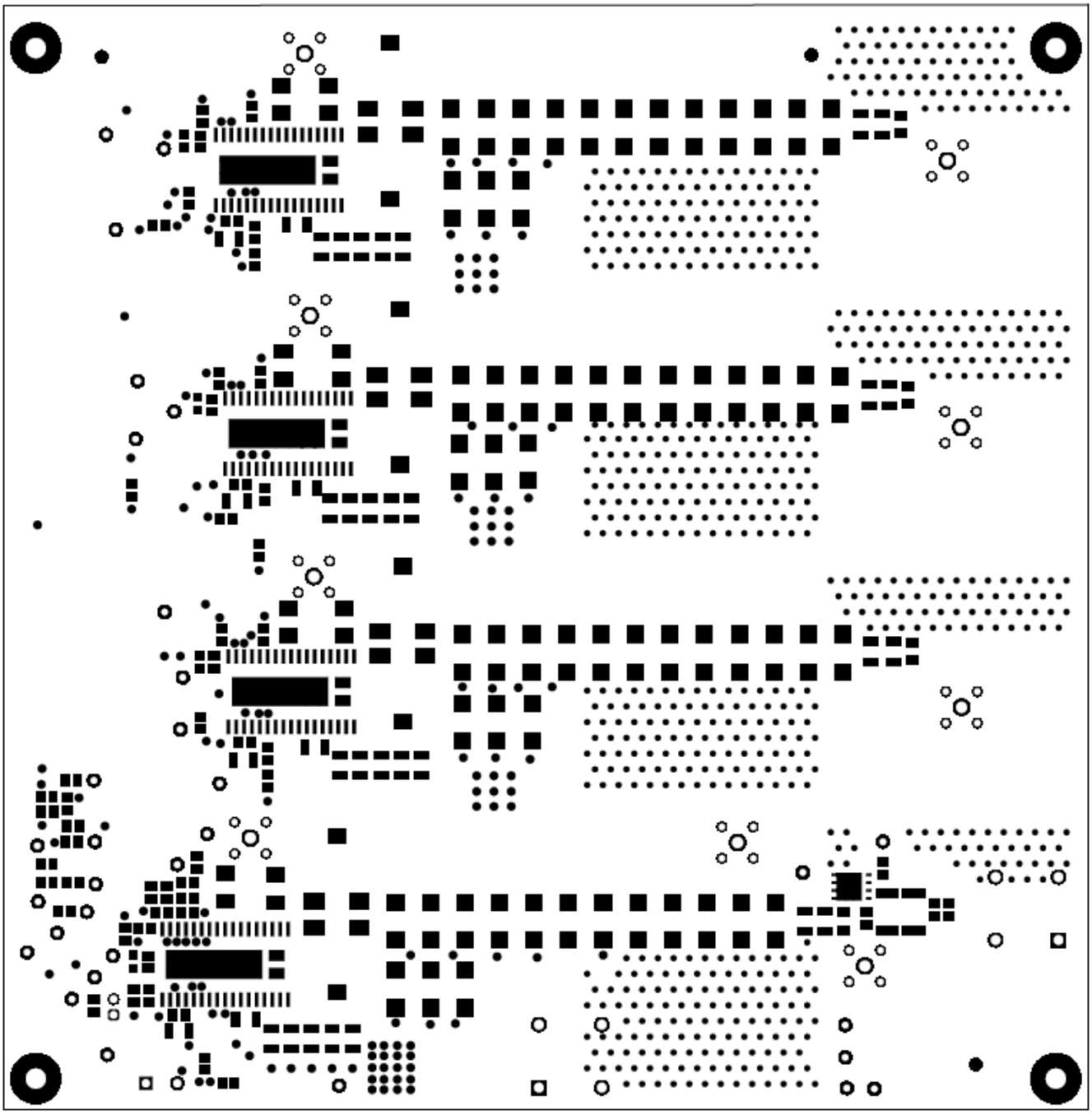

Figure 24. Top Solder

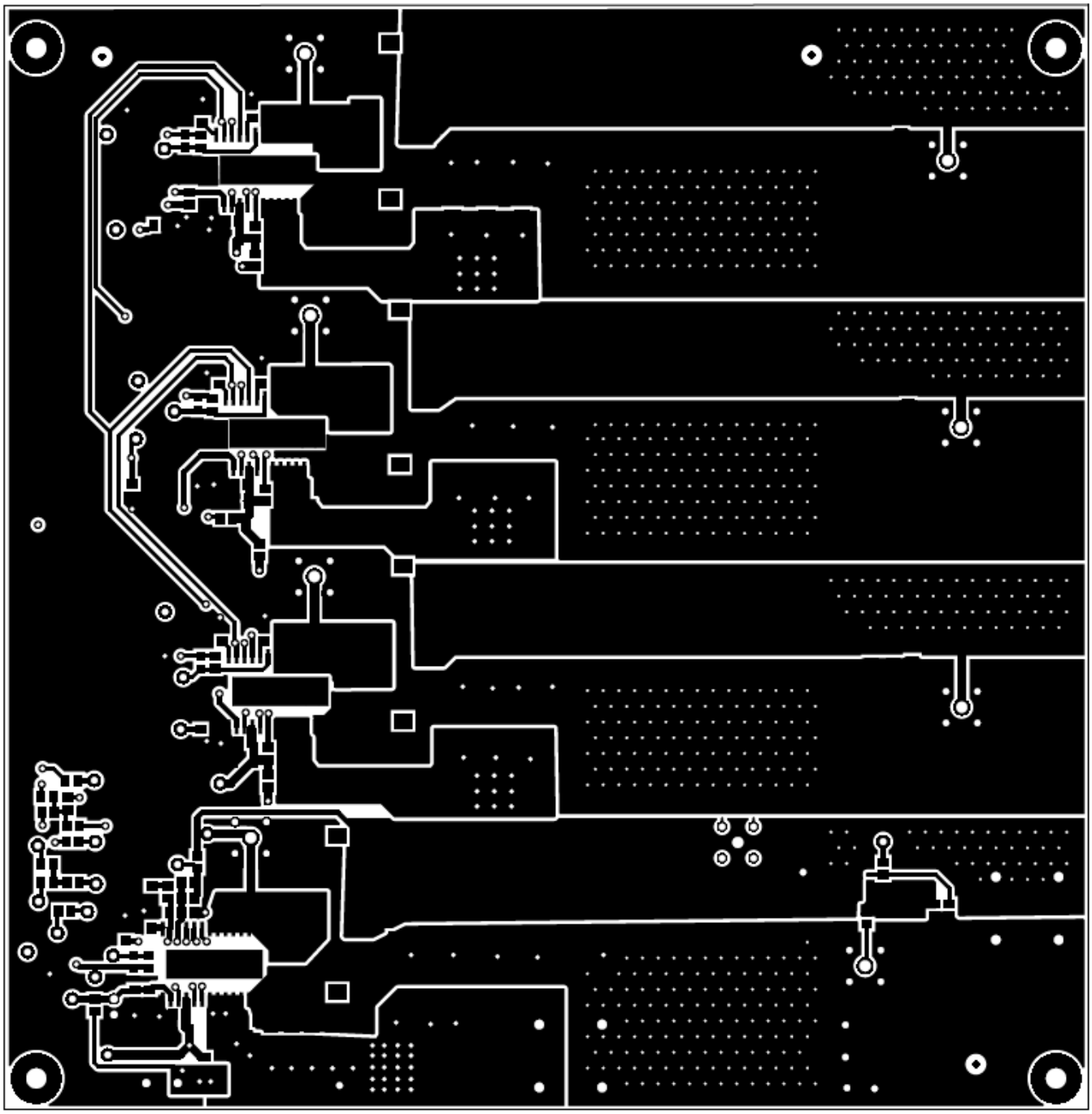

Figure 25. Top Layer

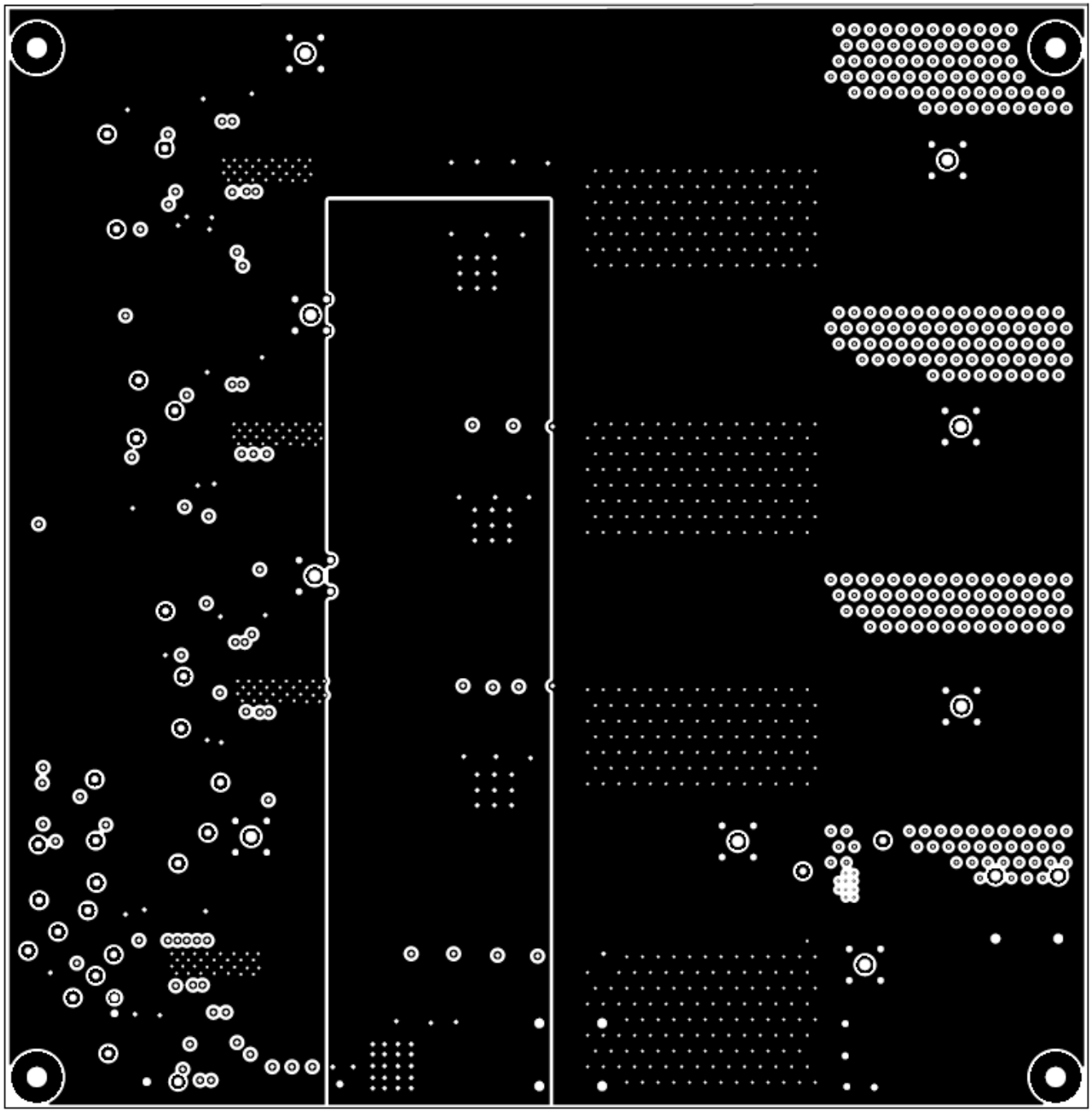

Figure 26. Signal Layer One

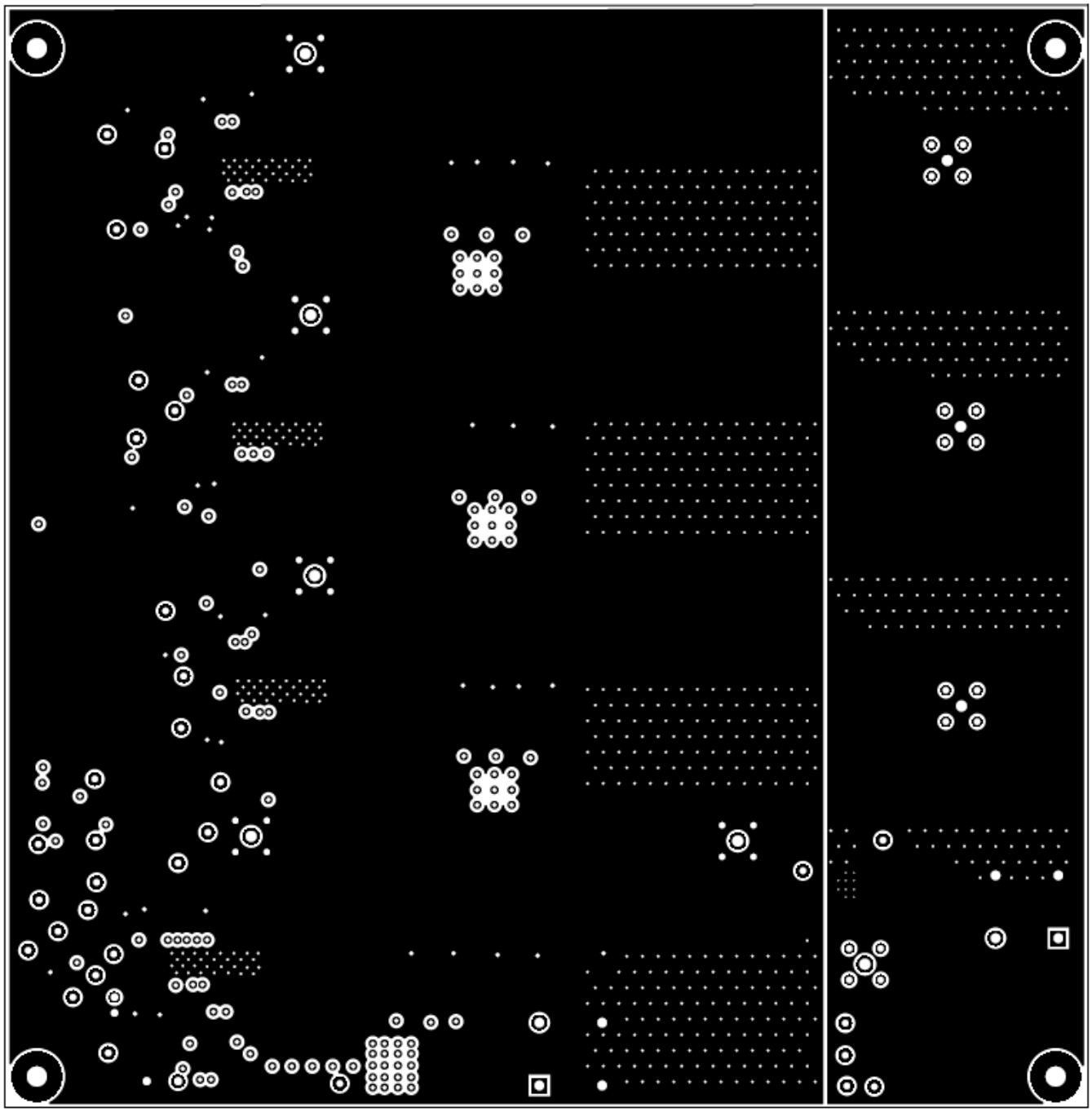

Figure 27. Signal Layer Two

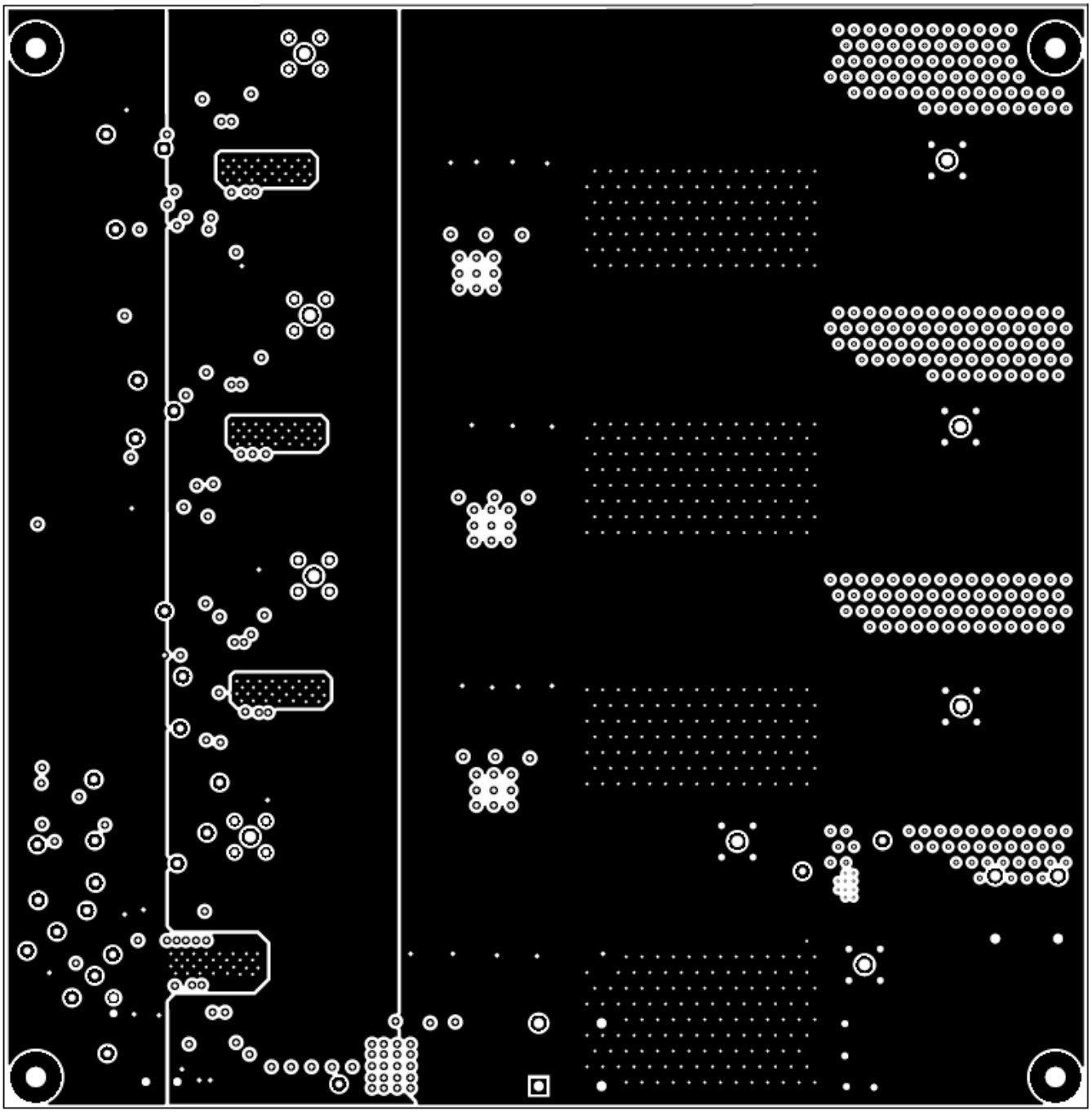

Figure 28. Signal Layer Three

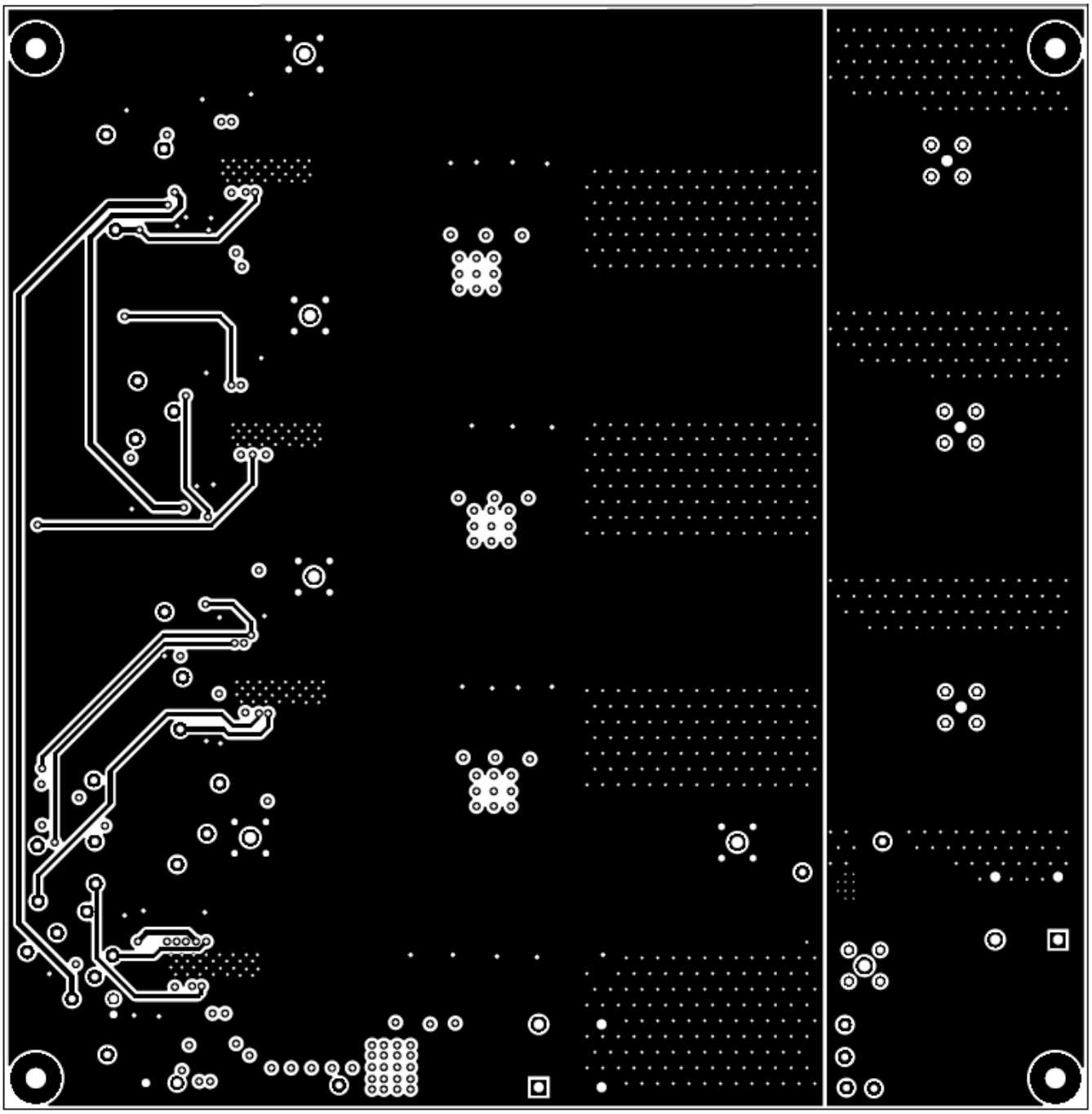

Figure 29. Signal Layer Four

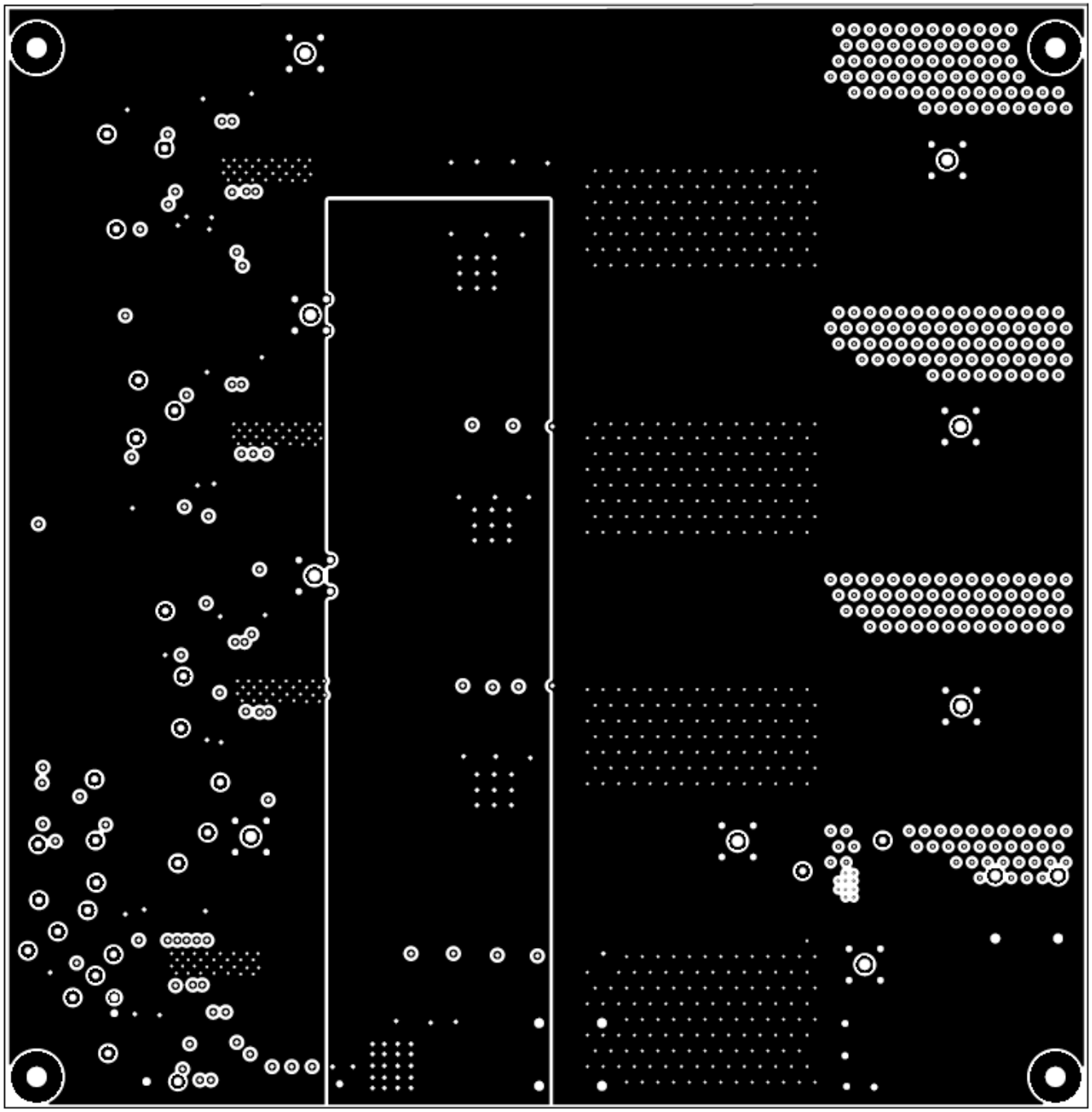

Figure 30. Signal Layer Five

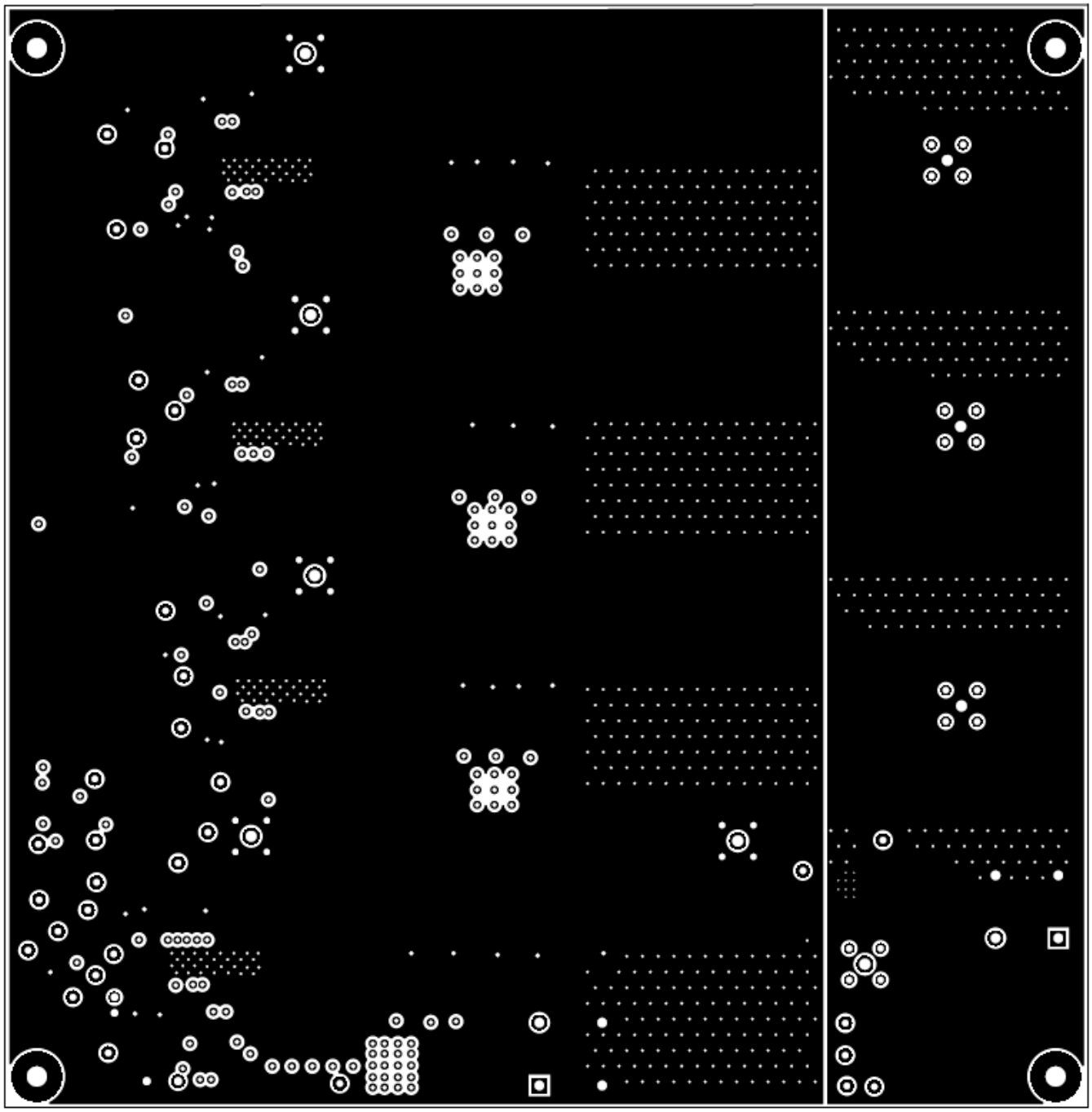

Figure 31. Signal Layer Six

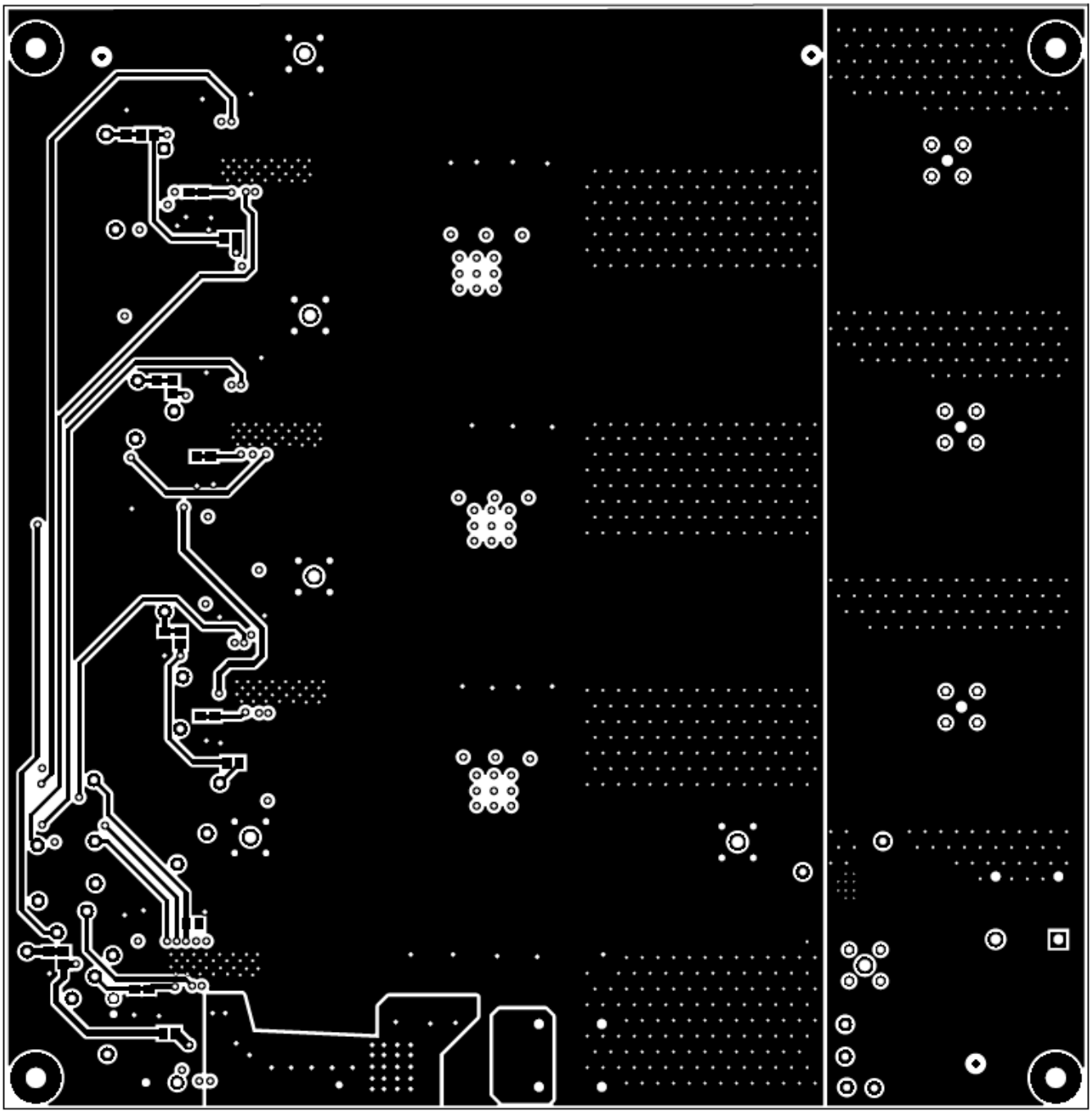

Figure 32. Bottom Layer

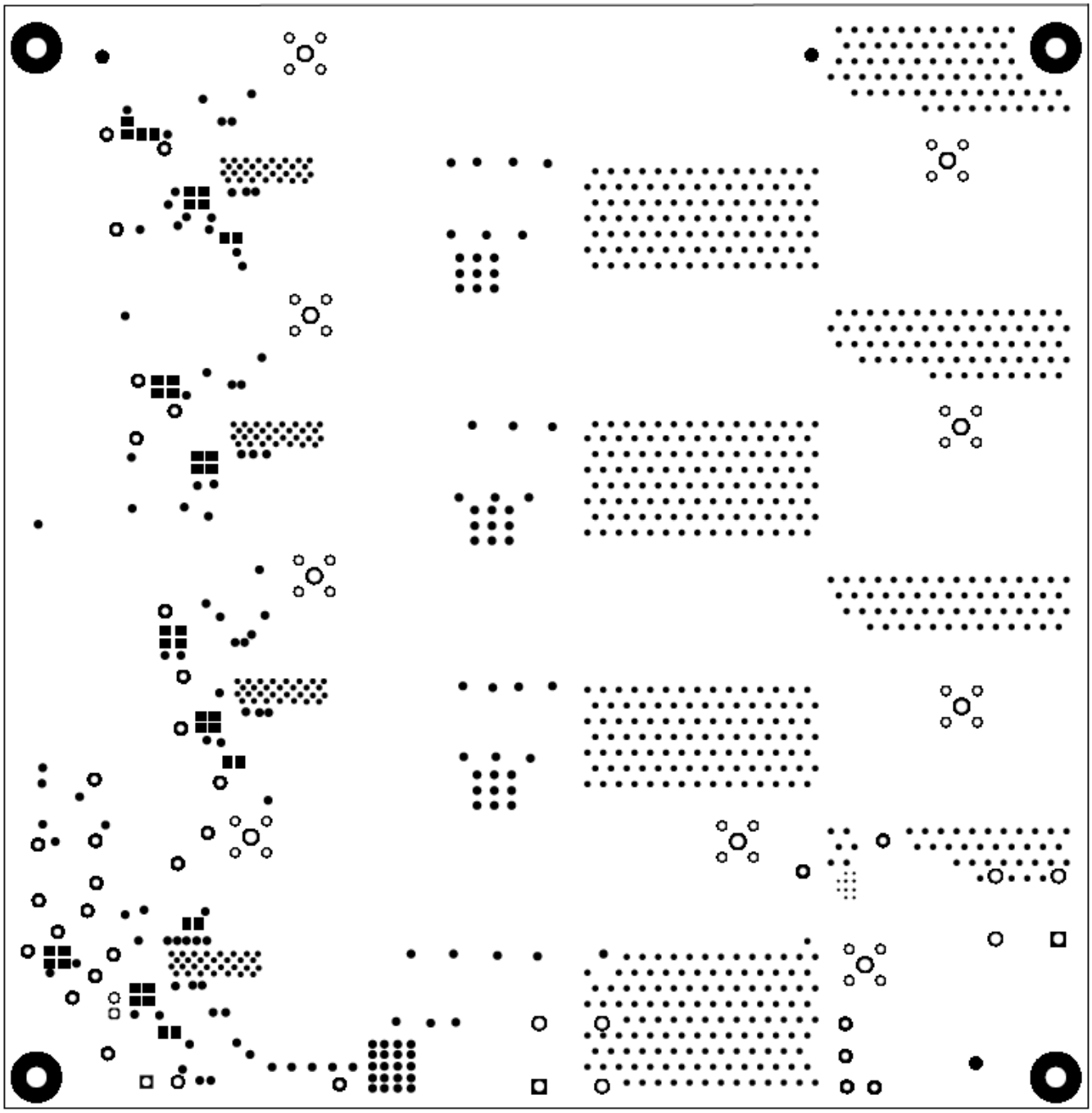

Figure 33. Bottom Solder

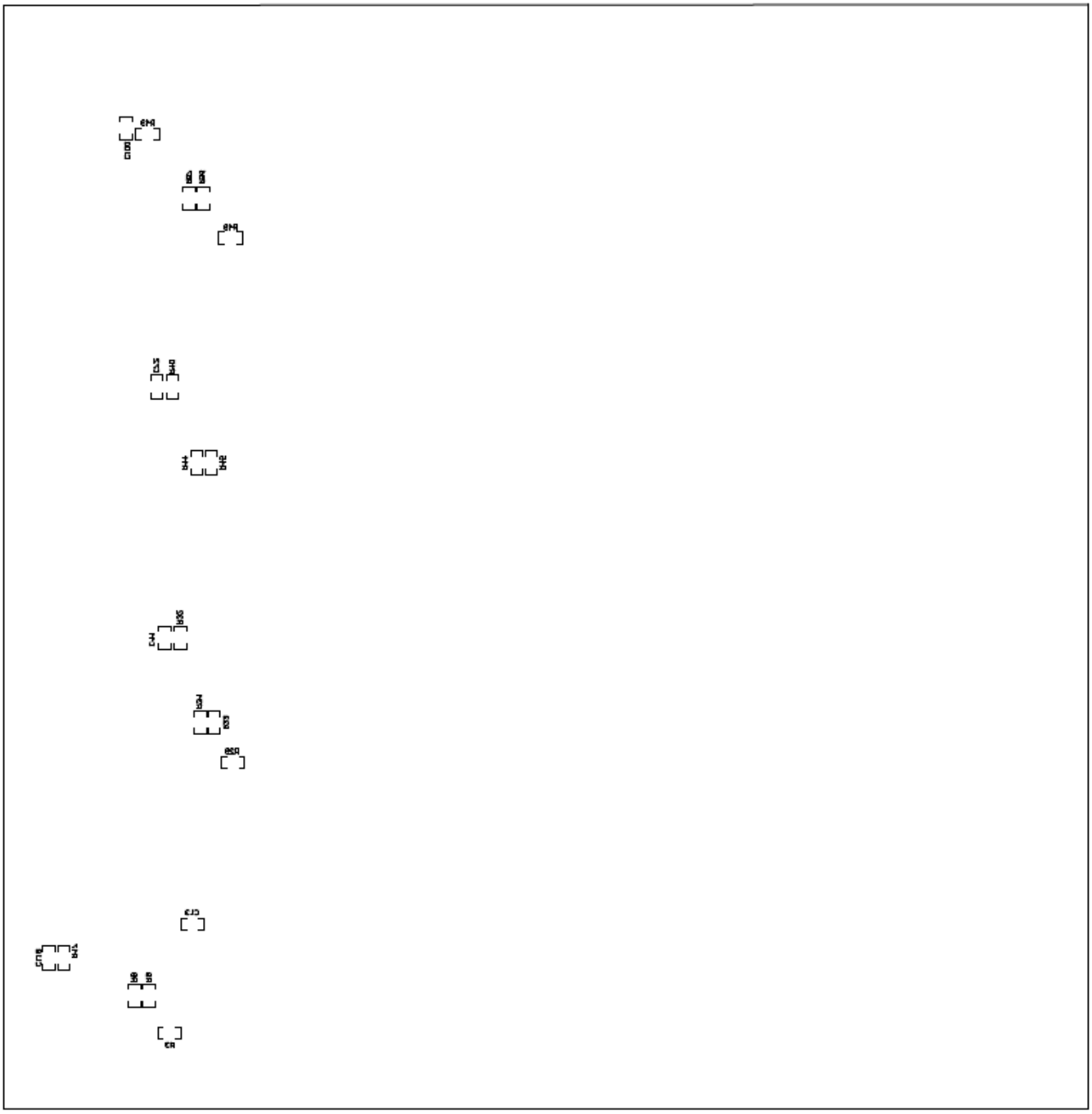

Figure 34. Bottom Overlay

8 Appendix A

The TPS7H4001EVM-CVAL hardware contains a sub-circuit which is useful when one wants to capture the transient response to a very high current step. For ‘low’ current transient steps, say less than 15 Amps, the response can be measured by simply switching the electronic load (e-load) between two currents states. However, the need exists to measure larger current step sizes when POLs are operating in parallel configurations. This poses a problem for this measurement technique as the inductance in the wire leads to the e-load causes undesirable spikes in the response. This problem is solved through the use of a transient sub-circuit that is provided on the EVM.

Figure 35 shows the schematic for this transient circuit. A power MOSEFT provided by Texas Instruments at Q1 is used to momentarily press the regulated VOUT voltage across power resistors R36 by modulating the gate of Q1 at TP29 with low duty cycle square wave.

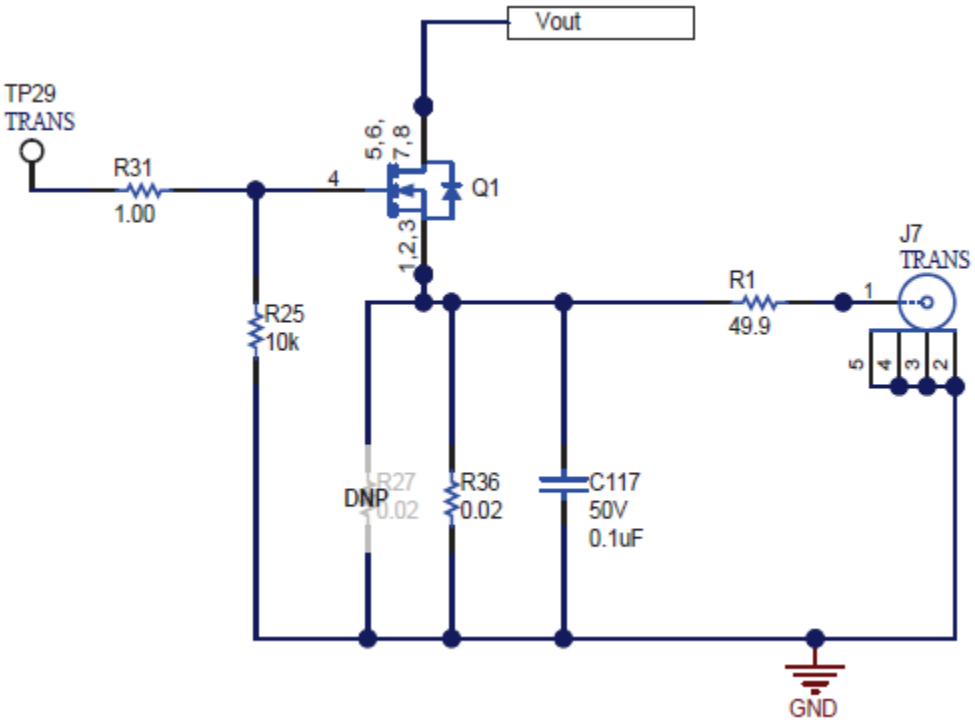

Figure 35. Transient Sub-circuit on the TPS7H4001QEVM-CVAL

Figure 36 shows an overview of the setup for measuring the transient resposne to a high current step.

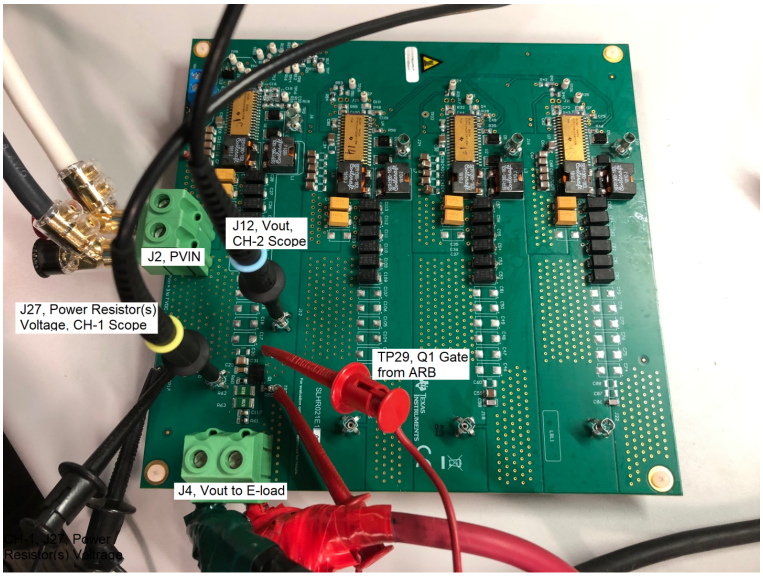

Figure 36. Setup for Measuring Transient Response to High Current Load Step

The transient current step size is determined as follows:

$$I_{Transient} = \frac{V_{OUT}}{(RDS(on)\_Q1 + R36)} \quad (1)$$

With VOUT= 1.0V, Rdson_Q1 = 3.6 mohms (per data sheet), R36 = 20 mohms, R27=DNI, the calculated current step response is ~42.4 A. Eliminating the uncertainty of Rdson in the calculation is possible by capturing the actual voltage at probe testpoint J7 and dividing by the power resistance.

$$I_{Transient} = \frac{VJ27}{R36} \quad (2)$$

The key to a successful measurement (i.e. one without a smoking resistor), is to determine the duty cycle to apply to the gate of Q1 to allow the right amount of current through so as to not exceed the power rating of resistor R36

$$Power = \left(\frac{1\ V}{0.020\ \Omega}\right) \times 1\ V = 50\ A \times 1\ V = 50\ W \quad (3)$$

Resistor R36 has a power rating of 1Watt.

$$\frac{1\ W}{50\ W} = 0.02 \text{ or } 2\% \quad (4)$$

To limit the power dissipated in R36 to 1 Watt, the maximum duty cycle of the gate voltage signal at Q1 should be 2%. For margin, a 1% duty cycle signal was used in the forthcoming measurements as shown on the arbitrary waveform generator setup in Figure 37.

Figure 37. Arbitrary Waveform Generator Setup for Modulating Gate of Power FET

The square wave signal was connected to test point TP29, the gate of Q1, but not activated initially. Scope probe CH-1 was placed at J7 (voltage across power resistor(s)) with rising edge trigger set, and scope probe CH-2 at J12, Vout voltage. An electronic load set to 27Amps was connected to J4 connector to set the initial current level. With the EVM powered and supplying 27Amps to e-load, the ARB signal was applied to the power MOSFET. The scope capture below shows the Vout response to the positive current step. Since the voltage across the power resistor settles at ~800mV, the current step size is estimated to be ~ 0.8V/0.02ohms = 40Amps. It is estimated that the current step is from 27Amps to 67Amps.

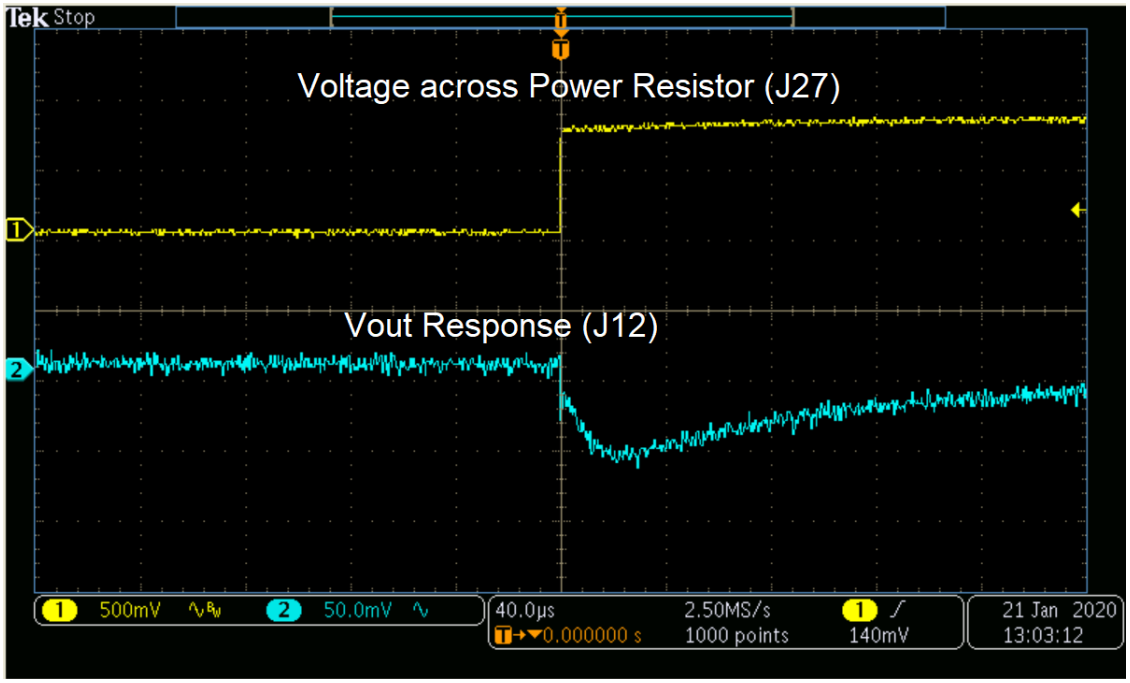

Figure 38. Vout Transient Response to Current Step from 27A to 67A

The same is repeated for a negative current step by setting the trigger to falling edge on CH-1.

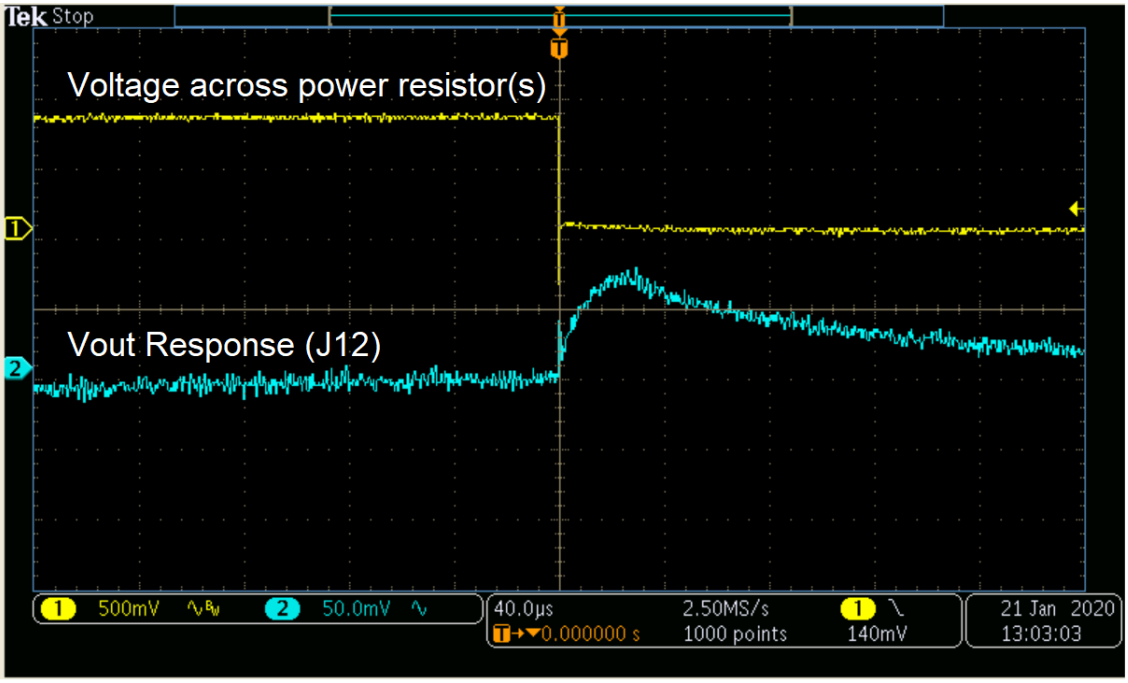

Figure 39. Vout Transient Response to Current Step from 67A to 27A

By changing the value of the power resistor(s) and the initial current set by the e-load, any desired current step size is achievable.

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