



## ABSTRACT

The TPSM63603EVM features the TPSM63603 synchronous-buck power module configured for operation with typical 3-V to 36-V input bus applications (the TPSM63603SEVM features the TPSM63603S; spread spectrum variant). The output voltage and switching frequency can be set to one of five popular values by using a configuration jumper. The EVM supplies the full output current rating of the device. Input and output capacitors are included to accommodate the entire range of input voltage and the selectable output voltages on the EVM. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points and jumpers are provided for use of the enable (EN), synchronization (SYNC), and power-good (PGOOD) features of the device. The recommended PCB layout of the EVM maximizes thermal performance and minimizes output ripple and noise. All feature test points, schematic and layout are the same for both EVMs, TPSM63603EVM and TPSM63603SEVM, the only difference being the U1 IC (see the device data sheet for information).

## Table of Contents

<b>1 EVM Setup</b> .....	<b>2</b>
<b>2 EVM Connectors and Test Points</b> .....	<b>3</b>
<b>3 Test Results</b> .....	<b>4</b>
<b>4 PCB Layouts</b> .....	<b>5</b>
<b>5 Schematics</b> .....	<b>8</b>
<b>6 Bill of Materials</b> .....	<b>9</b>
<b>7 Revision History</b> .....	<b>9</b>

## List of Figures

Figure 1-1. EVM User Interface.....	2
Figure 3-1. ENABLE Start-Up Waveform.....	4
Figure 3-2. ENABLE Shutdown Waveform.....	4
Figure 3-3. Output Voltage Ripple.....	4
Figure 3-4. Transient Performance.....	4
Figure 4-1. Top Silk Screen (Top View).....	5
Figure 4-2. Top Copper Layer (Top View).....	5
Figure 4-3. Signal Layer 1 (Top View).....	6
Figure 4-4. Signal Layer 2 (Top View).....	6
Figure 4-5. Bottom Layer (Top View).....	7
Figure 4-6. Bottom Layer Silk Screen (Bottom View).....	7
Figure 5-1. TPSM63603EVM Schematic.....	8

## List of Tables

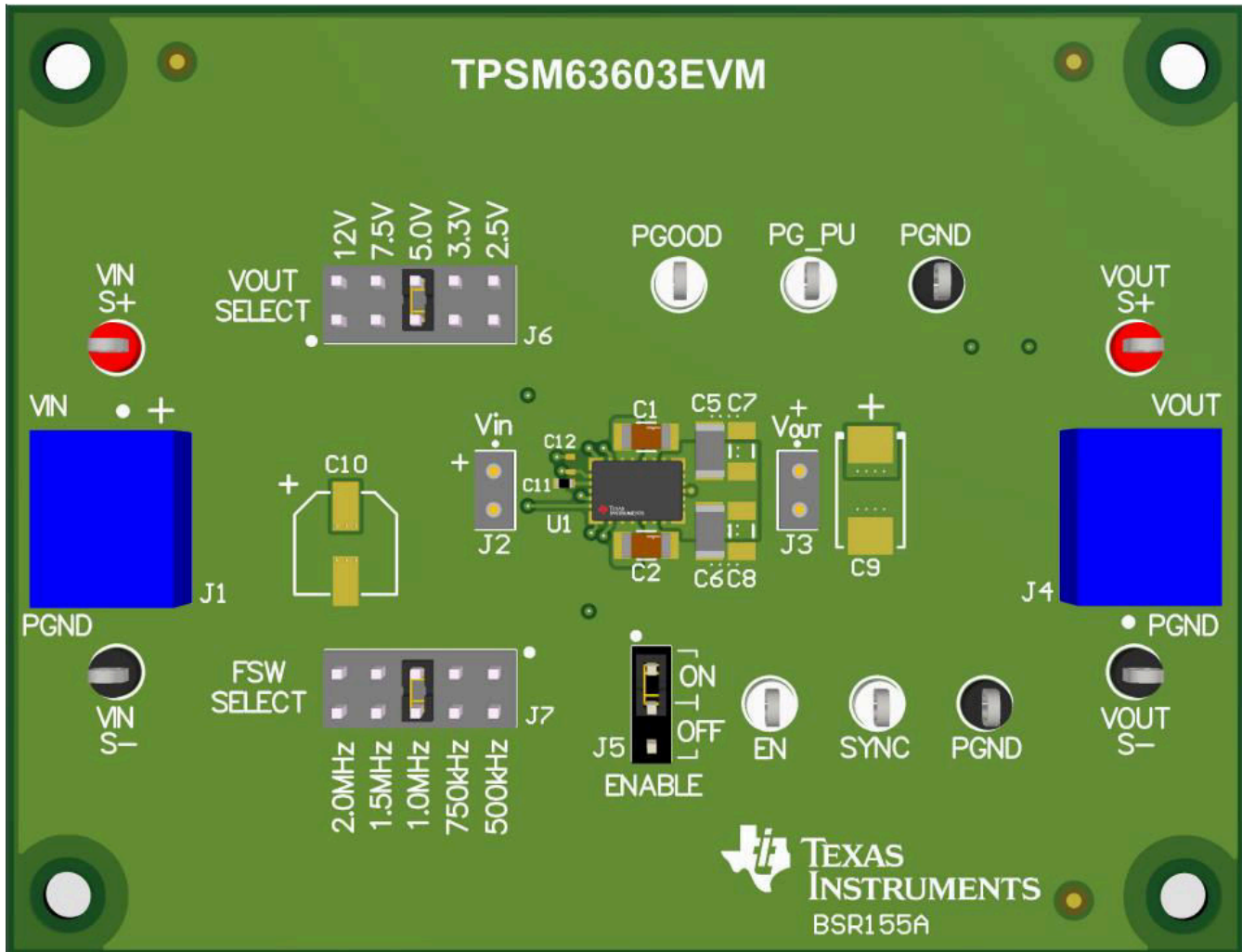
Table 2-1. Test Point Descriptions.....	3
Table 6-1. TPSM63603EVM BOM.....	9

## Trademarks

All trademarks are the property of their respective owners.

## 1 EVM Setup

Figure 1-1 highlights the user interface items associated with the EVM. The *VIN* Power terminal block (J1) is used for connection to the host input supply and the *VOUT* Power terminal block (J4) is used for connection to the load. These terminal blocks accept up to 16-AWG wire.



**Figure 1-1. EVM User Interface**

- Use the VIN S+ and VIN S- test points along with the VOUT S+ and VOUT S- test points located near the power terminal blocks as voltage monitoring points where voltmeters can be connected to measure VIN and VOUT. **Do not use these S+ and S- monitoring test points as the input supply or output load connection points.** The PCB traces connecting to these test points are not designed to support high currents.
- Use the VIN scope (J2) and VOUT scope (J3) test points to monitor VIN and VOUT waveforms with an oscilloscope. These test points are intended to use un-hooded scope probes outfitted with a low inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1-in centers. Connect the scope probe tip to the top socket labeled "+" and connect the scope ground lead to the bottom socket.
- The control test points located near the top and bottom of the EVM test the features of the device. Refer to the [EVM Connectors and Test Points](#) section for more information on the individual control test points.
- The VOUT SELECT jumper (J6) is provided to select the desired output voltage: 2.5 V, 3.3 V, 5.0 V, 7.5 V, or 12 V. Before applying power to the EVM, make sure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.
- The FSW SELECT jumper (J7) is provided to select the desired switching frequency: 500 kHz, 750 kHz, 1.0 MHz, 1.5 MHz, or 2.0 MHz. Before applying power to the EVM, make sure that the jumper is present and

properly positioned for the intended switching frequency. Always remove input power before changing the jumper settings.

- The device can be turned on or off using the enable jumper (J5). Place the jumper in the ON position to enable the device. Place the jumper in the OFF position to disable the device. The undervoltage lockout (UVLO) can be set by populating resistors R1 and R2 located on the bottom side of the EVM. Refer to the data sheet for recommended UVLO resistor values. The SYNC test point is provided for a convenient location to connect a clock signal. The power good (PGOOD) test point is available to monitor when a valid output voltage is present on the EVM. Additionally, the PG\_PU pin is present as a convenient point to connect a pullup voltage for the PGOOD signal.

## 2 EVM Connectors and Test Points

Wire-loop test points and scope probe sockets are included for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. [Table 2-1](#) describes each test point.

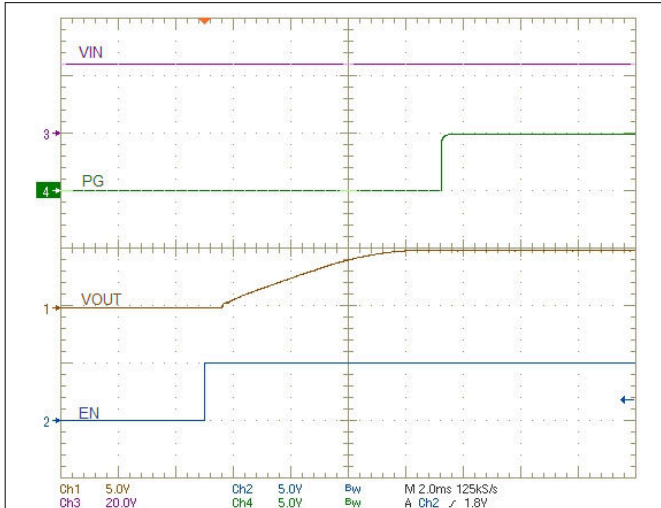
**Table 2-1. Test Point Descriptions**

Test Point <sup>(1)</sup>	Description
VIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
VIN S-	Input ground monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
VOUT S+	Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
VOUT S-	Output ground monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation, and load regulation.
PGND	Power ground test points.
VIN Scope (J2)	Input voltage scope monitor. Connect an oscilloscope probe to this set of points to measure input ripple voltage.
VOUT Scope (J3)	Output voltage scope monitor. Connect an oscilloscope probe to this set of points to measure output voltage ripple and transient response.
EN	Enable test point. Monitors the enable signal of the device. Use the ENABLE Control header (J5) to disable the device. If a logic signal is used to control the EN feature, remove the jumper from the J5 header.
ENABLE Control (J5)	Enable select jumper. Enable or disable the device using a jumper. When in the ON position, the EN pin is pulled up to VIN directly. If the SYNC feature is to be used, remove the jumper from the J5 header.
SYNC	Synchronization test point. Connect a valid clock signal to this test point to synchronize the switching frequency. Remove the ENABLE jumper (J5) when applying a synchronization clock signal.
PGOOD	Power good test point. Monitors the power good signal of the device. This is an open-drain signal. A 49.9-kΩ resistor is connected to this pin and the PG_PU pin on the EVM.
PG_PU	PGOOD pullup test point. Apply a voltage to this pin to use as a pullup voltage for the PGOOD signal. A 49.9-kΩ resistor is connected to this pin and the PGOOD pin on the EVM.

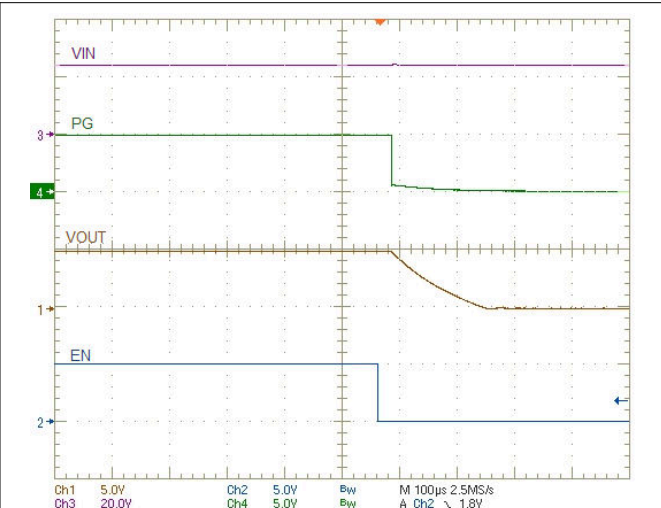
(1) Refer to the product data sheet for absolute maximum ratings associated with the features in this table.

### 3 Test Results

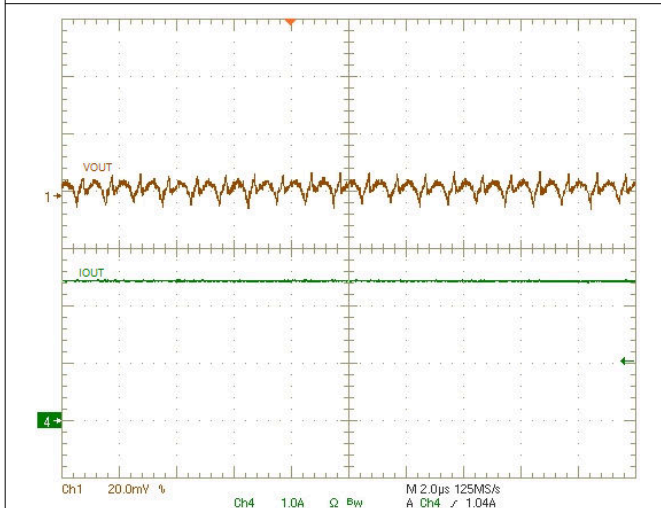
Figure 3-1 through Figure 3-4 demonstrate the performance of the TPSM63603EVM operating at 24-V input and 5-V output.



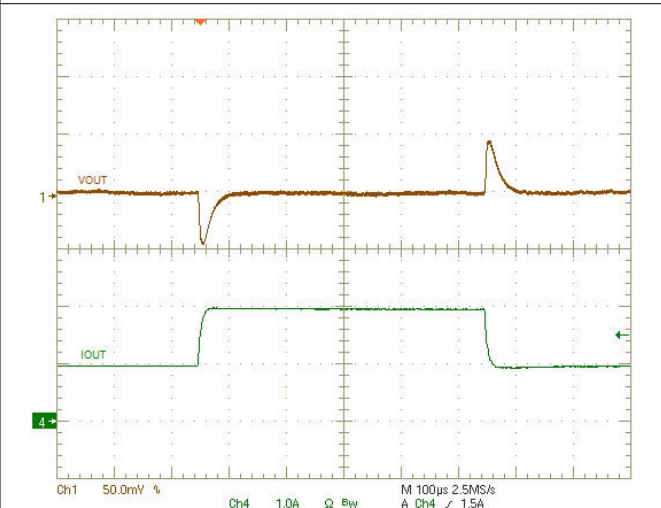
**Figure 3-1. ENABLE Start-Up Waveform**



**Figure 3-2. ENABLE Shutdown Waveform**



**Figure 3-3. Output Voltage Ripple**



**Figure 3-4. Transient Performance**

## 4 PCB Layouts

Figure 4-1 through Figure 4-6 show the EVM PCB layout images.

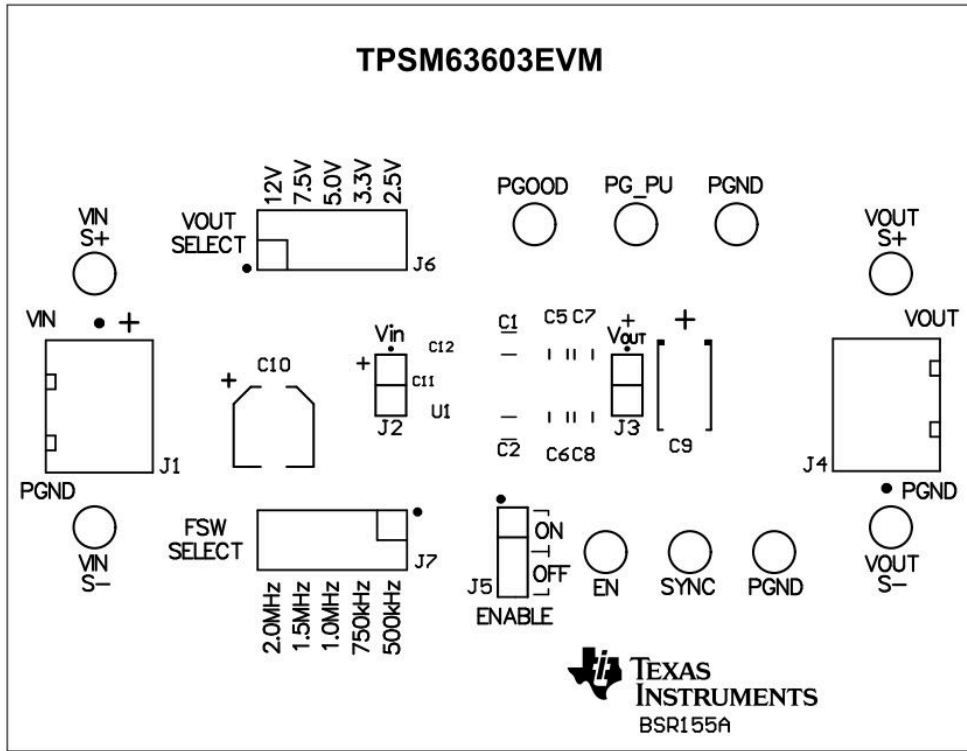


Figure 4-1. Top Silk Screen (Top View)

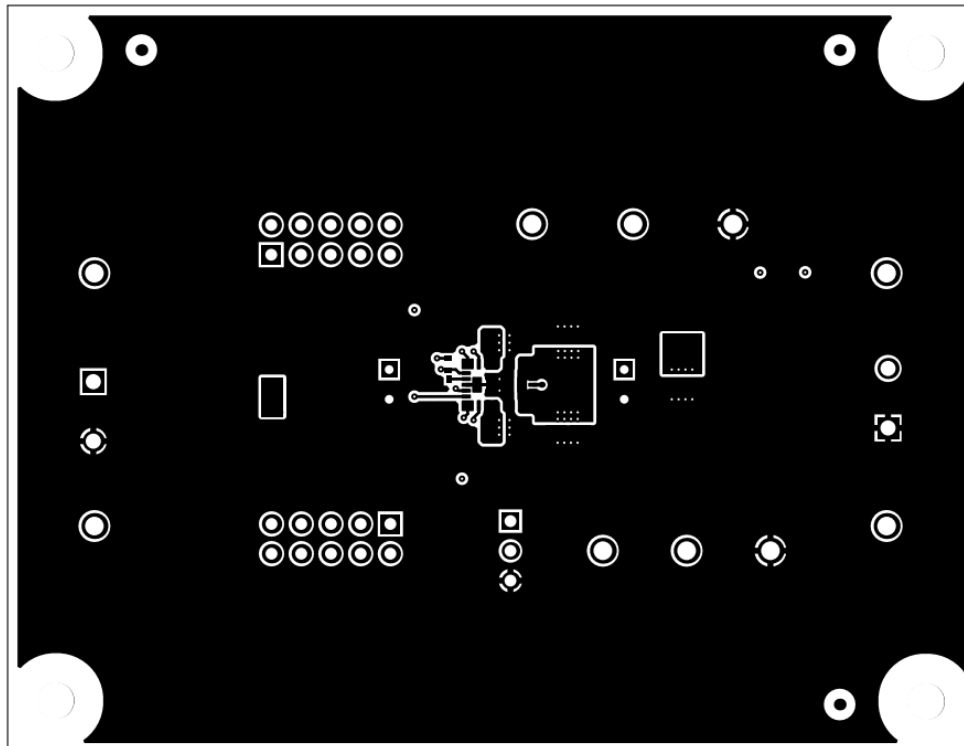
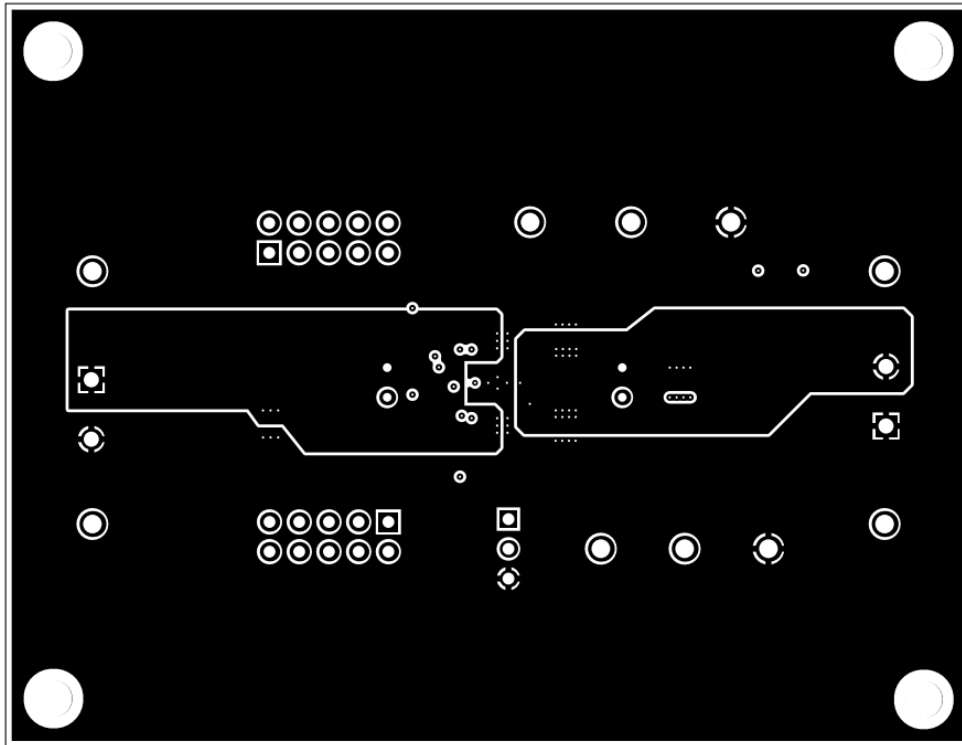
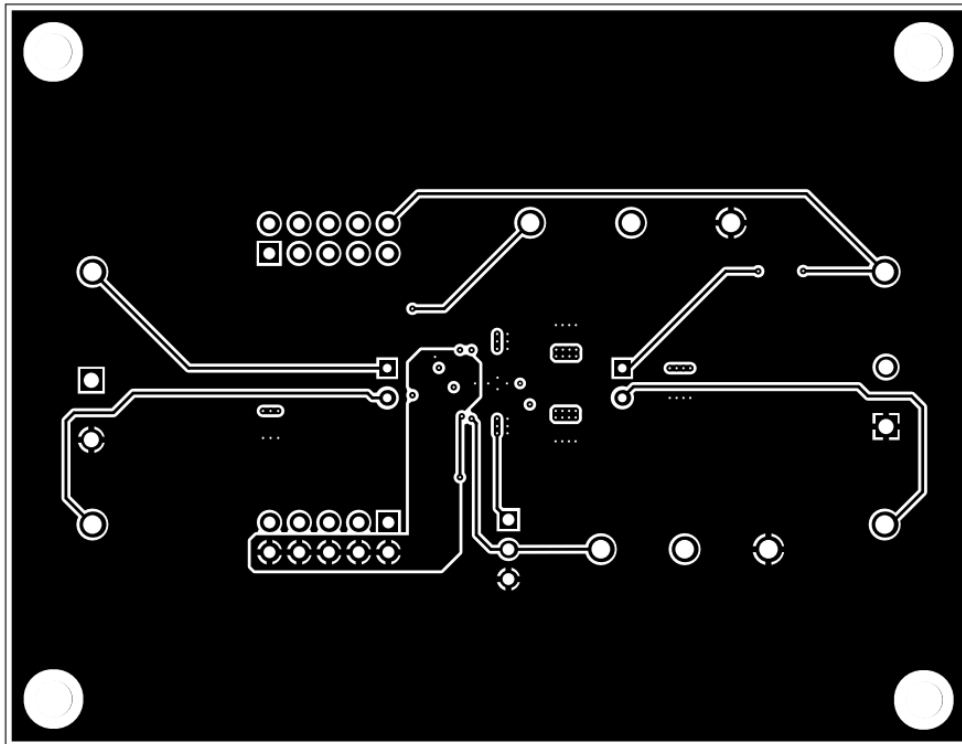


Figure 4-2. Top Copper Layer (Top View)



**Figure 4-3. Signal Layer 1 (Top View)**



**Figure 4-4. Signal Layer 2 (Top View)**

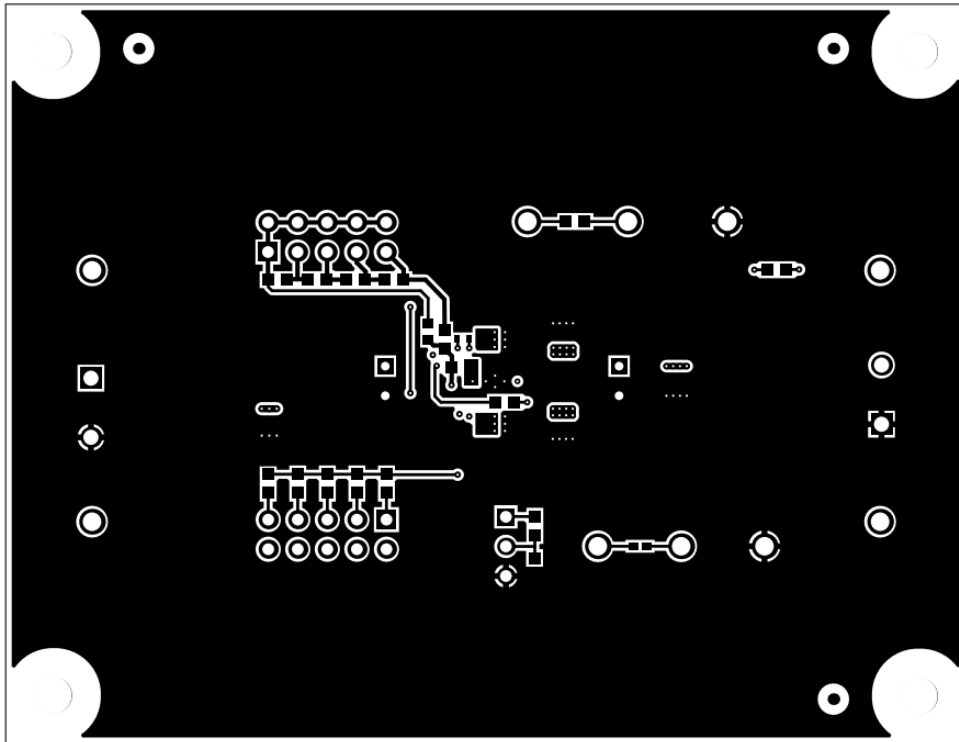


Figure 4-5. Bottom Layer (Top View)

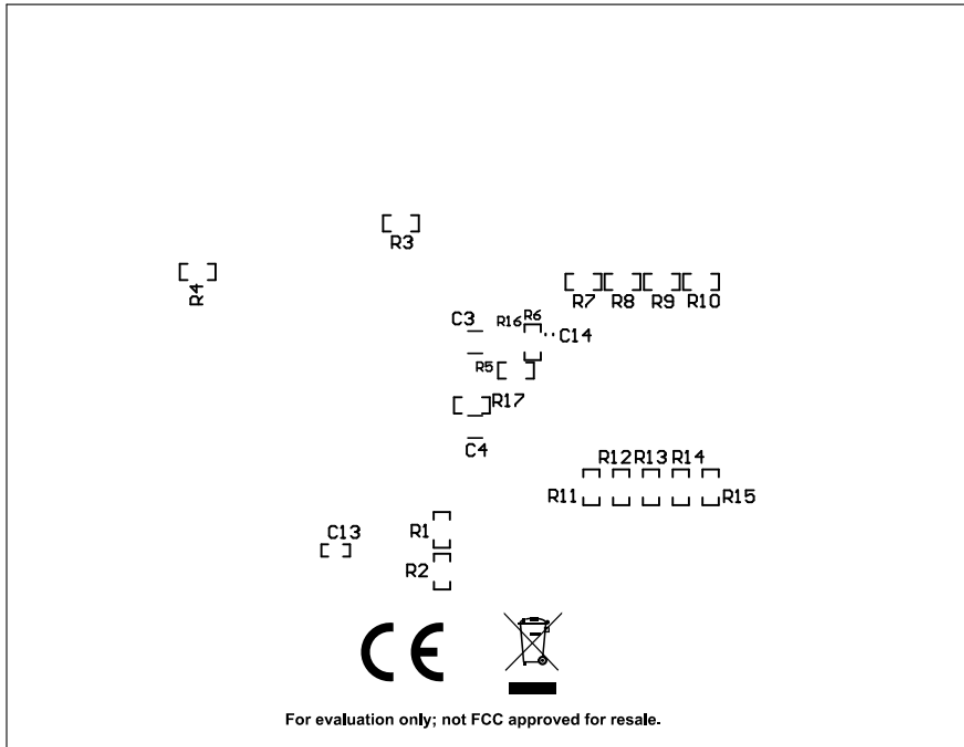


Figure 4-6. Bottom Layer Silk Screen (Bottom View)



## 5 Schematics

Figure 5-1 illustrates the TPSM63603EVM schematic.

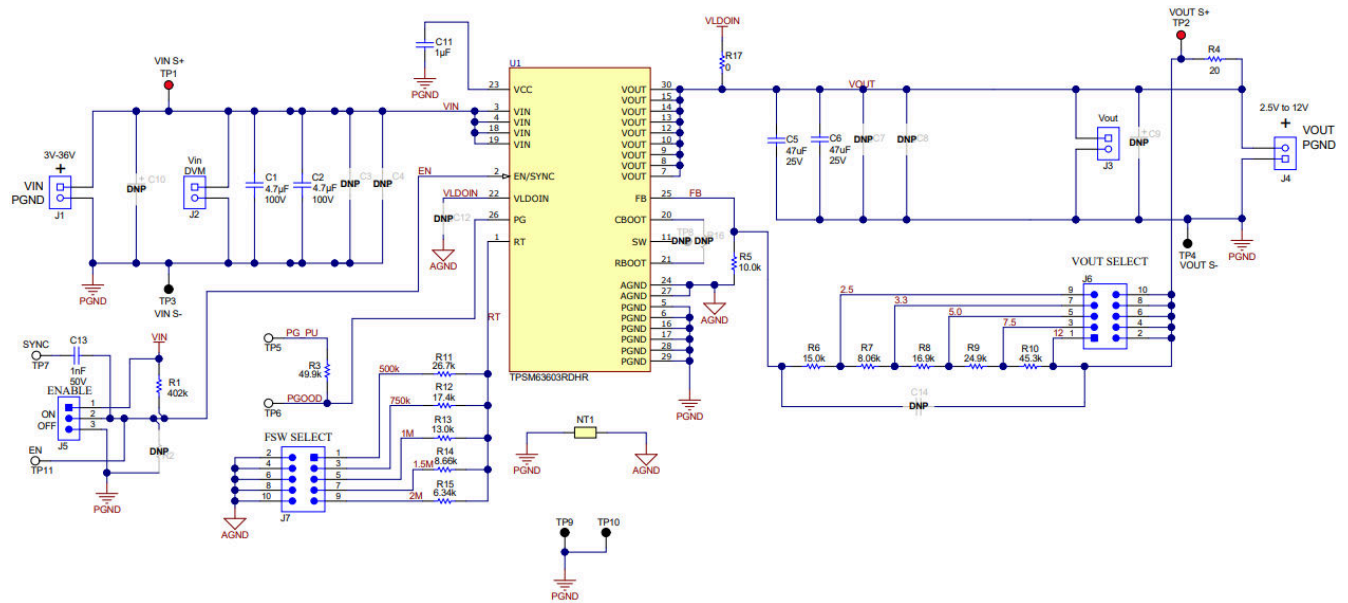


Figure 5-1. TPSM63603EVM Schematic



## 6 Bill of Materials

Table 6-1 lists the EVM bill of materials (BOM).

**Table 6-1. TPSM63603EVM BOM**

Designator	Quantity	Value	Description	Package Reference	Part Number
C1, C2	2	4.7µF	CAP, CERM, 4.7µF, 100V, X7S	1206	GRM31CC72A475KE11L
C5, C6	2	47uF	CAP, CERM, 47 uF, 25 V, X5R	1206	C3216X5R1E476M160AC
C11	1	1uF	CAP, CERM, 1 uF, 16 V, X5R	0402	EMK105BJ105KVHF
C13	1	1000pF	CAP, CERM, 1000 pF, 25 V, X5R	0402	GRM155R61E102KA01D
J1, J4	2		Terminal Block, 2x1, 5.08mm	2x1	OSTTA024163
J2, J3	2		Socket Strip, 2x1, 100mil	100mil, 2pin	310-43-102-41-001000
J5	1		Header, 100mil, 3x1	3 PIN, 100mil	PEC03SAAN
J6, J7	2		Header, 100mil, 5x2	5x2, 100mil	PEC05DAAN
R1	1	402k	RES, 402 k, 1%, 0.1 W	0603	CRCW0603402KFKEA
R3	1	49.9k	RES, 49.9 k, 1%, 0.1 W	0603	CRCW060349K9FKEA
R4	1	20	RES, 20, 5%, 0.1 W	0603	CRCW060320R0JNEA
R5	1	10.0k	RES, 10.0 k, 1%, 0.1 W	0603	CRCW060310K0FKEA
R6	1	15.0k	RES, 15.0 k, 1%, 0.1 W	0603	CRCW060315K0FKEA
R7	1	8.06k	RES, 8.06 k, 1%, 0.1 W	0603	CRCW06038K06FKEA
R8	1	16.9k	RES, 16.9 k, 1%, 0.1 W	0603	CRCW060316K9FKEA
R9	1	24.9k	RES, 24.9 k, 1%, 0.1 W	0603	CRCW060324K9FKEA
R10	1	45.3k	RES, 45.3 k, 1%, 0.1 W	0603	CRCW060345K3FKEA
R11	1	8.66k	RES, 8.66 k, 1%, 0.1 W	0603	CRCW06038K66FKEA
R12	1	13.0k	RES, 13.0 k, 1%, 0.1 W	0603	CRCW060313K0FKEA
R13	1	17.4k	RES, 17.4 k, 1%, 0.1 W	0603	CRCW060317K4FKEA
R14	1	26.7k	RES, 26.7 k, 1%, 0.1 W	0603	CRCW060326K7FKEA
R15	1	66.5k	RES, 66.5 k, 1%, 0.1 W	0603	CRCW060366K5FKEA
R17	1	0	RES, 0, 1%, 0.1 W	0603	RMCF0603ZT0R00
TP1, TP2	2		Red Test Point	Thru-hole	5010
TP3, TP4, TP9, TP10	4		Black Test Point	Thru-hole	5011
TP5, TP6, TP7, TP11	4		White Test Point	Thru-hole	5012
U1	1		36-V Input, 1-V to 13-V Output, 3-A Power Module	B3QFN	TPSM63603
	1		36-V Input, 1-V to 13-V Output, 3-A Power Module with Spread Spectrum	B3QFN	TPSM63603S
C3, C4, C7, C8	0			1206	
C9	0			7343-40	
C10	0			SMT 6.3x5.8mm	
C12	0			0402	
C14	0			0603	
R2	0			0603	
R16	0			0402	

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2021) to Revision A (July 2021)	Page
• Added information for the TPSM63603SEVM.....	1

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated