EVM User's Guide: TPSF12C1EVM-FILTER

Active EMI Filter Evaluation Module for Single-Phase AC Power Systems

Description

The TPSF12C1EVM-FILTER evaluation module (EVM) is specifically designed to validate the performance of the TPSF12C1 power-supply filter IC. The active EMI filter (AEF) helps to improve the common-mode (CM) electromagnetic interference (EMI) signature in single-phase AC power systems by amplification of the effective Y-capacitance value.

Get Started

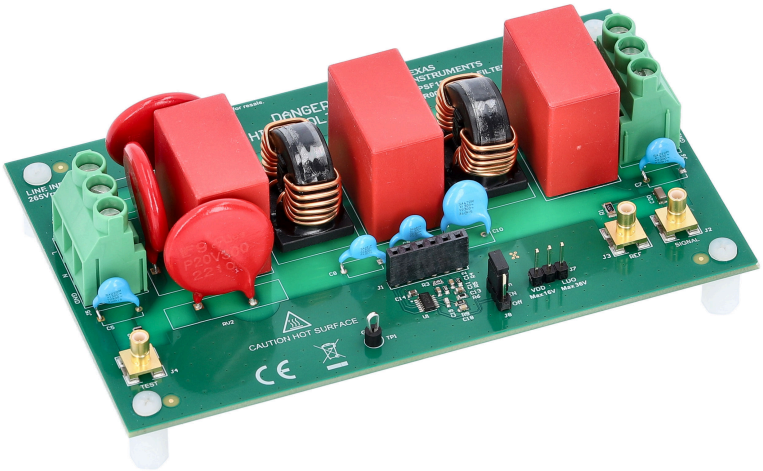
1. Order the TPSF12C1EVM-FILTER EVM
2. Study this EVM user's guide and PCB layout files
3. Use the TPSF12C1 quickstart calculator to assist with EMI filter design and component selection
4. Prior to connecting the power stage, test the active filter circuit with a low-voltage signal source
5. Connect the filter to an AC-input power stage and verify the INJ voltage swing is within limits
6. Measure the total (DM and CM) EMI signature and use a splitter to isolate the CM contribution

Features

- Improved CM EMI performance for applications with single-phase AC input
  - Voltage-sense, current-inject AEF topology presents low shunt impedance by amplifying the effective value of Y-capacitance
    - Up to 30 dB reduction in the CM EMI signature from 100 kHz to 3 MHz
  - A higher effective Y-capacitance enables a reduction in CM choke size, weight and cost
- Simple configuration for single-phase AC systems
  - Integrated sensing filter and summing network
  - Low Y-capacitor line-frequency leakage current to chassis ground maintains safety
  - Simplified compensation network
- Inherent protection features for reliable design
  - Withstands 6-kV+ surge with minimal external component count
    - Helps meet IEC 61000-4-5 surge immunity system-level specification
    - Integrated SENSE input surge protection
  - Wide VDD supply voltage range of 8 V to 16 V
    - Undervoltage lockout (UVLO) set to turn on and off at 7.7 V and 6.7 V, respectively
    - The EVM includes a high-PSRR LDO for step-down regulation to 12 V (if needed)
  - 175°C thermal shutdown protection
  - Integrated VDD-to-EN pullup allows use of an open-drain/collector device for disable function
- Fully assembled, tested and proven two-layer PCB design with 5" × 3" (127 mm × 76 mm) total area

Applications

- On-board charger for BEVs and PHEVs
- Power delivery – high-density server rack PSUs
- Welders and other industrial systems
- Telecom AC/DC rectifiers



1 Evaluation Module Overview

1.1 Introduction

The TPSF12C1EVM-FILTER evaluation module (EVM) is designed to conveniently evaluate the performance of the TPSF12C1 active filter IC. The EVM helps to improve the CM EMI signature in single-phase AC power systems.

The TPSF12C1 provides a low shunt impedance path for CM noise in the frequency range of interest for EMI measurement and helps to meet prescribed limits for EMI standards, such as:

- CISPR 11, EN 55011 – Industrial, Scientific and Medical (ISM) applications
- CISPR 25, EN 55025 – Automotive applications
- CISPR 32, EN 55032 – Multimedia applications

Enabling up to 30 dB of CM noise reduction at the lower end of specified frequency ranges (for example, 100 kHz to 3 MHz) significantly reduces the footprint, volume, weight and cost of the CM filter implementation, especially the CM choke components that are designed to attenuate lower-order harmonics – and hence are large size. The TPSF12C1 senses the high-frequency noise on each power line using two Y-rated sense capacitors and injects a noise-canceling current back into the power lines using a Y-rated inject capacitor. The GND terminal of the EVM requires a direct, low-inductance connection to the chassis ground or Earth terminal of the filter circuit.

1.2 Kit Contents

- A complete filter board (EVM) rated at 10 A, including the TPSF12C1 active EMI filter IC
- EVM Disclaimer Read Me
- High Voltage Read Me

1.3 Specifications

Table 1-1 lists the EVM specifications. The input accepts 120 VAC or 240 VAC standard single-phase mains supply voltages. V_{VDD} = 12 V, unless otherwise indicated.

Table 1-1. Electrical Performance Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS – EMI FILTER BOARD					
Filter input voltage, V_{AC}		85	240	265	V_{RMS}
Filter rated current, I_{AC}				10	A_{RMS}
INPUT CHARACTERISTICS – TPSF12C1 AEF IC					
VDD supply voltage, V_{VDD} (1)		8	12	16	V
VDD UVLO turn-on threshold, $V_{VDD(on)}$	V_{VDD} rising		7.7		
VDD UVLO turn-off threshold, $V_{VDD(off)}$	V_{VDD} falling		6.7		
VDD supply current, enabled, $I_{VDD(on)}$	EN open or tied high		12.5		mA
VDD supply current, disabled, $I_{VDD(off)}$	EN tied to GND		50		µA
OUTPUT CHARACTERISTICS – TPSF12C1 AEF IC					
Inject voltage, V_{INJ} (2)		2.5		V_{VDD} – 2	V
Inject current, I_{INJ}	V_{VDD} = 8 V to 16 V	–80		80	mA
SYSTEM CHARACTERISTICS					
Common-mode EMI reduction(3)	150 kHz to 1 MHz		20		dB
Ambient temperature, T_A		–40		85	°C
IC junction temperature, T_J		–40		150	

(1) The nominal VDD supply voltage (relative to chassis GND) of the TPSF12C1 is 12 V.
(2) Verify that the INJ pin voltage swing is between the prescribed limits to avoid saturation and clipping.
(3) The expected EMI reduction with this EVM is up to 30 dB (with the TPSF12C1 enabled vs. disabled) when swept from 100 kHz to 3 MHz. This performance metric can change based on the VDD supply voltage, passive filter component values, active circuit compensation and damping component values, ambient temperature, and other parameters.

1.4 Device Information

CM filters for both commercial (Class A) and residential (Class B) environments typically have limited Y-capacitance due to touch-current safety requirements and, thus require large-sized CM chokes to achieve the requisite attenuation; ultimately resulting in filter designs with bulky, heavy and expensive passive components. The deployment of active filter circuits enable more compact filters for next-generation power conversion systems.

The EVM, a practical filter circuit realization for a single-phase power system, showcases the EMI performance improvement or size reduction achievable with the TPSF12C1, a single-phase power-supply filter IC.

The circuit advantages summarize as:

1. Simple filter structure – with wide operating frequency range and high stability margins
2. Reduced CM choke size – for lower volume, weight and cost. This also enables much less copper loss and better high-frequency performance due to lower choke self-parasitics and higher self-resonant frequency
3. No additional magnetic components – only uses Y-rated sense and inject capacitors with minimal impact to peak touch current (measured according to IEC 60990)
4. Enhanced safety – using a low-voltage AEF IC referenced to chassis ground
5. Standalone AEF IC implementation – enables maximum flexibility in terms of placement near the filter components
6. Surge immunity – robust to line voltage surges to meet IEC 61000-4-5 (with appropriate voltage clamping internal or external to the IC).

Note

The damping and compensation component values included with this EVM can require modification if the passive filter components (the CM chokes in particular) are changed. Refer to the *TPSF12C1 Standalone Active EMI Filter for Common-mode Noise Mitigation in Single-Phase AC Automotive Power Systems* data sheet and *TPSF12C1 quickstart calculator* for additional guidance pertaining to AEF circuit operation and loop gain, passive component selection and expected EMI performance.

	**CAUTION** Hot surface. Contact can cause burns. Do not touch.
	**CAUTION** High Voltage. Risk of electric shock.

General Texas Instruments High Voltage Evaluation (TI HV EVM) User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and those working around you. Contact TI's Product Information Center http://ti.com/customer support for further information.

Save all warnings and instructions for future reference.

> **WARNING**
>
> Failure to follow warnings and instructions can result in personal injury, property damage or death due to electrical shock and burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is *intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise and knowledge of electrical safety risks in development and application of high voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments.* If you are not suitably qualified, then immediately stop from further use of the HV EVM.

1. Work Area Safety:
   a. Keep work area clean and orderly.
   b. Qualified observers must be present anytime circuits are energized.
   c. Effective barriers and signage must be present in the area where the TI HV EVM and the interface electronics are energized, indicating operation of accessible high voltages can be present, for the purpose of protecting inadvertent access.
   d. All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50Vrms/75VDC must be electrically located within a protected Emergency Power Off EPO protected power strip.
   e. Use stable and non-conductive work surface.
   f. Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
2. Electrical Safety:
   a. As a precautionary measure, a good engineering practice is to assume that the entire EVM has fully accessible and active high voltages.
   b. De-energize the TI HV EVM and all the inputs, outputs and electrical loads before performing any electrical or other diagnostic measurements. Revalidate that TI HV EVM power has been safely de-energized.
   c. With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
   d. Once EVM readiness is complete, energize the EVM as intended.

   > **WARNING**
   >
   > While the EVM is energized, never touch the EVM or the electrical circuits, as the ciruits can be at high voltages capable of causing electrical shock hazard.
3. Personal Safety
   a. Wear personal protective equipment e.g. latex gloves or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.

Limitation for safe use:

EVMs are not to be used as all or part of a production unit.

2 Hardware

2.1 EVM Description

The TPSF12C1EVM-FILTER can be used for evaluation and for system development of an EMI filter circuit and application. Figure 2-1 presents typical schematics of equivalent single-phase passive and active filter designs – with the active circuit component values corresponding to this EVM. Terminals designated L, N and PE refer to live, neutral and protective earth, respectively. Comparing the passive and active circuits in this example, the CM inductance of chokes L_{CM1} and L_{CM2} reduces from 12 mH to 2 mH by virtue of the higher effective Y-capacitance with AEF.

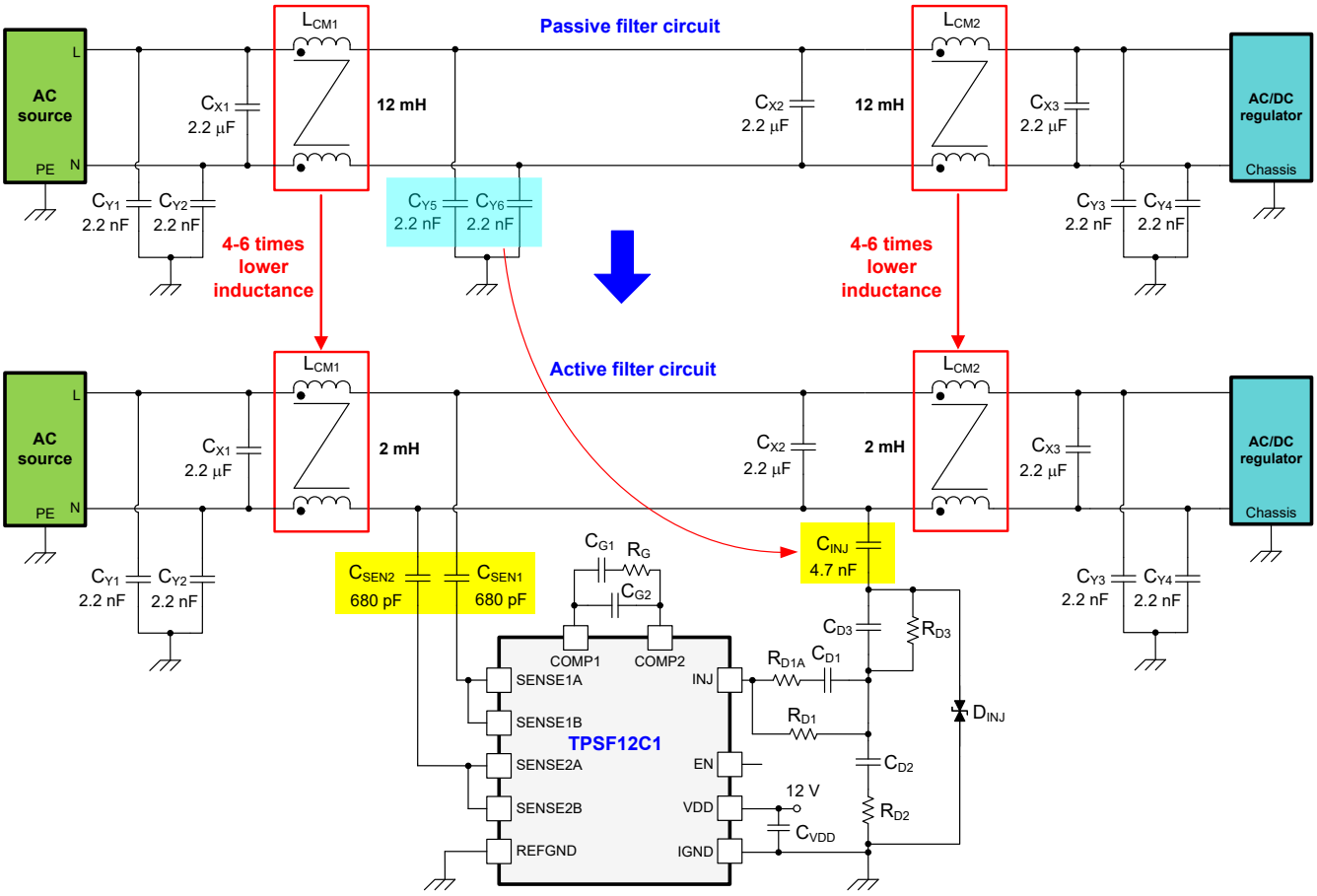


Figure 2-1. Passive and Active Filter Schematics

The AEF circuit uses a capacitive multiplier circuit in place of the two Y-capacitors normally placed between the CM chokes in a conventional two-stage passive filter design. The TPSF12C1 senses the high-frequency CM disturbance on the two power lines using two Y-rated sense capacitors and injects a noise-canceling current back into the power lines using a Y-rated inject capacitor. The X-capacitor placed between the two CM chokes provides a low-impedance path between the power lines from a CM standpoint, typically up to low-MHz frequencies. This allows current injection onto one power line (neutral in this case) using only one inject capacitor.

Acting as a complete filter with features such as surge immunity protection and X-capacitor resistive discharge, the EVM uses a recommended PCB layout to minimize the overall noise signature and required board area. If required, the user can add external components for inrush limiting and fuse protection.

2.2 Setup

Figure 2-2 shows a typical EMI measurement setup. A line impedance stabilization network (LISN) in series with each supply line enables measurement of the total EMI that includes DM and CM propagation components. A splitter/combiner can be used to extract the DM and CM noise signatures from the total noise measurement.

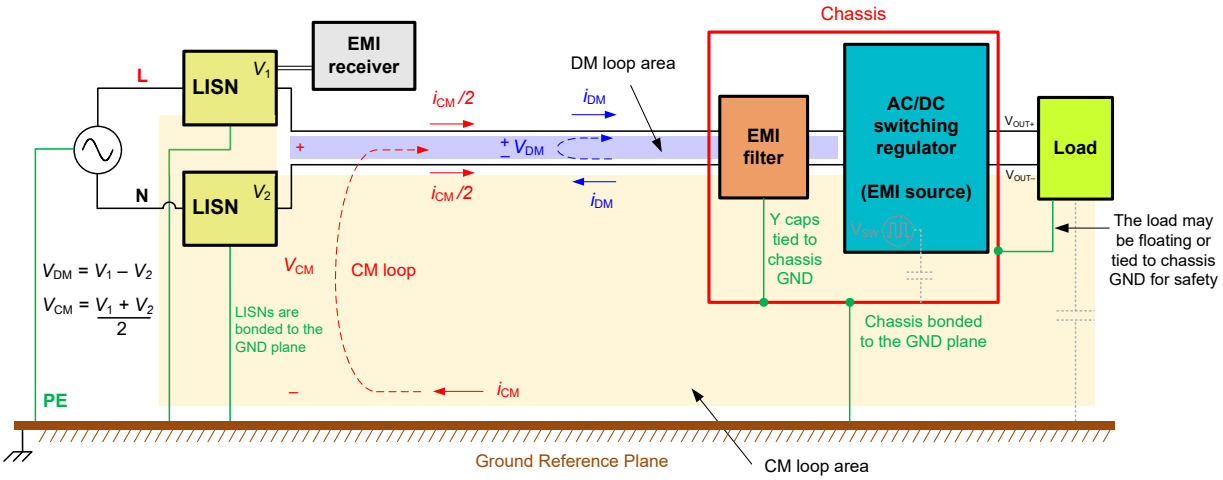


Figure 2-2. EMI Measurement Setup for a Single-Phase System

The AC/DC regulator has internal high-dv/dt switching nodes that can capacitively couple CM noise to the chassis. As such, verifying the Y-capactiors in the EMI filter are closely referenced to the chassis is imperative, as illustrated in Figure 2-2. The Y-capacitors can then return the CM noise current back to the noise source in a tight conduction loop. Otherwise, the noise current can flow in the reference ground plane back to the LISNs, rendering the EMI filter less effective.

Figure 2-3 shows the recommended setup to evaluate the performance of the TPSF12C1 with a power stage connected.

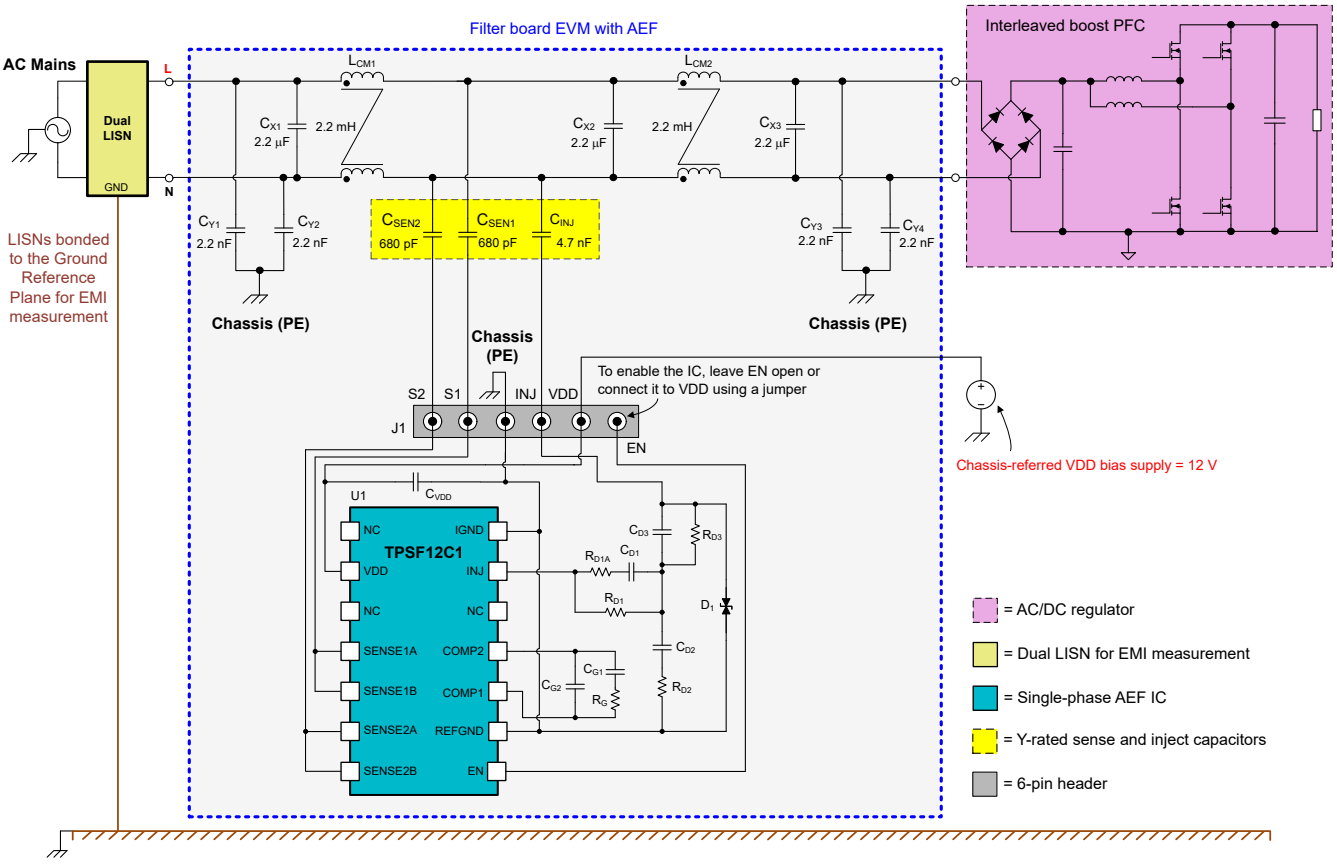


Figure 2-3. EVM Setup Schematic for High-Voltage Testing with AC/DC Power Stage Connected

A two-phase interleaved boost PFC topology in Figure 2-3 represents a typical single-phase AC/DC regulator and is drawn for illustrative purposes. The setup is essentially agnostic to regulator topology.

Meanwhile, Figure 2-4 shows a schematic that is designed for low-voltage testing of the active filter design, including insertion loss measurement and EMI performance characterization. This facilitates an easy and convenient verification of the active filter circuit prior to connection to a high-voltage switching regulator. A good signal source and coupling capacitor provide CM excitation that mimics the CM noise source voltage and noise source impedance related to the switch-node behavior of an actual power stage.

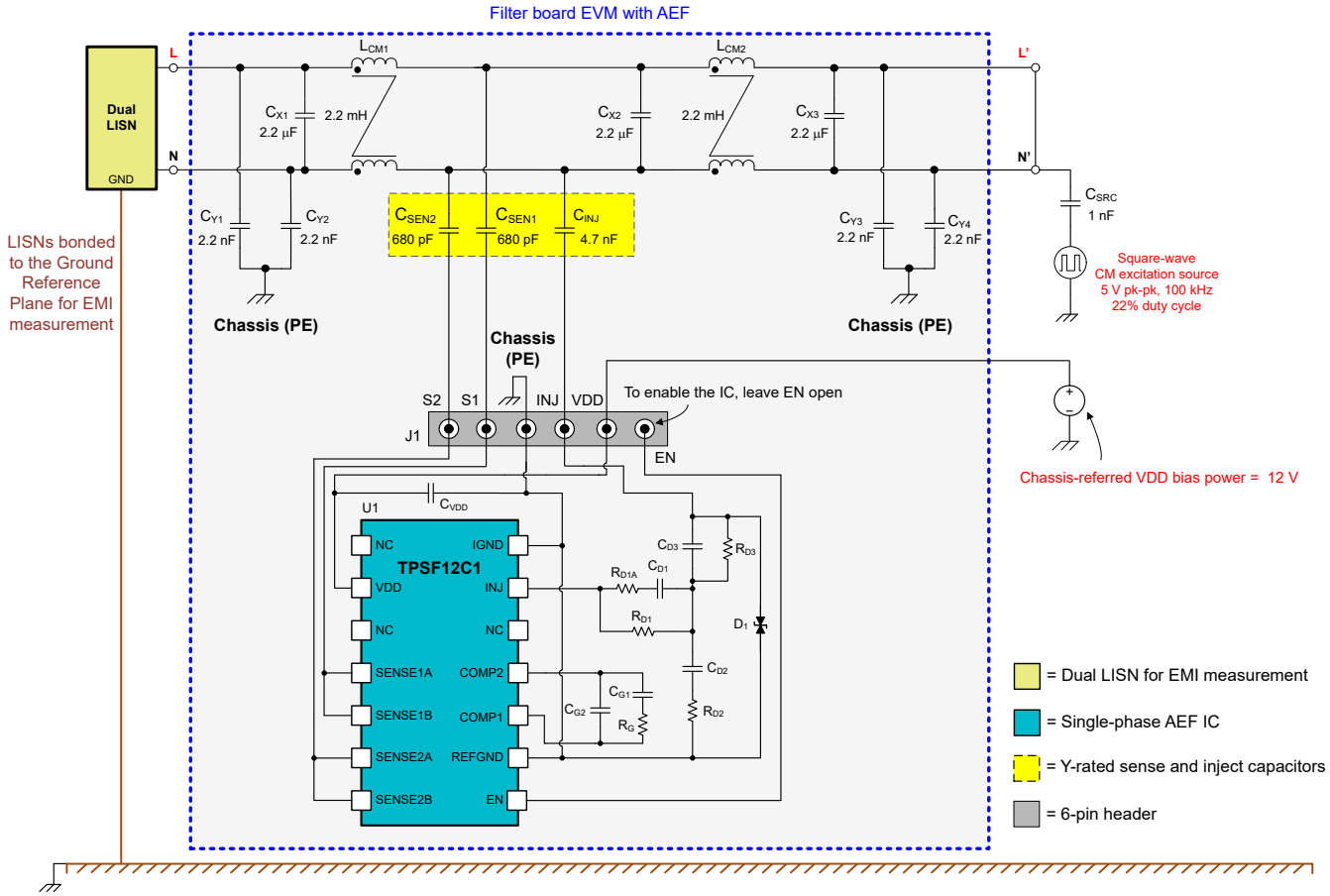


Figure 2-4. EVM Setup Schematic for Low-Voltage Testing

2.3 Header Information

Table 2-1, Table 2-2 and Table 2-3 detail the various signal headers installed on the EVM. In addition, SMB jacks designated J2, J3 and J4 on the PCB facilitate oscillator signal injection and frequency sweep for measurement of filter insertion loss or attenuation.

Header J1 specifically provides connections to the low-voltage side of the sense capacitors (corresponding to the SENSE pins of the TPSF12C1), the low-voltage side of the inject capacitor, the IC bias power supply (VDD and GND pins), which is set between 8 V and 16 V, and a remote enable (EN) signal.

Table 2-1. J1 Header Connections

POSITION(1)	LABEL	DESCRIPTION
1	EN	Enable input – leave open or tie high to enable the IC; tie to GND to disable
2	VDD	Supply voltage connection – connect to a 12-V bias power supply referenced to GND(2)
3	INJ	Low-voltage terminal of the Y-rated inject capacitor, C10. Also connects to the AEF damping network
4	GND	Ground – connect to the chassis ground of the system with a direct, low-inductance connection
5	S1	Low-voltage terminal of sense capacitor, C9. Also connects to the SENSE1A and SENSE1B pins of the IC
6	S2	Low-voltage terminal of sense capacitor, C8. Also connects to the SENSE2A and SENSE2B pins of the IC

(1) Pin positions of header J1 are designated right to left when viewed from the top side of the EVM.
(2) Working at an ESD-protected workstation, verify that any wrist straps, bootstraps or mats are connected and referencing the user to earth ground before power is applied to the EVM.

Table 2-2. J7 Header Connections

POSITION	LABEL	DESCRIPTION
1	VDD	Connect a low-noise external source (8 V to 16 V) between the VDD and GND terminals
2	GND	Connected by a trace on the PCB to GND
3	LDO	Connect an external source (maximum 36 V) between the LDO and GND terminals to supply the on-board LDO that outputs a regulated 12 V to VDD

Table 2-3. J8 Header Connections

POSITION	LABEL	DESCRIPTION
1	ON	Connected by a trace on the PCB to VDD
2	EN	Jumper EN to ON or OFF to enable and disable the TPSF12C1, respectively
3	OFF	Connected by a trace on the PCB to GND

2.4 EVM Performance Validation

1. Apply a bias supply voltage of 8 V to 16 V (nominal 12 V, with ripple voltage less than 20 mV peak-to-peak) between the VDD and GND terminals of J7. Probe the INJ terminal at header J1 with respect to GND; it should operate at a DC voltage of $V_{VDD}/2$ and have no AC perturbations that indicate instability. The VDD current consumption should be approximately 12 mA.
2. The user should perform *low-voltage testing* prior to connection to a high-voltage power stage. To provide CM excitation, connect a 5-V peak-to-peak square-wave source from a function generator on the regulator-side power connector J6, as shown in Figure 2-4. A 1-nF capacitor in series with the source emulates a practical CM noise source impedance.
   - Using the CM excitation source, verify the dynamic voltage range of the TPSF12C1 INJ pin. **Ensure that the INJ pin voltage relative to GND operates in a window between 2.5 V and V_{VDD} – 2 V**.
3. Connect a LISN on the input side at J5 and measure the EMI with AEF disabled (EN jumpered to OFF at J8) to benchmark the existing passive filter. The bottom terminal of inject capacitor can be shorted to GND when AEF is disabled by tying the INJ terminal of J1 to GND. This emulates the Y-capacitor connection in an equivalent passive filter design.
4. Remove the pulldown short on the inject capacitor and enable the AEF circuit by allowing the EN to float high. Repeat the EMI measurement, thus quantifying the EMI reduction related to AEF circuit operation.
5. In a similar fashion (but with the LISN replaced by a 50-Ω load connecting from L and N to GND), perform a comparison of filter *insertion loss* performance using a suitable network analyzer. SMB jacks J2, J3 and J4 on the EVM facilitate signal injection, reference measurement and test measurement, respectively.
6. Using *high-voltage safety precautions*, connect the switching power stage as shown in Figure 2-3. Depopulate components R1, R2 and C20 to maximize the clearance spacing from high-voltage nodes to ground adjacent the SMB jacks. Turn the regulator ON and perform EMI measurements with AEF enabled and disabled, similar to the procedure outlined in steps 3 and 4 above.
7. Turn the regulator OFF. Wait for all high-voltage capacitors to fully discharge.
8. Power down the IC and remove the VDD supply.

2.5 AEF Design Flow

Follow these steps to design an active filter circuit:

1. **Quickstart Calculator** – Use the TPSF12C1 quickstart calculator as a convenient starting point. See Figure 2-5 for illustration.

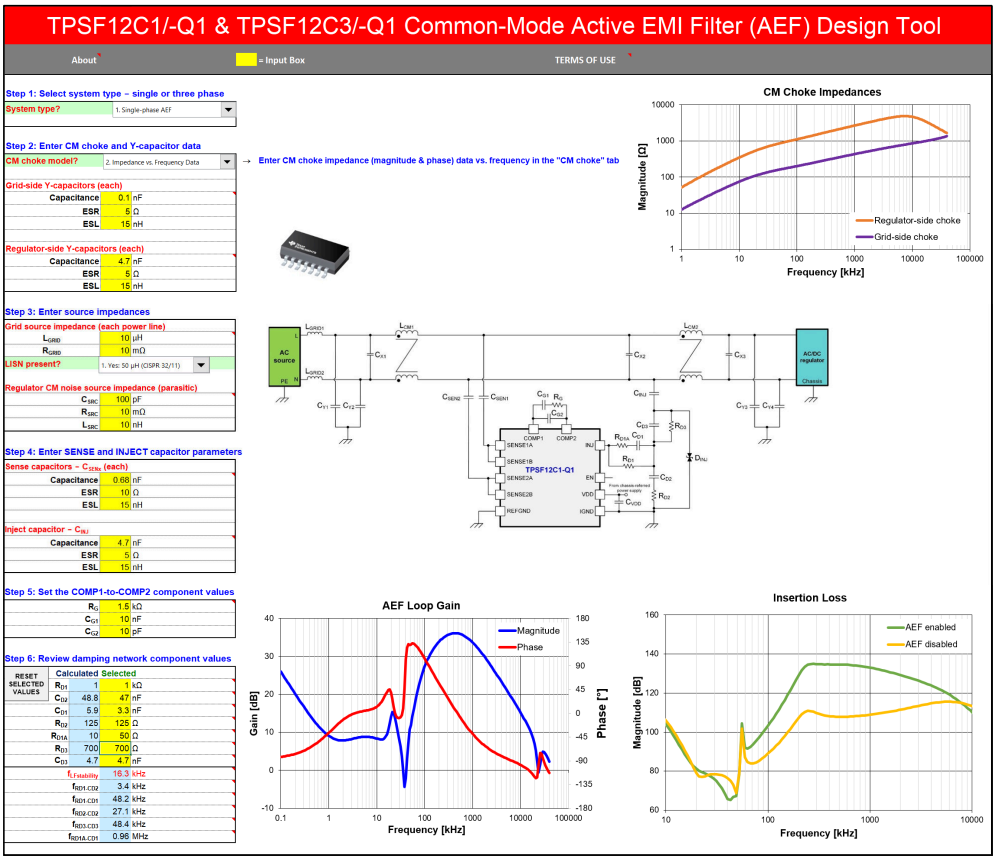


Figure 2-5. Quickstart Calculator With CM Choke Impedance, Loop Gain and Insertion Loss Plots

Typical steps to complete the quickstart calculator are as follows:

- Choose the core material for the CM chokes – the primary choices being nanocrystalline (NC) or ferrite. NC chokes are preferable for active filter designs given their higher permeability (and thus fewer winding turns), broader impedance characteristic over frequency, more damped impedance behavior with softer phase transition, and better stability over temperature.
- Define the CM choke impedances – two options are available:
  - Measure the CM impedance magnitude and phase vs. frequency using a network analyzer. Paste the data directly into the calculator file.
  - Enter the behavioral model parameters for each choke based on (a) a parallel LRC circuit for a ferrite choke (L_{CM} || R_{PAR} || C_{PAR}), or (b) a ladder network for an NC choke consisting of three parallel RL circuits connected in series along with a parasitic capacitance across the total network. An equivalent circuit model is the most convenient option if the choke data sheet includes the CM impedance data.
- Enter values for the grid-side and regulator-side Y-capacitors, sense capacitors and inject capacitor.
- Enter values for source impedance of the grid supply and the noise source. Select from a drop-down menu if a LISN (50 µH or 5 µH) is installed.
- Review the AEF loop gain plot for stability based on the calculated component values for the damping network. Adjust the damping network values to ensure the phase does not reach –180° at the resonant frequencies (when the gain is positive). Refer to the TPSF12C1 data sheet for guidance on component selection. Check the insertion loss plots with AEF enabled and disabled.

2. **Circuit Simulation** – Avail of PSPICE or SIMPLIS simulation models for the TPSF12C1 device. Use such models along with prepared test benches to investigate the operation of the complete active filter circuit. See the SIMPLIS schematic in Figure 2-6 as an example. Perform both time-domain and frequency-domain analyses as required.

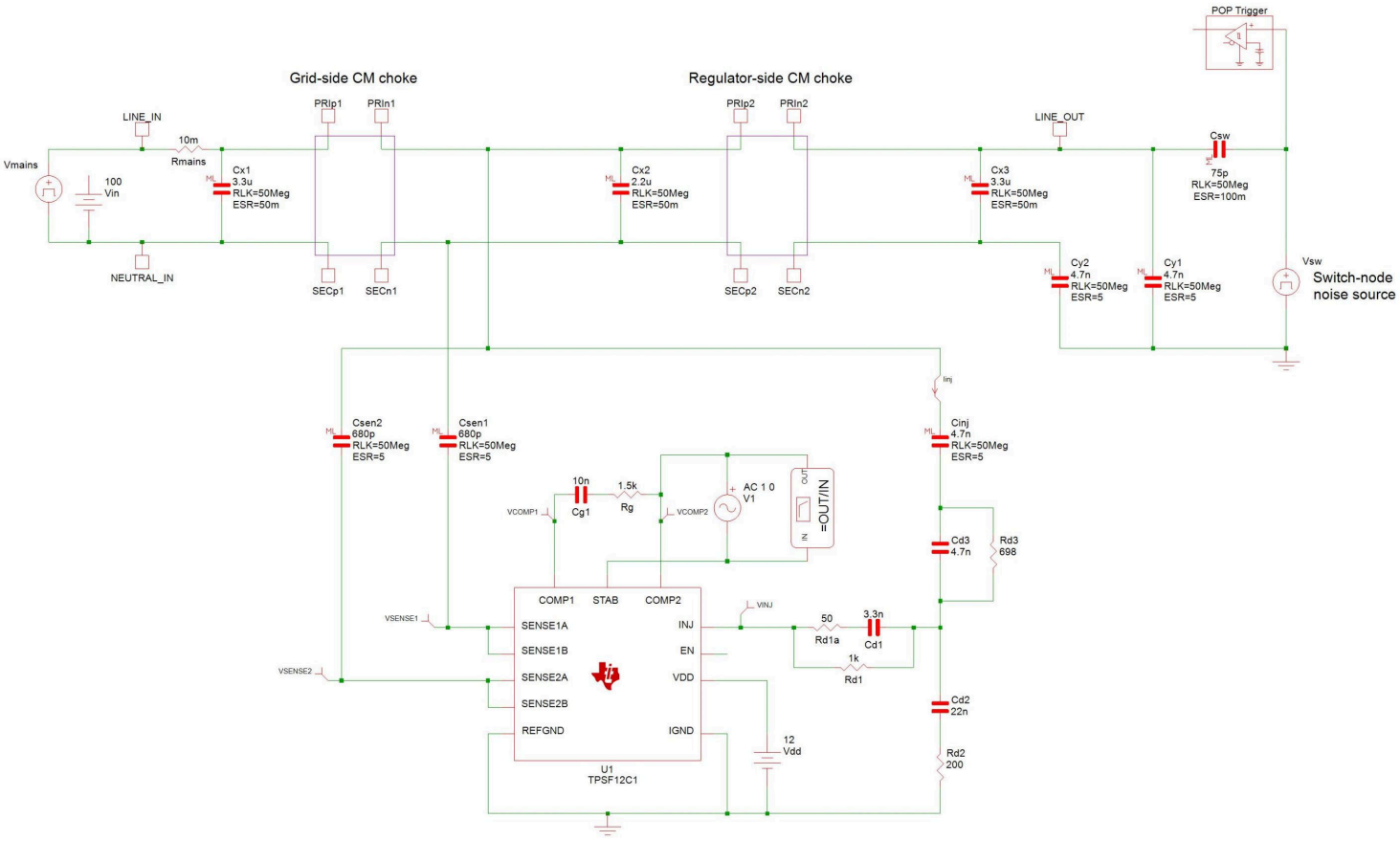


Figure 2-6. SIMPLIS Simulation Schematic of an Active Filter Circuit Using the TPSF12C1

Note that the CM choke model schematics are not shown above. If the choke model equivalent circuit parameters are defined in the quickstart calculator, transfer them directly to the simulation model as needed.

3. **Low-Voltage Tests** – Validate the filter design at low voltage prior to connecting to the switching regulator. This is a relatively easy step to confirm various aspect of the design, including filter stability, insertion loss, voltage swing on the INJ pin, and EMI performance with CM signal excitation. See Figure 2-4 and refer to tests 4 through 7 described in Section 2.4.
   - Insertion loss – measure with 50-Ω source and load impedances.
   - Apply a CM excitation signal with a function generator.
     - Check the dynamic voltage range of the INJ pin (TPSF12C1 pin 13).
     - Measure the EMI (CM only, there is no DM propagation in this test).
4. **High-Voltage Tests** – Validate the filter design while connected to the switching regulator. See Figure 2-3 and refer to tests 8 and 9 described in Section 2.4.
   - Check the dynamic voltage range of the INJ pin.
   - Calculate the device power dissipation based on V_{VDD}, I_{VDD}, T_A and $R_{\theta JA}$. Verify that the maximum junction temperature is less than 150°C under the worst case operating conditions.
   - Check the sense and inject capacitance variation over temperature and ensure the circuit is stable under all operating conditions.
   - Measure the total EMI. Separate the CM (asymmetrical) and DM (symmetrical) propagation components, as the TPSF12C1-based AEF circuit only attenuates the CM noise.

2.5.1 AEF Circuit Optimization and Debug

Here are some considerations and best practices to optimize AEF circuit operation:

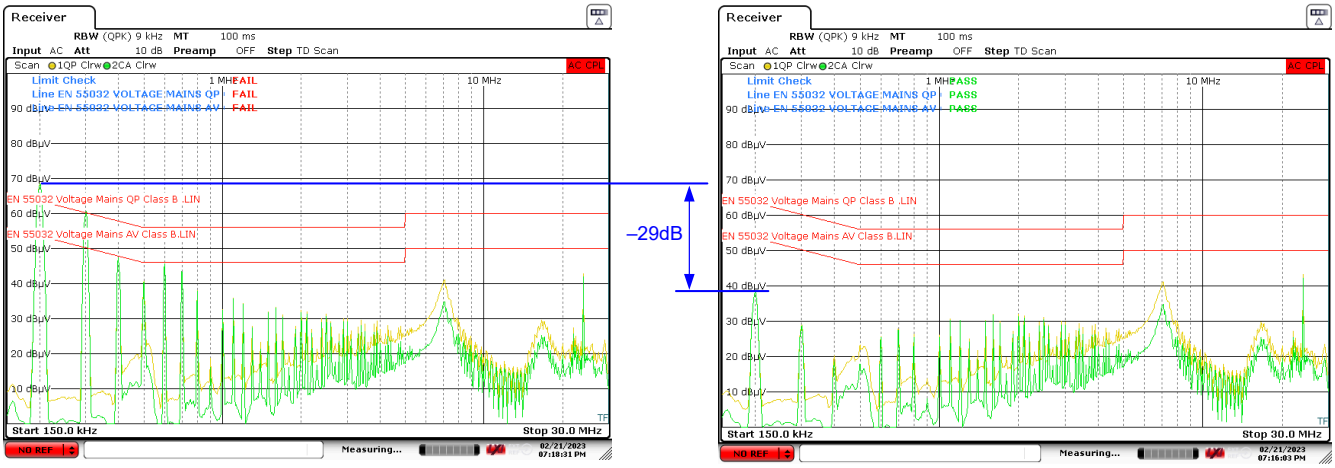
1. If the EMI measurement with AEF enabled is not performing as expected, probe the INJ pin voltage while the regulator is switching. Verify that the INJ pin voltage is not getting clipped near the positive or negative supply rails, as mentioned in step 2 of Section 2.4.
   - If the INJ pin voltage is getting clipped, increase the regulator-side Y-capacitance and/or the inject capacitance. Then recheck the loop stability using the TPSF12C1 quickstart calculator or by simulation.
2. The metallic chassis structure is a critical part of the overall filter implementation. The filter PCB typically mounts to the chassis structure using several screw attachments, and the chassis serves to connect the various GND nodes on the filter PCB. These nodes are not explicitly connected with copper on the PCB and instead rely on the chassis to complete the electrical connection. As such, the chassis becomes the lowest impedance return path for CM noise current.
   - When testing a power stage that includes a chassis as illustrated in Figure 2-2, CM noise can capacitively couple to the reference ground plane of the EMI measurement setup and thus bypass a filter circuit that is not closely referenced to this ground plane. In this case, TI recommends bonding the GND plane copper of the filter EVM directly to the reference ground plane. This also serves to minimize parasitic inductance in the GND connection to the AEF circuit. CM current emanating from the power stage then gets recirculated by the low shunt impedance of the filter Y-capacitors (both active and passive), thus preventing noise from reaching the LISN.
3. Based on the amplification of the effective Y-capacitance, AEF allows reduction of the CM choke inductance while maintaining the same LC corner frequency and CM attenuation characteristic. However, a choke with reduced CM inductance and smaller size normally has a lower leakage inductance, which is responsible for DM attenuation along with the X-capacitors.
   - If the DM inductance is significantly reduced with the smaller CM chokes, then increase the X capacitance or add a small discrete inductor to obtain sufficient DM attenuation. Otherwise, a high DM noise component (relative to the CM component) can dominate the total noise measurement, therefore concealing the impact of AEF on CM noise mitigation.
4. Typical values for the sense and inject capacitances are 680 pF and 4.7 nF, respectively. Depending on the final implementation in the target application, **the default damping and compensation component values installed on the EVM can require modification by the user to achieve acceptable loop stability**. Ferrite chokes are inherently more difficult to stabilize than their nanocrystalline equivalents.
   - For additional context pertaining to component selection and circuit optimization, refer to the TPSF12C1 product data sheet and the TPSF12C1 quickstart calculator.

3 Implementation Results

Because actual performance data can be affected by measurement techniques and environmental variables, these curves are presented for reference and can differ from actual field measurements. Unless otherwise indicated, V_{VDD} = V_{EN} = 12 V.

3.1 EMI Performance

See the *Schematic* and *Bill of Materials* for details of the EVM components for this measurement. The active filter schematic in Figure 2-1 also gives the passive circuit component values. As shown, the EMI is reduced by 29 dB at 200 kHz when AEF is enabled.



(a) (b)

Figure 3-1. CISPR 32 Class B Conducted Emissions with AEF Disabled (a) and Enabled (b)

3.2 Thermal Performance

Figure 3-2 shows the typical thermal performance of this active filter design with rated load of 10 A. The CM choke windings and TPSF12C1 device run at 28°C and 12°C above the local ambient temperature, respectively.

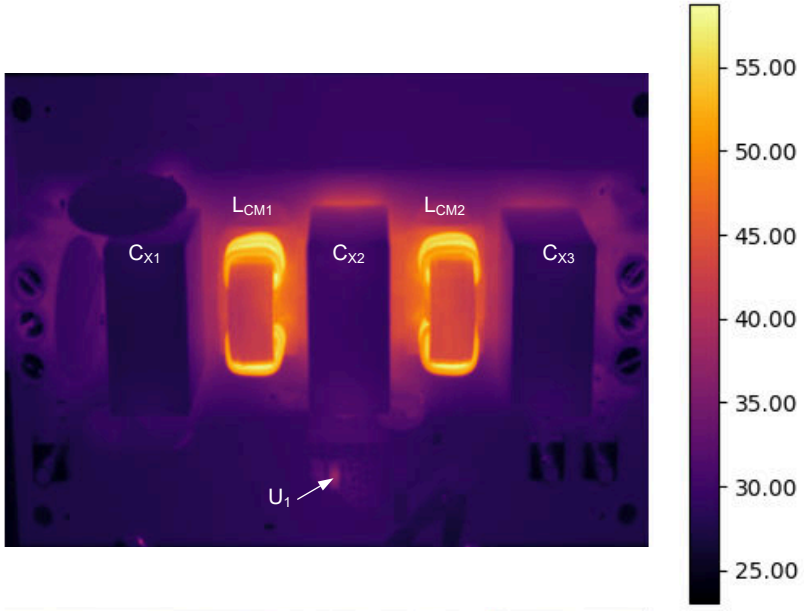


Figure 3-2. Thermal Image at 10-A Load

3.3 Surge Immunity

Figure 3-3, Figure 3-4 and Figure 3-5 show surge immunity results. The CM chokes are shorted during this test, but the MOVs are installed as required.

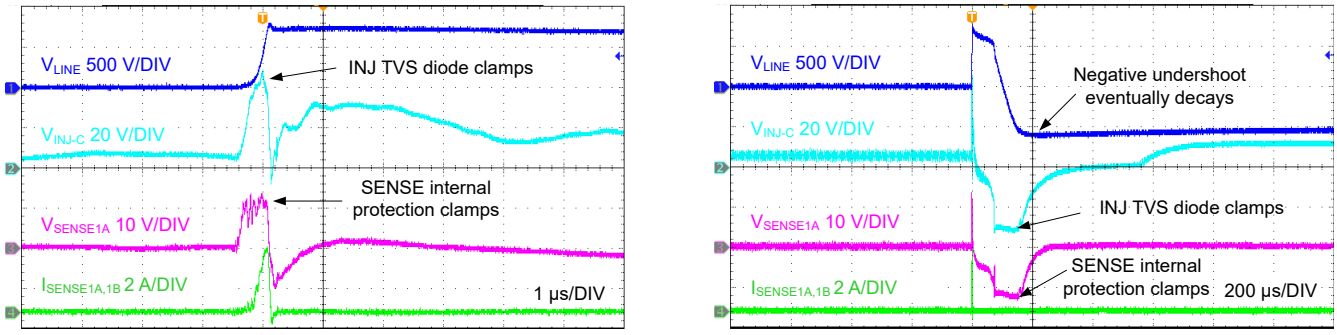


Figure 3-3. IEC 61000-4-5 Positive Surge, 6-kV Single Strike – 1 µs/div (a), 200 µs/div (b)

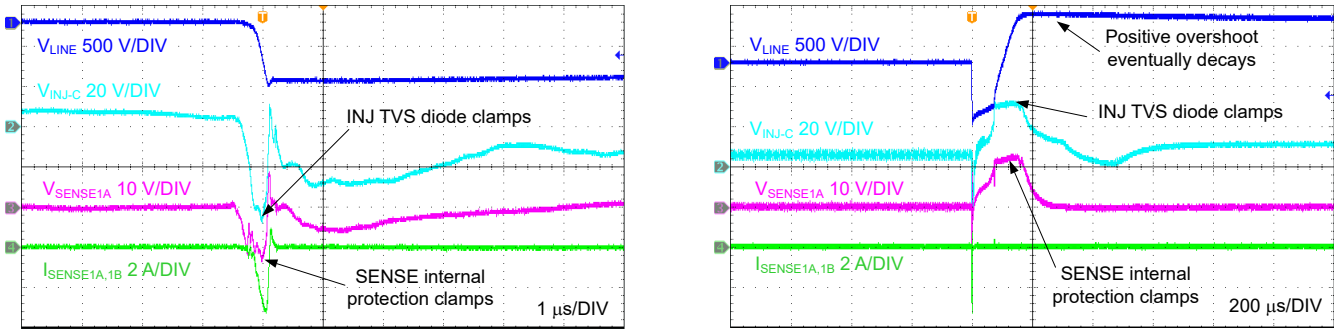


Figure 3-4. IEC 61000-4-5 Negative Surge, 6-kV Single Strike – 1 µs/div (a), 200 µs/div (b)

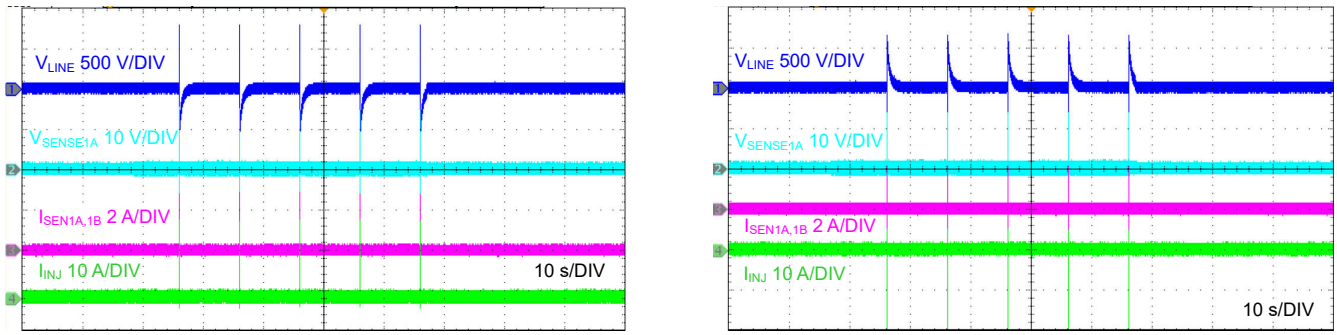


Figure 3-5. IEC 61000-4-5 Surge, 6-kV Repetitive Strike at 10-Second Intervals – Positive (a), Negative (b)

3.4 SENSE and INJ Voltages

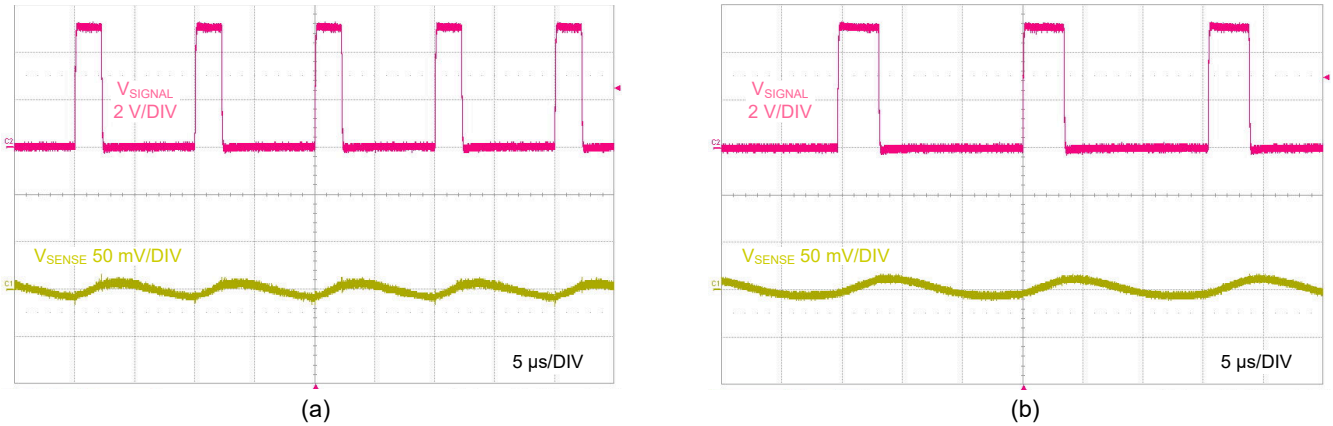


Figure 3-6. TPSF12C1 SENSE (pin 4) Voltage With CM Stimulus Applied – 100 kHz (a), 65 kHz (b)

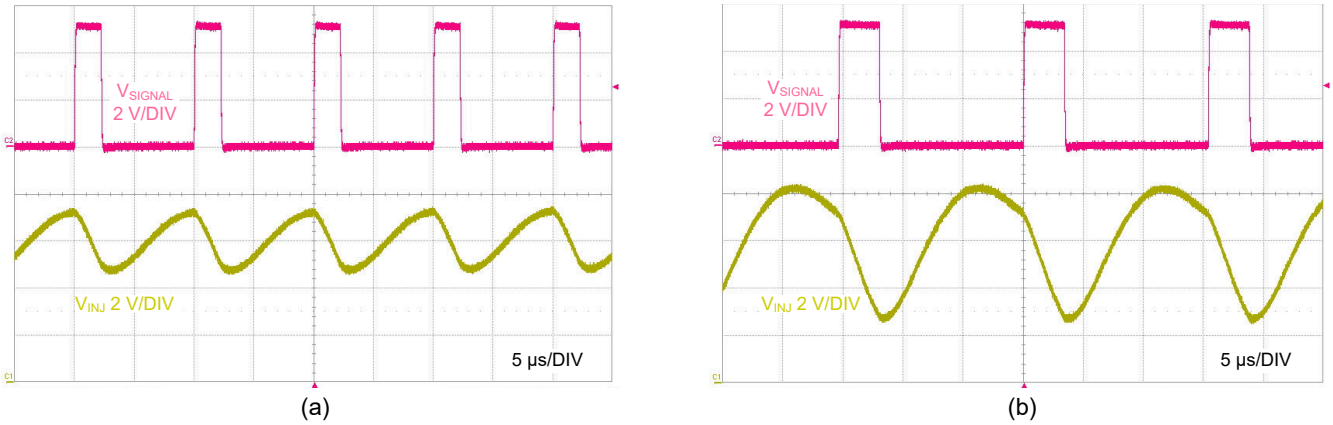


Figure 3-7. TPSF12C1 INJ (pin 13) Voltage With CM Stimulus Applied – 100 kHz (a), 65 kHz (b)

3.5 Insertion Loss

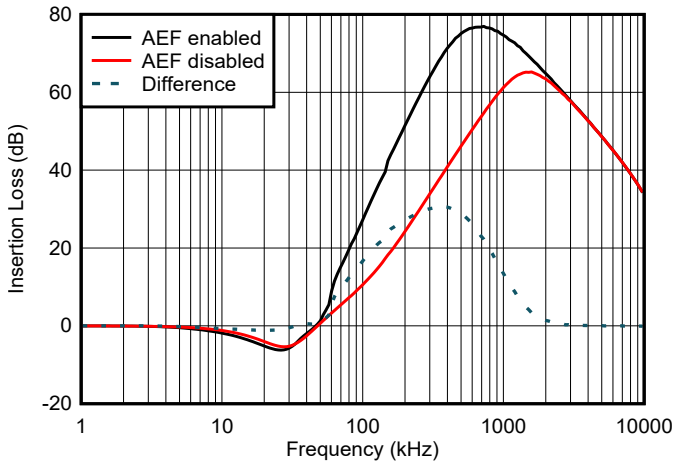


Figure 3-8. Typical Insertion Loss with AEF Enabled and Disabled

3.6 Passive vs. Active Solution Comparison

Table 3-1 captures the applicable parameters for the CM chokes in *equivalent* passive and active EMI filter designs when installed with two 12-mH and 2-mH chokes, respectively. The active design achieves a 60% total copper loss reduction at 10 A_{RMS} (P_{CU} = 6 W – 2.4 W = 3.6 W, neglecting the winding resistance increase due to temperature rise), which implies lower component operating temperatures, reduced heatsinking requirement, and improved capacitor lifetimes. The footprint, volume and weight of the chokes reduce by 41%, 52% and 62%, respectively.

Table 3-1. CM Choke Comparison in Equivalent Passive and Active Filter Designs

FILTER DESIGN	CM CHOKE PART NUMBER(1)	QTY	L_{CM} (mH)(2)	WINDING DCR (mΩ)	SIZE (mm)	TOTAL MASS (g)	TOTAL POWER LOSS at 25°C (W)
Passive	7448051012	2	12	15	23 × 34 × 33	72	6.0
Active	7448031002	2	2	6	17 × 23 × 25	20	2.4

(1) Manufactured by Würth Elektronik.
(2) Refer to the white paper, *How Active EMI Filter ICs Mitigate Common-Mode Emissions and Save PCB Space in Single- and Three-Phase Systems*, for more detail on these passive and active solutions.

Derived from the Würth Elektronik REDEXPERT tool, Figure 3-9 provides impedance curves for the CM chokes mapped out above. The curves highlight that the smaller-size 2-mH choke has a higher self-resonant frequency (SRF) and improved high-frequency performance.

As an example of the higher CM impedance at high frequencies due to lower intrawinding capacitance, the impedance of the CM choke at 30 MHz increases from 150 Ω to 2.2 kΩ (when going from 12 mH in the passive design to 2 mH in the active design). The × and o markers shown at 10 MHz and 30 MHz in Figure 3-9 demarcate the respective CM impedances for the passive and active designs. The higher choke impedance evident above 4 MHz for the active design may obviate the need for grid-side Y-capacitors (typically installed for high-frequency attenuation).

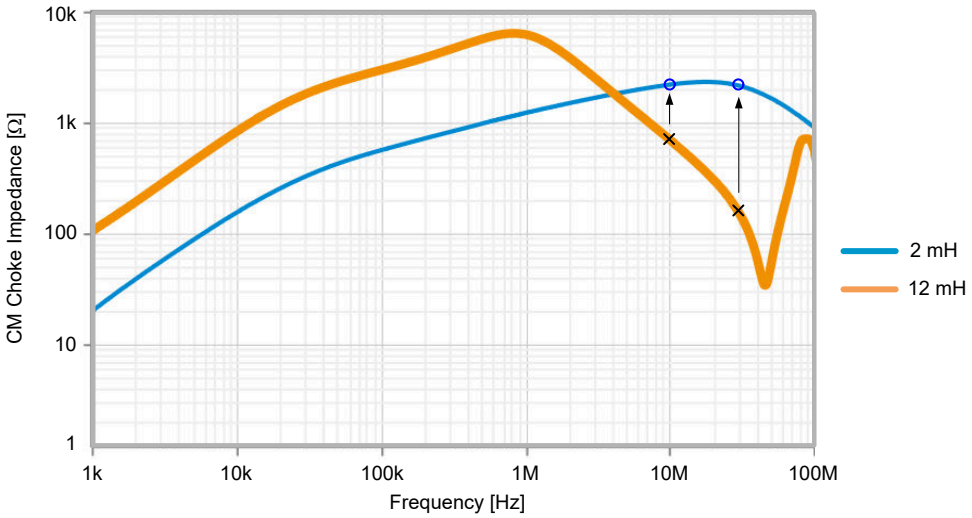


Figure 3-9. Impedance Characteristics of the Selected CM Chokes in the Passive Design (2 × 12 mH) and the Active Design (2 × 2 mH)

4 Hardware Design Files

For development support see the following:

- TPSF12C1 *Quickstart calculator*
- TPSF12C1EVM-FILTER *Altium layout source files*
- TPSF12C1 PSPICE for TI and SIMPLIS *simulation models*
- TPSF12C1QEVM *EVM user's guide*
- For TI's reference design library, visit *TI Reference Design library*
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*
- Technical Articles:
  - Texas Instruments, *How a stand-alone active EMI filter IC shrinks common-mode filter size*

4.1 Schematic

Figure 4-1 provides the EVM schematic.

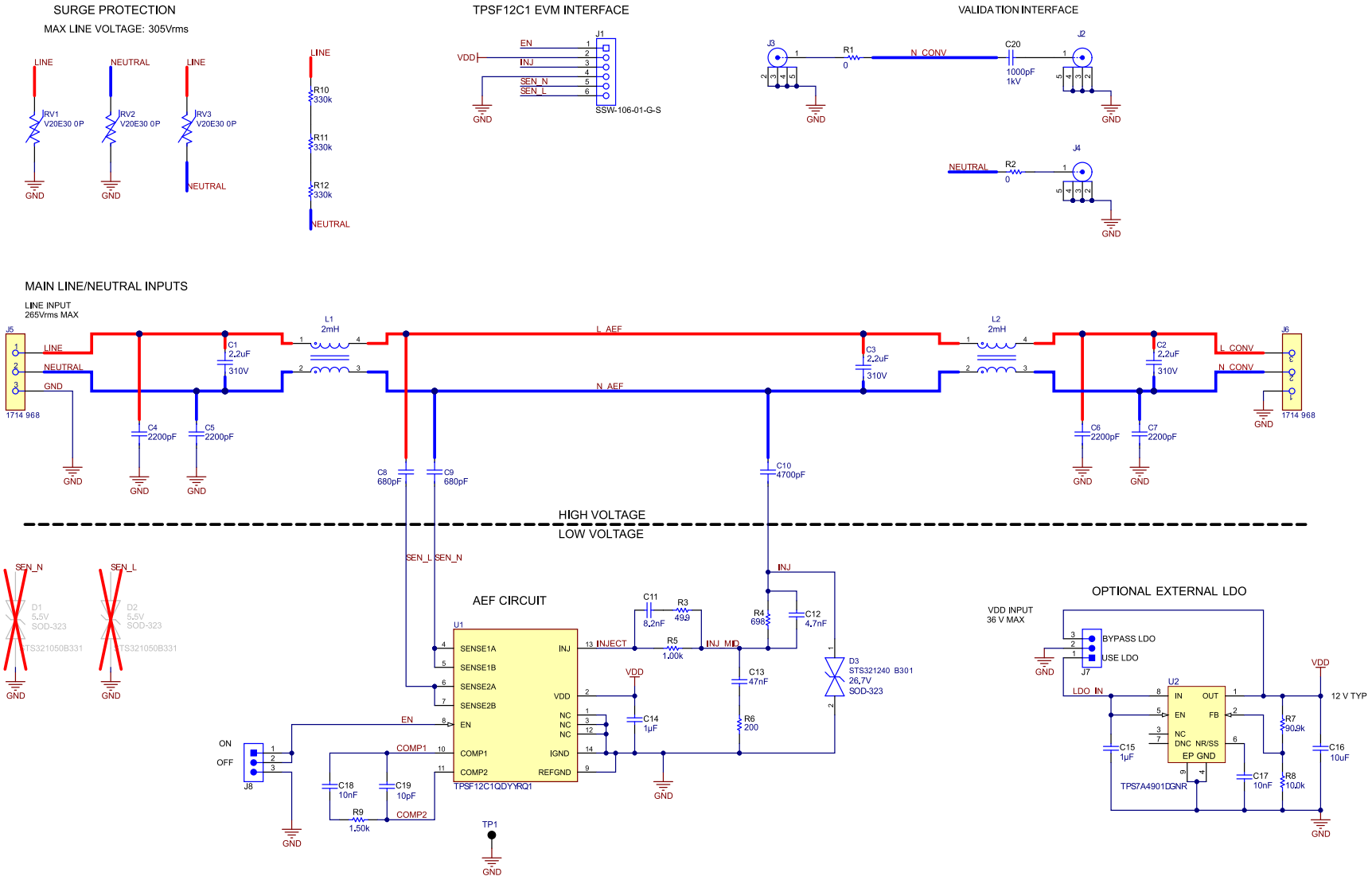


Figure 4-1. EVM Schematic

4.2 Bill of Materials

Table 4-1. EVM Component BOM

REF DES	QTY	VALUE	DESCRIPTION	PACKAGE	PART NUMBER	MANUFACTURER
C1, C2, C3	3	2.2 µF	CAP, MKP, 2.2 µF, 310 VAC, X2	26 x 15 x 25 mm	890334026034	Würth Elektronik
C4, C5, C6, C7	4	2.2 nF	CAP, CERM, 2.2 nF, 300 VAC, Y2	8 mm disc	DE2E3SA222MA3BX02F	MuRata
C8, C9	2	680 pF	CAP, CERM, 680 pF, 300 VAC, Y2	7 mm disc	DE2B3SA681KN3AX02F	MuRata
C10	1	4.7 nF	CAP, CERM, 4.7 nF, 300 VAC, Y2	10 mm disc	DE2E3SA472MA3BX02F	MuRata
C11	1	8.2 nF	CAP, CERM, 8.2 nF, 50 V, X7R	0603	GCD188R71H822KA01D	MuRata
C12	1	4.7 nF	CAP, CERM, 4.7 nF, 50 V, X7R	0603	C0603C472J5RACTU	Kemet
C13	1	47 nF	CAP, CERM, 47 nF, 50 V, X7R	0603	CGA3E2X7R1H473K080AA	MuRata
C14	1	1 µF	CAP, CERM, 1 µF, 25 V, X7R	0603	CGA3E1X7R1E105K080AC	TDK
C15	1	1 µF	CAP, CERM, 1 µF, 50 V, X7R	0603	C2012X7R1H105K085AC	TDK
C16	1	10 µF	CAP, CERM, 10 µF, 25 V, X7R	1206	GRM31CR71E106KA12L	MuRata
C17, C18	2	10 nF	CAP, CERM, 10 nF, 50 V, X7R	0603	C0603X103K5RACTU	Kemet
C19	1	10 pF	CAP, CERM, 10 pF, 50 V, C0G/NP0	0603	CGA3E2C0G1H100D080AA	TDK
C20	1	1 nF	CAP, CERM, 1 nF, 1 kV, X7R	1206	GRM31BR73A102KW01L	MuRata
D3	1	24 V	TVS diode, 24 V standoff, 50 V at 8 A	SOD-323	STS321240B301	Eaton
J1	1	–	Receptacle, 6 × 1, 2.54 mm, gold, TH	–	SSW-106-01-G-S	Samtec
J2, J3, J4	3	–	Connector, SMT, SMB jack assembly, 50 Ω	–	131-3711-201	Cinch Connectivity
J5, J6	2	–	3-position terminal block, 0.25"	–	1714968	Phoenix Contact
J7, J8	2	–	Header, 100 mil, 3 × 1, gold, TH	–	TSW-103-07-G-S	Samtec
L1, L2	2	2.2 mH	Common-mode choke, 2 mH, 10 A, 6 mΩ	23 x 17 x 25 mm	7448031002	Würth Elektronik
R1, R2	2	0 Ω	RES, 0 Ω, 5%, 0.25 W	1206	CRCW12060000Z0EA	Vishay-Dale
R3	1	49.9 Ω	RES, 49.9 Ω, 1%, 0.1 W	0603	CRCW060349R9FKEA	Vishay-Dale
R4	1	698 Ω	RES, 698 Ω, 1%, 0.1 W	0603	CRCW0603698RFKEA	Vishay-Dale
R5	1	1 kΩ	RES, 1 kΩ, 1%, 0.1 W	0603	CRCW06031K00FKEA	Vishay-Dale
R6	1	200 Ω	RES, 200 Ω, 1%, 0.1 W	0402	CRCW0603200RFKEA	Vishay-Dale
R7	1	90.9 kΩ	RES, 90.9 kΩ, 1%, 0.1 W	0602	CRCW060390k9FKEA	Vishay-Dale
R8	1	10 kΩ	RES, 10 kΩ, 1%, 0.1 W	0603	CRCW060310K0FKEA	Vishay-Dale
R9	1	1.5 kΩ	RES, 1.5 kΩ, 1%, 0.1 W	0402	CRCW06031K50FKEA	Vishay-Dale
R10, R11, R12	3	330 kΩ	RES, 330 kΩ, 1%, 0.25 W	1206	RC1206FR-07330KL	Yageo America
RV1, RV2, RV3	3	–	470 V, 10 kA varistor	20 mm disk	V20E300P	Littelfuse
TP1	1	–	Test point, multipurpose, black, TH	–	5011	Keystone Electronics
U1	1	–	TPSF12C1 common-mode active filter	SOT23-THIN (14)	TPSF12C1DYYR	Texas Instruments
U2	1	–	TPS7A4901 36 V, 150 mA LDO with high PSRR	MSOP (8)	TPS7A4901DGNR	Texas Instruments

4.3 PCB Layout

Figure 4-2 through Figure 4-8 show the PCB layout images, including 3D views, copper layers, assembly drawings, and layer stackup diagram. The PCB is 62-mils standard thickness with 2-oz copper thickness on top and bottom layers. Review the *Altium* source files for more detail.

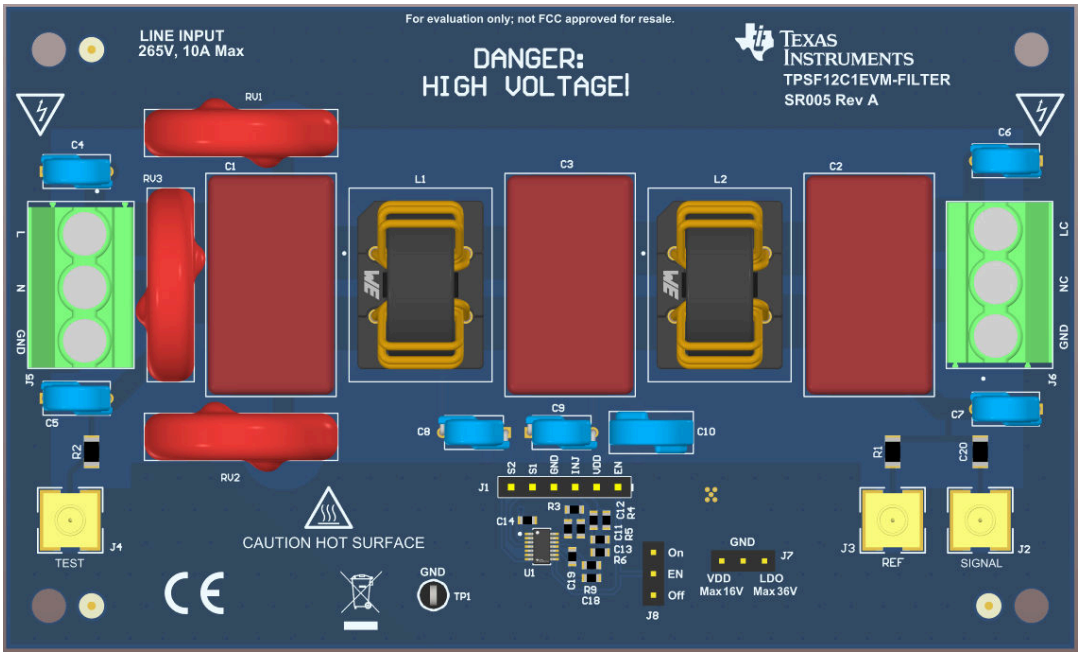


Figure 4-2. 3D Top View

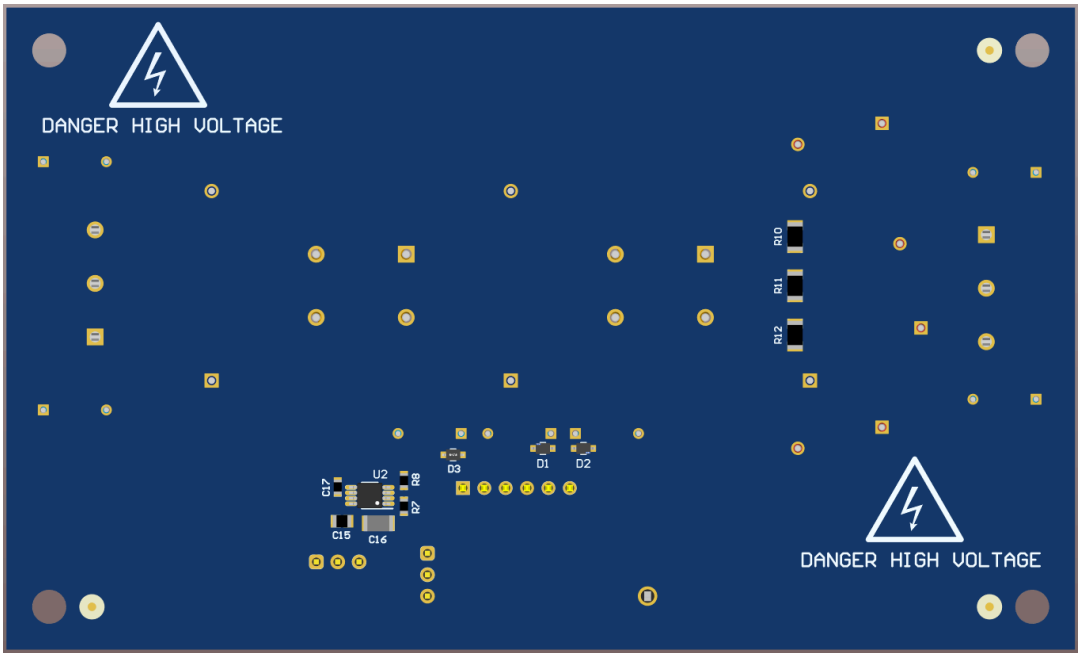


Figure 4-3. 3D Bottom View

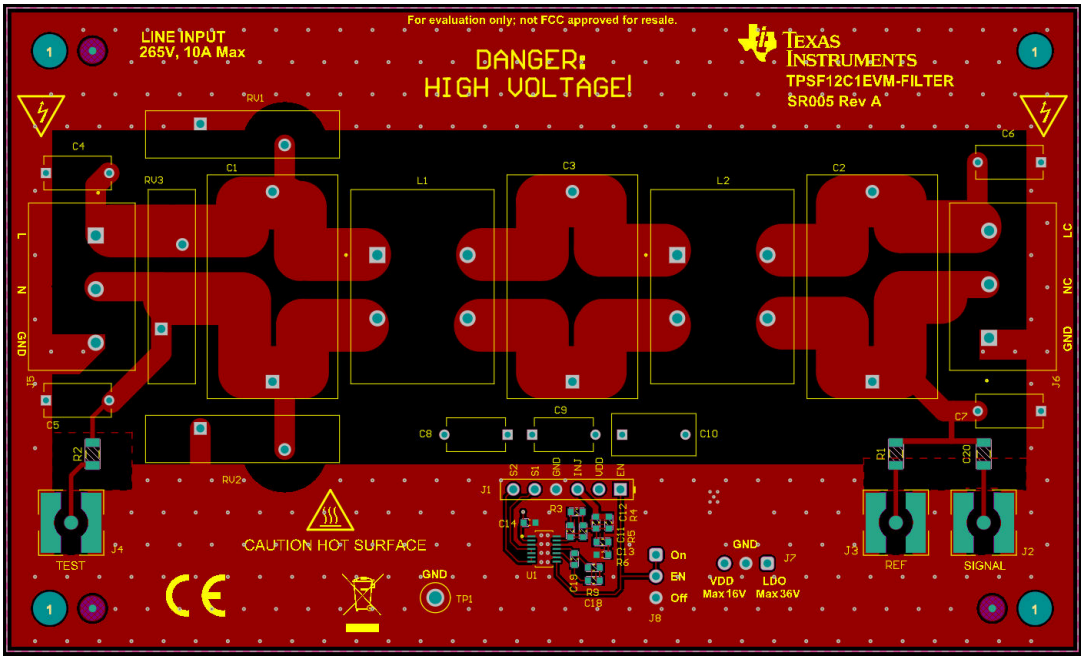


Figure 4-4. Top Layer Copper

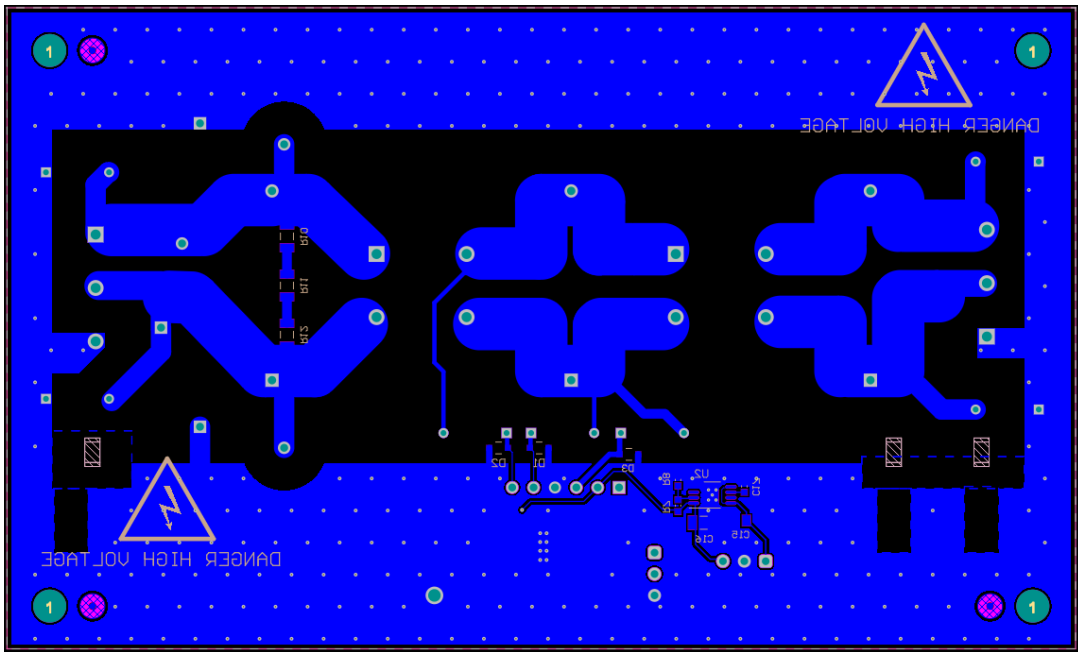


Figure 4-5. Bottom Layer Copper (Viewed From Top)

4.3.1 Assembly Drawings

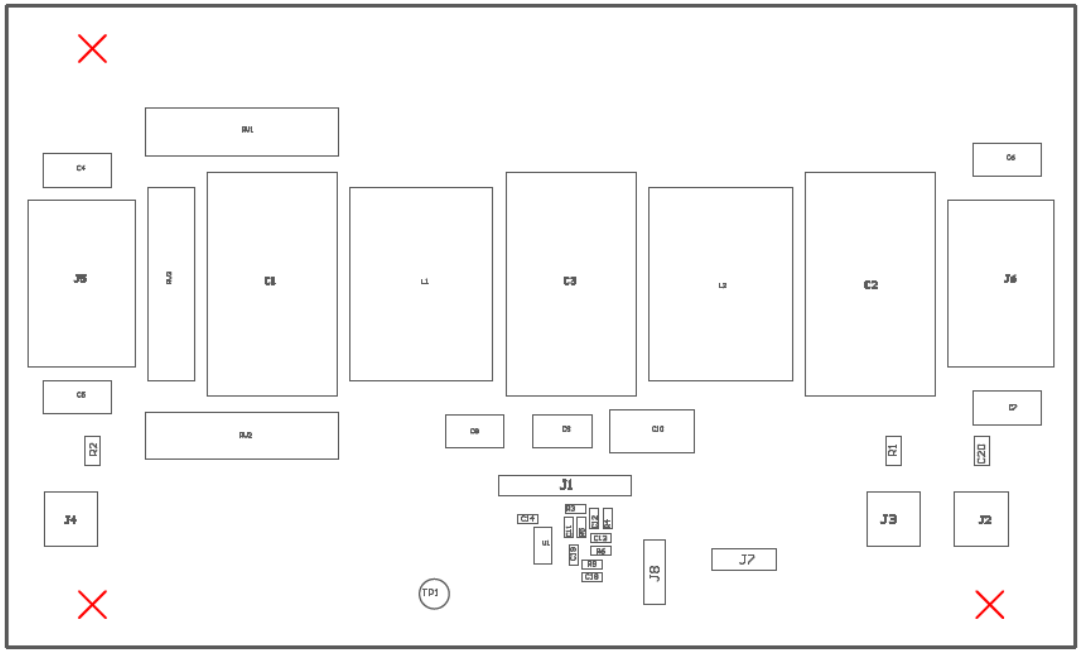


Figure 4-6. Top Assembly (Top View)

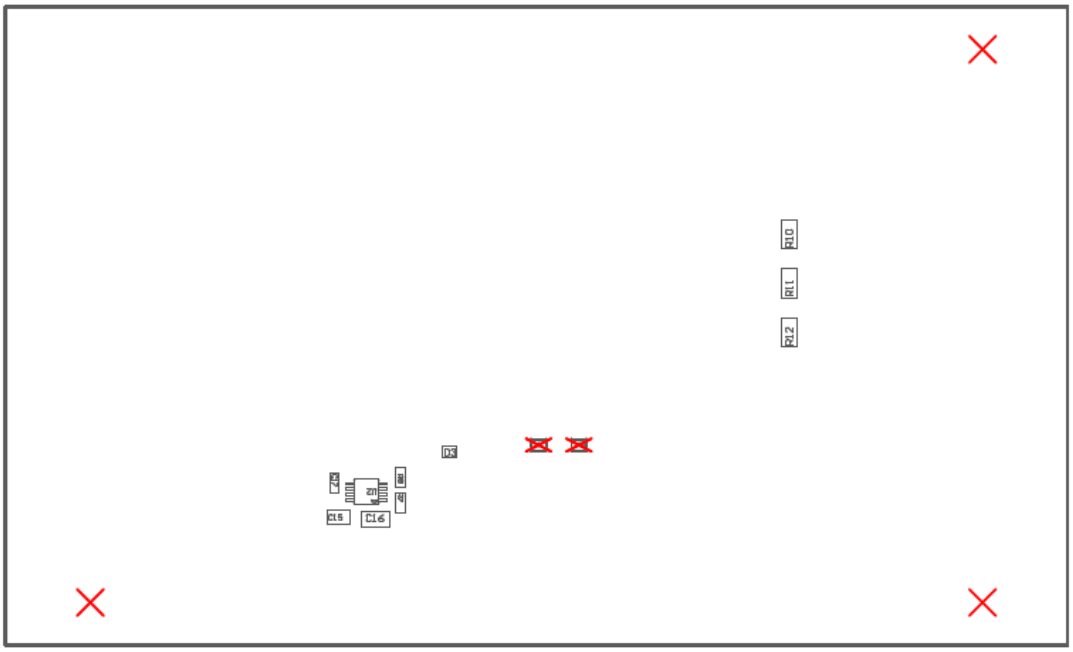


Figure 4-7. Bottom Assembly (Bottom View)

4.3.2 Multi-Layer Stackup

#	Name	Type	Material	Weight	Thickness	Dk
	Top Overlay	Overlay				
	Top Solder	Solder Mask	Solder Resist		0.4mil	3.5
1	Top Layer	Signal		2oz	2.756mil	
	Dielectric 1	Core	FR-4 High Tg		56mil	4.2
2	Bottom Layer	Signal		2oz	2.756mil	
	Bottom Solder	Solder Mask	Solder Resist		0.4mil	3.5
	Bottom Overlay	Overlay				

Figure 4-8. Layer Stackup

5 Compliance Information

5.1 Compliance and Certifications

- TPSF12C1EVM-FILTER EU Declaration of Conformity (DoC) for Restricting the use of Hazardous Substances (RoHS)

6 Additional Information

Trademarks

All trademarks are the property of their respective owners.

7 Related Documentation

7.1 Supplemental Content

For related documentation, see the following:

- Texas Instruments power-supply filter ICs
- Texas Instruments, press release *TI pioneers the industry's first stand-alone active EMI filter ICs, supporting high-density power supply designs*
- White Papers:
  - Texas Instruments, *How Active EMI Filter ICs Mitigate Common-Mode Emissions and Save PCB Space in Single- and Three-Phase Systems*
  - Texas Instruments, *An Overview of Conducted EMI Specifications for Power Supplies*
  - Texas Instruments, *An Overview of Radiated EMI Specifications for Power Supplies*
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *How a stand-alone active EMI filter IC shrinks common-mode filter size* technical article

To view a related EVM for the TPSF12C1 single-phase AEF device, see the TPSF12C1QEVM single-phase stand-alone active EMI filter EVM for CM noise mitigation.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2023) to Revision A (July 2023)	Page
• Added *AEF Design Flow* section	9
• Added thermal image	12
• Added *SENSE and INJ Voltages*	14
• Added insertion loss plot	14

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