

User's Guide

LMX2820EVM Evaluation Module



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ABSTRACT

The LMX2820EVM is designed to evaluate the performance of LMX2820. This board consists of a LMX2820 device.

The LMX2820 is a high-performance wideband synthesizer that can generate any frequency from 44.14 MHz to 22.6 GHz. The device runs from a single 3.3-V supply and has integrated LDOs that eliminate the need for onboard low noise LDOs.

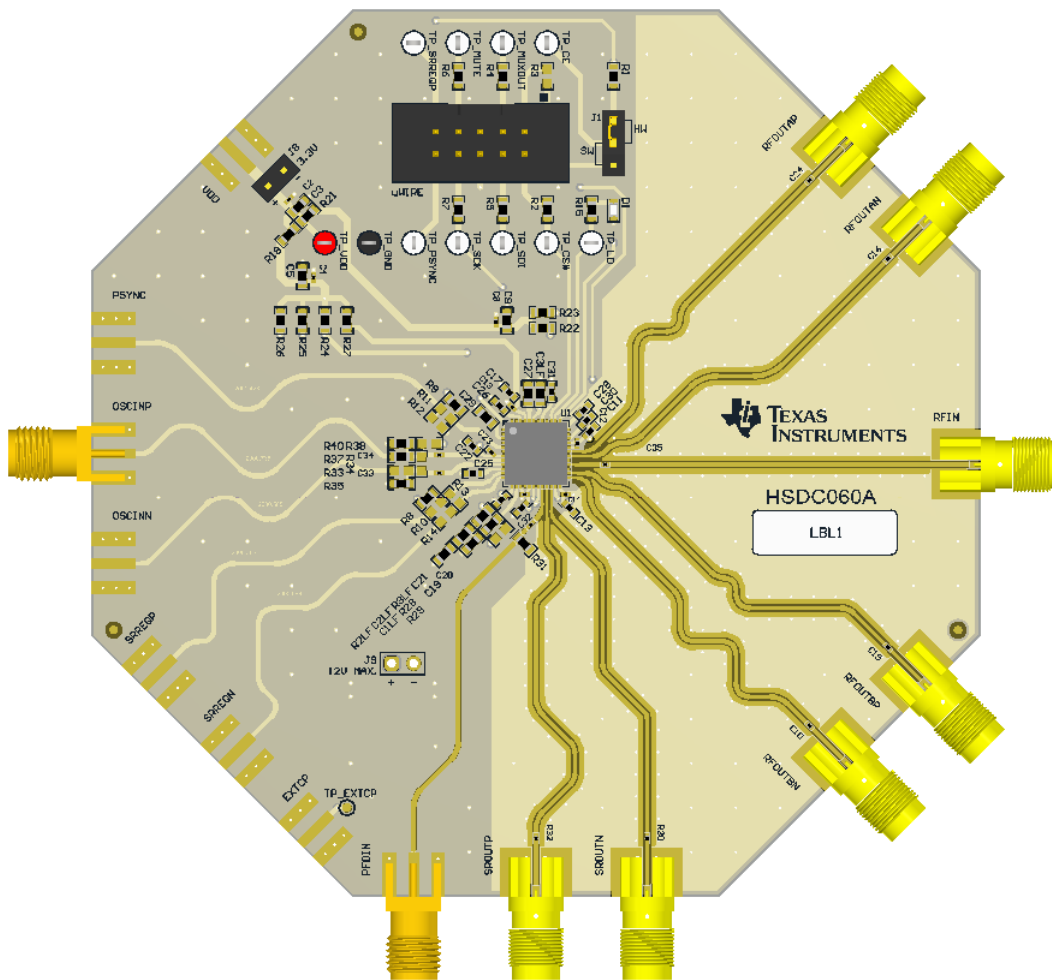


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1 Trademarks

PLLatinum™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

2 LMX2820EVM Evaluation Module

2.1 Evaluation Module Contents

In the box, there is:

- One LMX2820EVM board (HSDC060-001)
- One USB2ANY (HPA665)
- One USB cable
- One 10-pin ribbon cable

2.2 Evaluation Setup Requirement

The evaluation requires the following hardware and software:

- A DC power supply
- A spectrum analyzer or a signal analyzer
- A PC running Windows 7 or more recent version
- An oscilloscope (optional)
- A high quality signal generator (optional)
- Texas Instruments Clocks and Synthesizers TICS Pro software
- Texas Instruments PLLatinum™ Simulator Tool (optional)

2.3 Resources

Related evaluation and development resources are as follows:

- [TICS Pro software](#)
- [PLLatinum Simulator Tool](#) (PLL Sim)

3 Setup

3.1 Connection Diagram

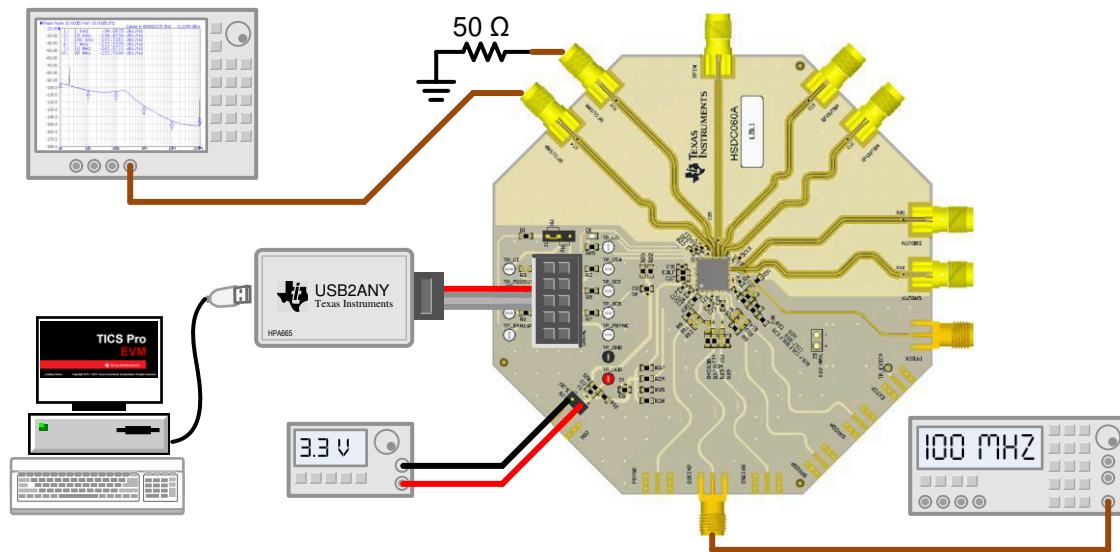


Figure 3-1. EVM Connection Diagram

3.2 Power Supply

Apply 3.3 V to the J8 header. The acceptable supply voltage range is 3.2 V to 3.4 V.

3.3 Reference Clock

Connect the OSCINP SMA connector to a high-quality, 100-MHz signal source. The OSCINN SMA connector can be left open because the OSCIN_N pin is terminated onboard.

The EVM is configured for single-ended input with the OSCIN_P pin connected to the OSCINP SMA connector and the OSCIN_N pin 50-Ω terminated onboard. If required, the EVM can be modified to operate with a different clock source in a different configuration. See [Appendix A](#) for more details.

3.4 RF Output

Connect either the RFOUTAP or RFOUTAN SMA connector to a signal analyzer. The unused connector must be terminated with a 50-Ω resistor or SMA load. Output frequency is 6 GHz and the amplitude is about +3 dBm.

By default, the TICS Pro evaluation software has RFOUTB power down. These SMA connectors can be left open.

3.5 Programming

Connect the ribbon cable from the USB2ANY to the LMX2820EVM.

Connect the USB cable from a PC to USB port in the USB2ANY. This provides power supply to the USB2ANY and communication with the TICS Pro. A firmware update may be required. See [Appendix B](#) for more details.

3.6 Evaluation Software

Download and install TICS Pro to a PC.

Run the software and follow these steps to start the program.

1. Go to **Select Device** → **PLL + VCO** → **LMX2820**.

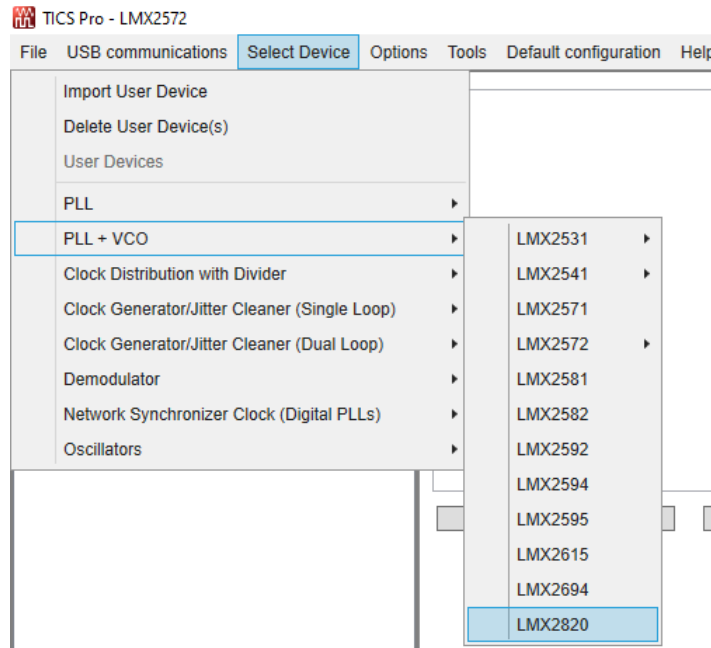


Figure 3-2. Select Device in TICS Pro

2. The "ReadMe" page will load. Please take a minute to read the content to have a basic understanding of the GUI.
3. Go to **Default Configuration** → **EVM Default Mode**.

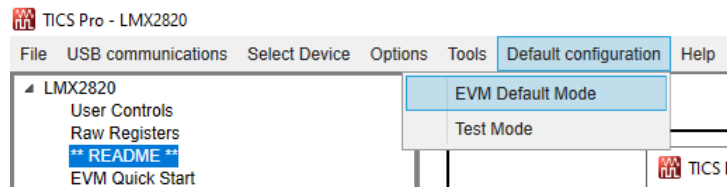


Figure 3-3. Default Mode

4 Typical Measurement

4.1 Default Configuration

4.1.1 Loop Filter

The parameters for the loop filter are listed in [Table 4-1](#).

Table 4-1. Loop Filter Configuration

PARAMETER	VALUE
C1_LF	470 pF
C2_LF	68 nF
C3_LF	2.2 nF
R2_LF	68.1 Ω
R3_LF	18.2 Ω

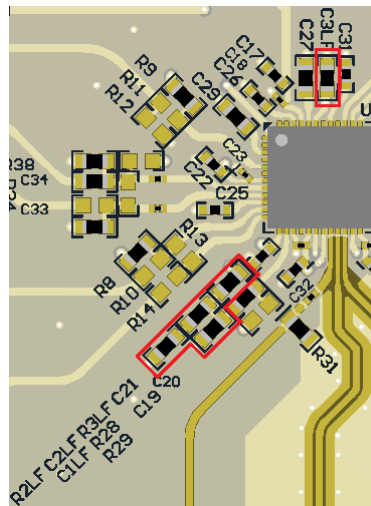


Figure 4-1. Loop Filter

4.1.2 Typical Output

1. Follow [Section 3](#) to set up the evaluation.
2. Click **Write All Registers** to write all the registers to LMX2820.

The default output is 6 GHz.

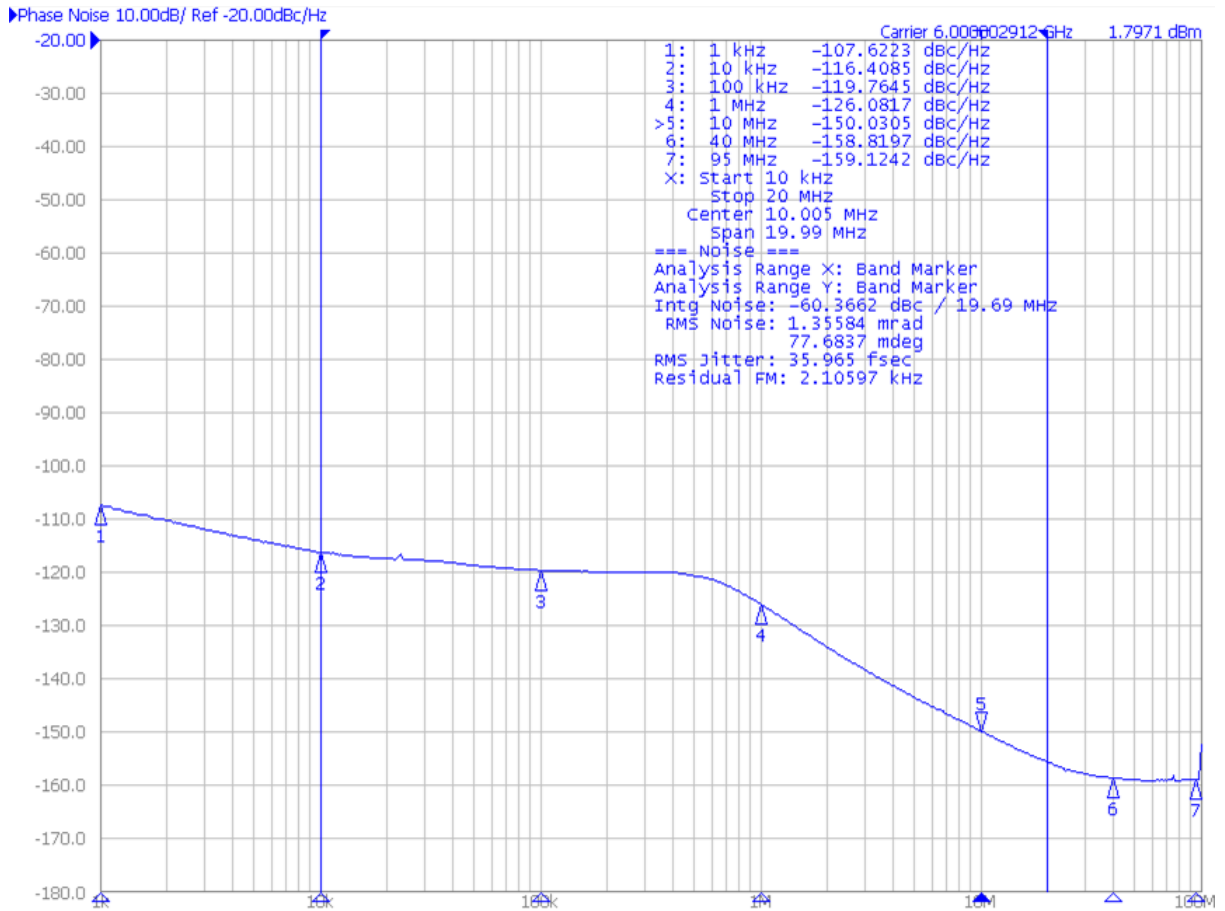


Figure 4-2. Default Output

4.2 Additional Tests

4.2.1 SYSREF Example

The SROUT of LMX2820 can be used to generate or duplicate SYSREF signal. The output of SROUT can be a single pulse, series of pulse, or a continuous stream of pulses. These pulses are synchronous with the RFOUT signal with an adjustable delay. To use the SYSREF capability, the PLL must be in phase SYNC mode with PHASE_SYNC_EN = 1. Here is an example of Pulsed mode.

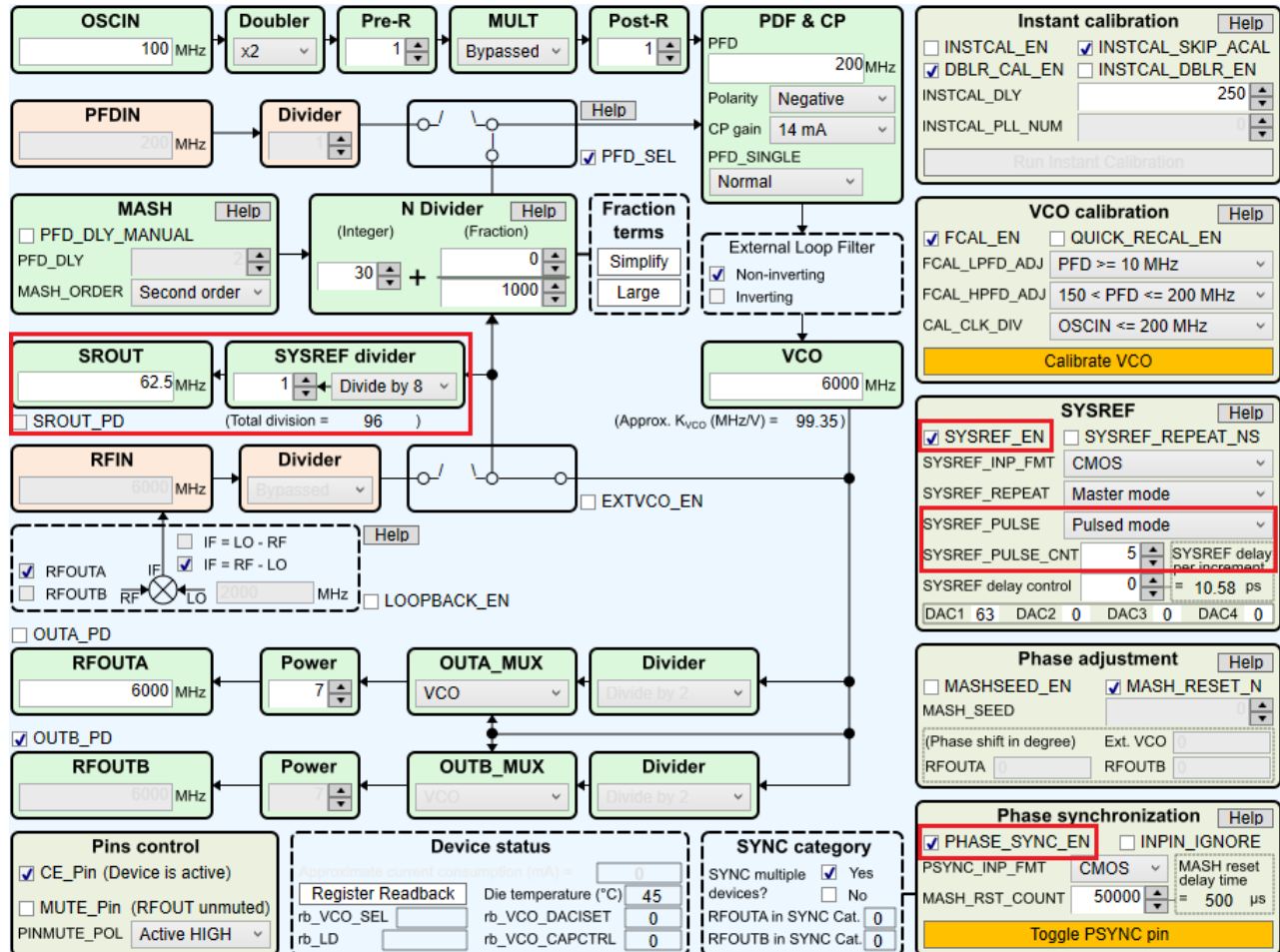


Figure 4-3. SYSREF Pulsed Mode Setting

4.2.2 Offset Mixing With PFDIN Pin

The LMX2820 supports offset mixing with PFDIN pin. In this mode, the internal N divider is bypassed.

When using offset mixing with PFDIN pin, the phase detector must operate with a single PFD. As a result, the charge pump current is equal to half the current setting made in register CPG.

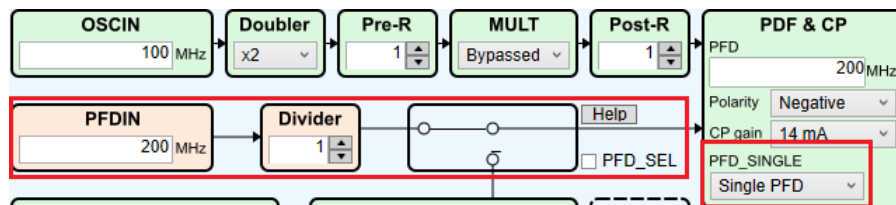


Figure 4-4. Offset Mixing With PFDIN Pin Setting

4.2.3 External VCO Mode

In addition to the internal VCO, LMX2820 also support working with an external VCO. The polarity of the phase detector has to be set properly to match with the actual Vtune characteristic. The LMX2820EVM offers various options to implement passive or active loop filter onboard.

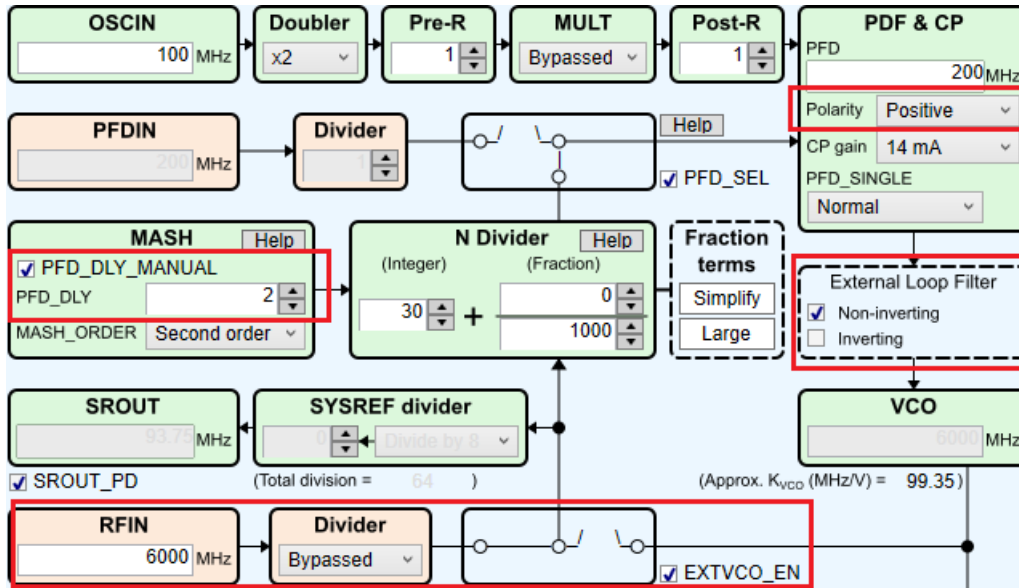


Figure 4-5. External VCO Mode Setting

4.2.4 Register Readback

To read back the written register values, follow these steps:

1. Click the Register Name that you want to read back.
2. Click **Read Register** to read back the register value.

Register Map		2 2 2 2 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0																									
Register Name	Address/Value	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		
R75	0x4B0000	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R74	0x4A0000	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R73	0x490000	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R72	0x480000	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R71	0x470000	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R70	0x46000E	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R69	0x450001	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Data: 0x4A0000

Write Register

Read Register

Read All Registers

Figure 4-6. Register Readback

5 Schematic

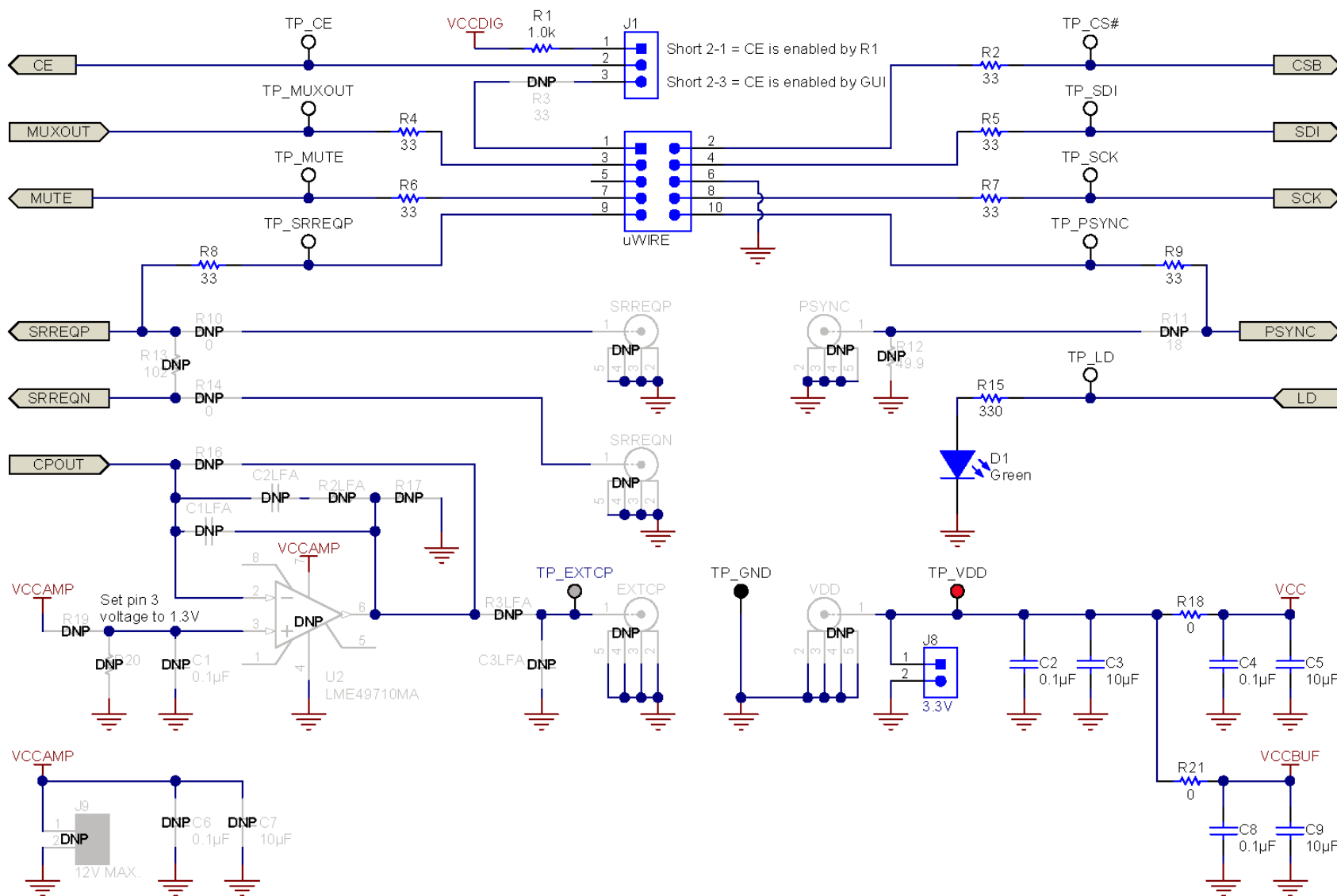


Figure 5-1. LMX2820EVM Schematic (Page 1)

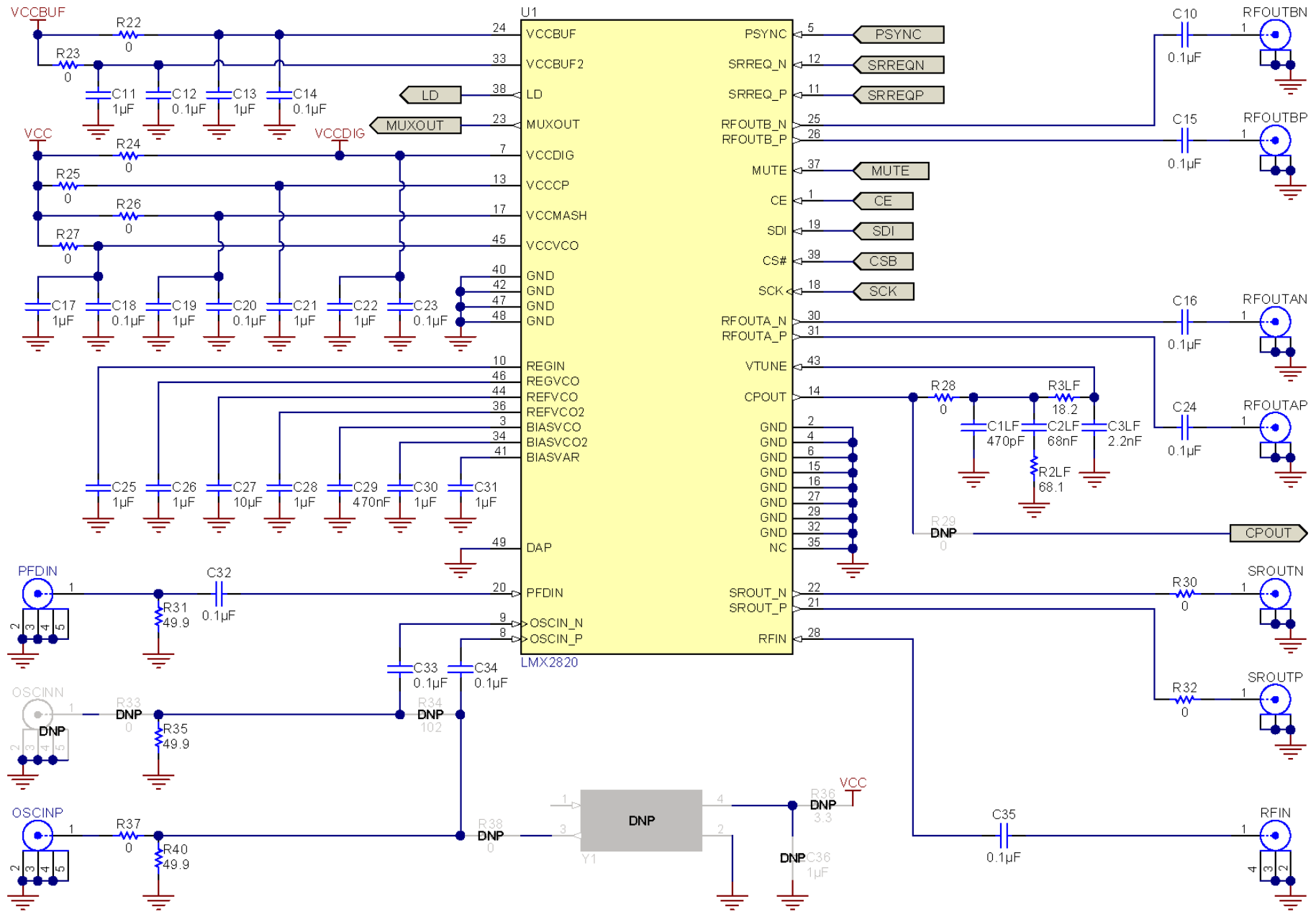


Figure 5-2. LMX2820EVM Schematic (Page 2)

6 PCB Layout and Layer Stack-Up

6.1 PCB Layer Stack-Up

The top layer is 1-oz. copper.

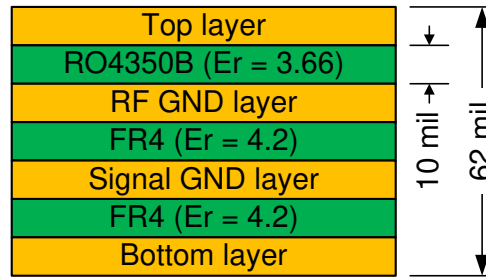


Figure 6-1. PCB Layer Stack-Up

6.2 PCB Layout

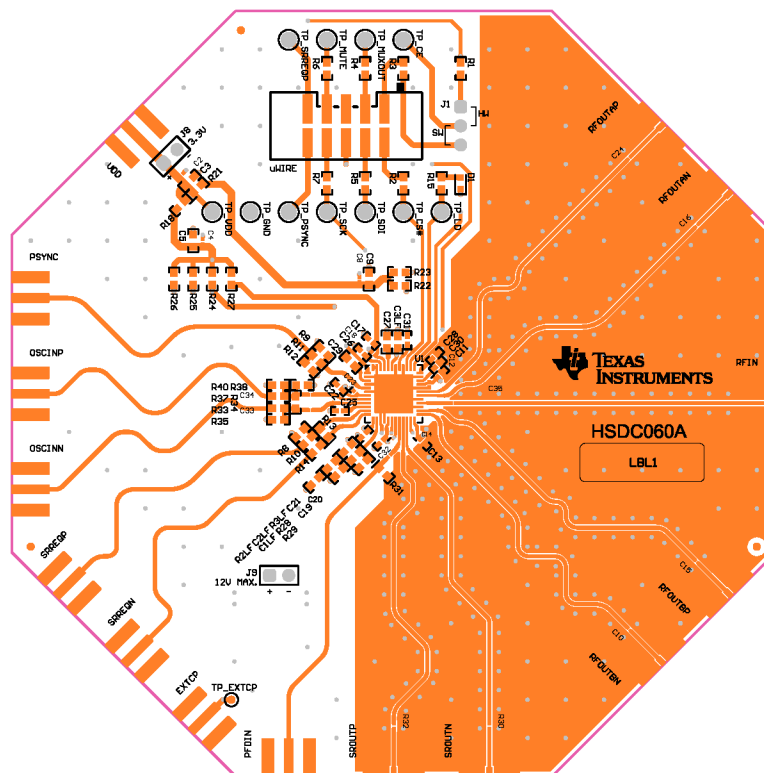


Figure 6-2. Top Layer

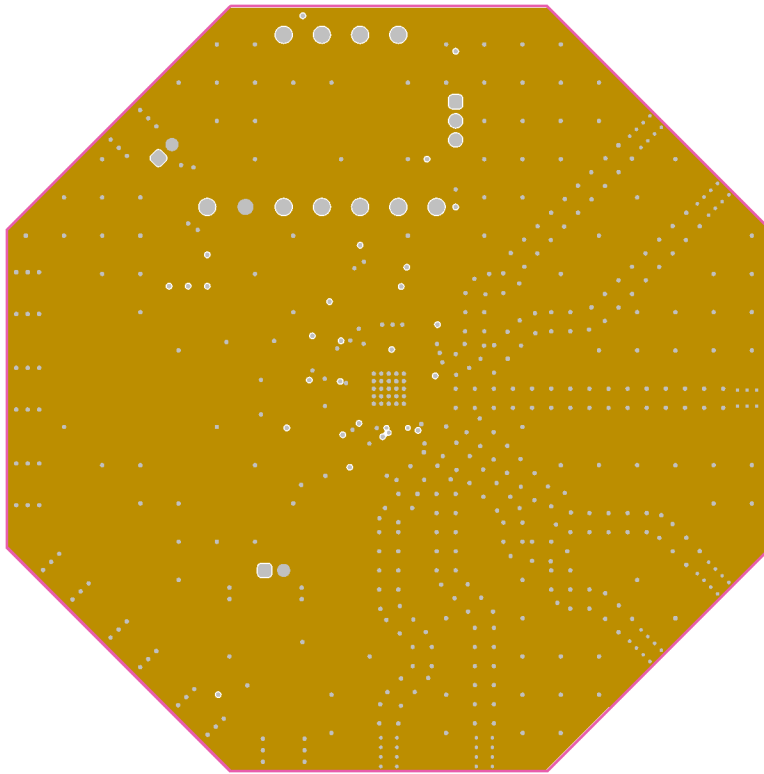


Figure 6-3. RF GND Layer

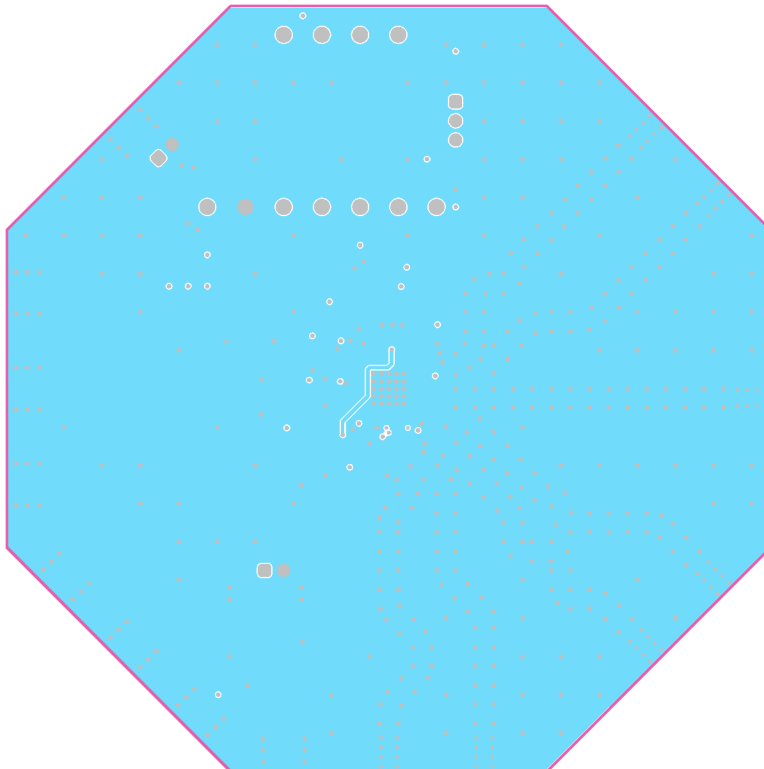


Figure 6-4. Signal GND Layer

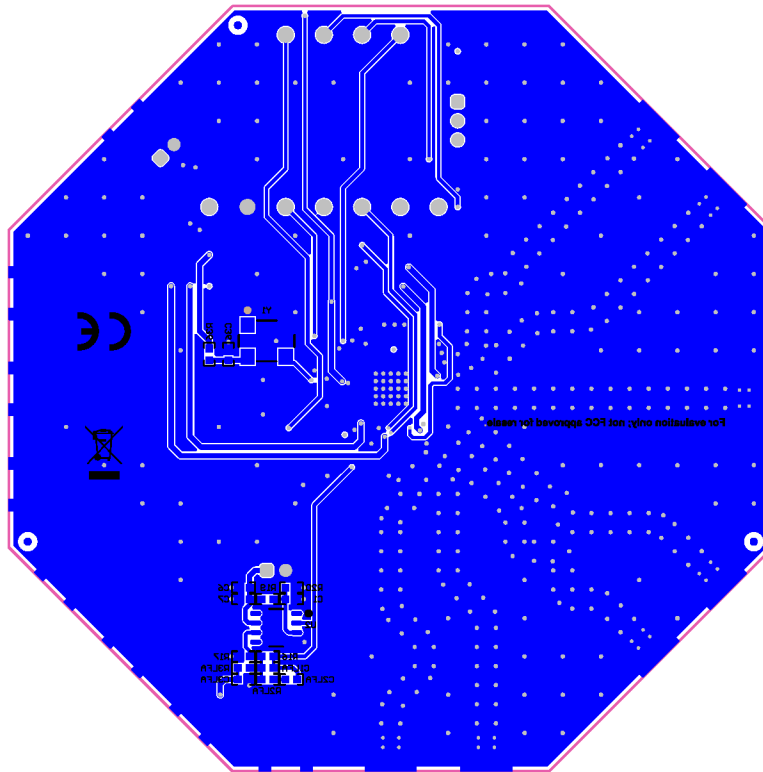


Figure 6-5. Bottom Layer

7 Bill of Materials

Table 7-1. Bill of Materials

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C1LF	1	CAP, CERM, 470 pF, 10 V,+/- 5%, C0G/ NP0, 0603	885012006012	Wurth Elektronik
C2, C4, C8, C12, C14, C18, C20, C23, C32, C33, C34	11	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X5R, 0201	GRM033R61C104K E84D	MuRata
C2LF	1	CAP, CERM, 0.068 µF, 25 V,+/- 10%, X7R, 0603	885012206070	Wurth Elektronik
C3, C5, C9, C27	4	CAP, CERM, 10 µF, 10 V,+/- 10%, X5R, 0603	GRM188R61A106K AALD	MuRata
C3LF	1	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0603	885012206036	Wurth Elektronik
C10, C15, C16, C24, C35	5	CAP, CERM, 0.1 µF, 10 V,+/- 10%, X5R, 0201	530Z104KT10T	American Technical Ceramics
C11, C13, C17, C19, C21, C22, C25, C26, C28, C30, C31	11	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0402	GRM155R61E105K A12D	MuRata
C29	1	CAP, CERM, 0.47 µF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E3X7R1E474 K080AB	TDK
D1	1	LED, Green, SMD	LTST-C190GKT	Lite-On
J1	1	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
J2	1	Header (shrouded), 100mil, 5x2, Gold, SMT	52601-S10-8LF	FCI
J8	1	Header, 100mil, 2x1, Gold, TH	TSW-102-07-G-S	Samtec
J10, J11, J12, J13, J15, J16, J19	7	JACK, SMA, 50 Ohm, Gold, Edge Mount	142-0771-831	Cinch Connectivity
J14, J18	2	CONN SMA JACK STR EDGE MNT	CON-SMA-EDGE-S	RF Solutions Ltd.
R1	1	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00JN EA	Vishay-Dale EA
R2, R4, R5, R6, R7, R8, R9	7	RES, 33, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333R0JN EA	Vishay-Dale EA
R2LF	1	RES, 68.1, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060368R1FK EA	Vishay-Dale EA
R3LF	1	RES, 18.2, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060318R2FK EA	Vishay-Dale EA
R15	1	RES, 330, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333R0JN EA	Vishay-Dale EA
R18, R21, R22, R23, R24, R25, R26, R27, R28, R37	10	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0 EA	Vishay-Dale EA
R30, R32	2	RES, 0, 5%, 0.05 W, 0201	CRCW02010000Z0 ED	Vishay-Dale ED
R31, R35, R40	3	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060349R9FK EA	Vishay-Dale EA
SH-J1	1	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9	Test Point, Miniature, White, TH	5002	Keystone
TP11	1	Test Point, Miniature, Black, TH	5001	Keystone
TP12	1	Test Point, Miniature, Red, TH	5000	Keystone
U1	1	RF Synthesizer	LMX2820	Texas Instruments

8 Troubleshooting Guide

If the EVM does not work as expected, use [Figure 8-1](#) to identify potential root causes. Consider the following:

- Do not make modifications to the EVM or change the default settings until AFTER it is verified to be working.
- Register read back requires the correct software setup. See [Section 4.2.4](#) for details.
- The POR current of the LMX2820EVM is approximately 220 mA.
- The power-down current of the LMX2820EVM is approximately 10 mA.

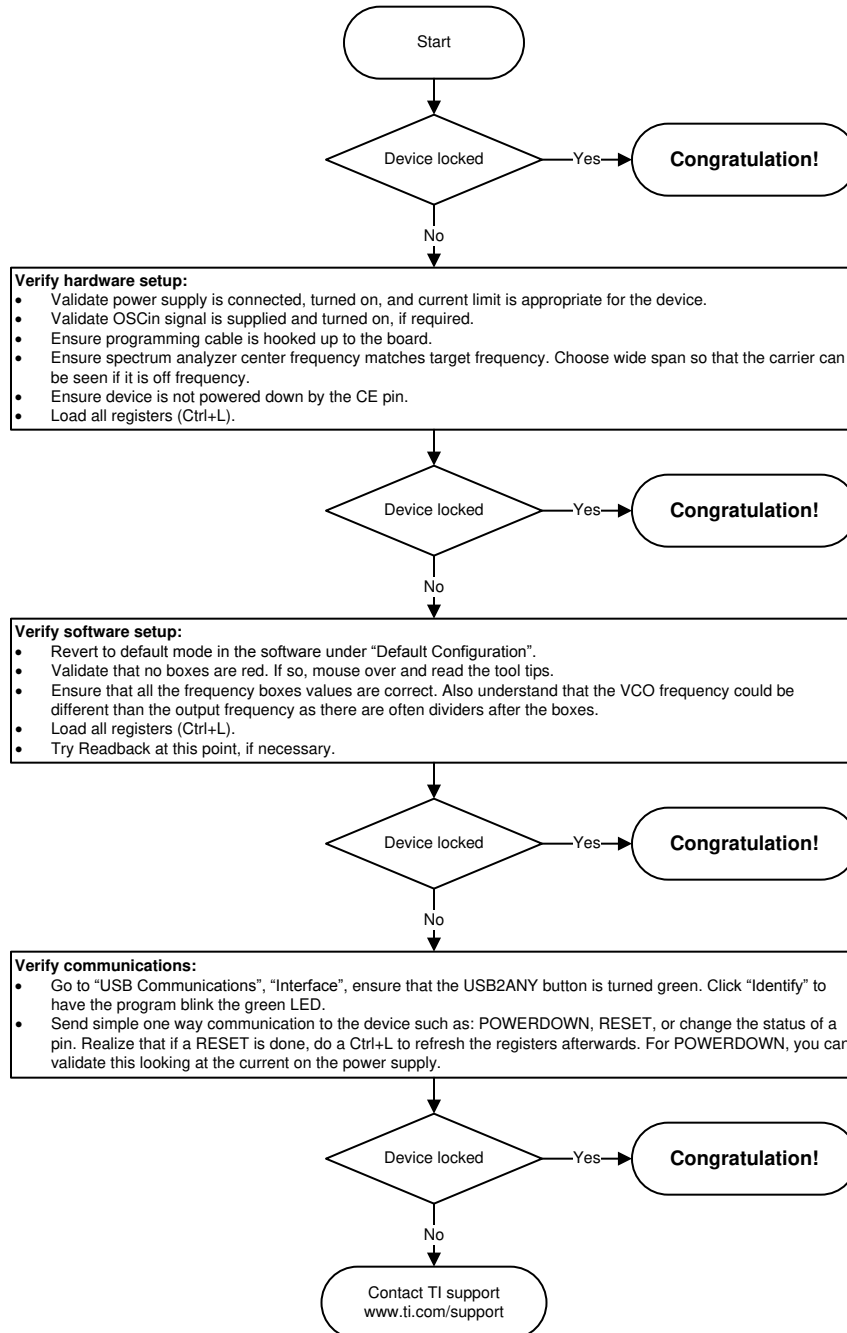
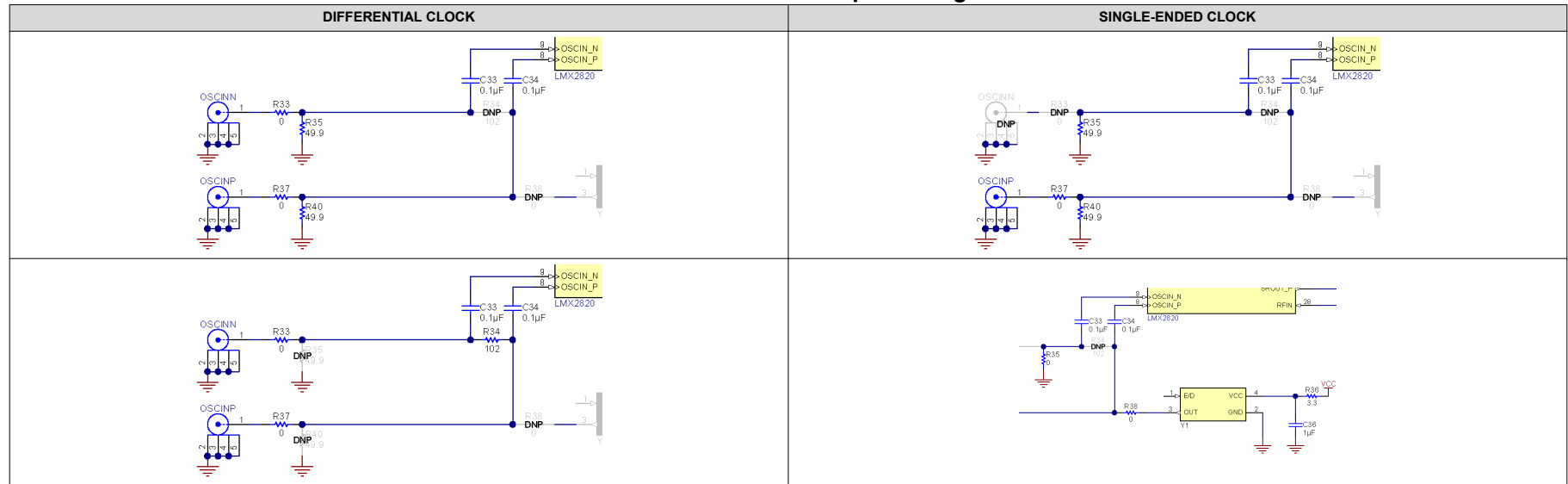


Figure 8-1. Troubleshooting Guide

A Using Different Reference Clock

These are the different options to provide a reference clock to LMX2820EVM. By default, the EVM is configured for an external single-ended clock.

Table A-1. Reference Clock Input Configuration



B USB2ANY Firmware Upgrade

Usually when the USB2ANY module is used the first time, TICS Pro will request a firmware update. Follow the pop-up instructions to complete the update. This is necessary to ensure that the USB connection between the PC and the USB2ANY module is properly set up, otherwise the programming to LMX2820EVM will not be successful.

1. When the *USB2ANY Firmware Requirement* pop-up window appears, click **OK** to continue.

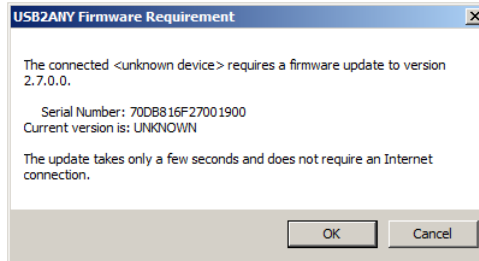


Figure B-1. Firmware Requirement

2. Next, follow the on-screen procedure shown in [Figure B-2](#).

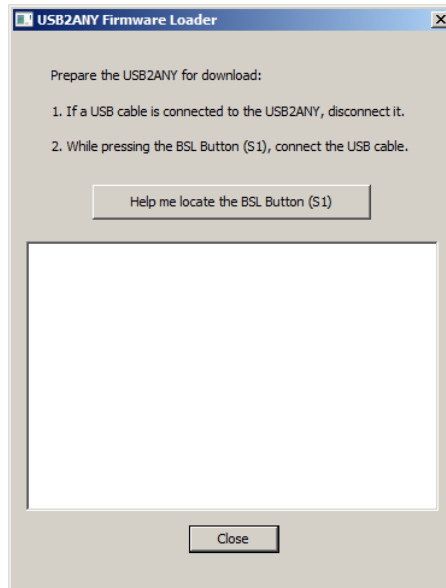


Figure B-2. Firmware Loader

3. If you do not know the location of the BSL button, click the **Help me locate the BSL Button (S1)** button to launch the *USB2ANY BSL Button (S1) Location* pop-up window.

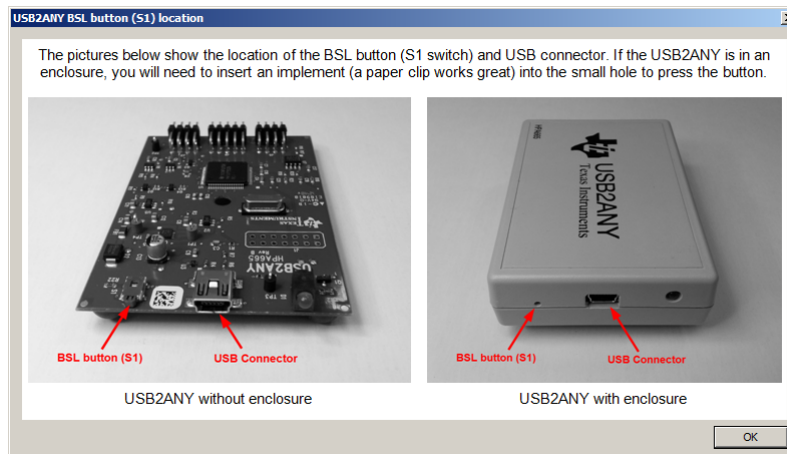


Figure B-3. BSL Button

- Click **OK** to close out of the *USB2ANY BSL Button (S1) Location* pop-up window and return to the previous screen. Follow the on-screen procedure until the *Update Firmware* screen appears.

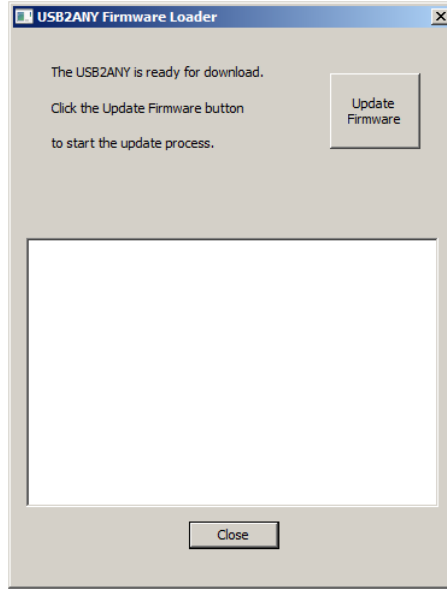


Figure B-4. Update Firmware

- Click **Upgrade Firmware** to start the firmware upgrade. Click **Close** after the upgrade is complete.

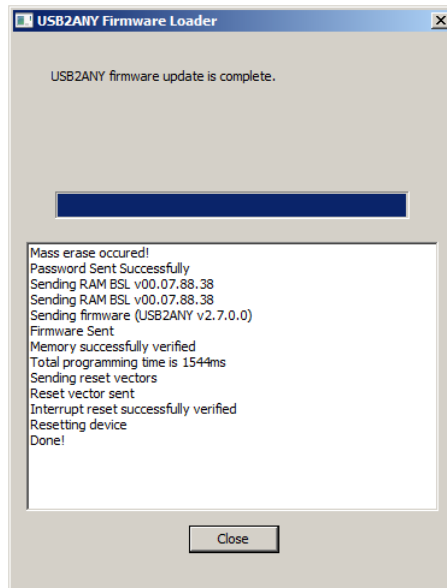


Figure B-5. Firmware Update Complete

- Go to **USB communications** → **Interface** in the TICS Pro software to check the USB connection. Make sure the *USB Connected* button is green.

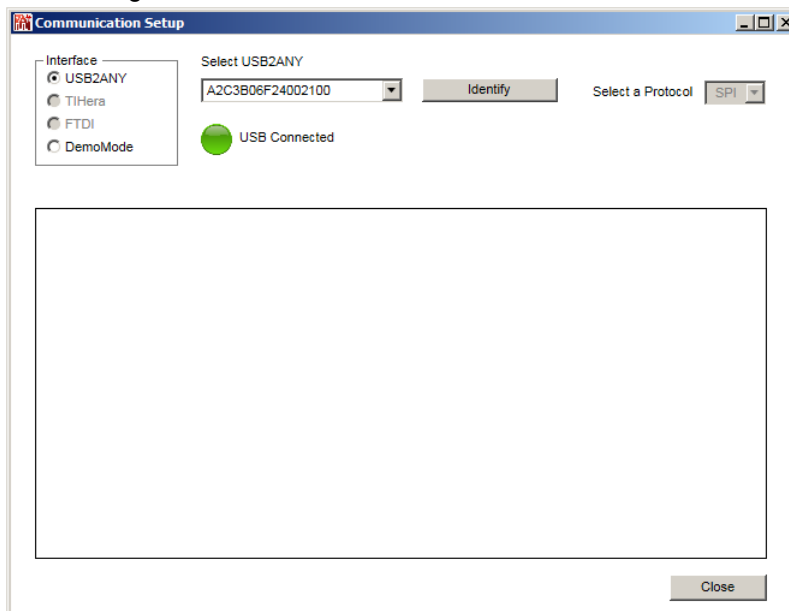


Figure B-6. USB Communications

C Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (January 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document. Updated the operating frequency range.....	1
• Updated graphics and added description to the ReadMe page to the <i>Evaluation Software</i> section.....	5
• Updated graphic in <i>SYSREF Example</i> section.....	8
• Updated graphic and changed external PFD mode to offset mixing with PFDIN pin in the <i>Offset Mixing With PFDIN Pin</i> section.....	8
• Updated graphic in <i>External VCO Mode</i> section.....	9

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