*User's Guide*
# LMK5C33414AEVM

**TEXAS INSTRUMENTS**

**ABSTRACT**

The LMK5C33414AEVM is an evaluation module for the LMK5C33414A Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping.

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## Trademarks
All trademarks are the property of their respective owners.

# 1 Introduction

**Overview**

The LMK5C33414AEVM is an evaluation module for the LMK5C33414AEVM Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping. The LMK5C33414A integrates three Analog PLLs (APLL) and three Digital PLLs (DPLL) with programmable loop bandwidth. The EVM includes SMA connectors for clock inputs, optional off-board APLL reference input, and clock outputs to interface the device with 50-Ω test equipment. The onboard TCXO allows for improved performance when using low DPLL loop bandwidths below 10 Hz and when evaluating holdover, locked, or free-run operational modes. The EVM can be configured through the onboard USB microcontroller (MCU) interface using a PC with TI's TICS Pro software graphical user interface (GUI). TICS Pro can be used to program the LMK5C33414A registers.

**Features**

* LMK5C33414AEVM

**What is Included**

* LMK5C33414AEVM
* 3-ft. mini-USB cable (MPN 3021003-03)

**What is Needed**

* Windows PC with TICS Pro Software GUI
* Test Equipment
  – DC power supply (12V, 1A for EVM Default setting or 5V, 2A for other settings in Table 3-2)

**What is Recommended**

* Test equipment:
  – Signal source analyzer
  – Signal generator / reference clock
  – Real-time oscilloscope
  – Precision frequency counter

Figure 1-1 shows the jumper position with red markings. Figure 1-1 shows the DIP switch positions in either green boxes (for ON) or red boxes (for OFF) in the appropriate location.
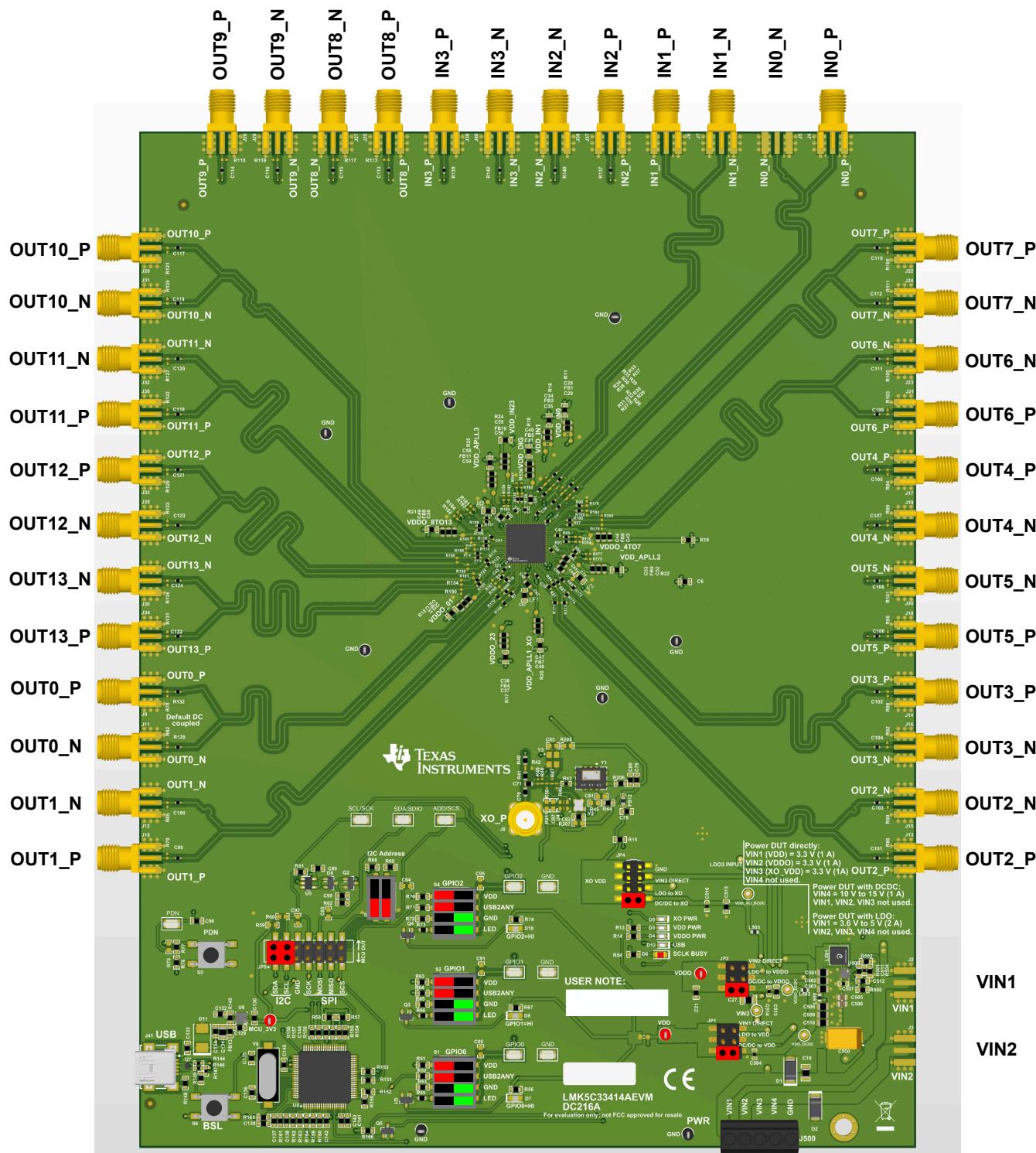


**Figure 1-1. LMK5C33414AEVM Default Setting of Jumpers and DIP Switches**

## 2 EVM Quick Start

Table 2-1 describes the default jumper positions for the EVM to power the device from a single 12-V supply provided to VIN4. In positional information about jumpers, "opposite designator" means the jumper is placed opposite of the silkscreen designator.

**Table 2-1. Default Jumper and DIP Switch Settings**

| CATEGORY | REFERENCE DESIGNATOR | POSITION | DESCRIPTION |
|---|---|---|---|
| Power | JP1 | 1-2 (opposite designator) | LMK5C33414A VDD = 3.3 V from DCDC provided by U500 on top of the PCB. |
| | JP2 | 1-2 (opposite designator) | LMK5C33414A VDDO = 3.3 V from DCDC provided by U500 on top of the PCB. |
| | JP4 | 1-2 (opposite designator) | XO VCC = 3.3 V DCDC provided by U500 on top of PCB. |
| Communication | JP5 | 1-2, 3-4 | Connect I$^2$C from onboard USB2ANY to LMK5C33414A |
| LMK5C33414A Control Pins | S3 | S3[1:2] = OFF | SCS_ADD = no pullup or pulldown. |
| | S1, S2, S4 | Sx[1,2] = OFF Sx[3,4] = ON | Enable 3.9 kΩ pulldown on GPIO0, GPIO1, and GPIO2 |

To begin using the LMK5C33414A, follow the steps below.

### Hardware Setup

1. Verify the EVM default jumper and DIP switch settings shown in Figure 1-1.
2. Connect the 12-V external power DC power supply (1-A limit) to:
   a. VIN4 and GND terminals on header J500 (pins 4 and 5, see Figure 3-2.)
3. Connect references:
   a. 156.25-MHz reference clock to IN0_P and/or,
   b. 10-MHzreference clock to IN1_P/N and/or,
   c. 25-MHz reference clock to IN2_P/N and/or,
   d. 1-PPS reference clock to IN3_P/N.
4. Connect the USB cable to the USB port at J41.

### Software Setup

1. If not already installed, install the TICS Pro software from the TI website: TICS Pro Software
2. If the MATLAB R2015b (9.0)* 64-bit Runtime is not already installed, download and install the software from the MathWorks website. While optional for programming and evaluating the default profile settings, Matlab Runtime is necessary for any application that needs to modify the DPLL loop filter settings. See Matlab Runtime.
3. Start the TICS Pro software.
4. Select the LMK5C33414A profile from *Select Device → Network Synchronizer Clock (Digital PLLs) → LMK5C33414A*.
5. Confirm communications with the board by:
   a. Click *USB communications* from the menu bar.
   b. Click *Interface* to launch the *Communication Setup* pop-up window.
   c. Check these fields in the *Communication Setup* pop-up window:
      i. Make sure USB2ANY is selected as the interface.
      ii. In case of multiple USB2ANY, select desired interface. If a USB2ANY is currently in use in another TICS Pro, then the user must release that interface by changing the interface setting to *DemoMode*.
      iii. Click *Identify* to trigger the LED shown in the image below. A blinking LED confirms the connection to the board. Be aware that USB2ANY devices connected to the PC but not attached to by a TICS Pro instance blink at a slow rate of 1 second on, 1 second off, continuously. After clicking the *Identify* button, the LED flashes quickly at about 0.5 seconds on, 0.5 seconds off, for about 5 seconds.
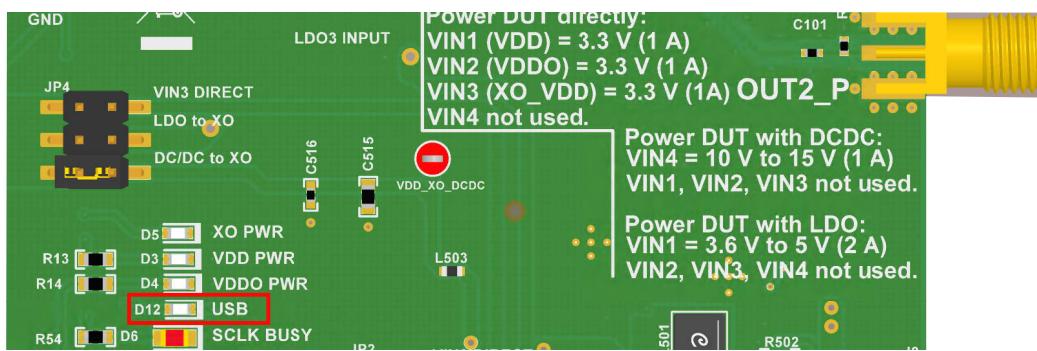
**Figure 2-1. USB LED**

### Program the LMK5C33414A

1. Toggle the switch S5 (PDN/RESET).
2. Program all the registers:
   a. Press the *Write All Regs* button in the toolbar.
   b. Select *USB Communications* in the menu bar, then select *Write All Registers*, or press Ctrl + L.
3. Check the current consumption.
4. Check LMK5C33414A Status as shown in Figure 2-2.
   a. Go to the *Status* page of the GUI.
   b. Click *Read Status Bits*.
   c. Make sure to clear the latched bits. To clear latched bits:
      i. Press the *Clear Latched Bits* button.
      ii. Select *Read Status Bits*.
   d. Wait to confirm the change. The DPLL status bits can take time to reflect the lock.



**Figure 2-2. Read Status Bits**

### Measure

Measurements can now be made at the clock outputs.

## 3 EVM Configuration

The LMK5C33414A is a highly-configurable clock chip with multiple power domains, PLL domains, and clock input and output domains. To support a wide range of LMK5C33414A use cases, the EVM was designed with more flexibility and functionality than needed to implement the chip in a customer system application.

This section describes the power, logic, and clock input and output interfaces on the EVM, as well as how to connect, set up, and operate the EVM. Refer to Figure 3-1.

**Table 3-1. Key Components Reference Designators and Descriptions**

| ITEM NO. | | REFERENCE DESIGNATORS | DESCRIPTION |
|---|---|---|---|
| 1 | | U1 | LMK5C33414A |
| 2 | | J500 (VIN4 terminal block header) | External Supply, +12 V using default configuration. |
| 3 | A | Y1 | Onboard TCXO. Y1 provides improved holdover stability and allow narrower DPLL loop bandwidths to be used in comparison to the external XO input. |
| | B | J8 | SMA connector for external XO. To use the external XO, remove the jumper from JP4 to power down the on-board TCXO. |
| 4 | | J4/5, J6/7, J37/J39, J40/J38 | SMA Ports for Clock Inputs (IN0_P/N, IN1_P/N, IN2_P/N, and IN3_P/N). IN0_N is not populated and IN0_P is configured for single ended input. IN1 is configured for a DC-coupled differential input. IN2 and IN3 are configured for an AC-coupled differential input. |
| 5 | | J9/11, J10/12, J13/15, J14/16, J17/19, J18/20, J21/J23, J22/24, J25/27, J26/28, J29/31, J30/32, J33/35, J34/36 | SMA Ports for Clock Outputs |
| 6 | | S5 | Normally open. Push button for device power down (PD# pin). R76 enables control of the PD# pin through the GUI. If GUI has PD# unchecked on User Controls page under PINS section, then the device is held in power-down condition no matter state of S5. R76 is installed by default. |
| 7 | | JP5 | Jumper header for I$^2$C/SPI interface (MCU to LMK5C33414A) |
| 8 | | D6 | SCL or SCK busy indication LED. |
| 9 | | J41 | USB Port for MCU |
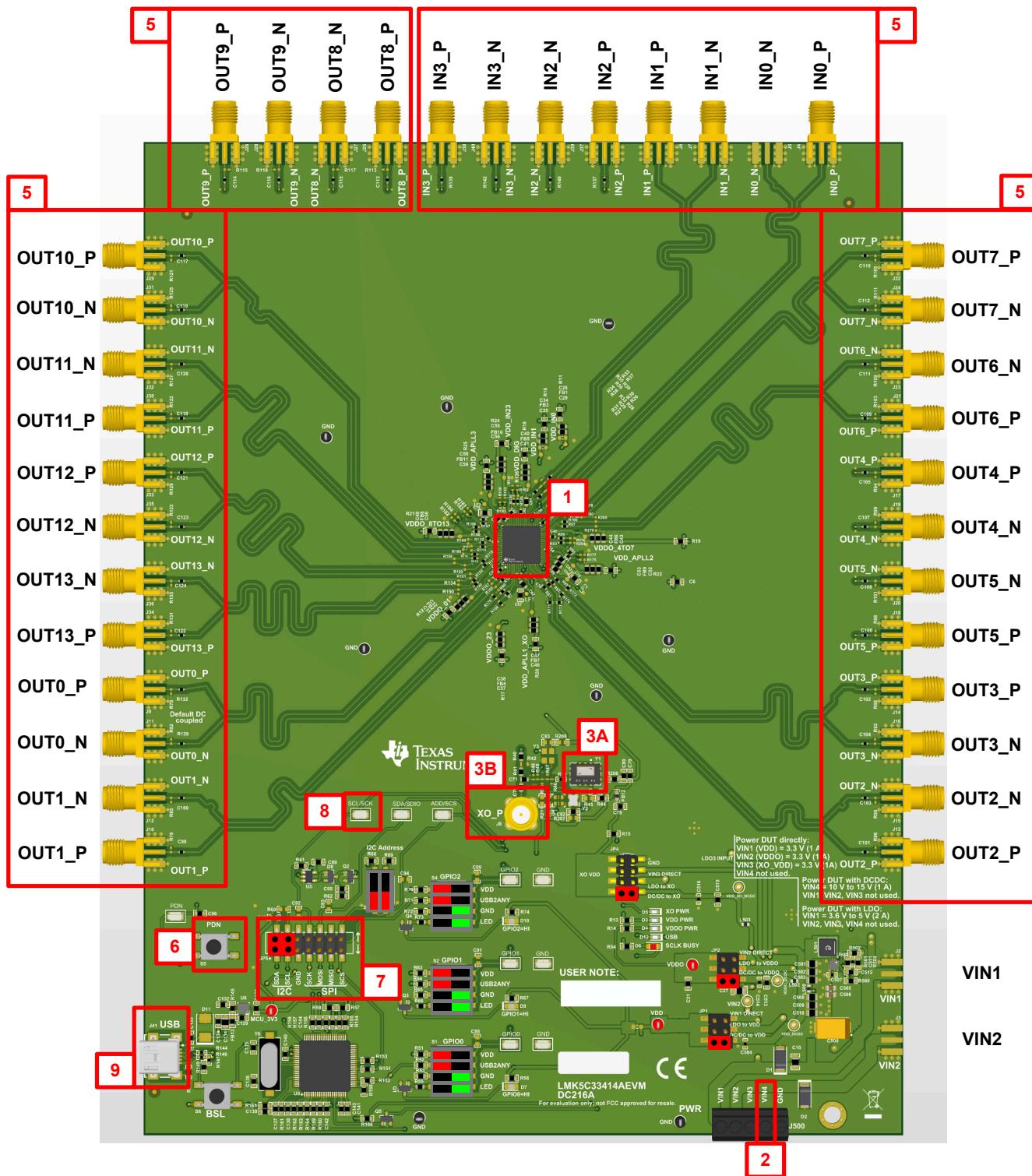
**Figure 3-1. Key Components - EVM Top Side**

## 3.1 Power Supply

The LMK5C33414A has VDD and VDDO supply pins that operate from 3.3 V ± 5%.

J500 is the main power terminal to the external power supply. Power SMA port VIN1 (J2) provides an alternative connector style to apply power through coax cable. By default this SMA connector is not populated.

On the EVM, there are three methods for supplying power.

1. The default power configuration uses the onboard DC/DC supply (U500) to power all VDD and VDDO pins as well as the onboard XO from an external 12-V supply input to VIN4 on J500.
2. The LDO power configuration uses three separate LDO regulators (U9, U10, and U11) to power the VDD, VDDO, and XO from an external 5-V supply input to VIN1 on J500 (or J2).
3. The direct power configuration allows for separate voltage supplies for the VDD, VDDO, and XO. In the direct power configuration mode, an external 3.3-V supply is provided to VIN1 to power the VDD pins, an external 3.3-V supply is provided to VIN2 to power the VDDO pins, and an external 3.3-V supply is provided to VIN3 to power the onboard XO.

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**Note**

Not every power connection is used or required to operate the EVM. Other power configurations are possible. See the power schematics in Figure 4-1 and Figure 4-3.

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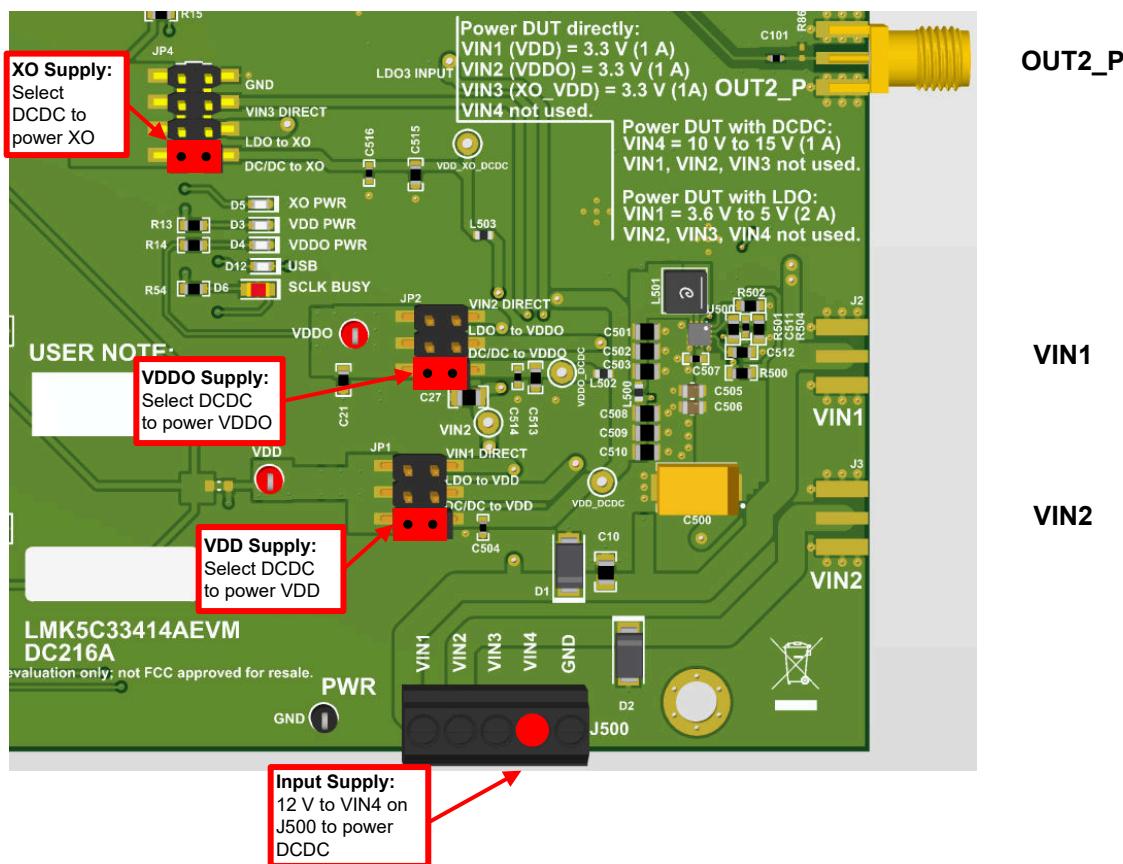


**Figure 3-2. Default Power Jumper Configuration**

Figure 3-2 shows the default power jumper locations and settings. Table 3-2 shows the suggested power configurations for the LMK5C33414A.

**Table 3-2. Suggested Power Configurations**

| CONNECTION | NAME | ONBOARD DC/DC SUPPLY (DEFAULT) VDD = 3.3 V (DCDC) VDDO = 3.3 V (DCDC) XO = 3.3 V (DCDC) | ONBOARD LDO REGULATORS VDD = 3.3 V (LDO1) VDDO = 3.3 V (LDO2) XO = 3.3 V (LDO3) | DIRECT EXTERNAL SUPPLIES VDD = 3.3 V (EXT. VIN1) VDDO = 3.3 V (EXT. VIN2) XO = 3.3 V (EXT. VIN3) |
|---|---|---|---|---|
| J500 | PWR | • Pin 1 (VIN1): n/a<br>• Pin 2 (VIN2): n/a<br>• Pin 3 (VIN3): n/a<br>• Pin 4 (VIN4): Connect to external 12-V supply<br>• Pin 5 (GND): Connect to supply ground | • Pin 1 (VIN1): Connect to external 5-V supply<br>• Pin 2 (VIN2): n/a<br>• Pin 3 (VIN3): n/a<br>• Pin 4 (VIN4): n/a<br>• Pin 5 (GND): Connect to supply ground | • Pin 1 (VIN1): Connect to external 3.3-V supply<br>• Pin 2 (VIN2): Connect to external 3.3-V supply<br>• Pin 3 (VIN3): Connect to external 3.3-V supply<br>• Pin 4 (VIN4): n/a<br>• Pin 5(GND): Connect to supply ground |
| JP1 | VDD | • Tie pins 1-2 (opposite to designator) to select 3.3 V from DCDC to VDD Plane | • Tie pins 3-4 (middle pins) to select 3.3 V from LDO1 to VDD Plane | • Tie pins 5-6 (adjacent to designator) to select external VIN1 to VDD Plane |
| JP2 | VDDO | • Tie pins 1-2 (opposite to designator) to select 3.3 V from DCDC to VDD Plane | • Tie pins 3-4 (middle pins) to select 3.3 V from LDO2 to VDDO Plane | • Tie pins 5-6 (adjacent to designator) to select external VIN2 to VDDO Plane |
| JP3 | XO | • Tie pins 1-2 (opposite to designator) to select 3.3V from DCDC to XO supply | • Tie pins 3-4 (middle pins) to select 3.3 V from LDO3 to XO supply | • Tie pins 5-6 (adjacent to designator) to select external VIN3 to XO supply |

## 3.2 Logic Inputs and Outputs

The logic I/O pins of the LMK5C33414A support different functions depending on the device start-up mode chosen by the GPIO1 input level upon power on reset (POR).

The default logic input pin states are determined by onboard pullup or pulldown resistors, but some input pins can be driven to high or low state by the MCU output or DIP switch control. The MCU can be controlled from a PC running TICS Pro software to program the device registers through I2C or SPI and also drive the LMK5C33414A logic inputs. To allow the MCU to control the pin input, SW[2] of the DIP switch correlating with the controlled GPIO must be set to on.

See Table 3-3 for the logic pin mapping tables for the device start-up modes.

**Table 3-3. Device Start-Up Modes**

| GPIO1 INPUT LEVEL[1] | START-UP MODE |
|---|---|
| Low | I$^2$C Mode |
| High | SPI Mode |

(1) The input levels on these pins are sampled only during POR.

## 3.3 Switching Between I2C and SPI

To switch the EVM between I2C and SPI modes, the switches and jumpers must be configured as follows:



**Figure 3-3. I2C Mode Jumper Configuration**

**Figure 3-4. SPI Mode Jumper Configuration**
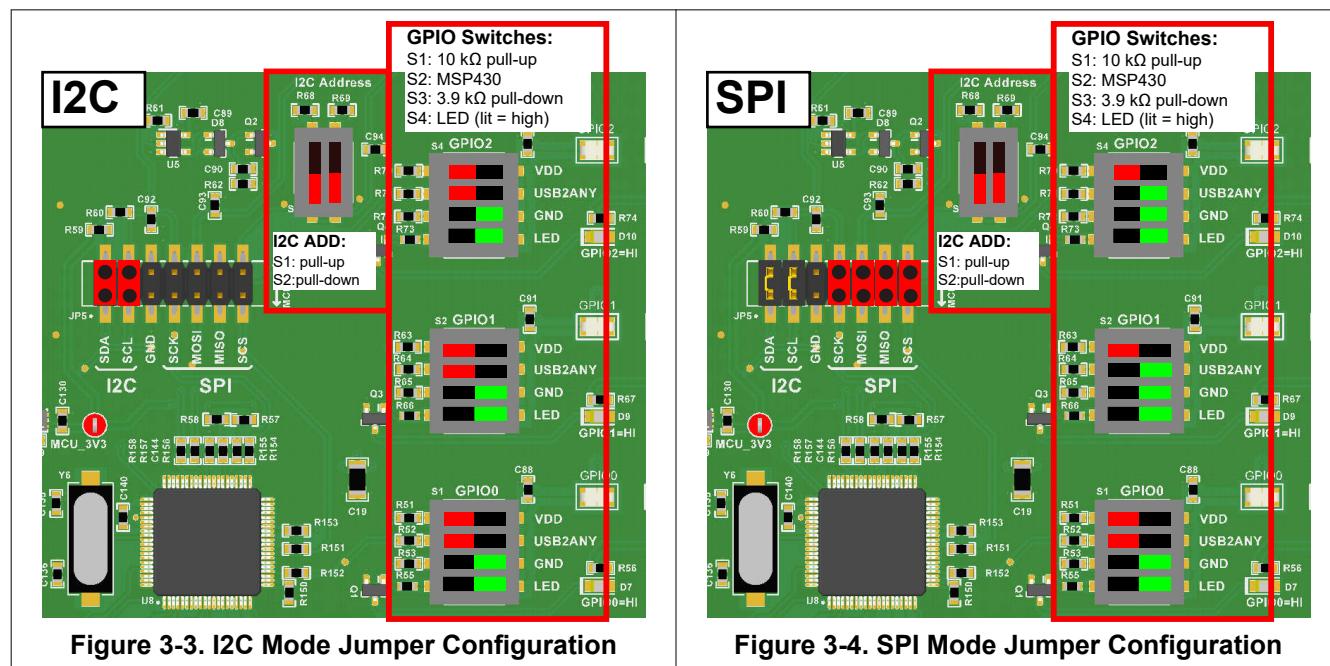
In SPI mode, based on EVM layout routing GPIO2 to SPI host input, GPIO2 must also be configured as *STATUS or INT*, *SPI Readback Data (SDO)*, *Active High*, and *CMOS* to support SPI readback.
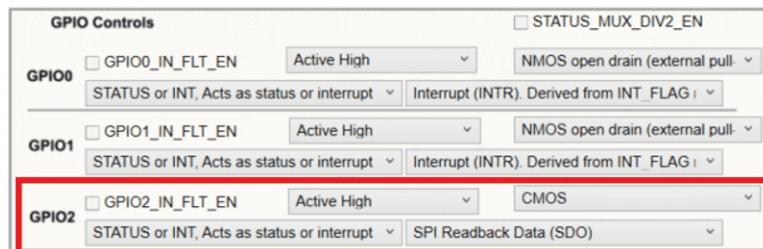


**Figure 3-5. GPIO2 Setting for SPI Mode**

Communication protocols must be set in TICS Pro. From the menu bar, select *USB communications → Interface* to get the Communication Setup window and change the protocol.
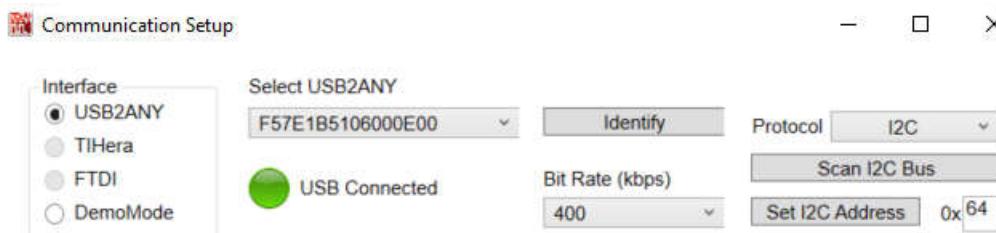


**Figure 3-6. Communication Setup Window (Changing from I2C to SPI)**

## 3.4 Generating SYSREF Request

Standard SPI/I2C programming, GPIO0, or GPIO1 can be used to generate a SYSREF request. The TICS Pro software and EVM is designed to use GPIO2 for SPI readback (SDO). Accordingly, GPIO2 is not listed in the pins as GPIO2 is dedicated for SPI readback. In a user application, any GPIO pin can be used.

Connect the desired GPIO pin to the MCU by setting S2 as ON on the switch block for the desired GPIO. Then, make sure the GPIO pin is configured for *SYSREF_REQ* on the GPIO tab of the GUI. A SYSREF Request can now be issued by toggling the GPIO buttons in the *Pins* section of the *User Controls* tab.
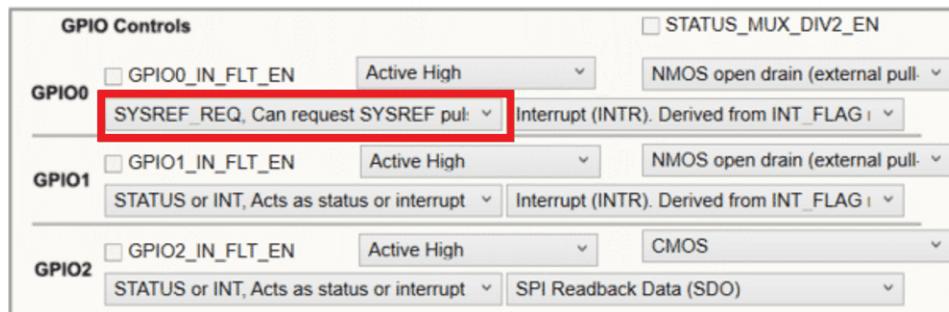


**Figure 3-7. GPIO Setting for SYSREF Request**
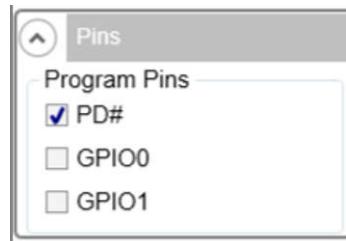


**Figure 3-8. GPIO Pin Selection for SYSREF**

## 3.5 XO Input

The LMK5C33414A has an XO input (XO pin) to accept a reference clock for the Fractional-N APLLs. The XO input determines the output frequency accuracy and stability in free-run or holdover modes. For synchronization applications like SyncE or IEEE 1588, the XO input is typically driven by a low-frequency TCXO or OCXO that conforms to the frequency accuracy and holdover stability requirements of the application. For proper DPLL operation, the XO frequency must have a non-integer frequency relationship with the VCO output frequency of any APLL that uses the XO input as the reference. The non-integer relationship needs to be greater than 0.05 away from an integer boundary (meaning > 0.05 and < 0.95). When configuring the LMK5C33414A as a clock generator (DPLL not used), then the XO frequency can have an integer relationship with the APLL output frequency.

The XO input of the LMK5C33414A has programmable on-chip input termination and AC-coupled input biasing options to support any clock interface type.
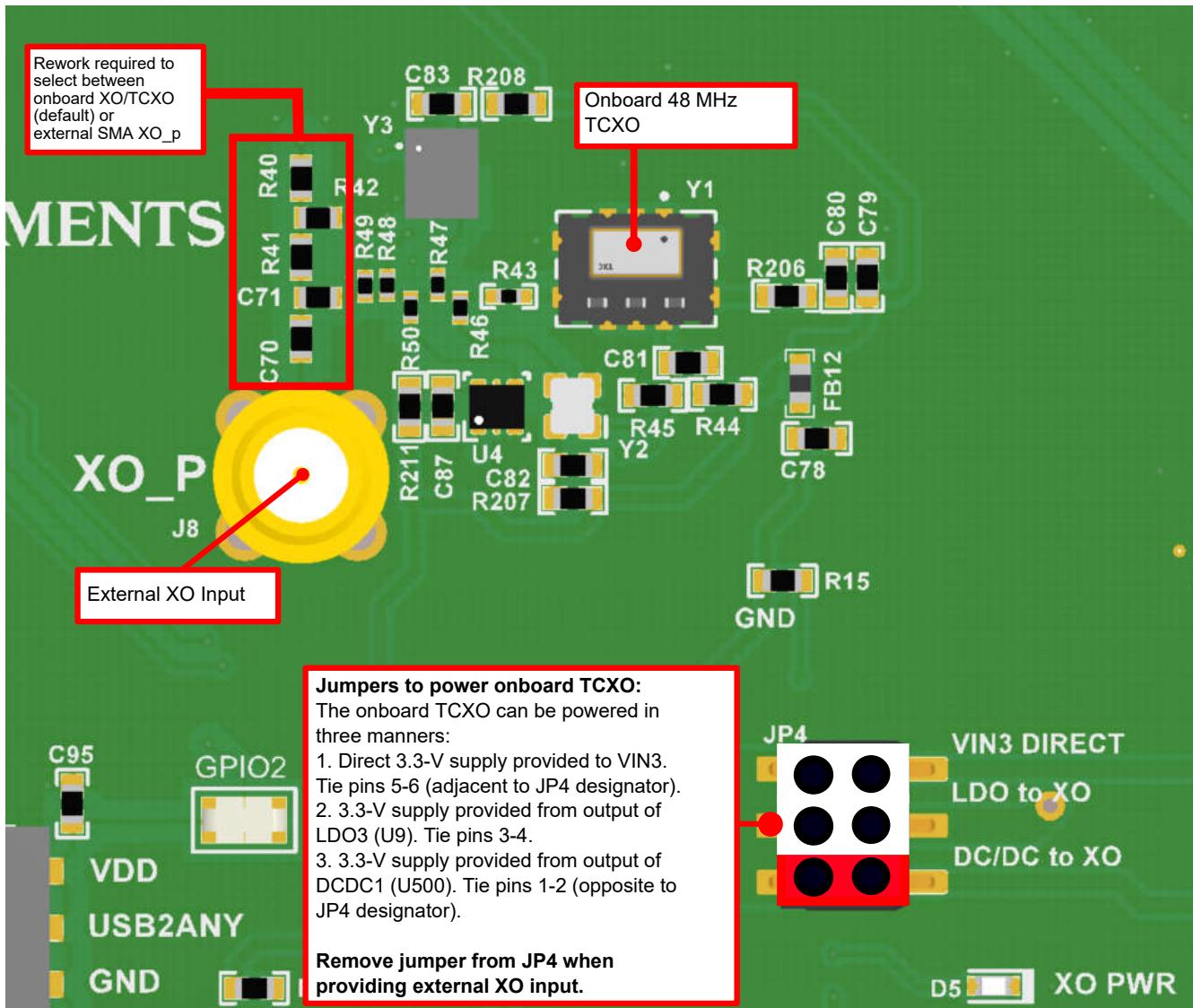
**Figure 3-9. XO Input**

### 3.5.1 48-MHz TCXO (Default)

By default, the EVM is populated with a 48-MHz, 3.3-V LVCMOS, low-jitter TCXO, designated as Y1 (3.2 mm × 2.5 mm), which drives the XO input of the LMK5C33414A with the onboard termination and AC coupling. See Figure 3-9. All LMK5C33414A EVMs have a TXC 7N48071001 48-MHz TCXO populated on Y1. Y1 can be used to evaluate various frequency configurations.

### 3.5.2 External Clock Input

Another option is to feed an external clock to the XO SMA port (J8) to drive the XO input. See Figure 3-9. This path can be connected to the XO input pins. Y1 needs to be powered down when using the external XO input path. To power down Y1 and use an external XO input, the jumper on JP4 must be removed. Suggested XO frequencies for best device performance are frequencies of 38.88 MHz and 48 MHz. When using an external XO input, TI recommends to remove the capacitor (C71) connecting the TCXO output to the XO input of the LMK5C33414A. This prevents any risk of backdriving the onboard TCXO.

### 3.5.3 Additional XO Input Options

For flexibility, the EVM provides additional XO input options (use one at a time). C70 allows an external reference to be provided at SMA connector XO (J8). C71 allows one of the onboard XO/TCXO/OCXO footprints to be used.

By default, Y1 is populated with a 48-MHz TCXO and selected with the populated R43 and R206. R43 provides the output clock of Y1 to the XO pin of the LMK5C33414A and R206 provides power to Y1.

Additional PCB footprints are available to install alternate components for performance evaluation of specific oscillators. These additional footprints are Y2 (2.5 × 2.0 mm), Y3 (3.2 mm × 2.5 mm), Y4 (9.7 mm × 7.5 mm), Y5 (25 mm × 22 mm), and U4 (2.5 mm × 2 mm).

When using Y2, Y3, Y4, Y5, or U4, R43 and R206 must be removed to power down and isolate the output of Y1. When populating Y2, R46 and R207 must be populated to power up Y2 and provide the output to the XO pin. When populating Y3, R47 must be populated to provide Y3's output to the XO pin. When populating Y4, R48 must be populated to provide Y4's output to the XO pin. When populating Y5, R49 must be populated to provide Y5's output to the XO pin. When populating U4, R50 must be populated to provide U4's output to the XO pin. Section 4.8 shows the components described above.

Be cautious when removing resistors, if more than one device is installed, to power down unused oscillators and isolate their outputs as described above.

### 3.5.4 APLL Reference Options

The LMK5C33414A APLLs can accept any other APLL output as a reference instead of the XO. The BAW on APLL3 provides a good option for a high-frequency cascaded APLL reference. Figure 6-2 shows how to configure the APLL reference to be cascaded from another APLL.

## 3.6 Reference Clock Inputs

The LMK5C33414A has four DPLL reference clock input pairs (IN0_P/N, IN1_P/N, IN2_P/N, and IN3_P/N) with configurable input priority and input selection modes. The inputs have programmable input type, termination, and biasing options to support any clock interface type.

External LVCMOS or differential reference clock inputs can be applied to the SMA ports, labeled IN0_P/N, IN1_P/N, IN2_P/N, and IN3_P/N. All SMA inputs are routed through 50-Ω single-ended traces. To accommodate evaluation of different input types, the EVM default assembly supports two AC-coupled differential inputs (IN2_P/N and IN3_P/N), one DC-coupled differential input (IN1_P/N) and one DC-coupled single-ended input (IN0_P). When applying a single-ended signal, connect to the noninverting input (IN0_P, IN1_P, IN2_P, or IN3_P).

## 3.7 Clock Outputs

The LMK5C33414A has 14 clock output pairs (OUT[0:13]_P/N).

OUT0 is configured as DC-coupled for LVCMOS evaluation purposes. OUT1, OUT2, and OUT3 have 50 Ω to GND followed by an AC-coupling capacitor for HCSL evaluation purposes. OUT4 to OUT13 are AC-coupled to the SMA ports for LVDS and HSDS evaluation purposes.

When changing output type in the programming software, make sure the required board modifications are also implemented for proper operation.

> **WARNING**
> DC-coupled clocks must not be directly connected to RF equipment, which cannot accept DC voltage greater than 0 V. For example, spectrum analyzers and phase noise analyzers.

## 3.8 Status Outputs and LEDs

Status outputs signals can be configured on the GPIO0, GPIO1, and GPIO2 pins. The status output types are 3.3-V LVCMOS or NMOS open-drain.

Additional to monitoring devices statuses, GPIO1 and GPIO2 can be used for SYSREF replication. This allows for two additional LVCMOS outputs to be provided from the LMK5C33414A. TP33 can be used to measure the GPIO1 output. TP38 can be used to measure the GPIO2 output. Figure 4-10 shows these test points.

## 3.9 Requirements for Making Measurements

When performing measurements with the LMK5C33414AEVM, the following procedures must be completed:

1. Make sure all required outputs have proper termination components installed to match the desired output types. Figure 3-10 shows the recommended output terminations for each output format.

| Driver | $R_B$ ($\Omega$) |
|--------|------------------|
| LVDS   | open             |
| HSDS   | open             |
| HCSL   | 50               |
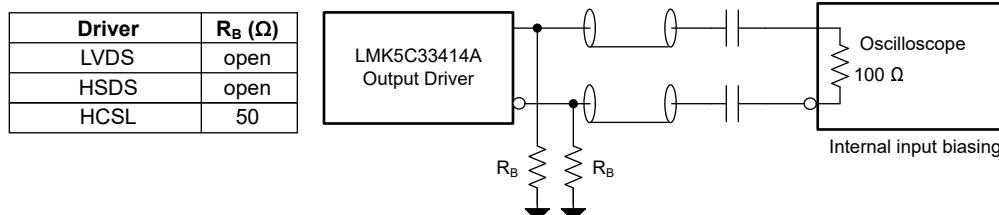


**Figure 3-10. Output Termination Recommendations**

2. Make sure all enabled outputs that are not connected to any test equipment have a 50-Ω SMA termination. Figure 3-11 shows an example of a 50-Ω SMA termination.



**Figure 3-11. 50-Ω SMA Termination**

## 3.10 Typical Phase Noise Characteristics

These plots show the typical phase noise performance for common frequencies outputted from the BAW (VCO3).

The EVM configuration used to obtain these measurements is as follows:

1. XO frequency = 48 MHz (Onboard TCXO)
2. Outputs were configured as HSDS outputs following the methods described in Section 3.9.
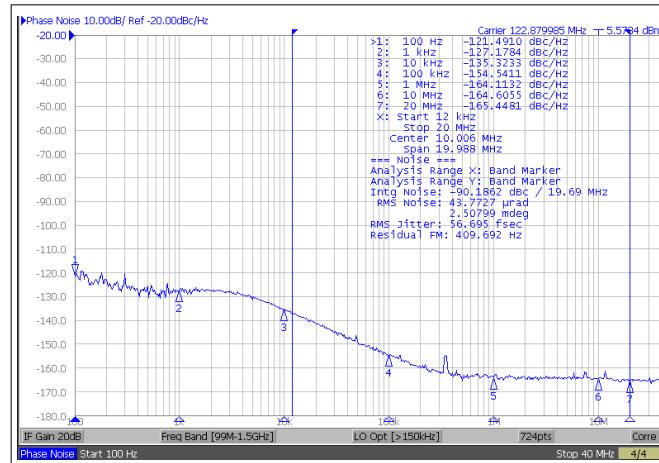


**Figure 3-12. APLL3 122.88MHz Phase Noise Performance**
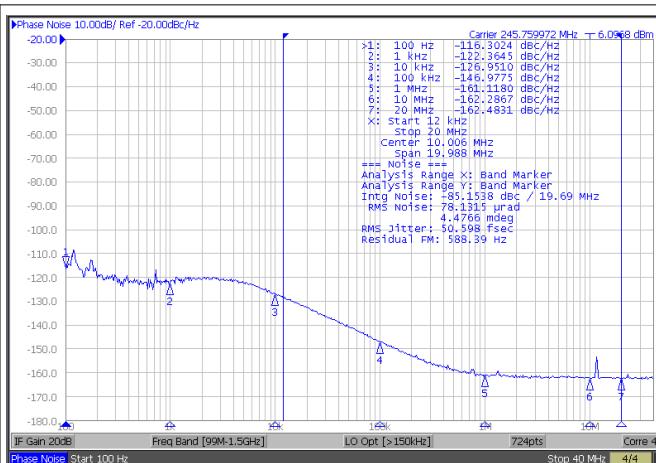


**Figure 3-13. APLL3 245.76MHz Phase Noise Performance**
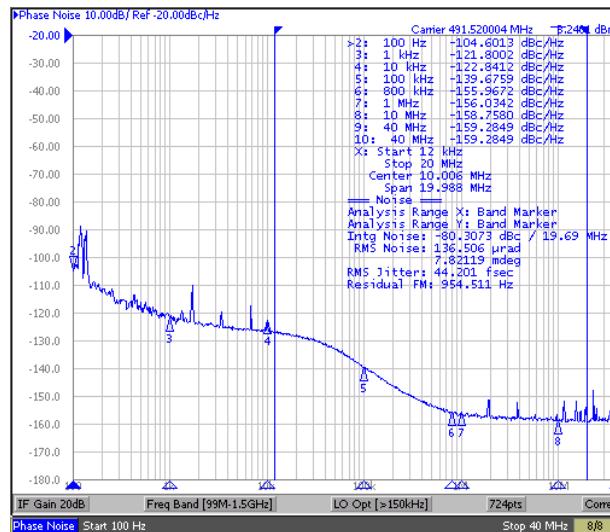


**Figure 3-14. APLL3 491.52MHz Phase Noise Performance**

# 4 EVM Schematics

## 4.1 Power Supply Schematic
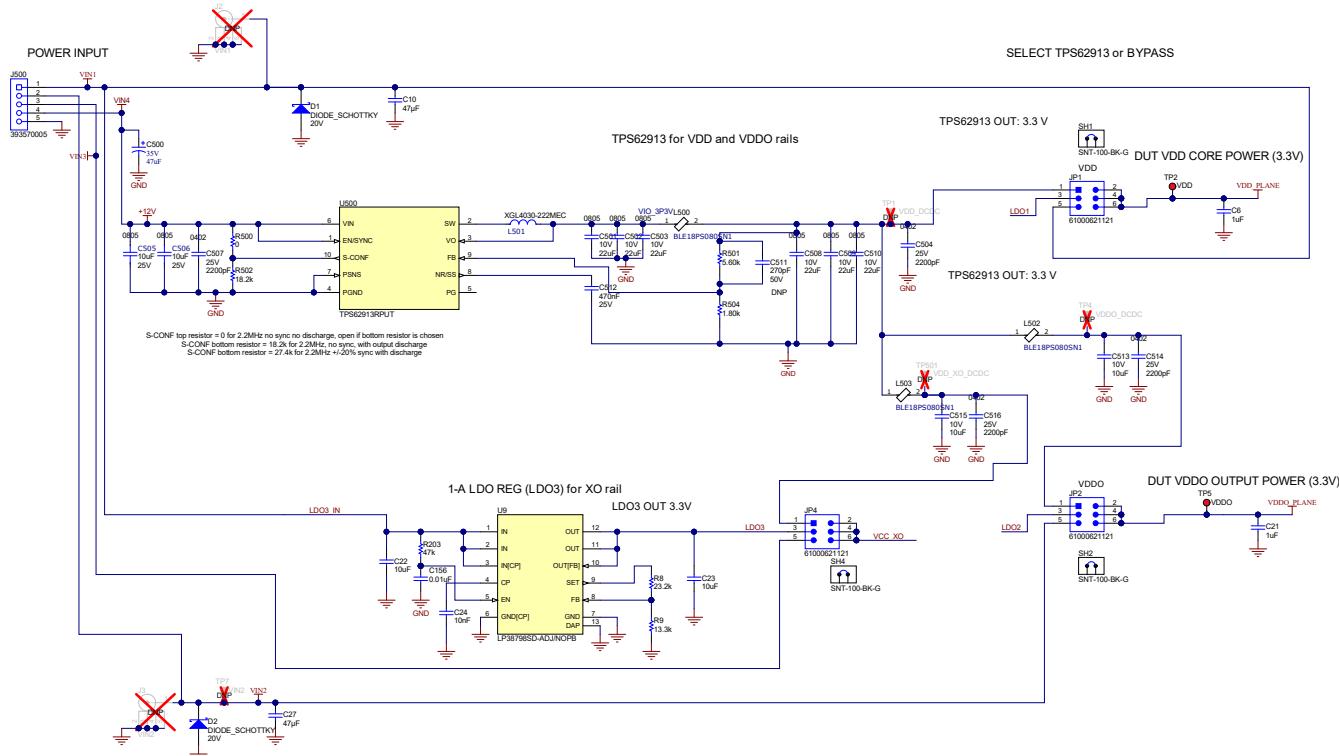


**Figure 4-1. Power Supplies**

## 4.2 Alternative Power Supply Schematic

### 1-A LDO REG (LDO1, LDO2) for DUT VDD & VDDO rails
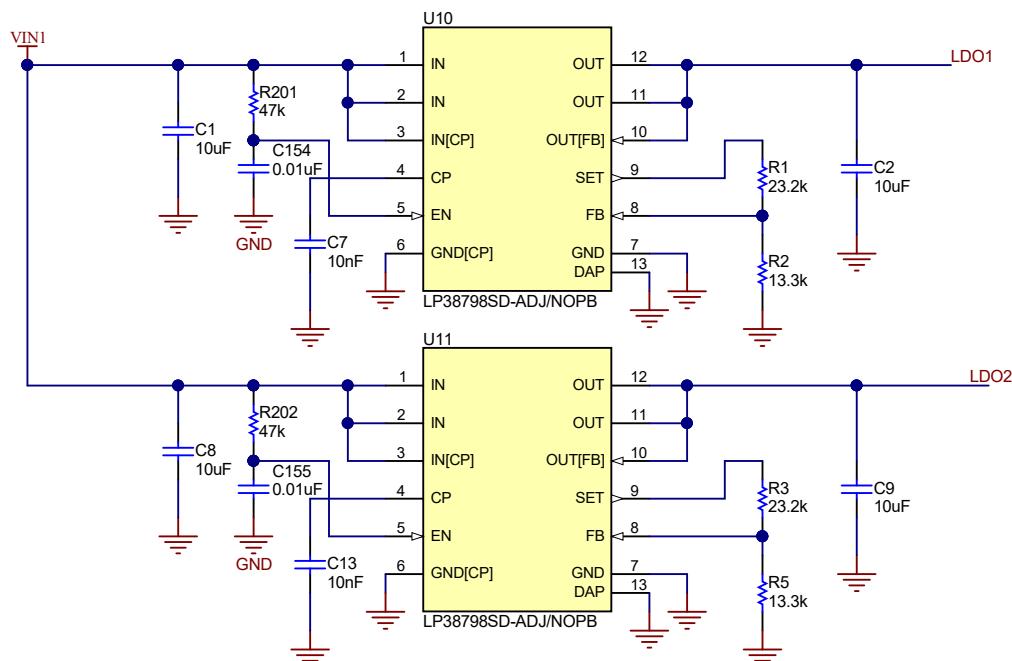


**Figure 4-2. Alternative Power Supply**

## 4.3 Power Distribution Schematic
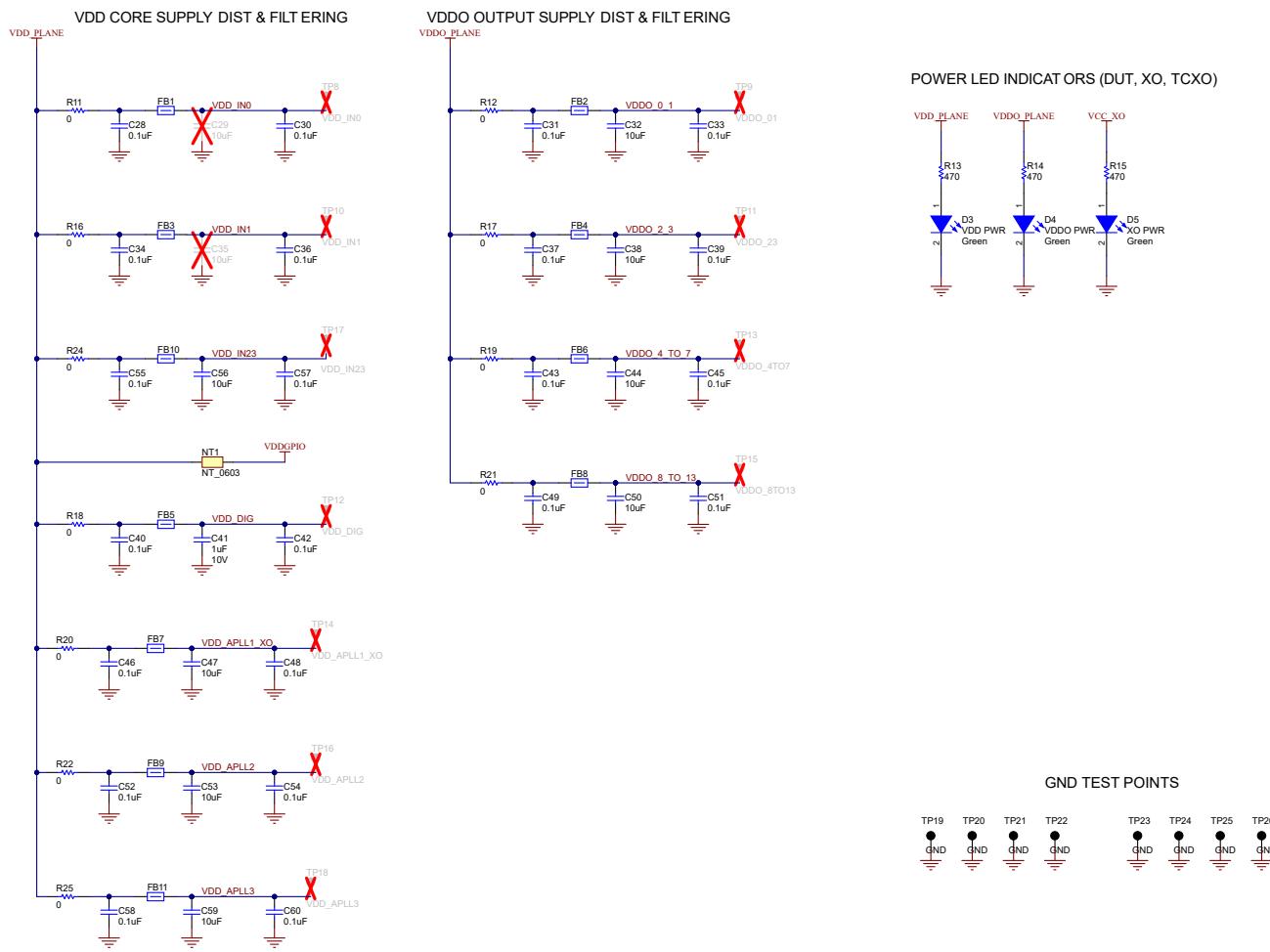


**Figure 4-3. Power Distribution**

## 4.4 LMK5C33414A and Input References IN0 to IN3 Schematic
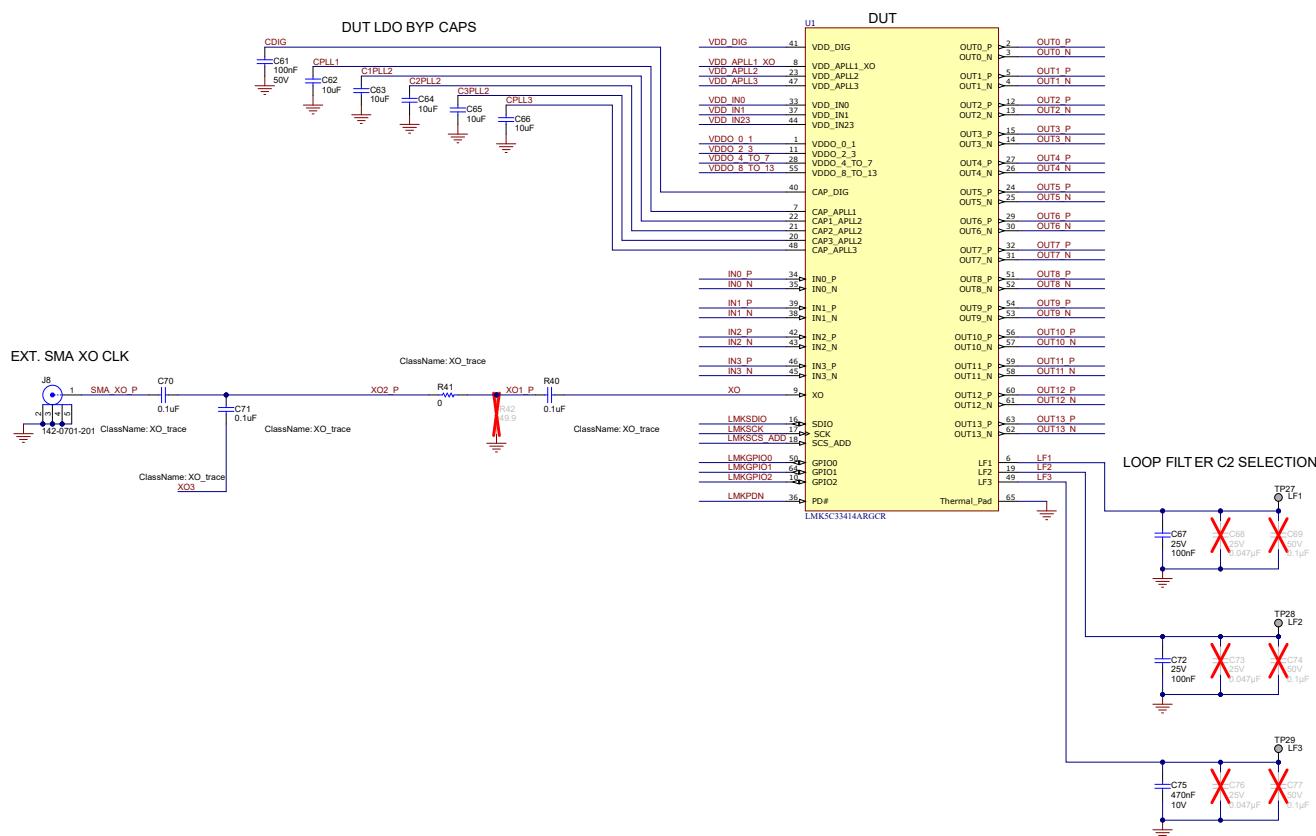


**Figure 4-4. LMK5C33414A Schematic**
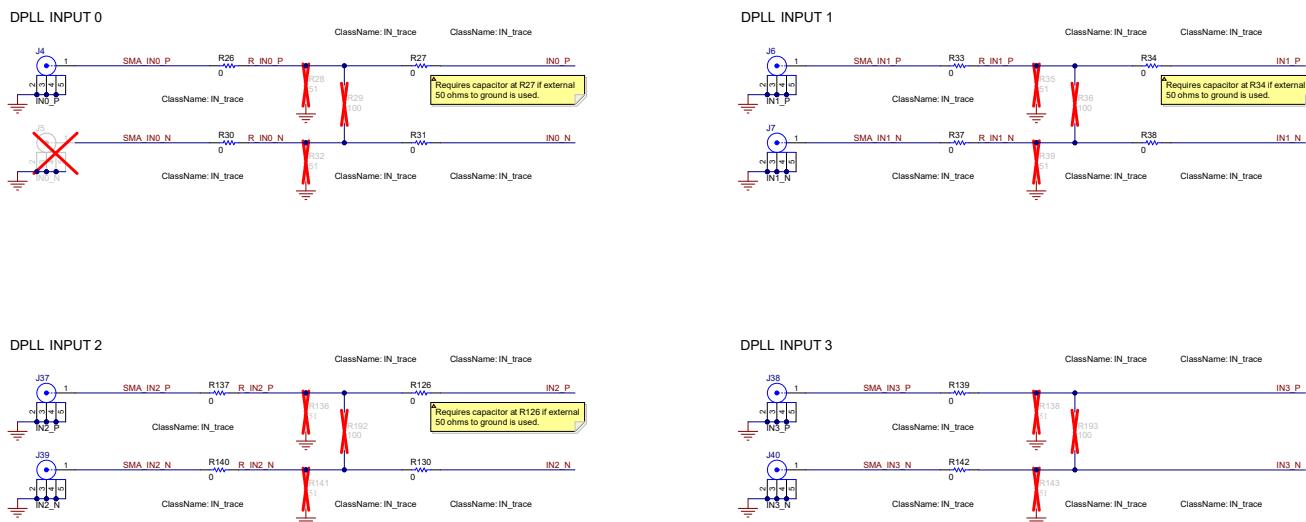


**Figure 4-5. Input References IN0 to IN3**

## 4.5 Clock Outputs OUT0 to OUT3 Schematic

OUT0-OUT3 CLOCK OUTPUTS

OUT0, Supported formats: CMOS, L  VDS, HSDS, and HCSL. Source may be XO, REF0-3, or VCO1-3
Default: DC-coupled, no termination (for 1 Hz outputs)
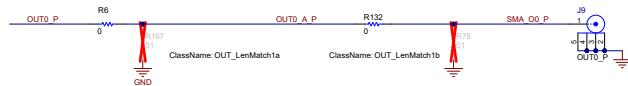
OUT1, Supported formats: CMOS, L  VDS, HSDS, and HCSL. Source may be XO, REF0-3, or VCO1-3
Default: 50-ohms to GND on each P   and N then AC-coupled (for HCSL outputs)

OUT2, Supported formats: L  VDS, HSDS, and HCSL. Source may be VCO1, VCO2, or VCO3
Default: 50-ohms to GND on each P   and N then AC-coupled (for HCSL outputs)
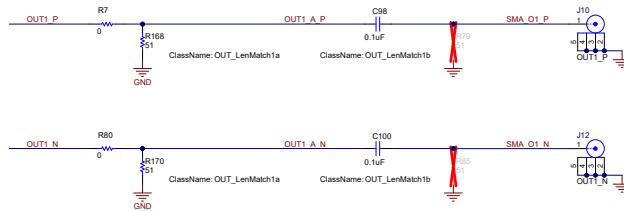
OUT3, Supported formats: L  VDS, HSDS, and HCSL. Source may be VCO1, VCO2, or VCO3
Default: 50-ohms to GND on each P   and N then AC-coupled (for HCSL outputs)
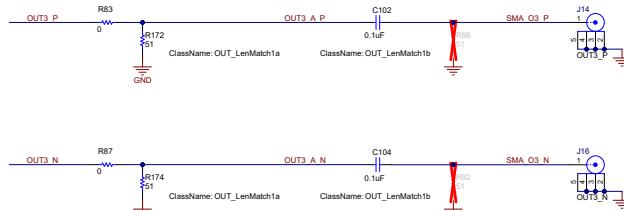
**Figure 4-6. Clock Outputs OUT0 to OUT3**

## 4.6 Clock Outputs OUT4 to OUT9 Schematic

OUT4-OUT9 CLOCK OUTPUTS
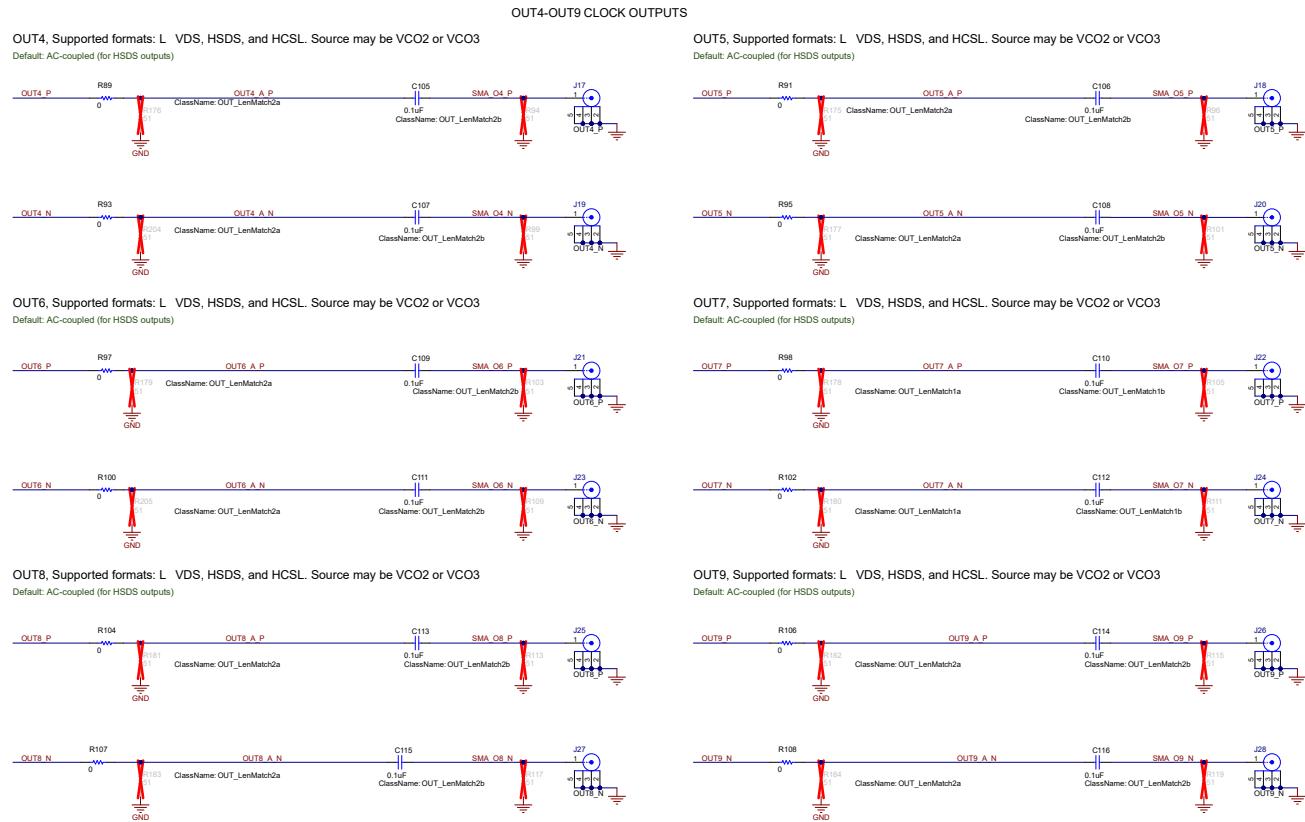


**Figure 4-7. Clock Outputs OUT4 to OUT9**

## 4.7 Clock Outputs OUT10 to OUT13 and Clock Inputs IN2 and IN3 Schematic

OUT10-OUT13 CLOCK OUTPUTS
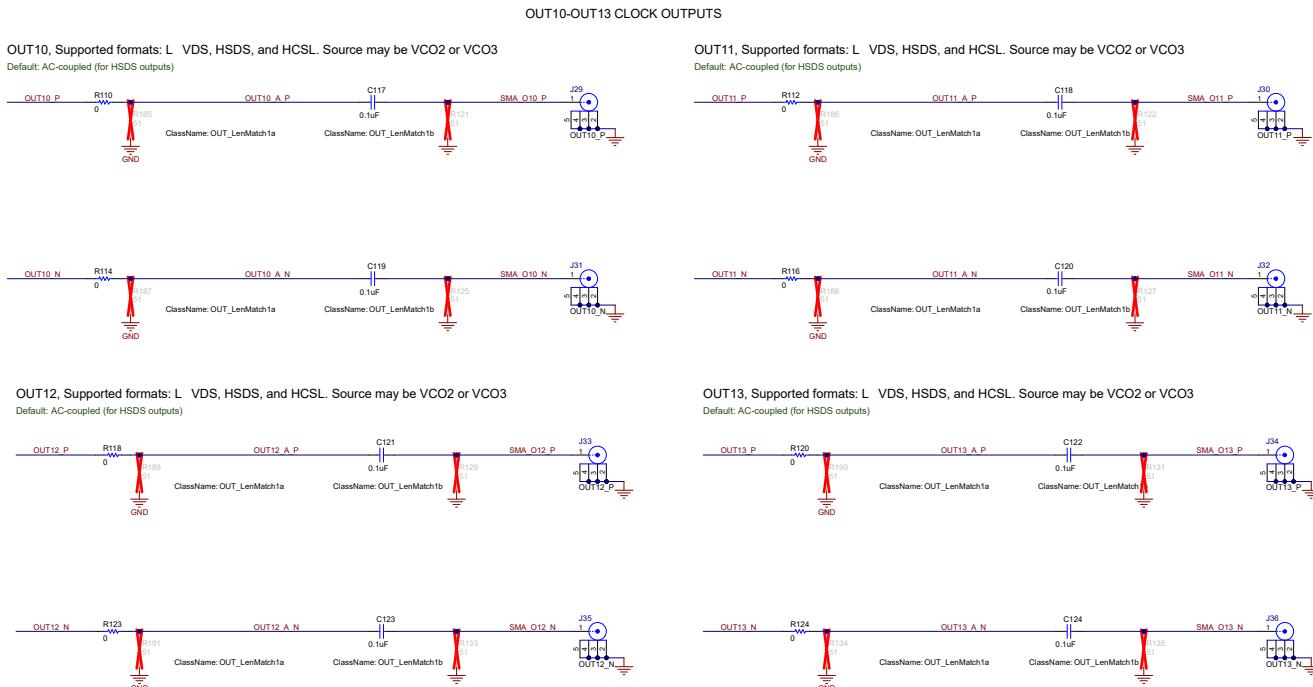


**Figure 4-8. Clock Outputs OUT10 to OUT13 and Clock Inputs IN2 and IN3**

## 4.8 XO Schematic
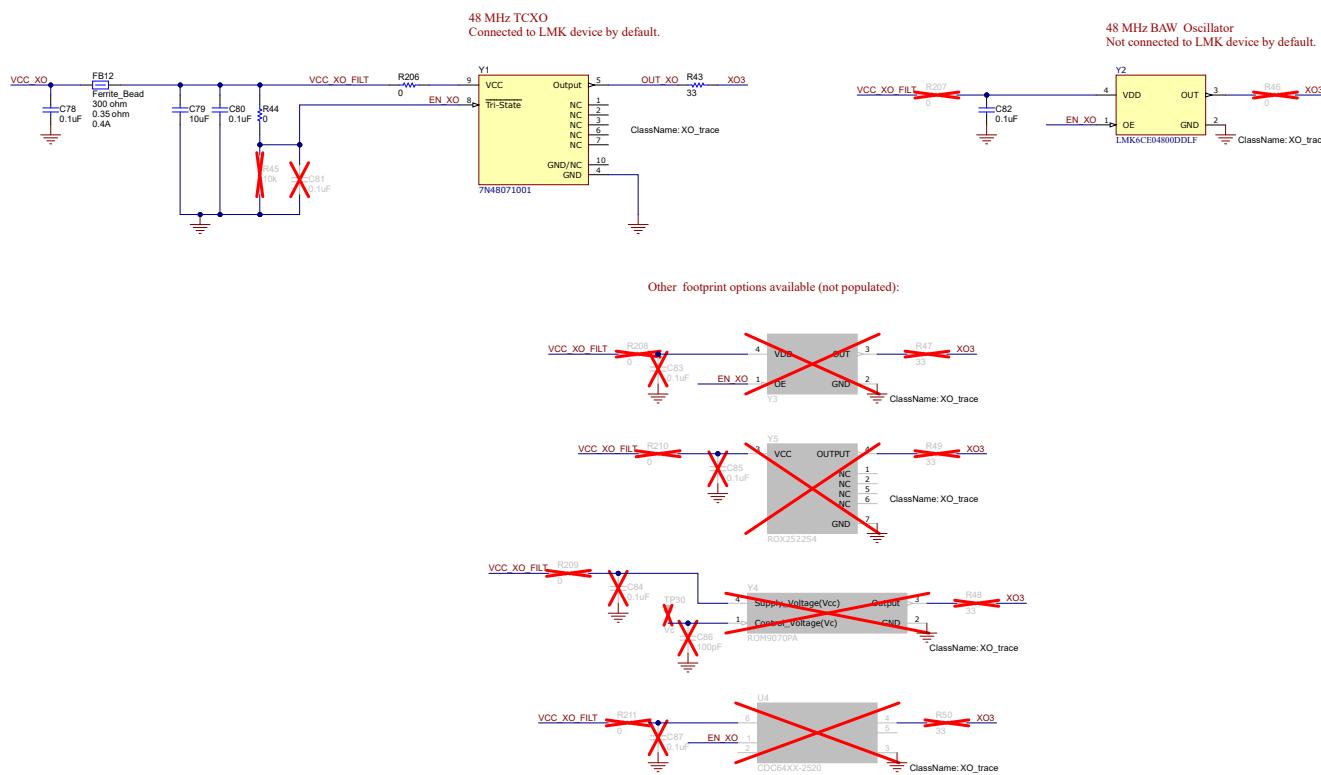


**Figure 4-9. XO**

## 4.9 Logic I/O Interfaces Schematic
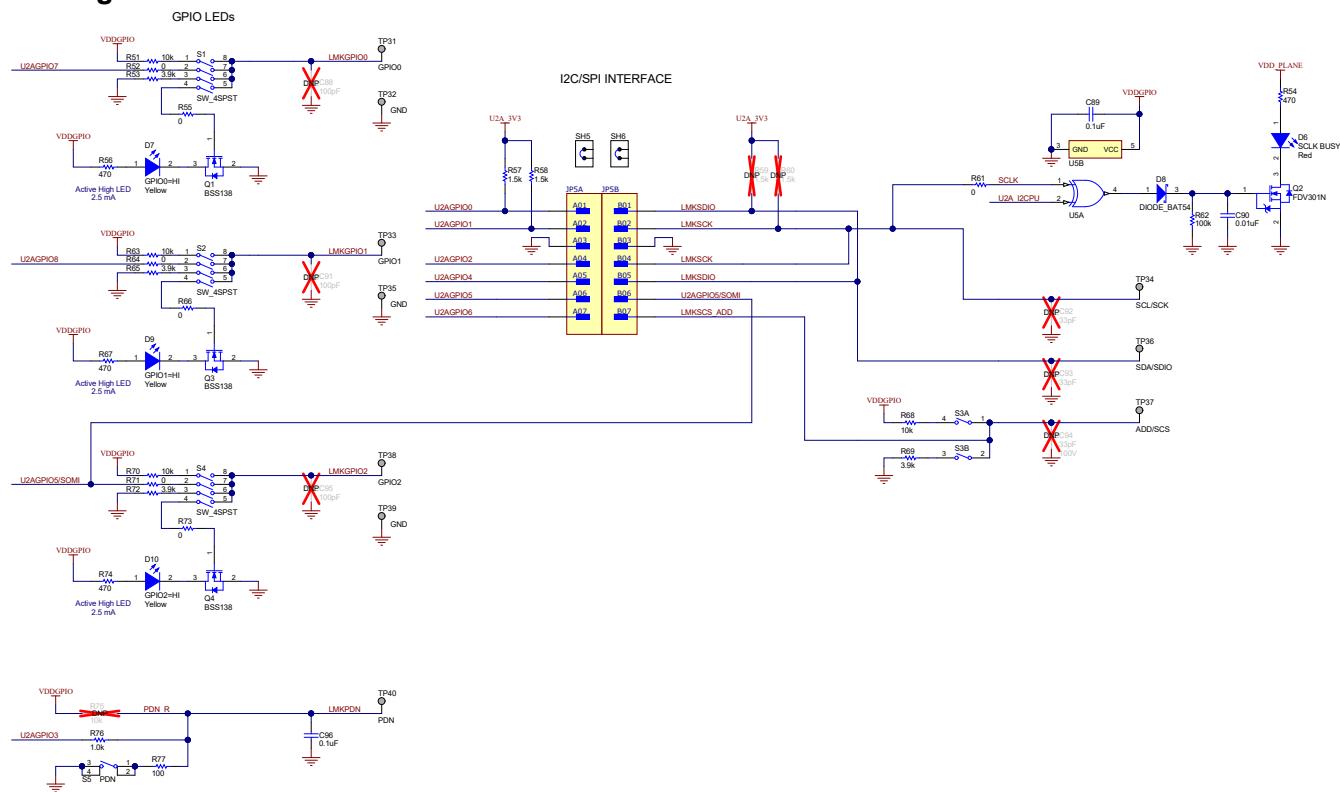


**Figure 4-10. Logic I/O Interfaces**

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## 4.10 USB2ANY Schematic
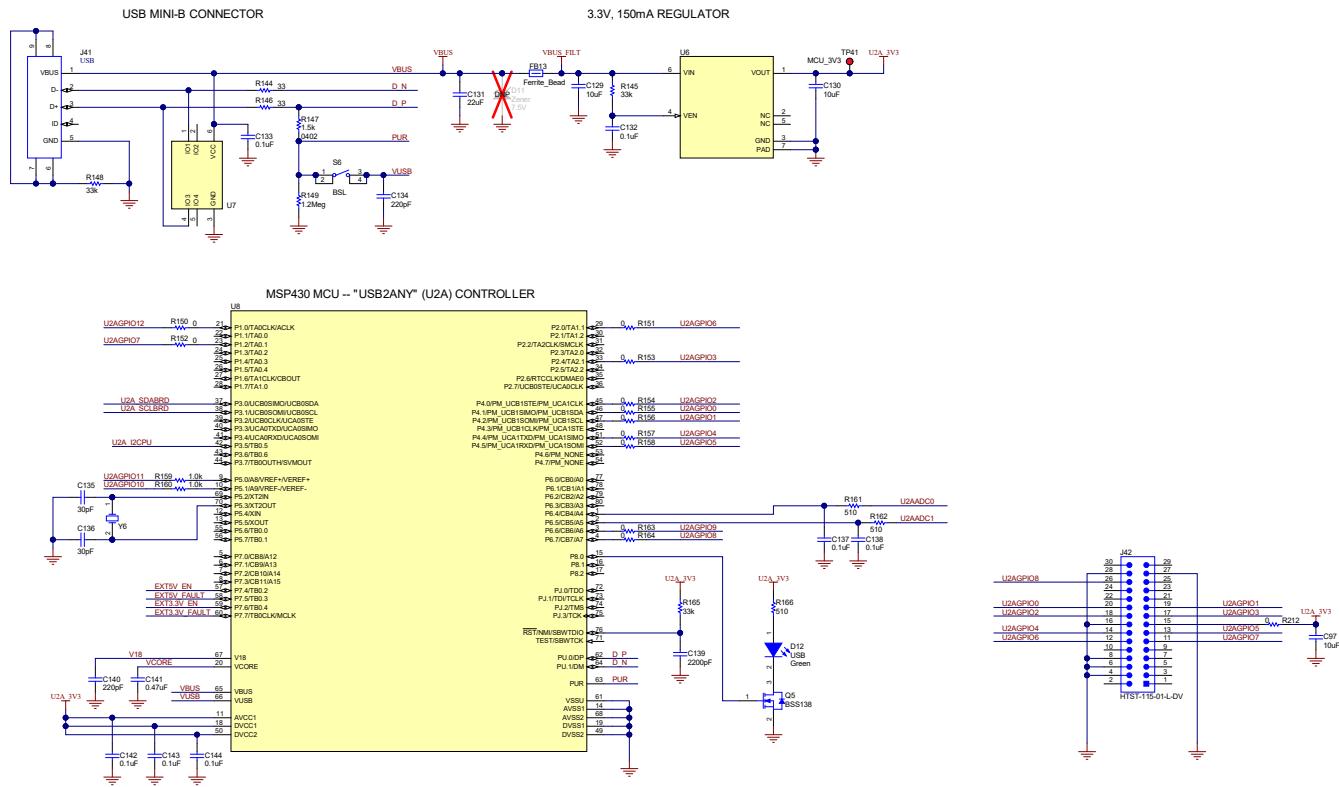


**Figure 4-11. USB MCU**

## 5 EVM Bill of Materials

### Table 5-1. Bill of Materials (BOM)

| DESIGNATOR | QTY | VALUE | DESCRIPTION | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|
| PCB1 | 1 | | Printed Circuit Board | HSDC145 | Any |
| C1, C2, C7, C8, C9, C13, C22, C23, C24, C32, C38, C44, C47, C50, C53, C56, C59, C62, C63, C64, C65, C66, C79, C97, C129, C130 | 26 | 10uF | CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603 | C1608X5R1A106M080AC | TDK |
| C6, C21, C41 | 3 | 1uF | CAP, CERM, 1 uF, 10 V, +/- 10%, X5R, 0603 | C0603C105K8PACTU | Kemet |
| C10, C27 | 2 | 47uF | CAP, CERM, 47 µF, 10 V,+/- 20%, X5R, 0805 | GRM21BR61A476ME15L | MuRata |
| C28, C31, C34, C37, C40, C43, C46, C49, C52, C55, C58, C67, C70, C71, C72, C78, C80, C82, C96, R40 | 20 | 0.1uF | CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603 | C0603C104J3RACTU | Kemet |
| C30, C33, C36, C39, C42, C45, C48, C51, C54, C57, C60 | 11 | 0.1uF | CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402 | C1005X5R1A104K050BA | TDK |
| C61 | 1 | 0.1uF | CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603 | C1608X7R1H104K080AA | TDK |
| C75, C141 | 2 | 0.47uF | CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603 | GRM188R71A474KA61D | MuRata |
| C89, C132, C133, C137, C138, C142, C143, C144 | 8 | 0.1uF | CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603 | C0603C104J4RACTU | Kemet |
| C90, C154, C155, C156 | 4 | 0.01uF | CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603 | C0603C103J5RACTU | Kemet |
| C98, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128 | 30 | 0.1uF | CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402 | GRM155R71E104KE14D | MuRata |
| C131 | 1 | 22uF | CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805 | LMK212BJ226MG-T | Taiyo Yuden |
| C134, C140 | 2 | 220 pF | CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603 | 06035A221FAT2A | AVX |
| C135, C136 | 2 | 30 pF | CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603 | GRM1885C2A300JA01D | MuRata |
| C139 | 1 | 2200 pF | CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603 | C0603C222K5RACTU | Kemet |

**Table 5-1. Bill of Materials (BOM) (continued)**

| DESIGNATOR | QTY | VALUE | DESCRIPTION | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|
| C500 | 1 | 47uF | CAP, TA, 47 uF, 35 V, +/- 10%, 0.3 ohm, SMD | T495X476K035ATE300 | Kemet |
| C501, C502, C503, C508, C509, C510 | 6 | 22uF | CAP, CERM, 22 uF, 10 V, +/- 20%, X7S, 0805 | C2012X7S1A226M125AC | TDK |
| C504, C507, C514, C516 | 4 | 2200 pF | CAP, CERM, 2200 pF, 25 V, +/- 10%, X7R, 0402 | GRM155R71E222KA01D | MuRata |
| C505, C506 | 2 | | 10 μF ±10% 25 V Ceramic Capacitor X7S 0805 (2012 Metric) | C2012X7S1E106K125AC | TDK |
| C511 | 1 | | CAP CER 270 PF 50 V NP0 0402 | UMK105CG271JV-F | Taiyo Yuden |
| C512 | 1 | 0.47uF | CAP, CERM, 0.47 μF, 25 V,+/- 10%, X7R, 0603 | C1608X7R1E474K080AE | TDK |
| C513, C515 | 2 | 10uF | CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 0603 | GRM188Z71A106MA73D | MuRata |
| D1, D2 | 2 | 20 V | Diode, Schottky, 20 V, 2 A, SMA | B220A-13-F | Diodes Inc. |
| D3, D4, D5, D12 | 4 | Green | LED, Green, SMD | LTST-C190GKT | Lite-On |
| D6 | 1 | Red | LED, Red, SMD | LTST-C170KRKT | Lite-On |
| D7, D9, D10 | 3 | Yellow | LED, Yellow , SMD | LTST-C170KSKT | Lite-On |
| D8 | 1 | 30 V | Diode, Schottky, 30 V, 0.2 A, SOT-23 | BAT54-7-F | Diodes Inc. |
| FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11 | 11 | 220 ohm | Ferrite Bead, 220 ohm @ 100 MHz, 2.5 A, 0603 | BLM18SG221TN1D | MuRata |
| FB12 | 1 | 300 ohm | Ferrite Bead, 300 ohm @ 100 MHz, 0.4 A, 1.6x0.8x0.95mm | LI0603D301R-10 | Laird-Signal Integrity Products |
| FB13 | 1 | 60 ohm | Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603 | MPZ1608S600ATAH0 | TDK |
| FID1, FID2, FID3, FID4, FID5, FID6 | 6 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A |
| H1, H2, H3, H4, H5, H6 | 6 | | BUMPER CYLIN 0.312" DIA | SJ61A6 | 3M |
| J4, J6, J7, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40 | 35 | | CONN SMA JACK STR EDGE MNT | CON-SMA-EDGE-S | RF Solutions Ltd. |
| J8 | 1 | | Connector, SMA, TH | 142-0701-201 | Cinch Connectivity |
| J41 | 1 | | Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT | 1734035-2 | TE Connectivity |
| J42 | 1 | | Header, 2.54mm, 15x2, Gold, SMD | HTST-115-01-L-DV | Samtec |

**Table 5-1. Bill of Materials (BOM) (continued)**

| DESIGNATOR | QTY | VALUE | DESCRIPTION | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|
| J500 | 1 | | Terminal Block, 3.5mm, 5x1, Tin, TH | 393570005 | Molex |
| JP1, JP2, JP4 | 3 | | Header, 2.54mm, 3x2, Gold, SMT | 61000621121 | Wurth Elektronik |
| JP5 | 1 | | Connector Header Surface Mount 14 position 0.100" (2.54mm) | 54202-G0807LF | Amphenol ICC |
| L500, L502, L503 | 3 | | Bead inductor BLE series, 8 A | BLE18PS080SN1 | Murata |
| L501 | 1 | | Inductor Power Shielded Wirewound 2.2uH 20% 1 MHz Composite 8.7A 15mOhm DCR Automotive T/R | XGL4030-222MEC | Coilcraft |
| LBL1 | 1 | | Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll | THT-14-423-10 | Brady |
| Q1, Q3, Q4, Q5 | 4 | 50 V | MOSFET, N-CH, 50 V, 0.22 A, SOT-23 | BSS138 | Fairchild Semiconductor |
| Q2 | 1 | 25 V | MOSFET, N-CH, 25 V, 0.22 A, SOT-23 | FDV301N | Fairchild Semiconductor |
| R1, R3, R8 | 3 | 23.2k | RES, 23.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060323K2FKEA | Vishay-Dale |
| R2, R5, R9 | 3 | 13.3k | RES, 13.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060313K3FKEA | Vishay-Dale |
| R6, R7, R10, R80, R81, R83, R84, R87, R89, R91, R93, R95, R97, R98, R100, R102, R104, R106, R107, R108, R110, R112, R114, R116, R118, R120, R123, R124, R126, R128, R130, R132 | 32 | 0 | RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | RK73Z1ETTP | KOA Speer |
| R11, R12, R16, R17, R18, R19, R20, R21, R22, R23, R25, R41, R52, R55, R61, R64, R66, R71, R73, R150, R151, R152, R153, R154, R155, R156, R157, R158, R163, R164, R212 | 31 | 0 | RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06030000Z0EA | Vishay-Dale |
| R13, R14, R15, R54, R56, R67, R74 | 7 | 470 | RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW0603470RJNEA | Vishay-Dale |
| R26, R27, R30, R31, R33, R34, R37, R38 | 8 | 0 | RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402 | CRCW04020000Z0EDHP | Vishay-Dale |
| R32 | 1 | 51 | RES, 51, 5%, 0.0625 W, 0402 | RC0402JR-0751RL | Yageo America |
| R43, R144, R146 | 3 | 33 | RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | CRCW040233R0JNED | Vishay-Dale |

**Table 5-1. Bill of Materials (BOM) (continued)**

| DESIGNATOR | QTY | VALUE | DESCRIPTION | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|
| R44, R500 | 2 | 0 | RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | ERJ-3GEY0R00V | Panasonic |
| R51, R63, R68, R70 | 4 | 10k | RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060310K0JNEA | Vishay-Dale |
| R53, R65, R69, R72 | 4 | 3.9k | RES, 3.9 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06033K90JNEA | Vishay-Dale |
| R57, R58 | 2 | 1.5k | RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06031K50JNEA | Vishay-Dale |
| R62 | 1 | 100k | RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW0603100KJNEA | Vishay-Dale |
| R76, R159, R160 | 3 | 1.0k | RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06031K00JNEA | Vishay-Dale |
| R77 | 1 | 100 | RES, 100, 5%, 0.25 W, AEC-Q200 Grade 0, 0603 | ESR03EZPJ101 | Rohm |
| R145, R148, R165 | 3 | 33k | RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060333K0JNEA | Vishay-Dale |
| R147 | 1 | 1.5k | RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | CRCW04021K50JNED | Vishay-Dale |
| R149 | 1 | 1.2Meg | RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06031M20JNEA | Vishay-Dale |
| R161, R162, R166 | 3 | 510 | RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW0603510RJNEA | Vishay-Dale |
| R168, R170, R171, R172, R173, R174 | 6 | 49.9 | RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402 | ERJ-2RKF49R9X | Panasonic |
| R201, R202, R203 | 3 | 47k | RES, 47 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060347K0JNEA | Vishay-Dale |
| R206, R208, R209, R210, R211 | 5 | 0 | RES, 0, 5%, 0.1 W, 0603 | RC0603JR-070RL | Yageo |
| R501 | 1 | 5.60k | RES, 5.60 k, 0.1%, 0.1 W, 0603 | RG1608P-562-B-T5 | Susumu Co Ltd |
| R502 | 1 | 18.2k | RES, 18.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060318K2FKEA | Vishay-Dale |
| R504 | 1 | 1.80k | RES, 1.80 k, 0.1%, 0.1 W, 0603 | RT0603BRD071K8L | Yageo America |
| S1, S2, S4 | 3 | | Switch, SPST 4 Pos, Top Actuated, SMT | 219-4LPST | CTS Electrocomponents |
| S3 | 1 | | Switch, Slide, SPST 2 poles, SMT | 219-2LPST | CTS Electrocomponents |
| S5, S6 | 2 | | Switch, Tactile, SPST-NO, 0.05A, 12 V, SMT | FSM4JSMA | TE Connectivity |
| SH1, SH2, SH4, SH5, SH6 | 5 | 1x2 | Shunt, 100mil, Gold plated, Black | SNT-100-BK-G | Samtec |
| TP2, TP5, TP41 | 3 | | Test Point, Miniature, Red, TH | 5000 | Keystone |
| TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26 | 8 | | Test Point, Miniature, Black, TH | 5001 | Keystone |

## Table 5-1. Bill of Materials (BOM) (continued)

| DESIGNATOR | QTY | VALUE | DESCRIPTION | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|
| TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40 | 10 | | Test Point, Miniature, SMT | 5019 | Keystone |
| U1 | 1 | | Ultra-Low Jitter Clock Synchronizer with JESD204B for Wireless Communications | LMK5C33414ARGCR | Texas Instruments |
| U5 | 1 | | Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5) | SN74LVC1G86DBVR | Texas Instruments |
| U6 | 1 | | 150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6) | LP5900SD-3.3/NOPB | Texas Instruments |
| U7 | 1 | | 4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6) | TPD4E004DRYR | Texas Instruments |
| U8 | 1 | | 25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br) | MSP430F5529IPN | Texas Instruments |
| U9, U10, U11 | 3 | | 800-mA Ultra-Low-Noise, High-PSRR LDO, DNT0012B (WSON-12) | LP38798SD-ADJ/NOPB | Texas Instruments |
| U500 | 1 | | 3 A Low Noise and Low Ripple buck converter, RPU0010A (VQFN-10) | TPS62913RPUT | Texas Instruments |
| Y1 | 1 | | SMD TCXO 7.0 * 5.0 48.000000MHz | 7N48071001 | TXC |
| Y2 | 1 | | High-Performance BAW Oscillator, 48 MHz LVCMOS; <1ps, +/- 50 ppm; 2.5V/3.3V, -40C to 105C and DLE package | LMK6CE04800DDLF | Texas Instruments |
| Y6 | 1 | | Crystal, 24.000 MHz, 20 pF, SMD | ECS-240-20-5PX-TR | ECS Inc. |
| C29, C35 | 0 | 10uF | CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603 | C1608X5R1A106M080AC | TDK |
| C68, C73, C76 | 0 | 0.047uF | CAP, CERM, 0.047 µF, 25 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805 | C0805C473J3GACTU | Kemet |
| C69, C74, C77 | 0 | 0.1uF | CAP, CERM, 0.1 µF, 50 V,+/- 5%, C0G/NP0, 1210 | C3225C0G1H104J250AA | TDK |
| C81, C83, C84, C85, C87 | 0 | 0.1uF | CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603 | C0603C104J3RACTU | Kemet |
| C86, C88, C91, C95 | 0 | 100 pF | CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603 | 06035A101JAT2A | AVX |
| C92, C93, C94 | 0 | 33 pF | CAP, CERM, 33 pF, 100 V, +/- 5%, C0G/NP0, 0603 | 06031A330JAT2A | AVX |

### Table 5-1. Bill of Materials (BOM) (continued)

| DESIGNATOR | QTY | VALUE | DESCRIPTION | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|
| D11 | 0 | 7.5V | Diode, Zener, 7.5 V, 550 mW, SMB | 1SMB5922BT3G | ON Semiconductor |
| J2, J3, J5 | 0 | | CONN SMA JACK STR EDGE MNT | CON-SMA-EDGE-S | RF Solutions Ltd. |
| R24 | 0 | 0 | RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06030000Z0EA | Vishay-Dale |
| R28, R35, R39 | 0 | 51 | RES, 51, 5%, 0.0625 W, 0402 | RC0402JR-0751RL | Yageo America |
| R29, R36 | 0 | 100 | RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW0603100RFKEA | Vishay-Dale |
| R42 | 0 | 49.9 | RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060349R9FKEA | Vishay-Dale |
| R45, R75 | 0 | 10k | RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW060310K0JNEA | Vishay-Dale |
| R46, R47, R48, R49, R50 | 0 | 33 | RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402 | CRCW040233R0JNED | Vishay-Dale |
| R59, R60 | 0 | 1.5k | RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603 | CRCW06031K50JNEA | Vishay-Dale |
| R78, R79, R82, R85, R86, R88, R90, R92, R94, R96, R99, R101, R103, R105, R109, R111, R113, R115, R117, R119, R121, R122, R125, R127, R129, R131, R133, R134, R135, R136, R137, R138, R139, R140, R141, R142, R143, R167, R169, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R189, R190, R191, R204, R205 | 0 | 49.9 | RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402 | ERJ-2RKF49R9X | Panasonic |
| R192, R193 | 0 | 100 | RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402 | CRCW0402100RFKED | Vishay-Dale |
| R207 | 0 | 0 | RES, 0, 5%, 0.1 W, 0603 | RC0603JR-070RL | Yageo |
| TP1, TP4, TP7, TP501 | 0 | | Test Point, Miniature, Red, TH | 5000 | Keystone |
| TP30 | 0 | | Test Point, Miniature, SMT | 5019 | Keystone |
| U4 | 0 | | CDC64XX-2520, DLF0006A (VSON-6) | CDC64XX-2520 | Texas Instruments |
| Y3 | 0 | | Crystal, Sealed Locked 50 MHz, 15 pF, SMD | 7X-50.000MBB-T | TXC Corporation |
| Y4 | 0 | | MERCURY+ 38.88MHz OCXO CMOS Oscillator 2.7 5 V 4-SMD | ROM9070PA | Rakon |

**Table 5-1. Bill of Materials (BOM) (continued)**

| DESIGNATOR | QTY | VALUE | DESCRIPTION | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|
| Y5 | 0 | | STANDARD OCXO 10 MHz Frequency | ROX2522S4 | Rakon |

## 5.1 Loop Filter and Vibration Nonsensitive Capacitors

The capacitors used on the EVM are X7R, which are ferromagnetic and, therefore, are sensitive to vibration due to the piezoelectric effect. TI recommends to use non-ferromagnetic capacitors such as NP0, C0G, or Tantalum for applications in which the best performance is required in the presence of vibration.

At and below 47 nF, C0G/NP0 capacitors are available in 0805 sized packages. For values 0.1 µF and above, Tantalum capacitors can be considered for vibration immune loop filter components.

**Table 5-2. Examples of Substitute Capacitors Which are Vibration Immune**

| CAPACITOR VALUE | VIBRATION SENSITIVE, X7R | VIBRATION IMMUNE |
|---|---|---|
| 3.3 nF | C0603C332K5RACTU, 0603 | GRM1885C1H332JA01D, C0G/NP0, 0603 |
| 33 nF | C0603C333J3RACTU, 0603 | C2012C0G1H333J125AA, C0G/NP0, 0805 |
| 47 nF | 06035C473JAT2A, 0603 | C0805X473G3GEC7800, C0G/NP0, 0805<br>C0805C473J3GACTU, C0G/NP0, 0805 |
| 0.1 µF | C0603C104J3RACTU, 0603 | GRM31C5C1E104JA01L, C0G/NP0, 1206<br>TAJR104K020RNJ, Tantalum, 0805 |
| 0.47 µF | GRM188R71A474KA61D, 0603 | F921C474MPA, Tantalum, 0805 |

# 6 Appendix A - TICS Pro LMK5C33414A Software

## 6.1 Using the Start Page

The Start page can be used to configure the PLLs for specific VCO frequencies and DPLL operation.
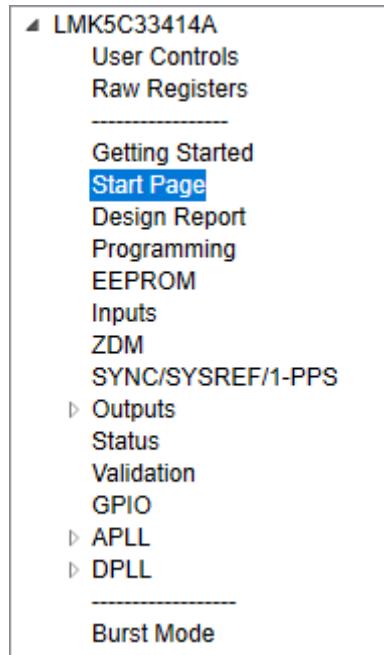


**Figure 6-1. Start Page Location**

### 6.1.1 Step 1

Set up the XO_P input frequency and interface type. Set up the input to the APLL by specifying the reference to each PLL and associated settings for PLL phase detector frequency.

### 6.1.2 Step 2

Set up the clock input frequencies and the interface type. Cascaded APLLs can also be assigned from this page using the PLL R-divider and phase detector preview to the right.



**Figure 6-2. Step 1 and 2: XO Input and Clock Inputs**

### 6.1.3 Step 3

Set the clock input select mode for the DPLLs, input priority, and maximum TDC frequency. The recommended Input Select Mode is *Auto Revertive*. REF0, REF1, REF2, and REF3 shown below correspond with IN0, IN1, IN2, and IN3, respectively. REF4 and REF5 priorities can be set if the DPLLs input is fed from one of the APLL post divider frequencies. The corresponding APLL is listed next to the REF4 and REF5. The REF with the highest priority is fed as the DPLL input.



**Figure 6-3. Step 3: DPLL Clock Input Selection**

### 6.1.4 Step 4

Set the clock output for ZDM. The PLL drives the PLL source mux for the selected output set for ZDM.
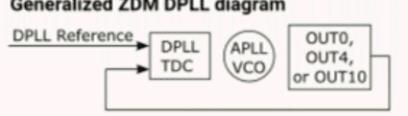


**Figure 6-4. Step 4: Zero Delay Mode**

### 6.1.5 Step 5

Enter the desired target frequencies for each output, as well as the desired output format, output source, whether the output is SYSREF, and whether the output is being used or not.

Press the *Calculate VCO Frequency Options* button to generate a list of possible VCO frequency combinations.



**Figure 6-5. Step 5: Clock Outputs**

Select a desired combination of VCO frequencies from the list of calculated values. If a specific VCO frequency is not in this list, a manual override can occur by selecting the *Enable User Override* checkbox and typing in the desired VCO frequencies. The *Copy to Selected VCO Frequency* box can also be used to copy the VCO frequency in the list selections to the VCO overrides.

Press the *Assign Selected VCO Settings to Device* button to update the VCO frequencies, then press the *Apply Output Clock Settings to Device* button. By default, the analog PLL frequencies are shown. The DPLL calculated frequency from step 6, however, results in exact output frequencies.

After the output frequency plan is calculated, make sure that a valid XO input is fed into the device so the APLLs can lock and generate the required frequencies. The device does not output any clocks until all enabled APLLs are locked.

### 6.1.6 Step 6

For step 6, simply enter the desired DPLL loop bandwidth.

---

**Note**

Any time an approximate symbol is shown, the user can move the mouse over the tool tip to see exact output frequency.

---



**Figure 6-6. Step 6: PLLs**

### 6.1.7 Step 7

To calculate the DPLL divider settings, select the desired DPLL loop filters and dividers and press the *Run Script* button. The software runs and calculates the necessary settings for the selected DPLL loop filters.



**Figure 6-7. Step 7: Run Script**

## 6.2 Using the Status Page

The Status page shows fields pertaining to the current status of the device. To update these fields, press the *Read Status Bits* button or the *Read RO Regs* button in the toolbar. The *Read RO Regs* button reads all read only registers which provides more information on other pages including the status fields but can take longer to read back. The read status bits just reads the status bits for this page.

For the DPLL to lock, a reference must be validated and selected in the *Active Reference/Holdover* and *Reference Validated* portions of the window shown in Figure 6-8.

As the DPLL locks, an expectation is to see the LOPL_DPLLx as the last bit to become clear when the phase lock is acquired.

When INT_EN = 1, any live status flag which occurs latches to the INTR Latched bit columns. These remains asserted until the *Clear Latched Bits* button is pressed. This gives additional insight into the behavior of the device.

Press the *Soft-chip reset* button in the toolbar to reset the device and restart the lock.



**Figure 6-8. Status Page**

## 6.3 Using the Input Page

The Input page provides a high-level view of all the inputs for the device, the APLL frequencies, and DPLL frequencies of the device.

When the DPLL dividers and loop filter are calculated by running the script in step 7 on the Start page, this page displays the DPLL divider values which set the DPLL frequency. This example shows that the DPLL frequency is the exact desired frequency.

Each DPLL supports two sets of DPLL dividers which can be selected. At this time, the tool calculates the divider for FB Config 1 only. To use two different feedback dividers, the following procedure needs to be preformed.

1. Div #1 settings can be copied into Div #2 settings and selected for use by the *DPLL Div Select* control.
2. The references that require the Div #2 settings needs to be set to FB Config 2.
3. The user can run a second calculation (re-perform a run script, step 7 on Start page, of the DPLL), which repopulates Div #1 settings with the new values for FB Config 1.
   a. Div #2 settings remains the same as the ones initial copied over in step 1.

When using both feedback dividers, the TDC rates do not have to be exactly the same, only that the TDC rates are within ±5% for the two DPLL feedback configurations.

## Inputs

DPLL1: SP   No input selected! Holdover!

Selected (Readback): 0: Holdove ▾   Auto Revertive ▾   REF0 ▾   Register ▾

**Reference Inputs**

| REF0 | 156.25 | MHz |
| REF1 | 10.0 | MHz |
| REF2 | 25.0 | MHz |
| REF3 | 1e-06 | MHz |

**DPLL1 R Div**
| 125 |
| 8 |
| 0 |
| 0 |
| 20 |
| 0 |

**REF Priority**
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |

**DPLL Div Select**
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |

Reference Doubler Enable

**DPLL1 Div#1**
| 4000 |
| 0 |
| 0 |

**DPLL1 Div#2**
| 4000 |
| 0 |
| 0 |

**APLL1**
SRC: VCO3 feedback ▾
| REF: | 1228.8 | MHz |
| PDF: | 122.88 | MHz |
| VCO: | 5000.0 | MHz |

**DPLL1**
| REF: | 10.0 | MHz |
| TDC: | 1.25 | MHz |
| VCO: | 5000.0 | MHz |

VCO1 Reference to other APLLs
1250.0 MHz ○ — 0 — ÷4

VCO1 Reference to other DPLLs
625.0 MHz — 0 — ÷8 ——— 5000.0 MHz

**XO Frequency**

48.0 MHz

XO_OUT_BUF_EN (Autoset)
9

DPLL2: HP   No input selected! Holdover!

Selected (Readback): 1: REF0 ▾   Auto revertive ▾   REF0 ▾   Register ▾

**DPLL2 R Div**
| 16 |
| 0 |
| 0 |
| 0 |
| 0 |
| 0 |

**REF Priority**
| 2nd ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |

**DPLL Div Select**
| FB Config 1 ▾ |
| FB Config 2 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |

Reference Doubler Enable

**DPLL2 Div#1**
| 576 |
| 0 |
| 0 |

**DPLL2 Div#2**
| 562 |
| 549755813888 |
| 0 |

**APLL2**
SRC: VCO3 feedback ▾
| REF: | 1228.8 | MHz |
| PDF: | 122.88 | MHz |
| VCO: | 5625.0 | MHz |

**DPLL2**
| REF: | 156.25 | MHz |
| TDC: | 9.765625 | MHz |
| VCO: | 5625.0 | MHz |

VCO2 Reference to other APLLs
1406.25 MHz ○ — 0 — ÷4

VCO2 Reference to other DPLLs
562.5 MHz — 0 — ÷10 ——— 5625.0 MHz

**Figure 6-9. APLL or DPLL Frequency Selection**

DPLL3: BAW   No input selected! Holdover!

Selected (Readback): 2: REF1 ▾   Auto revertive ▾   REF0 ▾   Register ▾

**DPLL3 R Div**
| 125 |
| 8 |
| 0 |
| 0 |
| 0 |
| 257 |

**REF Priority**
| 2nd ▾ |
| 1st ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |
| Not availa ▾ |

**DPLL Div Select**
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |
| FB Config 1 ▾ |

Reference Doubler Enable

**DPLL3 Div#1**
| 1966 |
| 87960930222 |
| 1099511627775 |

**DPLL3 Div#2**
| 245 |
| 835628837109 |
| 1099511627775 |

**APLL3**
SRC: XO ▾
| REF: | 48.0 | MHz |
| PDF: | 96.0 | MHz |
| VCO: | ~2457.600000 | MHz |

**DPLL3**
| REF: | 10.0 | MHz |
| TDC: | 1.25 | MHz |
| VCO: | 2457.6 | MHz |

VCO3 Reference to other APLLs
1228.8 MHz ○ — 3 — ÷2

VCO3 Reference to other DPLLs
614.4 MHz — 0 — ÷4 ——— 2457.6 MHz

**Figure 6-10. PLL3 Input**

### 6.3.1 Cascaded Configurations

Cascaded configurations can be created using the input page, where the relevant VCO buffers and dividers are automatically enabled by inferring the state of source selection registers.

At least one PLL must always be active and set to XO reference source for cascaded configurations to be valid. APLL start-up priority automatically chooses XO-source APLLs to start up before all other PLLs whenever possible. Start-up priority cannot be properly inferred, therefore users must set this priority themselves in the *User Controls* page if in pin-selection mode. In the example image below, APLL3 is referenced to XO input and APLL1 and APLL2 are referenced from APLL3. Priority is controlled in ascending order, with 0 first and 2 last. APLLs can share priorities; if all APLL priorities are set to 0, all APLLs start up simultaneously.



**Figure 6-11. Cascade APLL Start Priorities**

#### 6.3.1.1 Cascade VCO to APLL Reference

Cascading APLLs is controlled by the APLL source box, circled in Figure 6-12. This box is programmed bitwise and is automatically set when generating a frequency plan. The XO_OUT_BUF_EN register in the *Input Control* section of the *User Controls* tab is automatically set to enable or disable the XO Output Buffer. The PLLx_RDIV_XO_EN is automatically checked/unchecked in each APLLx tab depending on whether each APLL is using the XO input.
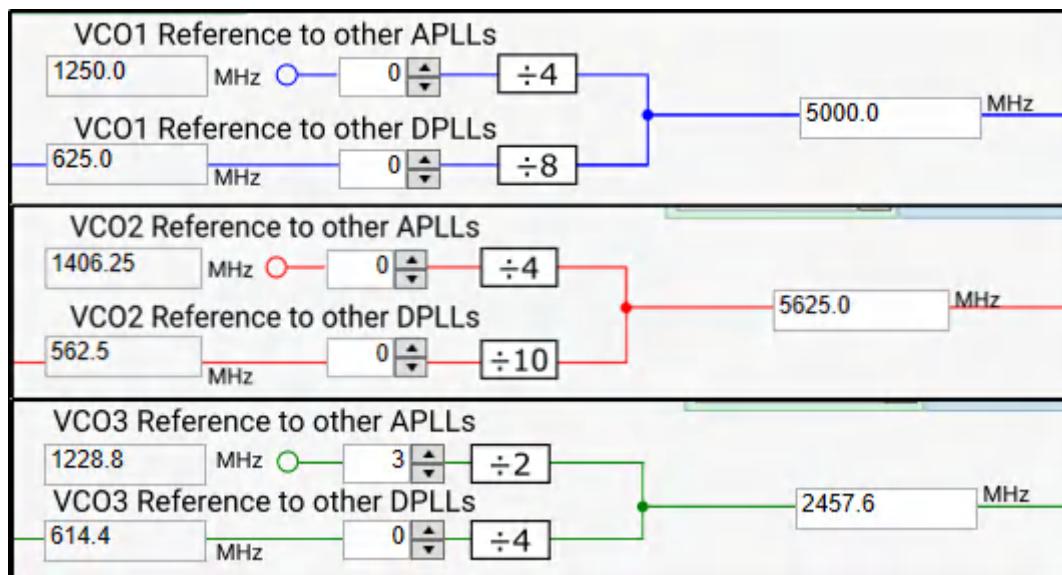


Located on Inputs page.

**Figure 6-12. APLL Source Box**

## 6.4 Using APLL1, APLL2, and APLL3 Pages

The APLL pages can be used to see detailed information on APLL behavior including the output dividers. A possibility is to type a VCO frequency into the PLL1 VCO frequency box (as shown in red circle) to have the fractional N value re-calculated.

When the DPLL is not used, the APLLs support an APLL-only mode with a programmable 24-bit denominator. Support for this mode is currently not implemented in the TICS Pro software.
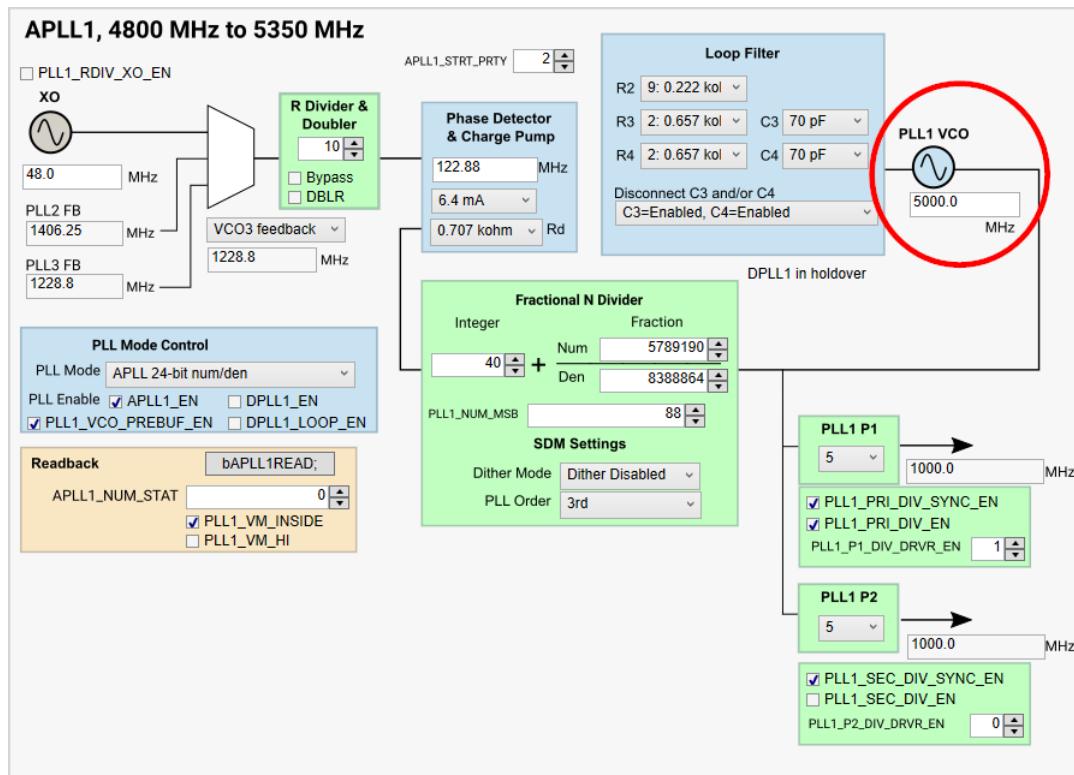


**Figure 6-13. APLL1 Page**

Figure 6-14 shows the post divider for PLL2. Figure 6-15 shows the post divider for PLL3. PLL3 supports all outputs of the LMK5C33414A.
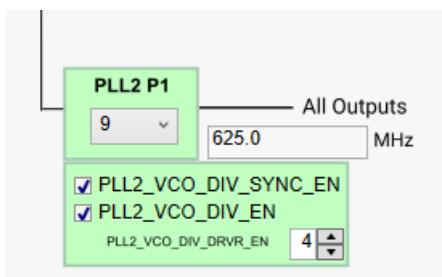


**Figure 6-14. PLL2 Post Divider**
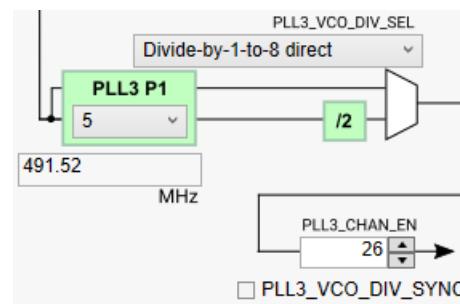


**Figure 6-15. PLL3 Dividers**

### 6.4.1 APLL DCO

To use the DCO shift controls on a given APLL, enter the DCO ppb step value into the *DCO Step Size (ppb)* box shown below. The entered step size is used to calculate a numerator deviation and a 2 s complement numerator deviation. To perform the shift, the increment or decrement button must be pressed. An increment writes the numerator deviation to the DPLLx_FREE_RUN control, which results in a positive frequency shift in the amount specified by the *DCO Step Size (ppb)*. An decrement writes the 2 s complement numerator deviation to the DPLLx_FREE_RUN control, which results in a negative frequency shift in the amount specified by the *DCO Step Size (ppb)*.

The slew rate at which the adjustment occurs is set on the DPLLx_HOLD_SLEW_STEP control. Make sure the DPLLx_HOLD_SLEW_STEP is NOT equal to 0, otherwise the adjustment does not occur. The recommended DPLLx_HOLD_SLEW_STEP value is 63 (maximum value). A value of 63 results in the fastest adjustment.
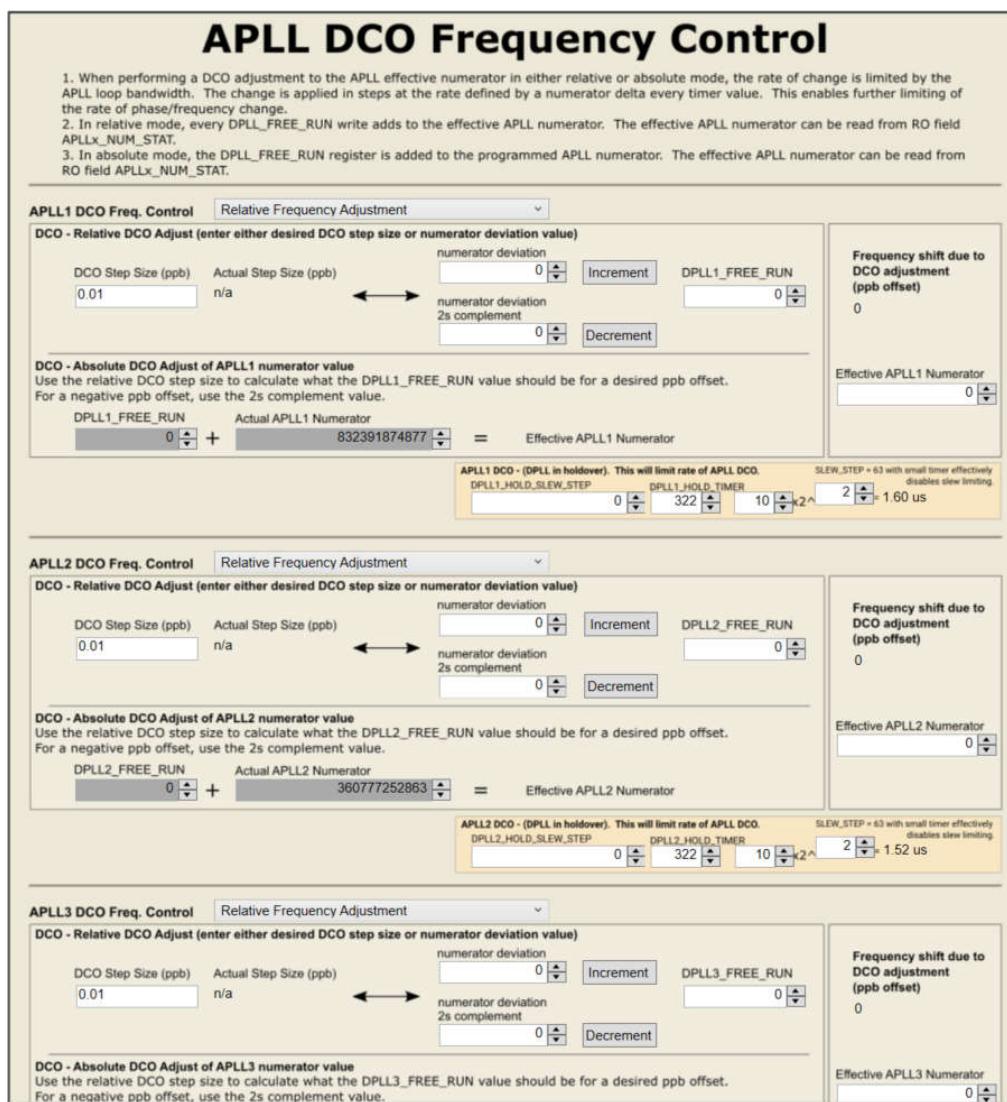


**Figure 6-16. APLL DCO Controls**

## 6.5 Using the DPLL1, DPLL2, and DPLL3 Pages

The DPLL pages contain many advanced controls that are normally set during the *Run Script* calculation.
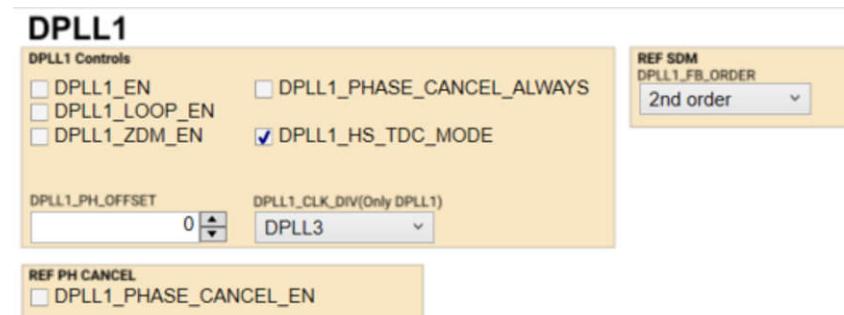


**Figure 6-17. Primary DPLL Controls**

## 6.6 Using the Validation Page

The Validation page allows you to enable/disable different detectors for reference validation along with DPLL frequency and phase lock requirements. Press the *Reassign All* button at the top of the page to recalculate the validation values.



**Figure 6-18. Validation Page**

### 6.6.1 DPLL DCO

To use the DCO shift controls on a given DPLL, enter the DCO ppb step value into the *DCO Step Size (ppb) box* shown below. The entered step size are used to calculate a frequency deviation that is applied to the DPLL numerator. This frequency deviation is shown in the DPLLx_FDEV control. To perform the shift, you must press the increment or decrement button.
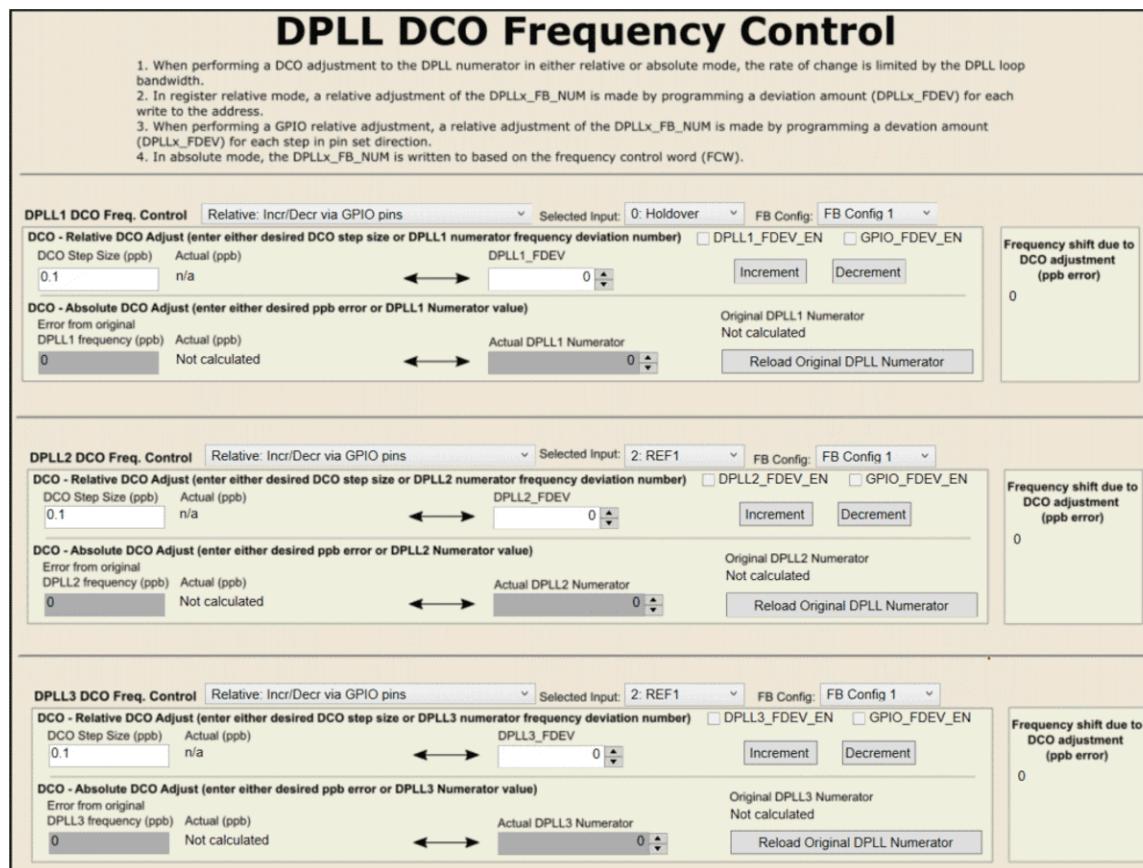


**Figure 6-19. DPLL DCO Controls**

## 6.7 Using the GPIO Page

The GPIO page allows users to configure the GPIO0, GPIO1, and GPIO2 pins.

When using SPI readback on the EVM, GPIO2 must be configured as *STATUS or INT…* and *SDO output*. When using the device in I$^2$C mode, refer to Section 3.3.
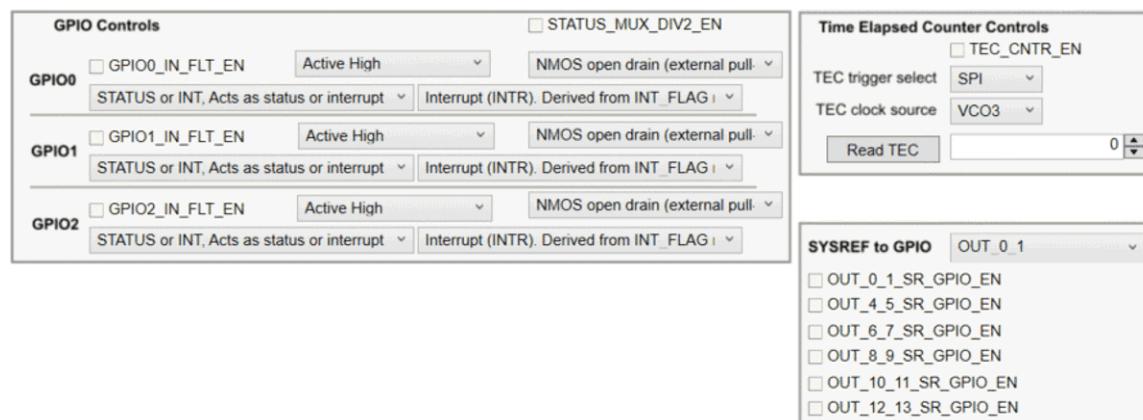


**Figure 6-20. GPIO Page**

## 6.8 SYNC/SYSREF/1-PPS Page

The SYNC/SYSREF/1-PPS page shows all the SYSREF block settings and allows the user to configure the GPIO1 or GPIO2 for continuous SYSREF or 1-PPS clock output.

The SYSREF divider output signals can be replicated on either GPIO1 and GPIO2 to provide additional single-ended, 3.3-V CMOS clocks after start-up if desired. To configure the SYSREF/1PPS output replication, the GPIO must be enabled as an output (GPIOx_OUTEN = 1) and one of the SYSREF output to GPIO replication sources must be active. The SYSREF replication source comes from any one of the SYSREF dividers in use from OUT0/1, OUT4/5, OUT6/7, OUT/9, OUT10/11 or OUT12/13 by register programming (OUT_x_y_SR_GPIO_EN = 1 and GPIO_SYSREF_SEL to the appropriate OUT_x_y). The GPIOx replicated SYSREF output is a continuous frequency. Pulsed SYSREF mode is not supported for the GPIOx replica outputs.

**Figure 6-21. SYNC/SYSREF/1-PPS Page**

## 6.9 Using the Outputs Page

The Outputs page shows all the possible source frequencies to the output channels. To simplify settings fields necessary to providing an output frequency, a source mux lists all possible sources for each output. Be sure to enable or disable the desired outputs on the right-hand side of the screen.

There are many detailed output pages beneath the Outputs page that show the individual controls for each set of outputs.

The black box around OUT2 to OUT3, OUT4 to OUT7, and OUT8 to OUT13 signifies that all these outputs needs to be sourced from the same VCO.
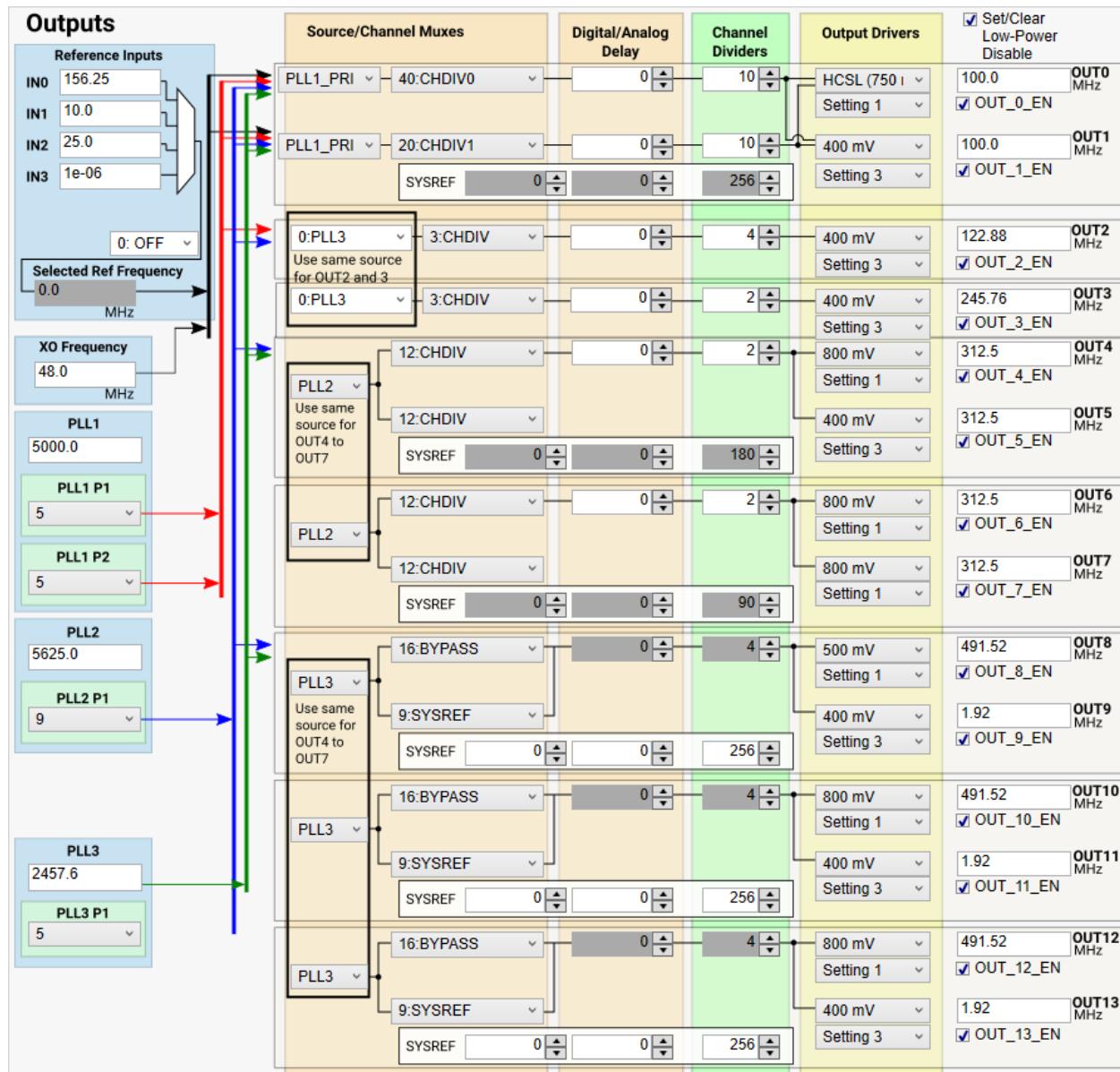


**Figure 6-22. Outputs Page**

## 6.10 EEPROM Page

The EEPROM page is used to write the currently loaded device settings into the device EEPROM. To program the EEPROM, press the *Program EEPROM* button.

Press the *Register commit method* button to display the registers that is written to the EEPROM. The register sequence populates under the OUTPUT section of Figure 6-23, where the user can copy the sequence and use to program the device with a personal tool if the user does not want to use the TICS Pro GUI.



**Figure 6-23. EEPROM Page**

## 6.11 Design Report Page

The Design Report page shows an overview of the current profile settings.

**Design Report**

| Generate Design Report | Save design report text to file |

--== Design Report ==--  Press Generate Design Report to update report
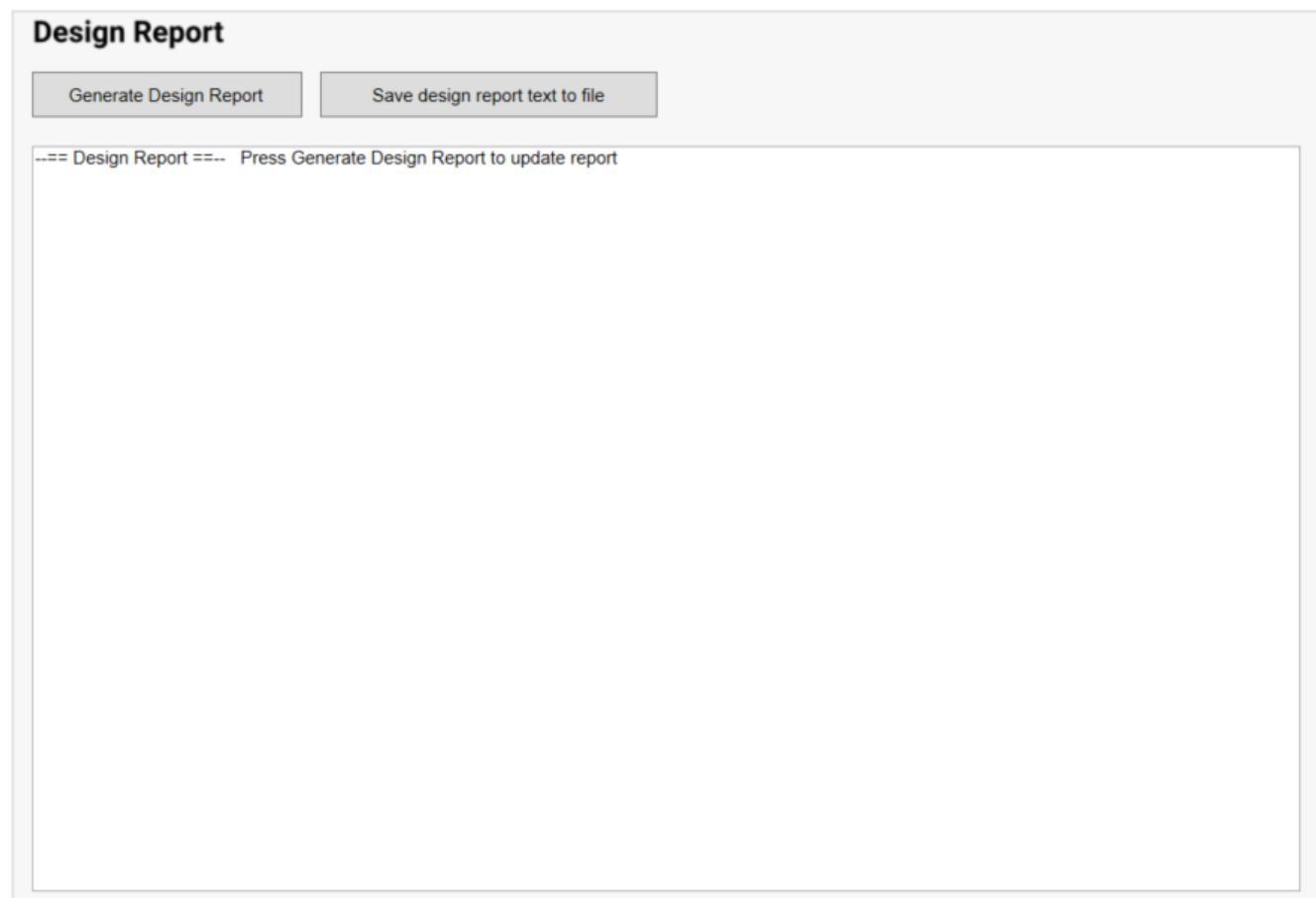
**Figure 6-24. Design Report Page**

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