User's Guide

DS160PR1601 and DS320PR1601 Programming Guide

ABSTRACT

This document provides a programming reference for the DS160PR1601 16-Lane PCI-Express Gen-4 Linear Redriver and the DS320PR1601 16-Lane PCI-Express Gen-5 Linear Redriver. This document contains detailed information related to the DS160PR1601 and DS320PR1601 advanced configuration options. The intended audience includes software engineers working on system diagnostics and control software.

TI recommends that the reader be familiar with the *DS160PR1601 16 Gbps 16-Lane Linear Redriver for PCIe 4.0 Data Sheet* for DS160PR1601 users, or the *DS320PR1601 32 Gbps 16-Lane Linear Redriver for PCIe 5.0 Data Sheet* for DS320PR1601 users. These documents and all other collateral data related to the DS160PR1601 redriver and DS320PR1601 redriver (application notes, models, and so forth) are available to download from the TI website. Alternatively, contact your local Texas Instruments field sales representative.

Table of Contents

List of Tables

Trademarks

1 Access Methods

There are two ways to access the DS160PR1601 and DS320PR1601 registers. The two methods are:

- Register control through the Serial Management Bus (SMBus/I^2C)
- Automatic configuration through an external EEPROM

The DS160PR1601 and DS320PR1601 consist of eight individual I^2C addresses to configure all 16 lanes of the redriver. Each address pair configures 8 channels.

Table 1-1. DS160PR1601 and DS320PR1601 Address Mapping

x_ADDR1_x Pin Level	x_ADDR0_x Pin Level	Bank 0: Channels 0-3: 7-Bit Address [HEX]	Bank 1: Channels 4-7: 7-Bit Address [HEX]
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L0	L4	Reserved	Reserved
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L1	L4	Reserved	Reserved
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L2	L4	Reserved	Reserved
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37

1.1 Typical PCIe x16 Lane to DS160PR1601 and DS320PR1601 Channel Mapping

The example below demonstrates the PCIe lane to DS160PR1601/DS320PR1601 channel mapping in a typical PCIe x16 application using the DS160PR1601 or DS320PR1601.

Table 1-2. Downstream: CPU -> DS160PR1601/DS320PR1601 A-Side -> Endpoint

PCIe Lane	DS160PR1601 Channel	I²C ADDR CONFIG PINS		Channel Bank	Example I²C Address	Bank Channel#	PD Pin Control
0	A_PEx0	A_ADDR1_7-0 {Example Pin State = L0}	A_ADDR0_7-0 {Example Pin State = L0}	0	18h	0	PD_3_0
1	A_PEx1				18h	1	PD_3_0
2	A_PEx2				18h	2	PD_3_0
3	A_PEx3				18h	3	PD_3_0
4	A_PEx4			1	19h	4	PD_7_4
5	A_PEx5				19h	5	PD_7_4
6	A_PEx6				19h	6	PD_7_4
7	A_PEx7				19h	7	PD_7_4
8	A_PEx8	A_ADDR1_15-8 {Example Pin State = L0}	A_ADDR0_15-8 {Example Pin State = L1}	0	1Ah	0	PD_11_8
9	A_PEx9				1Ah	1	PD_11_8
10	A_PEx10				1Ah	2	PD_11_8
11	A_PEx11				1Ah	3	PD_11_8
12	A_PEx12			1	1Bh	4	PD_15_12
13	A_PEx13				1Bh	5	PD_15_12
14	A_PEx14				1Bh	6	PD_15_12
15	A_PEx15				1Bh	7	PD_15_12

Table 1-3. Upstream: Endpoint-> DS160PR1601/DS320PR1601 B-Side -> CPU

PCIe Lane	DS160PR1601 Channel	I²C ADDR CONFIG PINS		Channel Bank	Example I²C Address	Bank Channel#	PD Pin Control
0	B_PEx0	B_ADDR1_7-0 {Example Pin State = L0}	B_ADDR0_7-0 {Example Pin State = L2}	1	1Dh	7	PD_7_4
1	B_PEx1				1Dh	6	PD_7_4
2	B_PEx2				1Dh	5	PD_7_4
3	B_PEx3				1Dh	4	PD_7_4
4	B_PEx4			0	1Ch	3	PD_3_0
5	B_PEx5				1Ch	2	PD_3_0
6	B_PEx6				1Ch	1	PD_3_0
7	B_PEx7				1Ch	0	PD_3_0
8	B_PEx8	B_ADDR1_15-8 {Example Pin State = L0}	B_ADDR0_15-8 {Example Pin State = L3}	1	1Fh	7	PD_15_12
9	B_PEx9				1Fh	6	PD_15_12
10	B_PEx10				1Fh	5	PD_15_12
11	B_PEx11				1Fh	4	PD_15_12
12	B_PEx12			0	1Eh	3	PD_11_8
13	B_PEx13				1Eh	2	PD_11_8
14	B_PEx14				1Eh	1	PD_11_8
15	B_PEx15				1Eh	0	PD_11_8

1.2 Device Configuration Through External EEPROM

The DS160PR1601 and DS320PR1601 can automatically read its initial configuration from the EEPROM at power up. Detailed information on EEPROM hex file generation for this device is applicable in the *Understanding EEPROM Programming for PCI-Express Gen-4 Redrivers*.

2 Register Mapping

The DS160PR1601 and DS320PR1601 have two types of registers:

- **Share Registers** – These registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers** – These registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group via broadcast writes to bank 0 or bank 1.

2.1 Share Registers

Table 2-1. General Register (Offset = 0xE2) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	rst_i2c_regs	R/W/SC	0x0	Device Reset Control: Reset all I^2C registers to default values (self- clearing).
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	frc_eeprm_rd	R/W/SC	0x0	Override MODE and READ_EN_N status to force manual EEPROM Configuration Load.

Table 2-2. DEVICE_ID0 Register (Offset = 0xF0) [reset = 0x06]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	device_id0_3	R	0x0	Device ID0 [3:1]: 011
2	device_id0_2	R	0x1	see MSB
1	device_id0_1	R	0x1	see MSB
0	RESERVED	R	X	Reserved

Table 2-3. DEVICE_ID1 Register (Offset = 0xF1) [reset = 0x28]

Bit	Field	Type	Reset	Description
7	device_id[7]	R	0x0	Device ID 0010 1000: DS160PR1601, DS320PR1601
6	device_id[6]	R	0x0	see MSB
5	device_id[5]	R	0x1	see MSB
4	device_id[4]	R	0x0	see MSB
3	device_id[3]	R	0x1	see MSB
2	device_id[2]	R	0x0	see MSB
1	device_id[1]	R	0x0	see MSB
0	device_id[0]	R	0x0	see MSB

2.2 Channel Registers

The DS160PR1601 and DS320PR1601 feature two banks of channels for sides A and B, Bank 0 (Channels 0-3) and Bank 1 (Channels 4-7), each featuring a separate register set and requiring a unique SMBus secondary address.

Table 2-4. Channel Register Base Address Mapping

Channel Registers Base Address	Channel Bank 0 Access	Channel Bank 1 Access
0x00	Channel 0 registers	Channel 4 registers
0x20	Channel 1 registers	Channel 5 registers
0x40	Channel 2 registers	Channel 6 registers
0x60	Channel 3 registers	Channel 7 registers
0x80	Broadcast write channel bank 0 registers, read channel 0 registers	Broadcast write channel bank 1 registers, read channel 4 registers
0xA0	Broadcast write channel 0-1 registers, read channel 0 registers	Broadcast write channel 4-5 registers, read channel 4 registers
0xC0	Broadcast write channel 2-3 registers, read channel 2 registers	Broadcast write channel 6-7 registers, read channel 6 registers
0xE0	Bank 0 Share registers	Bank 1 Share registers

Table 2-5. RX Detect Status Register (Channel register base + Offset = 0x00) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	rx_det_comp_p	R	0x0	Rx Detect Positive Polarity Status: 0: Not detected 1: Detected - the value is latched.
6	rx_det_comp_n	R	0x0	Rx Detect Negative Polarity Status: 0: Not detected 1: Detected - the value is latched.
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

Table 2-6. EQ Control Register (Channel register base + Offset = 0x01) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	eq_stage1_bypass	R/W	0x0	Enable EQ Stage 1 Bypass: 0: Bypass disabled 1: Bypass enabled
6	eq_stage11_3	R/W	0x0	EQ Boost Stage 1 Control. For details, see the device-specific data sheet.
5	eq_stage1_2	R/W	0x0	
4	eq_stage1_1	R/W	0x0	
3	eq_stage1_0	R/W	0x0	
2	eq_stage2_2	R/W	0x0	EQ Boost Stage 2 Control. For details, see the device-specific data sheet.
1	eq_stage2_1	R/W	0x0	
0	eq_stage2_0	R/W	0x0	

Table 2-7. Mute EQ Control Register (Channel register base + Offset = 0x02) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	mute_eq	R/W	0x0	Mute EQ output
2	RESERVED	R	0x1	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x1	Reserved

Table 2-8. EQ Gain / Flat Gain Control Register (Channel register base + Offset = 0x03) [reset = 0x5]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	eq_profile_3	R/W	0x0	EQ mid-frequency boost profile For details, see the device-specific data sheet.
5	eq_profile_2	R/W	0x0	
4	eq_profile_1	R/W	0x0	
3	eq_profile_0	R/W	0x0	
2	Flat_gain_2	R/W	0x1	Flat Gain Select. For details, see the device-specific data sheet.
1	Flat_gain_1	R/W	0x0	
0	Flat_gain_0	R/W	0x1	

Table 2-9. RX Detect Control Register (Channel register base + Offset = 0x04) [reset = 0x0]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	mr_rx_det_man	R/W	0x0	Manual override of rx_detect_p/n decision: 0: Rx Detect state machine is enabled 1: Rx Detect state machine is overridden – always valid Rx termination detected
1	en_rx_det_count	R/W	0x0	Enable additional RX detect polling: 0: Additional Rx Detect Polling disabled 1: Additional Rx detect Polling enabled
0	sel_rx_det_count	R/W	0x0	Select number of Valid Rx detect polls - gated by en_rx_det_count = 1. 0: 2x consecutive valid detections 1: 3x consecutive valid detections

Table 2-10. PD Override Register (Channel register base + Offset = 0x05) [reset = 0x3F]

Bit	Field	Type	Reset	Description
7	Device_en_override	R/W	0x0	Enable power down overrides through SMBus/I2C 0: Manual override disabled 1: Manual override enabled
6:0	Device_en	R/W	0x111111	Manual power down of redriver various blocks – gated by device_en_override = 1 000000: All blocks are disabled 111111: All blocks are enabled

Table 2-11. Bias Register (Channel register base + Offset = 0x06) [reset = 0x20]

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	bias_current_2	R/W	0x1	Control bias current
4	bias_current_1	R/W	0x0	See MSB.
3	bias_current_0	R/W	0x0	See MSB.
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

3 Equalization Control Settings

Table 3-1. CTLE Index Equalization Settings

Equalization Setting					Typical EQ Boost (dB)	
	SMBus/I2C Mode					
EQ Index	EQ Control Register Eq_stage1_3:0	EQ Control Register Eq_stage2_2:0	EQ GAIN / Flat Gain Control Register Eq_profile_3:0	EQ Control Register Eq_stage1_bypass	@ 8 GHz	@ 16 GHz (DS320PR1601 only)
0	0	0	0	1	For values, see the device-specific data sheet	For values, see the device-specific data sheet
1	1	0	0	1		
2	3	0	0	1		
Default	0	0	0	0		
5	0	0	1	0		
6	1	0	1	0		
7	2	0	1	0		
8	3	0	3	0		
9	4	0	3	0		
10	5	1	7	0		
11	6	1	7	0		
12	8	1	7	0		
13	10	1	7	0		
14	10	2	15	0		
15	11	3	15	0		
16	12	4	15	0		
17	13	5	15	0		
18	14	6	15	0		
19	15	7	15	0		

4 CTLE Index and Flat Gain Selection Matrix

Table 4-1. CTLE Index/Flat Gain Setting Matrix

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
0	-6dB	0x80	0x00
0	-4dB	0x80	0x01
0	-2dB	0x80	0x03
0	0dB(Default)	0x80	0x05
0	2dB	0x80	0x07
1	-6dB	0x88	0x00
1	-4dB	0x88	0x01
1	-2dB	0x88	0x03
1	0dB(Default)	0x88	0x05
1	2dB	0x88	0x07
2	-6dB	0x98	0x00
2	-4dB	0x98	0x01
2	-2dB	0x98	0x03
2	0dB(Default)	0x98	0x05
2	2dB	0x98	0x07
Default	-6dB	0x00	0x00
Default	-4dB	0x00	0x01
Default	-2dB	0x00	0x03
Default	0dB(Default)	0x00	0x05
Default	2dB	0x00	0x07
5	-6dB	0x00	0x08
5	-4dB	0x00	0x09
5	-2dB	0x00	0x0B
5	0dB(Default)	0x00	0x0D
5	2dB	0x00	0x0F
6	-6dB	0x08	0x08
6	-4dB	0x08	0x09
6	-2dB	0x08	0x0B
6	0dB(Default)	0x08	0x0D
6	2dB	0x08	0x0F
7	-6dB	0x10	0x08
7	-4dB	0x10	0x09
7	-2dB	0x10	0x0B
7	0dB(Default)	0x10	0x0D
7	2dB	0x10	0x0F
8	-6dB	0x18	0x18
8	-4dB	0x18	0x19
8	-2dB	0x18	0x1B
8	0dB(Default)	0x18	0x1D
8	2dB	0x18	0x1F
9	-6dB	0x20	0x18
9	-4dB	0x20	0x19
9	-2dB	0x20	0x1B
9	0dB(Default)	0x20	0x1D
9	2dB	0x20	0x1F

Table 4-1. CTLE Index/Flat Gain Setting Matrix (continued)

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
10	-6dB	0x29	0x38
10	-4dB	0x29	0x39
10	-2dB	0x29	0x3B
10	0dB(Default)	0x29	0x3D
10	2dB	0x29	0x3F
11	-6dB	0x31	0x38
11	-4dB	0x31	0x39
11	-2dB	0x31	0x3B
11	0dB(Default)	0x31	0x3D
11	2dB	0x31	0x3F
12	-6dB	0x41	0x38
12	-4dB	0x41	0x39
12	-2dB	0x41	0x3B
12	0dB(Default)	0x41	0x3D
12	2dB	0x41	0x3F
13	-6dB	0x51	0x38
13	-4dB	0x51	0x39
13	-2dB	0x51	0x3B
13	0dB(Default)	0x51	0x3D
13	2dB	0x51	0x3F
14	-6dB	0x52	0x78
14	-4dB	0x52	0x79
14	-2dB	0x52	0x7B
14	0dB(Default)	0x52	0x7D
14	2dB	0x52	0x7F
15	-6dB	0x5B	0x78
15	-4dB	0x5B	0x79
15	-2dB	0x5B	0x7B
15	0dB(Default)	0x5B	0x7D
15	2dB	0x5B	0x7F
16	-6dB	0x64	0x78
16	-4dB	0x64	0x79
16	-2dB	0x64	0x7B
16	0dB(Default)	0x64	0x7D
16	2dB	0x64	0x7F
17	-6dB	0x6D	0x78
17	-4dB	0x6D	0x79
17	-2dB	0x6D	0x7B
17	0dB(Default)	0x6D	0x7D
17	2dB	0x6D	0x7F
18	-6dB	0x76	0x78
18	-4dB	0x76	0x79
18	-2dB	0x76	0x7B
18	0dB(Default)	0x76	0x7D
18	2dB	0x76	0x7F
19	-6dB	0x7F	0x78
19	-4dB	0x7F	0x79

Table 4-1. CTLE Index/Flat Gain Setting Matrix (continued)

CTLE Index	Flat Gain	Reg. Range Offset 0x01	Reg. Range Offset 0x03
19	-2dB	0x7F	0x7B
19	0dB(Default)	0x7F	0x7D
19	2dB	0x7F	0x7F

5 Programming Examples

In the examples below, assume Device Secondary Address 0x18 is used for Bank0(Channels 0-3) and address 0x19 is used for Bank1(Channels 4-7). Example code using TotalPhase Aardvark I2C controller.

- ***PD/PD1 control via register programming***
  - Broadcast write to Channel Bank 0 and Bank1 registers at Channel register 0x85(Channel base register 0x80 + PD Override register 0ffset 0x05) with value of 0x80 to **power down** all channels.
    - <i2c_write addr="0x18" count="0" radix"16">85 80</i2c_write>
    - <i2c_write addr="0x19" count="0" radix"16">85 80</i2c_write>
  - Broadcast write to Channel Bank 0 and Bank1 registers at Channel register 0x85(Channel base register 0x80 + PD Override register 0ffset 0x05) with value of 0x7F to **power on** all channels.
    - <i2c_write addr="0x18" count="0" radix"16">85 7F</i2c_write>
    - <i2c_write addr="0x19" count="0" radix"16">85 7F</i2c_write>
- ***Broadcast Channel CTLE Index/Flat Gain Selection via register programming (CTLE Index 2, FlatGain 0dB)***

  To select CTLE Index 2 with flat Gain of 0B on all channels:

  - Broadcast write to Channel Bank 0 and Bank1 registers at Channel register 0x81(Channel base register 0x80 + EQ Control register 0ffset 0x01) with value of 0x98.
  - Broadcast write to Channel Bank 0 and Bank1 registers at Channel register 0x83(Channel base register 0x80 + EQ/Gain Control register 0ffset 0x03) with value of 0x05
    - <i2c_write addr="0x18" count="0" radix"16">81 98</i2c_write>
    - <i2c_write addr="0x18" count="0" radix"16">83 05</i2c_write>
    - <i2c_write addr="0x19" count="0" radix"16">81 98</i2c_write>
    - <i2c_write addr="0x19" count="0" radix"16">83 05</i2c_write>
- ***Individual Channel CTLE Index / Flat Gain Selection via register programming (CTLE Index 2, FlatGain 0dB)***

  To select CTLE Index 2 with flat Gain of 0B on a single channel (Channel 0):

  - Write to Channel 0 register on Bank 0 and Bank 1 registers at Channel register 0x01(Channel 0 base register 0x00 + EQ Control register 0ffset 0x01) with value of 0x98.
  - Write to Channel 0 register on Bank 0 and Bank1 registers at Channel register 0x03(Channel 0 base register 0x00 + EQ/Gain Control register 0ffset 0x03) with value of 0x05
    - <i2c_write addr="0x18" count="0" radix"16">01 98</i2c_write>
    - <i2c_write addr="0x18" count="0" radix"16">03 05</i2c_write>
    - <i2c_write addr="0x19" count="0" radix"16">01 98</i2c_write>
    - <i2c_write addr="0x19" count="0" radix"16">03 05</i2c_write>

6 References

- Texas Instruments: *DS160PR1601 16 Gbps 16-Lane Linear Redriver for PCIe 4.0 Data Sheet*
- Texas Instruments: *DS320PR1601 32 Gbps 16-Lane Linear Redriver for PCIe 5.0 Data Sheet* (SNLS683)
- Texas Instruments: *Understanding EEPROM Programming for PCI-Express Gen-4 Redrivers*

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2023) to Revision A (June 2023)	Page
• Updated the Abstract in this document	1
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updated Section 1	2
• Updated Section 1.1	3
• Added Section 1.2	3
• Updated Section 2	4
• Updated Section 2.1	4
• Updated Section 2.2	5
• Updated Section 3	7
• Updated Section 4	8

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