DS92LV3241/DS92LV3242 Demonstration Kit User Manual

P/N LV32EVK01

Rev 1.0

Table of Contents

Introduction:

National Semiconductor's SERDES evaluation kit contains one (1) DS92LV3241 Serializer (Tx) board, one (1) DS92LV3242 Deserializer (Rx) board, and one (1) standard (~2) meter CAT 6 style cable assembly.
Note: *The demo boards are not intended for EMI testing. These demo boards were designed for easy accessibility to device pins with tap points for monitoring or applying signals, and additional pads for termination.*

The DS92LV3241/3242 chipset supports a variety of display and imaging applications. Typical applications include: navigation displays, automated teller machines (ATMs), POS, video cameras, global positioning systems (GPS), portable equipment/instruments, factory automation, printers, etc.

The DS92LV3241 and DS92LV3242 can also be used as a 32-bit general purpose LVDS Serializer and Deserializer chipset designed to transmit data at clocks speeds ranging from 20 to 50 MHz in dual mode or 40MHz to 85 MHz in quad mode.

The DS92LV3241 serializer board accepts LVCMOS input signals at either 3.3V or 1.8V.
Note: *IOV_{DD} must be set to 3.3V for 3.3V input levels or 1.8V for 1.8V input levels.*

The LVDS Serializer converts the LVCMOS parallel lines into either two (2) serialized LVDS data pairs with an embedded LVDS clock on each channel or four (4) serialized LVDS data pairs with an embedded LVDS clock on each channel.

The DS92LV3242 deserializer board accepts the LVDS serialized data streams with an embedded clock on each LVDS stream and converts the data back into parallel LVCMOS signals and clock. Note that NO reference clock is needed to prevent harmonic lock as with other devices currently on the market.

Suggested equipment to evaluate the chipset include: an LVCMOS signal source, such as a video generator, word generator, or pulse generator and oscilloscope.

The user needs to provide the proper LVCMOS clock and data inputs to the serializer and also provide a proper interface from the deserializer output to an LCD panel or test equipment. The serializer and deserializer boards can also be used to evaluate device parameters.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

Contents of the Evaluation Kit:

1) One serializer board with the DS92LV3241
2) One deserializer board with the DS92LV3242
3) One 2-meter standard CAT 6 cable assembly
4) Evaluation Kit Documentation (this manual)
5) DS92LV3241/3242 Datasheet

How to set up the Evaluation Kit:

The PCB routing for the serializer input pins (TxIN) have been laid out to accept incoming LVCMOS signals from a 50-pin IDC connector. The serial interface between the DS92LV3241 and the DS92LV3242 uses a standard RJ-45 connector and CAT-5/6 cable assembly (small CAT-6 cable provided). The PCB routing for the Rx output pins (RxOUT) are accessed through a 50-pin IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) A two (2) meter CAT 6 connector/cable assembly has been included in the kit. Connect one side of cable to the serializer board and the other side to the deserializer board. This completes the LVDS interface connection.

2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration Settings for more details. From the transmitting test equipment, connect a flat cable or fly wires (not supplied) to the Serializer board and connect another flat cable or fly wires (not supplied) from the Deserializer board to the receiving test equipment. Caution: The LVCMOS input levels should be within the specified range for optimal performance, not to exceed the absolute maximum rating of -0.3V to (V_{DD} +0.3V).
   Note: For 50 ohm signal sources, add 50 ohm parallel termination resistors R1-R32 on the DS92LV3241 Serializer board and provide appropriate 3.3V LVCMOS input signal levels into TxIN[32:0] and TxCLKIN.
   Note: The Rx board may require the use of LVCMOS buffers to drive 50 ohm inputs found in some test equipment.

3) Power for the Tx and Rx boards must be supplied externally through Power Jack (V_{DD}). Grounds for both boards are connected through Power Jack (V_{SS}) (see section below).

Power Connection:

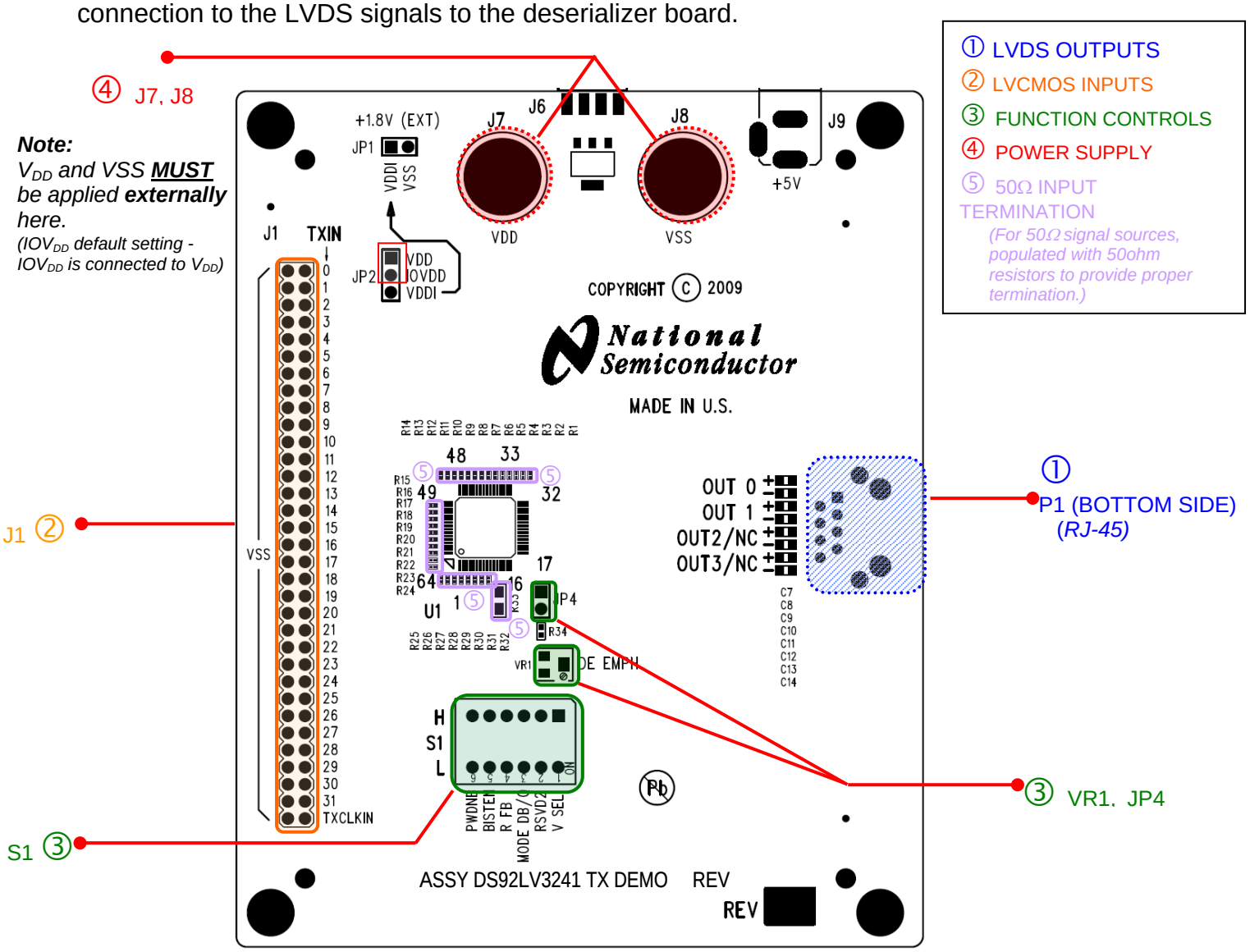
The serializer and deserializer boards must be powered by supplying power externally through J7 (V_{DD}) and J8 (V_{SS}) on the serializer Board and J6 (VDD) and J7 (VSS) on the deserializer board. Note +4V is the absolute MAXIMUM voltage (not operating voltage) that should ever be applied to the serializer (DS92LV3241) or deserializer (DS92LV3242) VDD terminal. Damage to the device(s) can result if the voltage maximum is exceeded.

Serializer (Tx) Board Description:

The 50-pin IDC connector J1 accepts 32 bits of LVCMOS RGB/generic data (TxIN0-TxIN32) along with the clock input (TCLK).

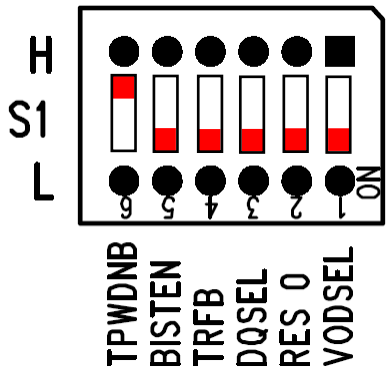
The SERDES serializer board is powered externally from the J7 (V_{DD}) and J8 (V_{SS}) connectors shown below. For the serializer to be operational, the Power Down (PWDNB) switch on S1 must be set HIGH. The board is factory configured (with series 0.1µF capacitors on the LVDS outputs. Rising or falling edge input clock is also selected on S1-TRFB: HIGH (rising) or LOW (falling). JP2 is configured from the factory to be tied to V_{DD} (3.3V), which sets the LVCMOS I/O pins to operate at 3.3V logic levels.

The RJ-45 connector P1 (on the bottom side of the board) provides the interface connection to the LVDS signals to the deserializer board.

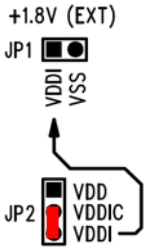
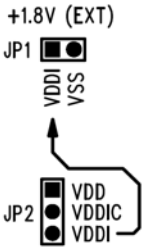


Configuration Settings for the Serializer Board

S1: Serializer Input Features Selection

Reference	Description	Input = L	Input = H	S1
PWDNB	**P**o**W**er**D**ow**N** **B**ar	Powers Down	Normal operation **(Default)**	
BISTEN	**BIST EN**able	BIST mode disabled **(Default)**	BIST mode enabled	
TRFB	Latch input data on **R**ising or **F**alling edge of TCLK	Falling Edge **(Default)**	Rising Edge	
MODE DB/Q	**D**ual or **Q**uad mode	Dual mode **(Default)**	Quad mode	
RES_0	**RES**erved	MUST be tied low for normal operation **(Default)**	Not allowed	
V SEL	LVDS output **V_{OD}** **SEL**ect	≈440 mV_{P-P} **(Default)**	≈850 mV_{P-P}	

JP2: Serializer Input Features Selection

Reference	Description	Default	External	JP2
IOVDD	1.8V input option. For 1.8V input swing IOVDD is connected to VDDI. VDDI must be applied on JP1 pin 1.	Connected to VDD (J7) 		

JP4,VR1: Pre-Emphasis Feature Selection

Reference	Description	OPEN (floating)	CLOSED (Path to GND)	
JP4	Pre-Emphasis – helps to increase the eye pattern opening in the LVDS streams by providing current boost	Disabled – no jumper **(Default)** 	Enabled – With jumper 	
JP4 & VR1	Pre-Emphasis adjustment (via screw) JP1 **MUST** have a jumper to use VR1 potentiometer. VR1 = 0Ω to 20 kΩ, JP1 + VR1 + 12 kΩ *(R34)* = ~12 kΩ (maximum pre-emphasis) to ~32 kΩ (minimum pre-emphasis*). $I_{PRE} = [1.2/(R_{PRE})] \times 40$, $R_{PRE\ (minimum)} \geq 12\ k\Omega$ **Note: maximum is based on resistor value. In this case ~32KΩ value is based on the ~12kΩ fixed resistor plus ~20KΩ maximum potentiometer value. User can use hundreds of k Ohms to reduce the pre-emphasis value.*	Clockwise  increases R_{PRE} value which decreases pre-emphasis	Counter-Clockwise  decreases R_{PRE} value which increases pre-emphasis		

Pre-emphasis user note:
Pre-emphasis must be adjusted correctly based on application frequency, cable quality, cable length, and connector quality. Maximum pre-emphasis should only be used under worse case conditions; for example at the upper frequency specification of the part and/or low grade cables at maximum cable lengths. Typically all that is needed is minimum pre-emphasis. Users should start with no pre-emphasis first and gradually apply pre-emphasis until there is clock lock and no data errors. The best way to monitor the pre-emphasis effect is to hook up a differential probe across the AC-coupling capacitors for the (+) and (-) inputs of the LVDS channels on the DS92LV3242 Rx demo board (NOT across the AC-coupling capacitors for the LVDS channels on the DS92LV3241 Tx demo board).

Serializer LVCMOS and LVDS Pinout by IDC Connector

The following two (2) tables illustrate how the serializer inputs are mapped to the IDC connector J1, the LVDS outputs on the RJ-45 connector P1 pinout.
Note: Labels are also printed on the demo boards for both the LVCMOS input and LVDS outputs.

TTL INPUT	
J1 Pin No.	**Symbol**
2	TxIN0
4	TxIN1
6	TxIN2
8	TxIN3
10	TxIN4
12	TxIN5
14	TxIN6
16	TxIN7
18	TxIN8
20	TxIN9
22	TxIN10
24	TxIN11
26	TxIN12
28	TxIN13
30	TxIN14
32	TxIN15
34	TxIN16
36	TxIN17
38	TxIN18
40	TxIN19
42	TxIN20
44	TxIN21
46	TxIN22
48	TxIN23
50	TxIN24
52	TxIN25
54	TxIN26
56	TxIN27
58	TxIN28
60	TxIN29
62	TxIN30
64	TxIN31
66	TxCLKIN
All Odd Pins	GND

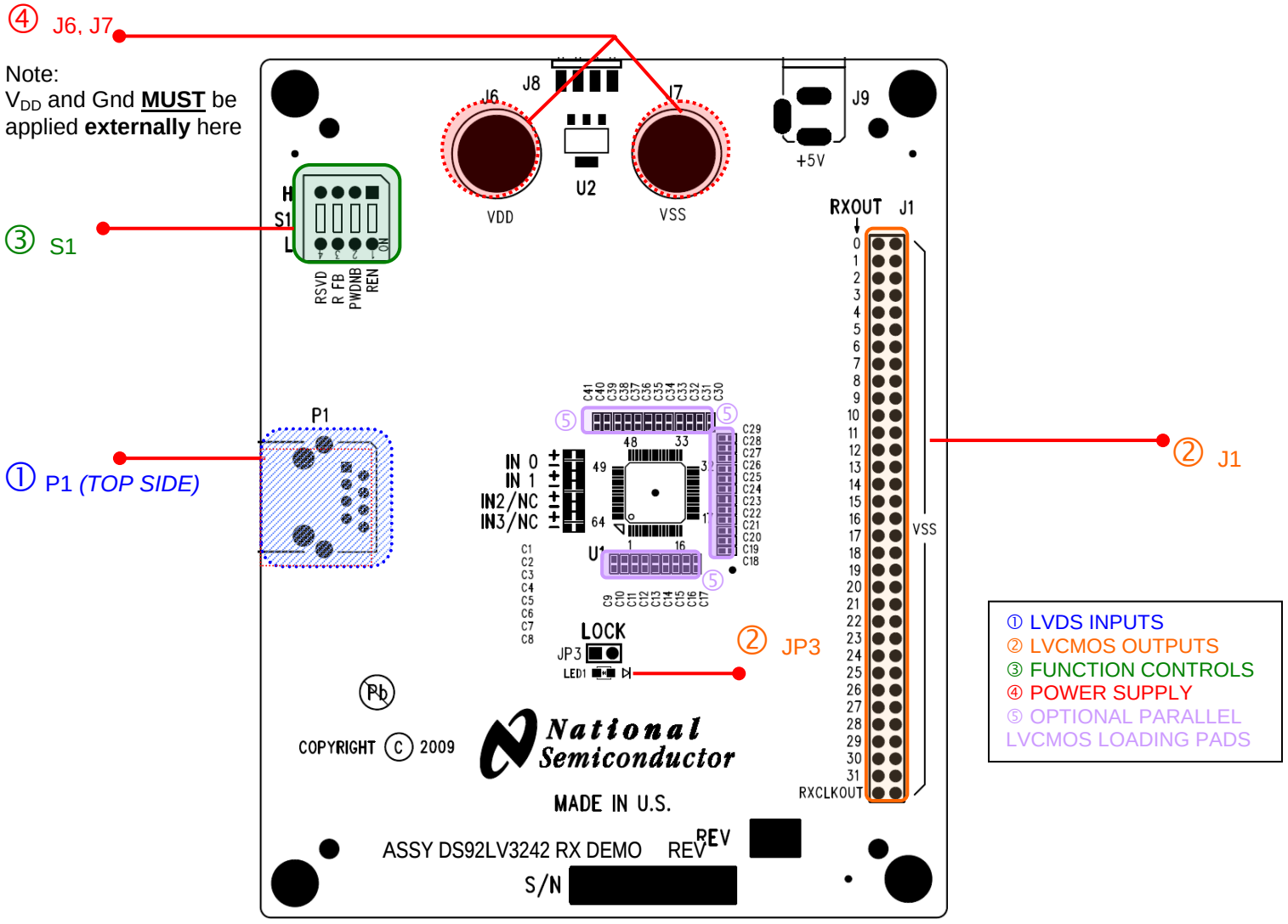
LVDS OUTPUT	
P1 Pin No.	**Symbol**
1	OUT 0 +
2	OUT 0 -
3	OUT 1 +
4	OUT 2 +
5	OUT 2 -
6	OUT 1 -
7	OUT 3 +
8	OUT 3 -

Deserializer (Rx) Board:

The RJ-45 connector P1 provides the interface connection for LVDS signals to the deserializer board.

The deserializer board is powered externally from the J6 (VDD) and J7 (VSS) connectors shown below. For the deserializer to be operational, the Power Down (PWDNB) and Receiver Enable (REN) switches on S1 must be set HIGH. Rising or falling edge output clock is also selected by S1(R FB): HIGH (rising) or LOW (falling).

The 50 pin IDC Connector J1 provides access to the 32 LVCMOS data and clock outputs.



Configuration Settings for the Deserializer Board

S1: Deserializer Input Features Selection

Reference	Description	Input = L	Input = H	S1
RSVD	**R**e**S**er**V**e**D**	MUST be tied low for normal operation **(Default)**	Not allowed	
RRFB	Latch input data on **R**ising or **F**alling edge of RxCLKOUT	Falling Edge **(Default)**	Rising Edge	
PWDNB	**P**o**W**er**D**ow**N** **B**ar	Power Down (Disabled)	Normal Operational **(Default)**	
REN	**R**eceiver Output Data **EN**abled	Disabled	Enabled **(Default)**	

Output Monitor Pins for the Deserializer Board

JP3: Output Lock Monitor

Reference	Description	Output = L	Output = H	JP3
LOCK	Receiver PLL **LOCK** Status ***Note:*** *DO NOT PUT A SHORTING JUMPER IN JP3.*	Unlocked	PLL LOCKED (LED1 will illuminate)	

Deserializer LVDS and LVCMOS Pinout by Connector

The following two tables illustrate how the LVDS inputs are mapped to the RJ-45 connector J1 and the Rx outputs are mapped to the IDC connector J1.
Note: Labels are also printed on the demo boards for both the LVDS inputs and LVCMOS outputs.

LVDS INPUT	
P1 Pin No.	**Symbol**
1	IN 0 +
2	IN 0 -
3	IN 1 +
4	IN 2 +
5	IN 2 -
6	IN 1 -
7	IN 3 +
8	IN 3 -

LVCMOS OUTPUT	
J1 Pin No.	**Symbol**
1	RxOUT0
3	RxOUT1
5	RxOUT2
7	RxOUT3
9	RxOUT4
11	RxOUT5
13	RxOUT6
15	RxOUT7
17	RxOUT8
19	RxOUT9
21	RxOUT10
23	RxOUT11
25	RxOUT12
27	RxOUT13
29	RxOUT14
31	RxOUT15
33	RxOUT16
35	RxOUT17
37	RxOUT18
39	RxOUT19
41	RxOUT20
43	RxOUT21
45	RxOUT22
47	RxOUT23
49	RxOUT24
51	RxOUT25
53	RxOUT26
55	RxOUT27
57	RxOUT28
59	RxOUT29
61	RxOUT30
63	RxOUT31
65	RxCLKOUT
All Even Pins	GND

LVCMOS OUTPUT	
JP3 pin no.	**Symbol**
1	LOCK (PLL)
2	GND

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

1) Digital Video Source – for generation of specific display timing such as Digital Video Processor or Graphics Controller with digital RGB (LVCMOS) output.
2) Astro Systems VG-835 - This video generator may be used for video signal sources for 6-bit Digital TTL/RGB.
3) Any other signal / video generator that generates the correct input levels as specified in the datasheet.
4) Logic Analyzer or Oscilloscope

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (LVCMOS) inputs.
2) National Semiconductor DS92LV3241 Serializer (Tx)
3) Optional – Logic Analyzer or Oscilloscope
4) Any SCOPE with a bandwidth of at least 170 MHz for TTL and/or 1 GHz for looking at the LVDS signals.

LVDS signals may be easily measured with high impedance, low capacitance, high bandwidth differential probes such as the TEK P6330 differential probes.

Typical Applications:

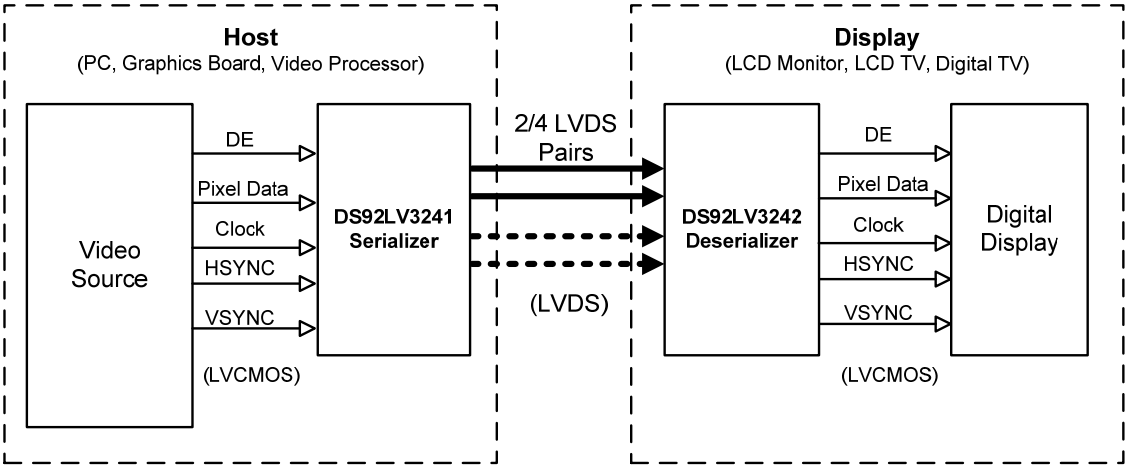


Figure 1. Typical SERDES Application

The chipset supports up to 30-bit color depth TFT LCD Panels. The picture below shows a typical test set up using a Graphics Controller and LCD Panel.

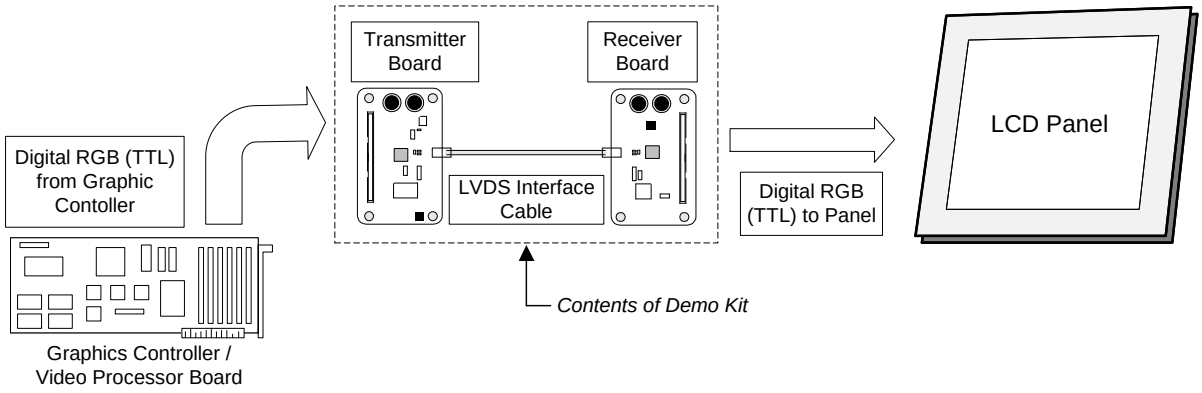


Figure 2. Typical SERDES Setup of LCD Panel Application

The picture below shows a typical test set up using a generator and scope.

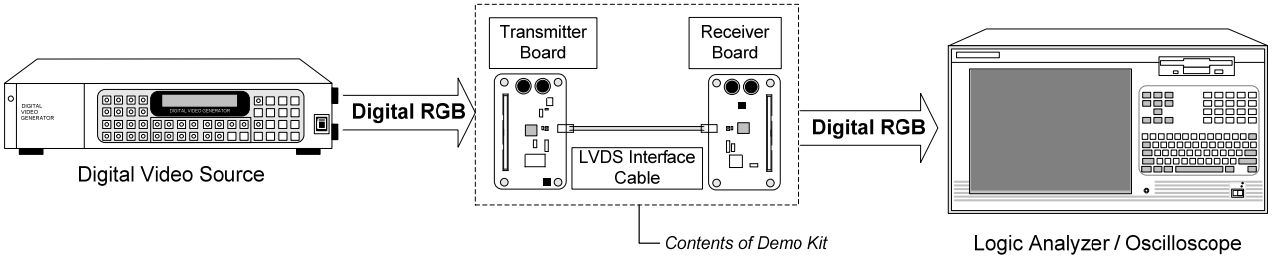


Figure 3. Typical SERDES Test Setup for Evaluation

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards. The Serializer board should draw about 150-200 mA with clock and all data bits switching at 85 MHz in Quad Mode, (R_{PRE}=12 kΩ). The Deserializer board should draw about 240-265mA with clock and all data bits switching at 85 MHz in Quad Mode (8pF RxOUT loading).
3. Verify input clock and input data signals meet requirements for V_{IL}min, V_{IL}max, V_{IH}min, V_{IH}max, t_{STC}, t_{HTC}), also verify that data is strobed on the selected rising/falling (RFB pin) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	**Solution…**
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and Deserializer boards to make sure that the devices are enabled (/PWDB=V_{DD}) for operation. Also check DEN on the Serializer board and REN on the Deserializer board is set HIGH.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Appendix

BOM (Bill of Materials) Serializer PCB:

DS92LV3241 Tx Demo Board - Board Stackup Revised: Monday, September 21, 2009
DS92LV3241 Tx Demo Board Revision: 1
Bill Of Materials September 21, 2009

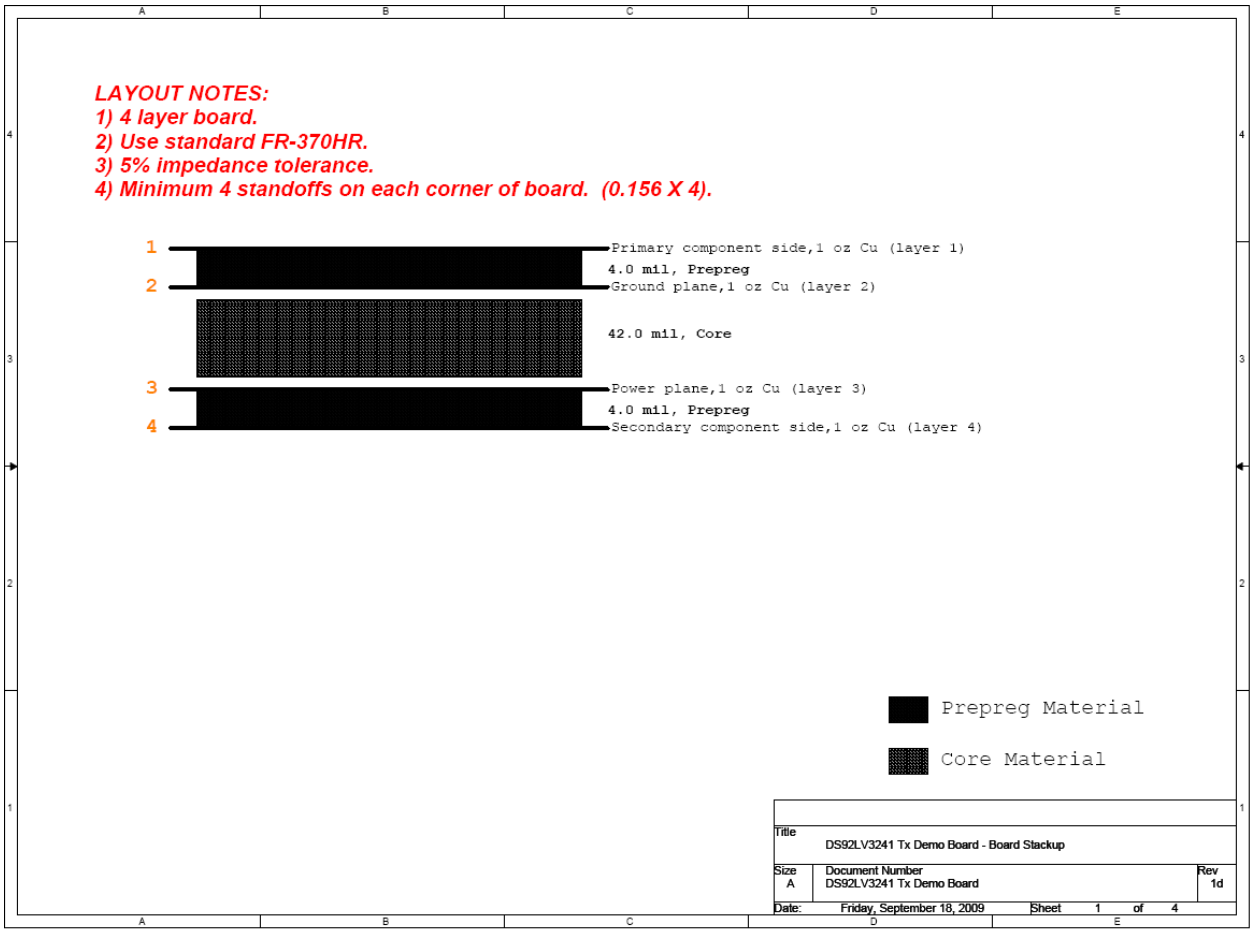
Item	Qty	Reference	Part	PCB Footprint
1	2	C4,C1	22uF	CAP/N
2	2	C5,C2	2.2uF	3528-21_EIA
3	2	C3,C6	0.1uF	CAP/HDC-1206
4	8	C7,C8,C9,C10,C11,C12,C13, C14	0.1uF	CAP/HDC-0603
5	8	C15,C16,C17,C26,C31,C34, C35,C38	22uF	CAP/EIA-B 3528-21
6	8	C18,C21,C22,C25,C28,C29, C36,C37	0.1uF	CAP/HDC-0603
7	8	C19,C20,C23,C24,C27,C30, C32,C33	0.01uF	CAP/HDC-0603
8	2	JP1,JP4	2-Pin Header	Header/2P
9	1	JP2	3-Pin Header	Header/3P
10	2	JP3,JP5	2-Pin Header_open	Header/2P
11	1	J1	IDC2X33_Unshrouded	IDC-66
12	4	J2,J3,J4,J5	IDC2X2_Unshrouded	IDC-2x2
13	1	J6	2x4 pin Jumper_OPEN	IDC_2x4
14	2	J7,J8	BANANA	CON/BANANA-S
15	1	J9	CONN JACK PWR_open	3-terminal thru hole power jack
16	1	P1	RJ-45 8pin_open	RJ-45_thru_hole
17	32	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29,R30,R31,R32	49.9ohm_open	RES/HDC-0201
18	1	R33	49.9ohm_open	RES/HDC-0805
19	1	R34	12.0K, 0402	RES/HDC-0402
20	2	R36,R35	332 ohm_open	RES/HDC-0805
21	10	R37,R38,R39,R40,R41,R42, R43,R44,R45, R52	0 Ohm,0402	RES/HDC-0402
22	6	R46,R47,R48,R49,R50,R51	10K	RES/HDC-0805
24	1	S1	SW DIP-6	DIP-12
25	1	U1	DS92LV3241	64ld TQFP
26	1	U2	LM3940/SOT223_open	SOT223
27	1	VR1	SVR20K	Surface Mount 4mm Square

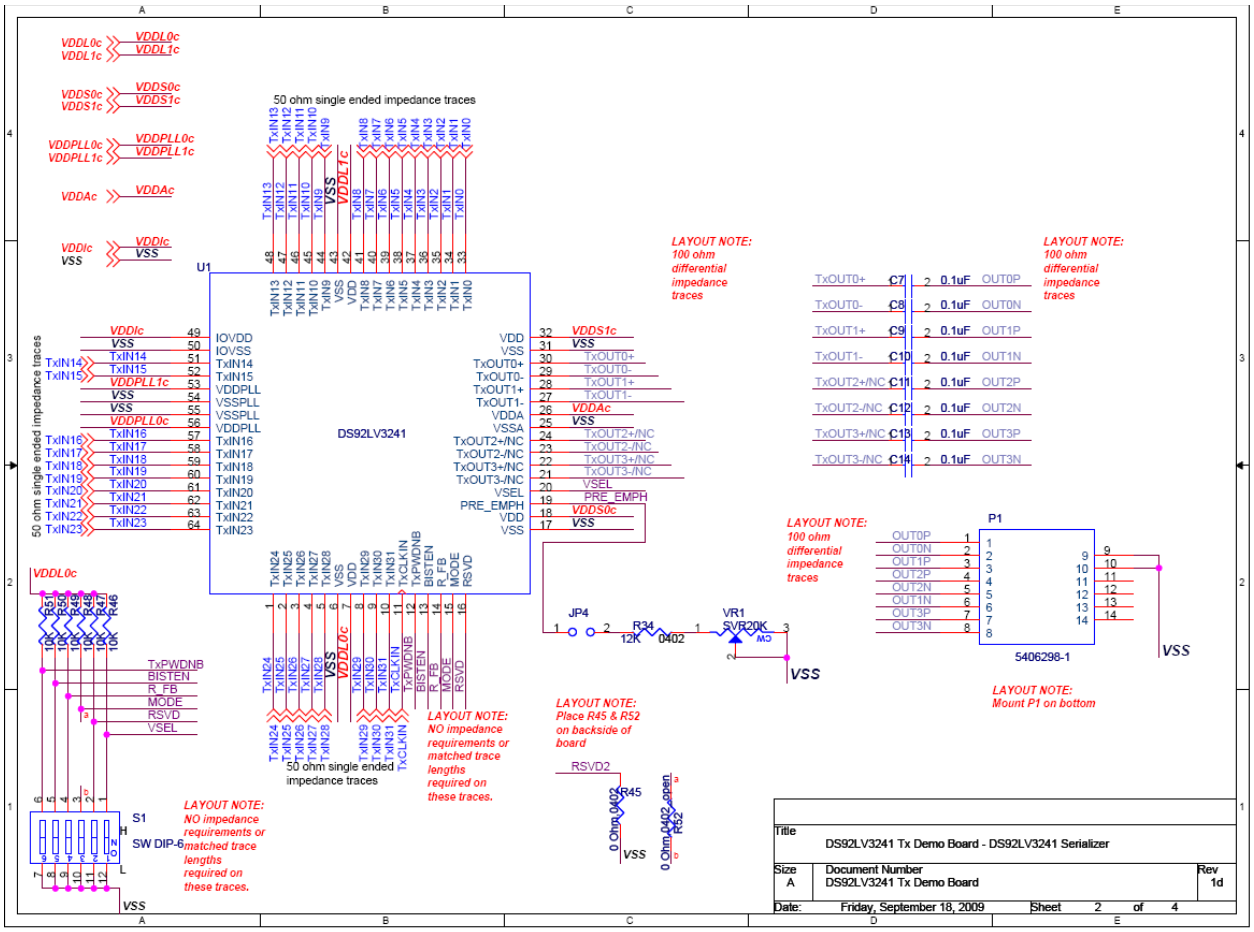
BOM (Bill of Materials) Deserializer PCB:

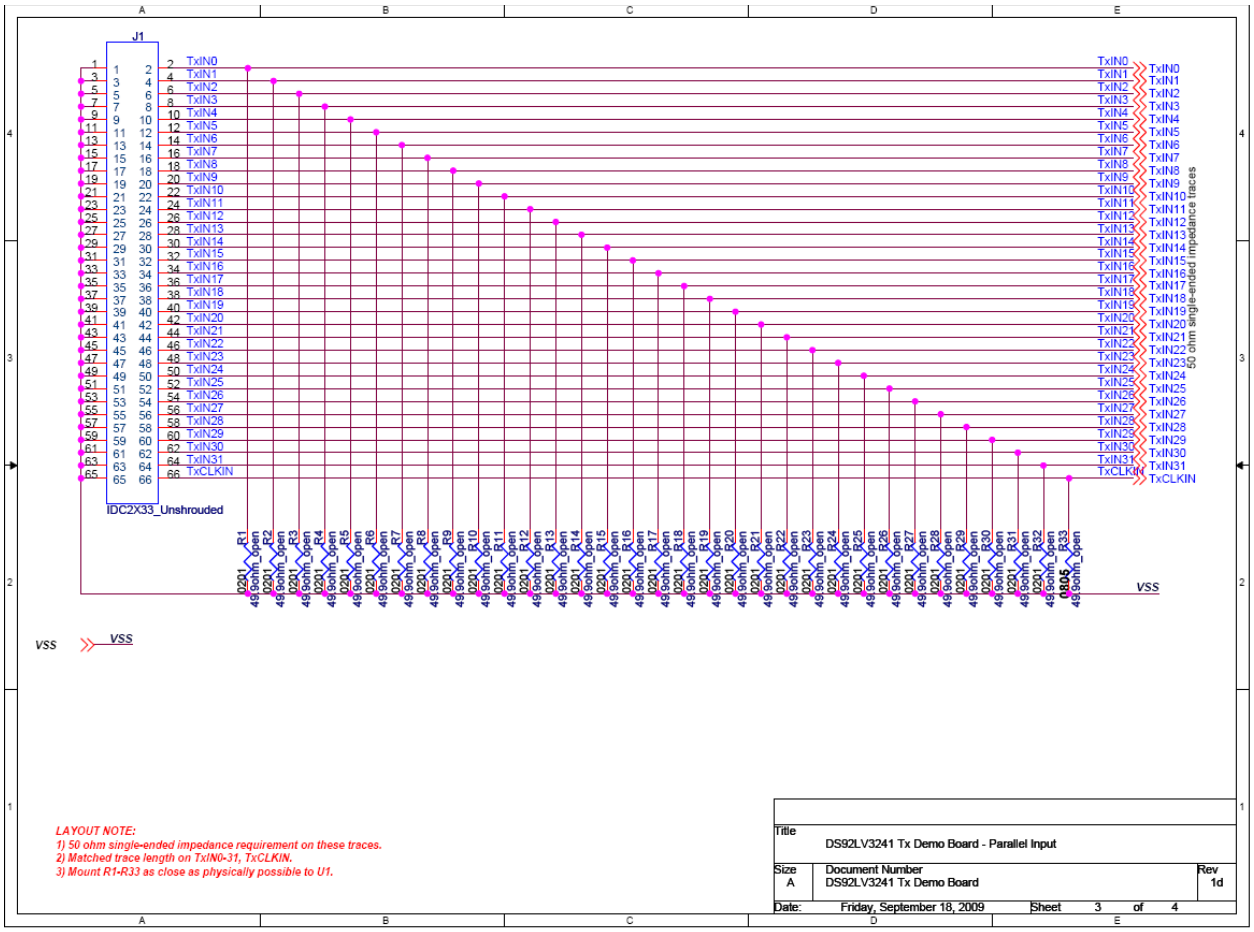
DS92LV3242 Rx Demo Board - Board Stackup Revised: Monday, September 21, 2009
DS92LV3242 Rx Demo Board Revision: 1
Bill Of Materials September 21, 2009

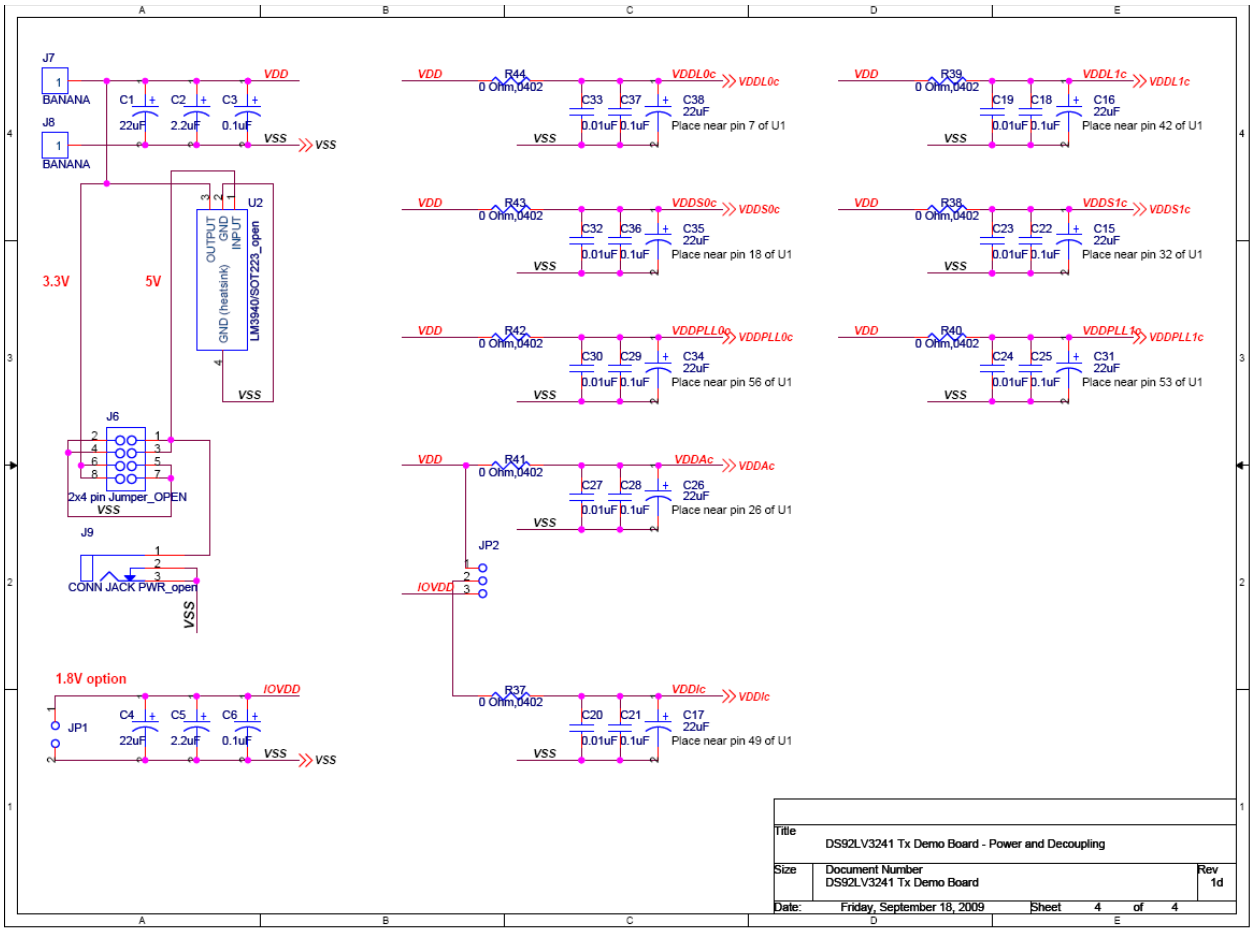
Item	Qty	Reference	Part	PCB Footprint
1	8	C1,C2,C3,C4,C5,C6,C7,C8	0.1uF	CAP/HDC-0603
2	33	C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C22,C23,C24,C25,C26, C27,C28,C29,C30,C31,C32, C33,C34,C35,C36,C37,C38, C39,C40,C41	open0402	CAP/HDC-0402
3	1	C42	22uF	CAP/N
4	1	C43	2.2uF	3528-21_EIA
5	1	C44	0.1uF	CAP/HDC-1206
6	9	C45,C46,C47,C54,C55,C66, C69,C70,C71	22uF	CAP/EIA-B 3528-21
7	9	C48,C51,C53,C57,C59,C61, C62,C64,C67	0.01uF	CAP/HDC-0603
8	9	C49,C50,C52,C56,C58,C60, C63,C65,C68	0.1uF	CAP/HDC-0603
9	2	JP1,JP2	2-Pin Header_open	Header/2P
10	1	JP3	2-Pin Header	Header/2P
11	1	J1	IDC2X33_Unshrouded	IDC-66
12	4	J2,J3,J4,J5	IDC2X2_Unshrouded	IDC-2x2
13	2	J6,J7	BANANA	CON/BANANA-S
14	1	J8	2x4 pin Jumper_OPEN	IDC_2x4
15	1	J9	CONN JACK PWR_open	3-terminal thru hole power jack
16	1	LED1	0603_green_LED	0603 (Super Thin)
17	1	P1	RJ-45 8pin	RJ-45_thru_hole
18	2	R2,R1	332 ohm_open	RES/HDC-0805
19	4	R3,R4,R5,R6	10K	RES/HDC-0805
20	10	R7,R8,R9,R10,R11,R12,R13, R14,R15,R16	0 Ohm,0402	RES/HDC-0402
21	1	S1	SW DIP-4	DIP-8
22	1	U1	DS92LV3242	64ld TQFP
23	1	U2	LM3940/SOT223_open	SOT223

Serializer (Tx) PCB Schematic:

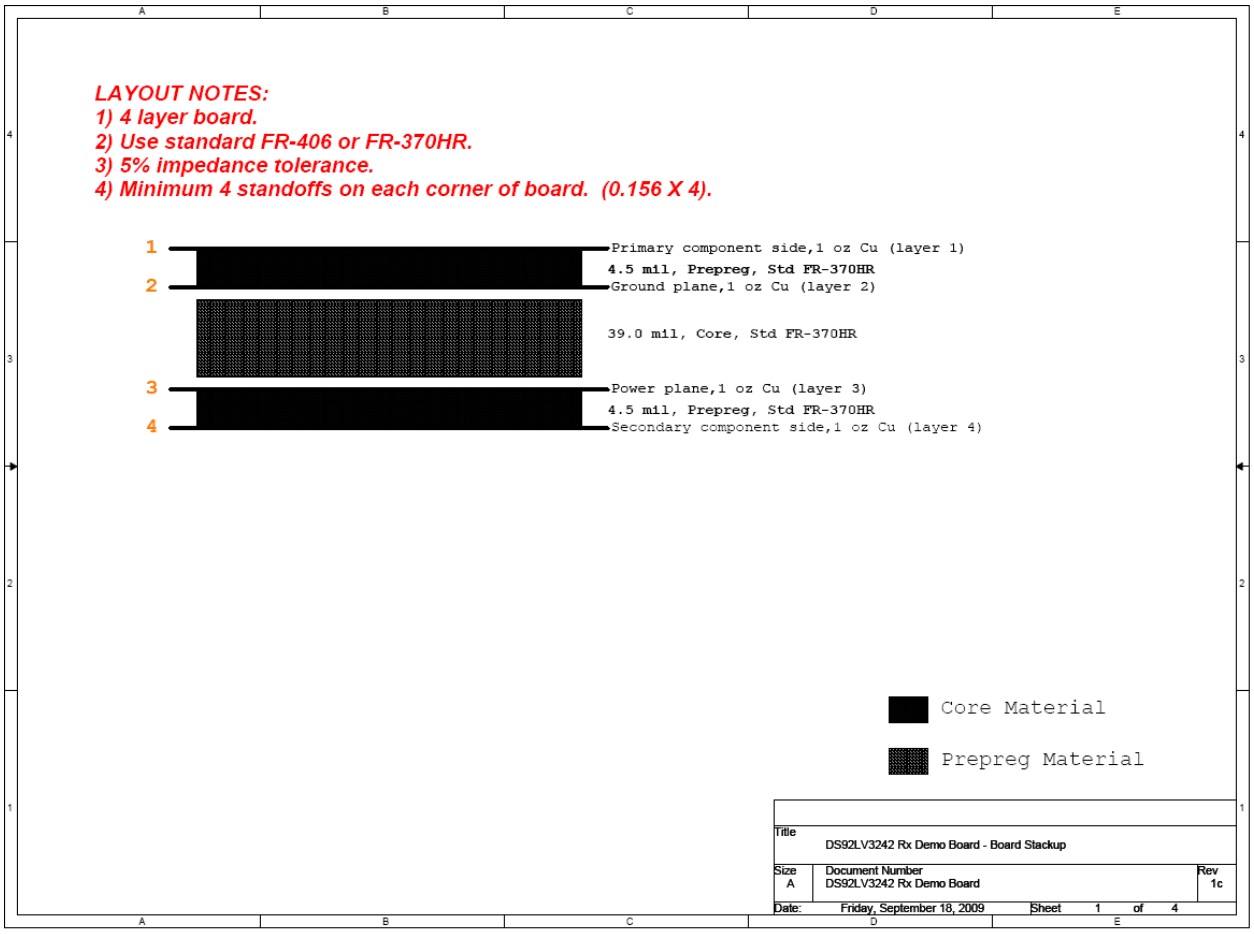


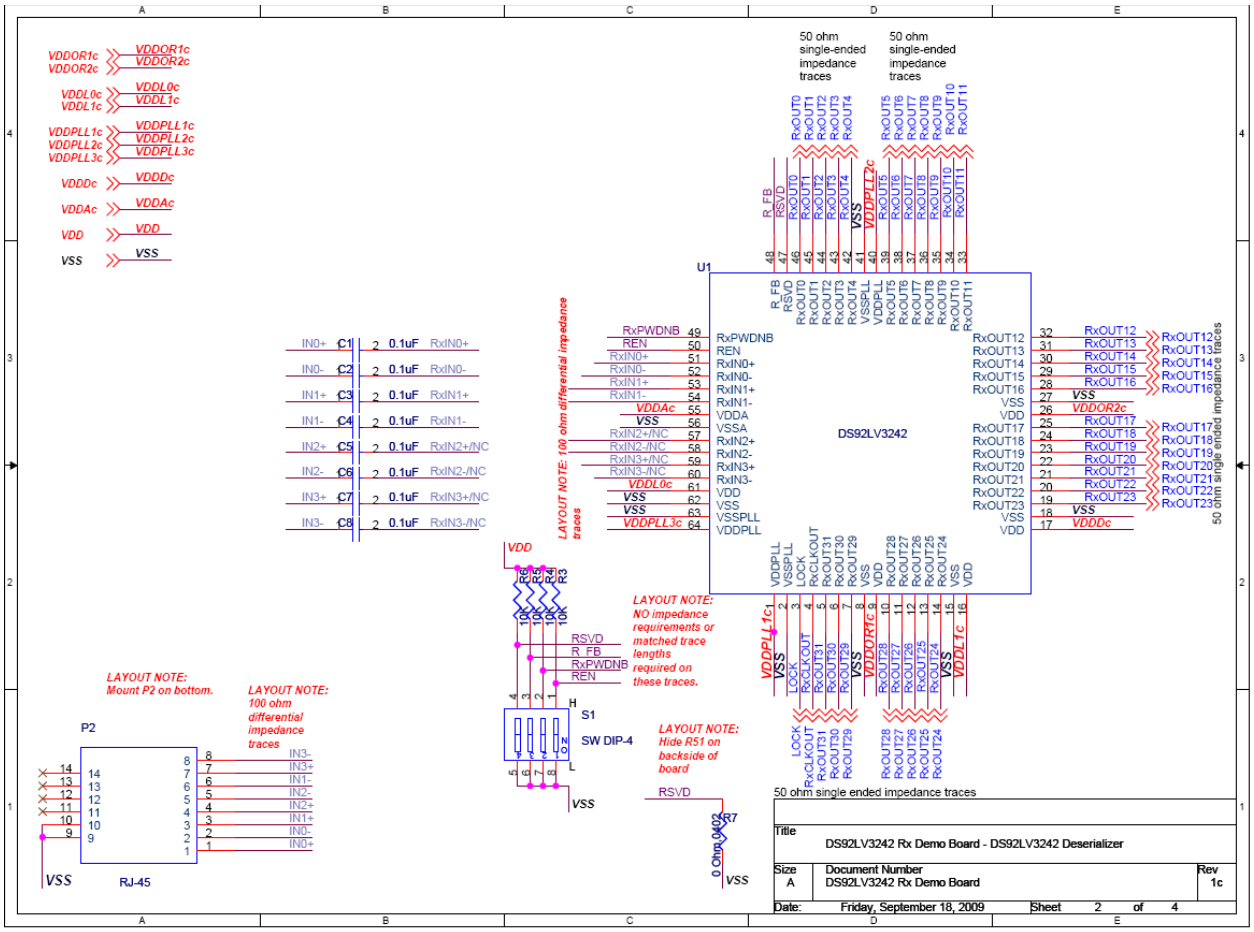

50 ohm single ended impedance traces
U1
DS92LV3241
50 ohm single ended impedance traces
50 ohm single ended impedance traces
LAYOUT NOTE: 100 ohm differential impedance traces
LAYOUT NOTE: 100 ohm differential impedance traces
LAYOUT NOTE: 100 ohm differential impedance traces
LAYOUT NOTE: NO impedance requirements or matched trace lengths required on these traces.
LAYOUT NOTE: NO impedance requirements or matched trace lengths required on these traces.
LAYOUT NOTE: Place R45 & R52 on backside of board
LAYOUT NOTE: Mount P1 on bottom
P1
5406298-1
JP4
VR1
S1
SW DIP-6
Title
DS92LV3241 Tx Demo Board - DS92LV3241 Serializer
Size A
Document Number DS92LV3241 Tx Demo Board
Rev 1d
Date: Friday, September 18, 2009
Sheet 2 of 4

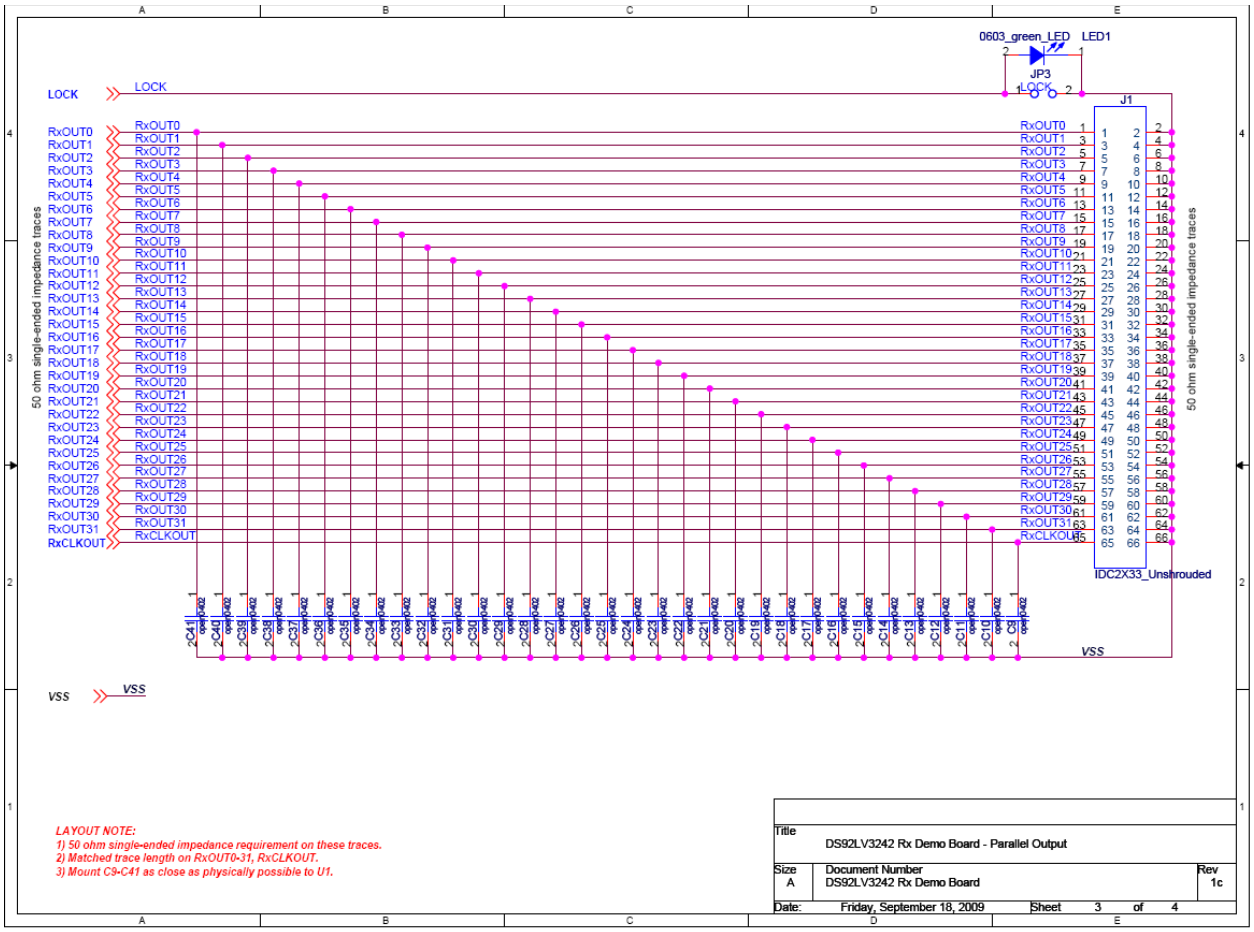

J1
IDC2X33_Unshrouded
TxIN0
TxIN1
TxIN2
TxIN3
TxIN4
TxIN5
TxIN6
TxIN7
TxIN8
TxIN9
TxIN10
TxIN11
TxIN12
TxIN13
TxIN14
TxIN15
TxIN16
TxIN17
TxIN18
TxIN19
TxIN20
TxIN21
TxIN22
TxIN23
TxIN24
TxIN25
TxIN26
TxIN27
TxIN28
TxIN29
TxIN30
TxIN31
TxCLKIN
50 ohm single-ended impedance traces
VSS
LAYOUT NOTE:
1) 50 ohm single-ended impedance requirement on these traces.
2) Matched trace length on TxIN0-31, TxCLKIN.
3) Mount R1-R33 as close as physically possible to U1.
Title
DS92LV3241 Tx Demo Board - Parallel Input
Size
A
Document Number
DS92LV3241 Tx Demo Board
Rev
1d
Date:
Friday, September 18, 2009
Sheet
3
of
4


J7
BANANA
J8
BANANA
C1 22uF
C2 2.2uF
C3 0.1uF
VDD
VSS
U2
LM3940/SOT223_open
OUTPUT
GND (heatsink)
INPUT
3.3V
5V
J6
2x4 pin Jumper_OPEN
J9
CONN JACK PWR_open
1.8V option
JP1
C4 22uF
C5 2.2uF
C6 0.1uF
IOVDD
JP2
R44 0 Ohm,0402
C33 0.01uF
C37 0.1uF
C38 22uF
VDDL0c
Place near pin 7 of U1
R43 0 Ohm,0402
C32 0.01uF
C36 0.1uF
C35 22uF
VDDS0c
Place near pin 18 of U1
R42 0 Ohm,0402
C30 0.01uF
C29 0.1uF
C34 22uF
VDDPLL0c
Place near pin 56 of U1
R41 0 Ohm,0402
C27 0.01uF
C28 0.1uF
C26 22uF
VDDAc
Place near pin 26 of U1
R37 0 Ohm,0402
C20 0.01uF
C21 0.1uF
C17 22uF
VDDIc
Place near pin 49 of U1
R39 0 Ohm,0402
C19 0.01uF
C18 0.1uF
C16 22uF
VDDL1c
Place near pin 42 of U1
R38 0 Ohm,0402
C23 0.01uF
C22 0.1uF
C15 22uF
VDDS1c
Place near pin 32 of U1
R40 0 Ohm,0402
C24 0.01uF
C25 0.1uF
C31 22uF
VDDPLL1c
Place near pin 53 of U1
Title
DS92LV3241 Tx Demo Board - Power and Decoupling
Size
Document Number
DS92LV3241 Tx Demo Board
Rev
1d
Date: Friday, September 18, 2009
Sheet 4 of 4

Deserializer (Rx) PCB Schematic:




U1
DS92LV3242
50 ohm single-ended impedance traces
50 ohm single ended impedance traces
LAYOUT NOTE: 100 ohm differential impedance traces
LAYOUT NOTE: NO impedance requirements or matched trace lengths required on these traces.
LAYOUT NOTE: Hide R51 on backside of board
LAYOUT NOTE: Mount P2 on bottom.
LAYOUT NOTE: 100 ohm differential impedance traces
P2
RJ-45
S1
SW DIP-4
R7
0 Ohm 0402
Title
DS92LV3242 Rx Demo Board - DS92LV3242 Deserializer
Size A
Document Number DS92LV3242 Rx Demo Board
Rev 1c
Date: Friday, September 18, 2009
Sheet 2 of 4


0603_green_LED
LED1
JP3
LOCK
J1
IDC2X33_Unshrouded
50 ohm single-ended impedance traces
50 ohm single-ended impedance traces
RxOUT0
RxOUT1
RxOUT2
RxOUT3
RxOUT4
RxOUT5
RxOUT6
RxOUT7
RxOUT8
RxOUT9
RxOUT10
RxOUT11
RxOUT12
RxOUT13
RxOUT14
RxOUT15
RxOUT16
RxOUT17
RxOUT18
RxOUT19
RxOUT20
RxOUT21
RxOUT22
RxOUT23
RxOUT24
RxOUT25
RxOUT26
RxOUT27
RxOUT28
RxOUT29
RxOUT30
RxOUT31
RxCLKOUT
LOCK
VSS
LAYOUT NOTE:
1) 50 ohm single-ended impedance requirement on these traces.
2) Matched trace length on RxOUT0-31, RxCLKOUT.
3) Mount C9-C41 as close as physically possible to U1.
Title
DS92LV3242 Rx Demo Board - Parallel Output
Size
A
Document Number
DS92LV3242 Rx Demo Board
Rev
1c
Date:
Friday, September 18, 2009
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3
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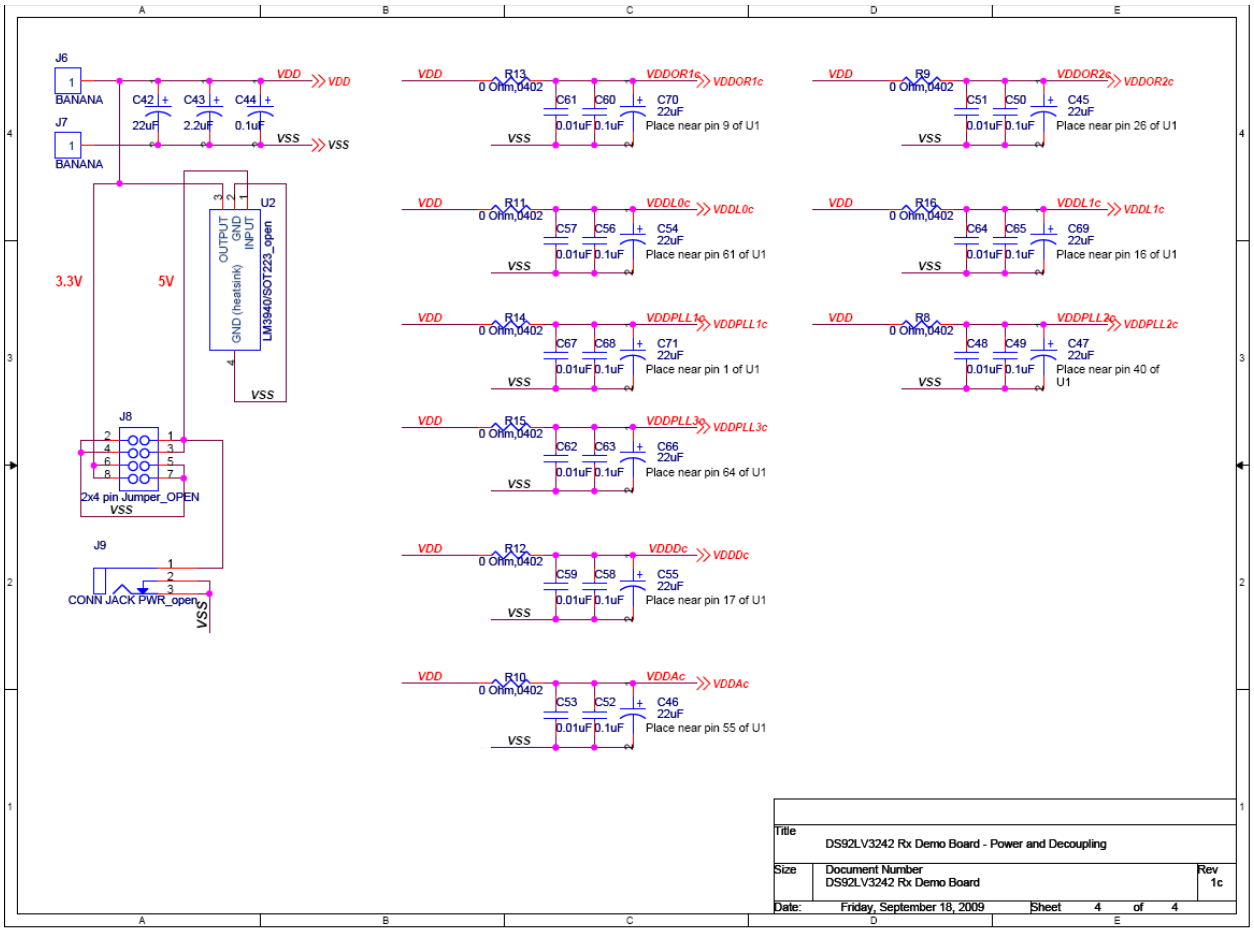
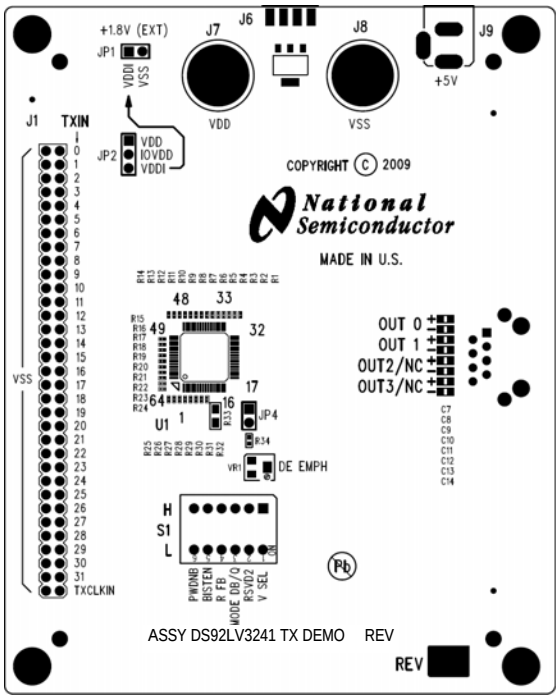
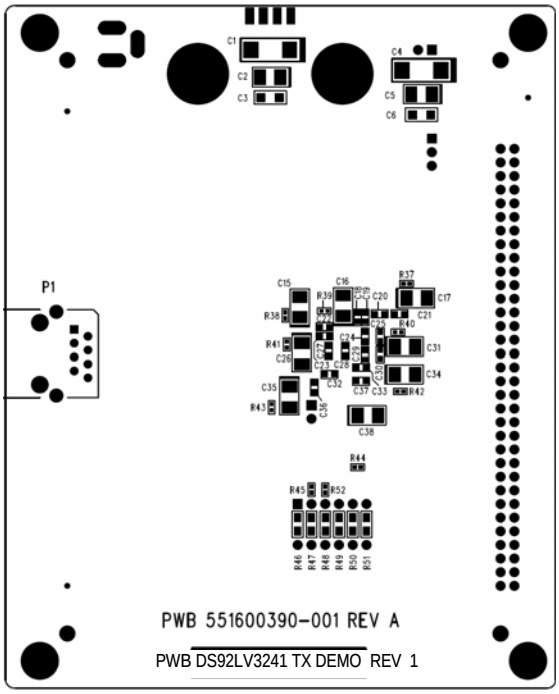
4


J6
BANANA
J7
BANANA
C42 22uF
C43 2.2uF
C44 0.1uF
VDD
VSS
3.3V
5V
U2
OUTPUT
GND
INPUT
GND (heatsink)
LM3940IS0T223_open
J8
2x4 pin Jumper_OPEN
J9
CONN JACK PWR_open
R13 0 Ohm,0402
C61 0.01uF
C60 0.1uF
C70 22uF
VDDOR1c
Place near pin 9 of U1
R11 0 Ohm,0402
C57 0.01uF
C56 0.1uF
C54 22uF
VDDL0c
Place near pin 61 of U1
R14 0 Ohm,0402
C67 0.01uF
C68 0.1uF
C71 22uF
VDDPLL1c
Place near pin 1 of U1
R15 0 Ohm,0402
C62 0.01uF
C63 0.1uF
C66 22uF
VDDPLL3c
Place near pin 64 of U1
R12 0 Ohm,0402
C59 0.01uF
C58 0.1uF
C55 22uF
VDDDc
Place near pin 17 of U1
R10 0 Ohm,0402
C53 0.01uF
C52 0.1uF
C46 22uF
VDDAc
Place near pin 55 of U1
R9 0 Ohm,0402
C51 0.01uF
C50 0.1uF
C45 22uF
VDDOR2c
Place near pin 26 of U1
R16 0 Ohm,0402
C64 0.01uF
C65 0.1uF
C69 22uF
VDDL1c
Place near pin 16 of U1
R8 0 Ohm,0402
C48 0.01uF
C49 0.1uF
C47 22uF
VDDPLL2c
Place near pin 40 of U1
Title
DS92LV3242 Rx Demo Board - Power and Decoupling
Size
Document Number
DS92LV3242 Rx Demo Board
Rev
1c
Date: Friday, September 18, 2009
Sheet 4 of 4

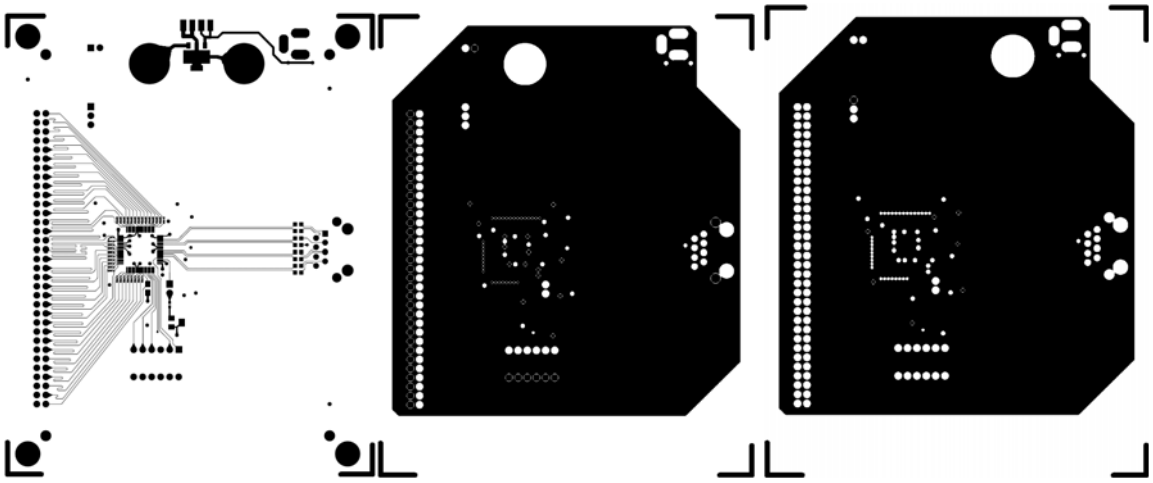
Serializer (Tx) PCB Layout:



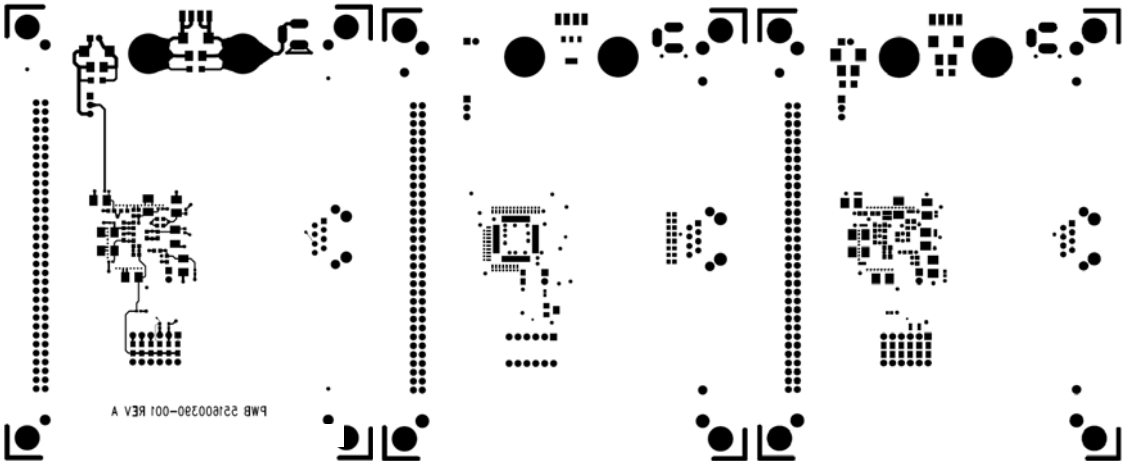
TOP VIEW



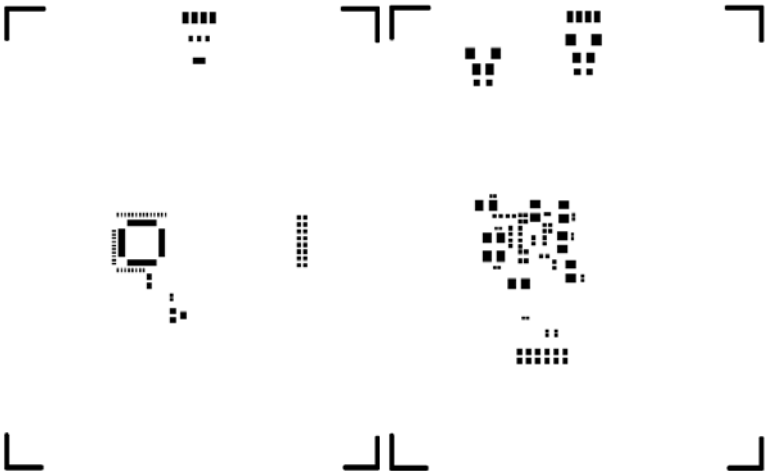
BOTTOMSIDE VIEW



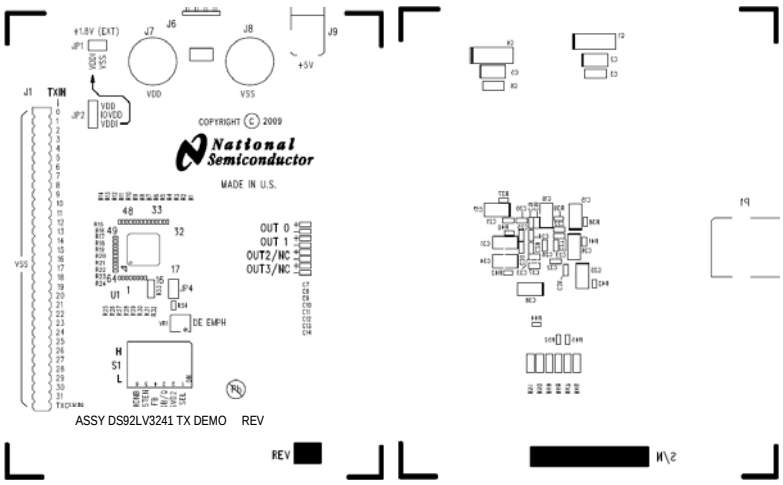
PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3



SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)



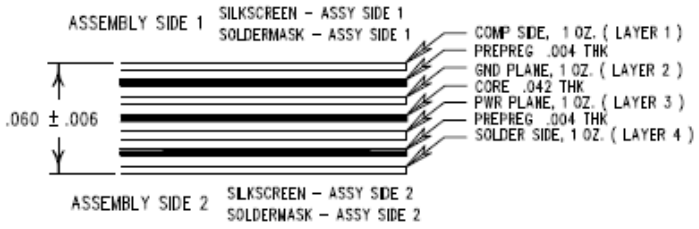
PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1) SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)



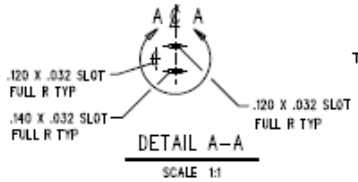
PRIMARY COMP SIDE – SILKSCREEN (LAYER 1)

SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

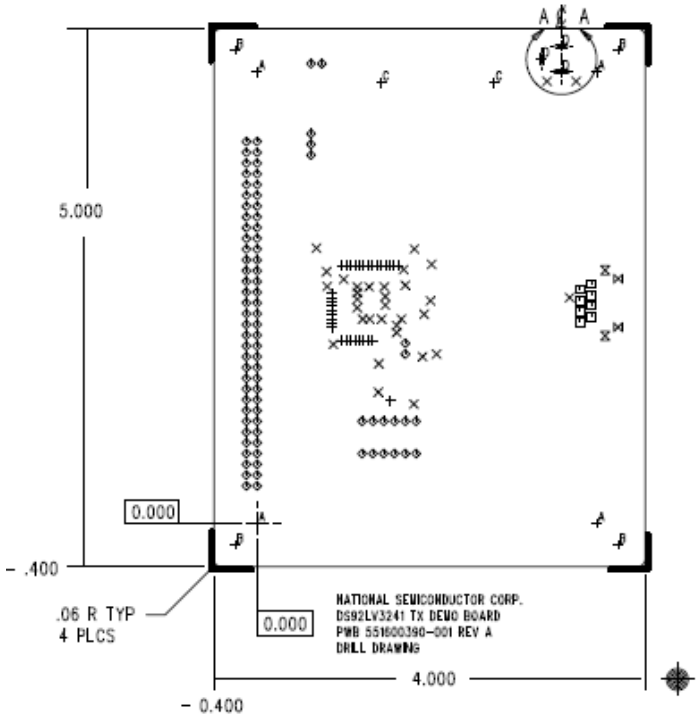
Serializer (Tx) PCB Stackup:



HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	32	YES	± .003
×	0.014	33	YES	± .003
□	0.035	8	YES	± .003
◇	0.043	85	YES	± .003
⧖	0.062	2	YES	± .002
⋈	0.128	2	NO	± .003
A	0.125	4	NO	+.003 -.000
B	0.156	4	YES	± .004
C	0.265	2	YES	± .005
D	0.032	3	YES	± .004



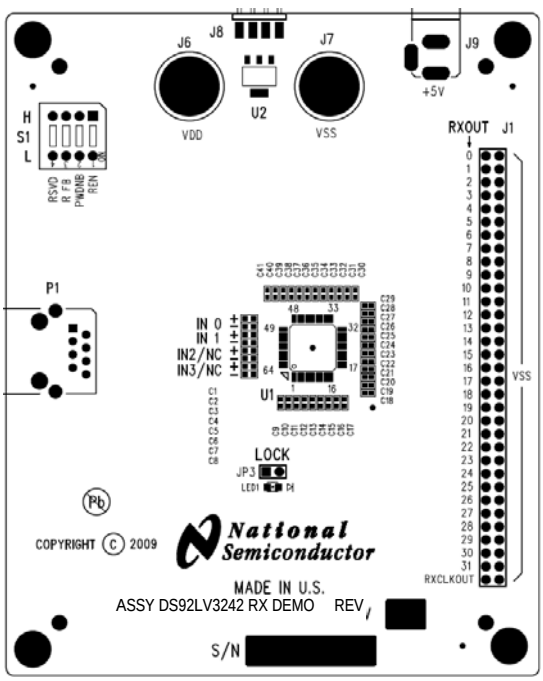
THRU HOLE SLOT – SEE DETAIL A–A



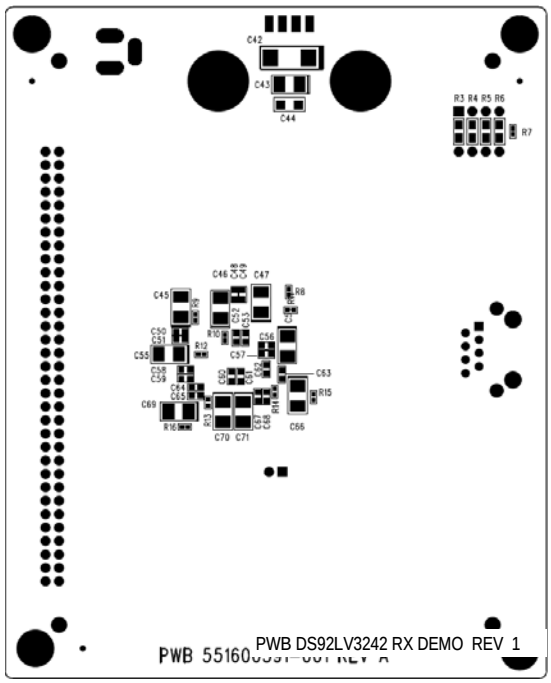
NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM 551600390–001 REV A. USE GERBER FILE B576BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS FR 370HR OR EQUIVALENT. COLOR GREEN, 0.060 +/–.005 INCH NOM. THICKNESS COPPER CLADDING SHALL BE 1 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. SURFACE PLATING TO BE ELECTROLESS NICKEL .000150" / IMMERSION GOLD .000030" (ENIG).
7. FABRICATION TOLERANCES: END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .002 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .07 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .005 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE THE .0044 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE, AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 10%.
11. THE PCB SHALL BE E.U. ROHS COMPLIANT.

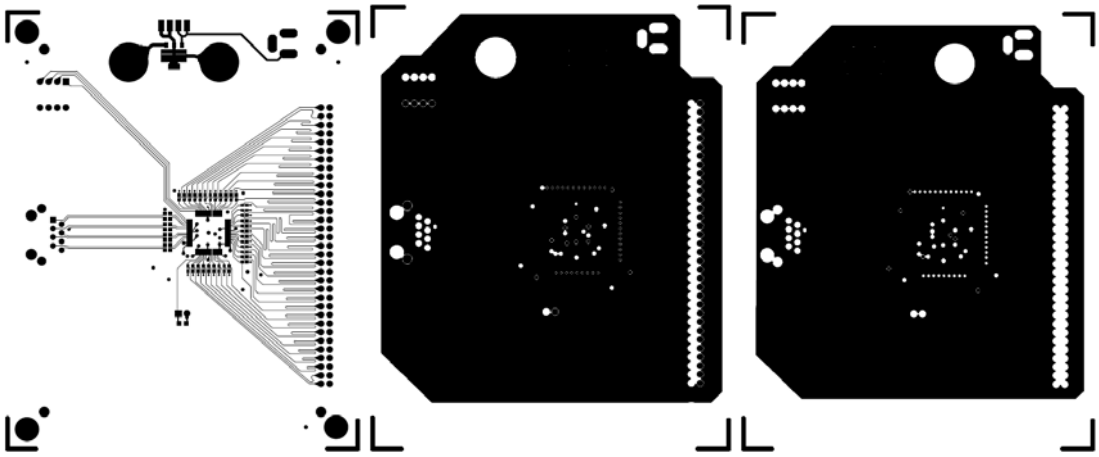
Deserializer (Rx) PCB Layout:



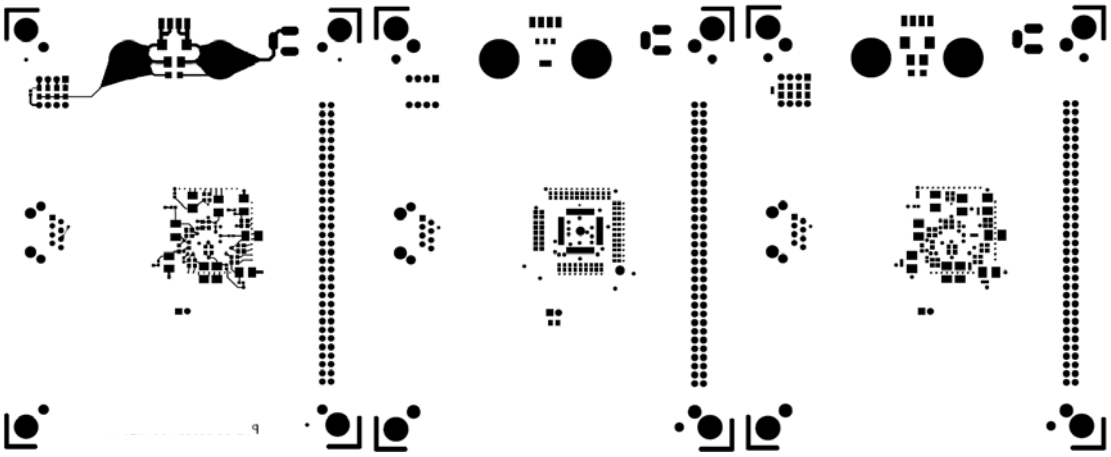
TOP VIEW



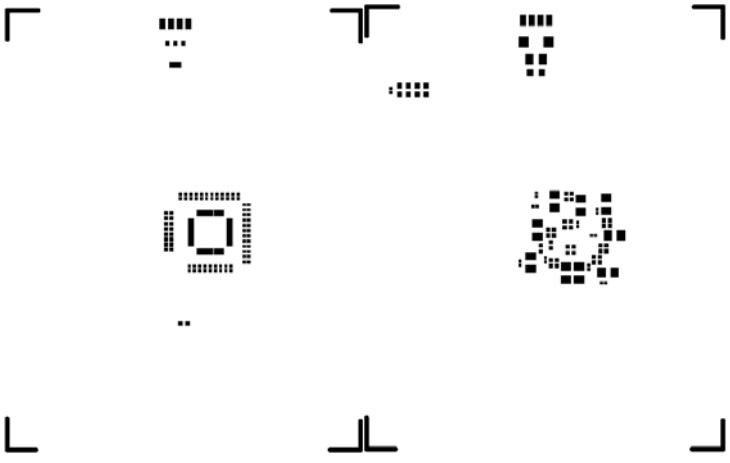
BOTTOMSIDE VIEW



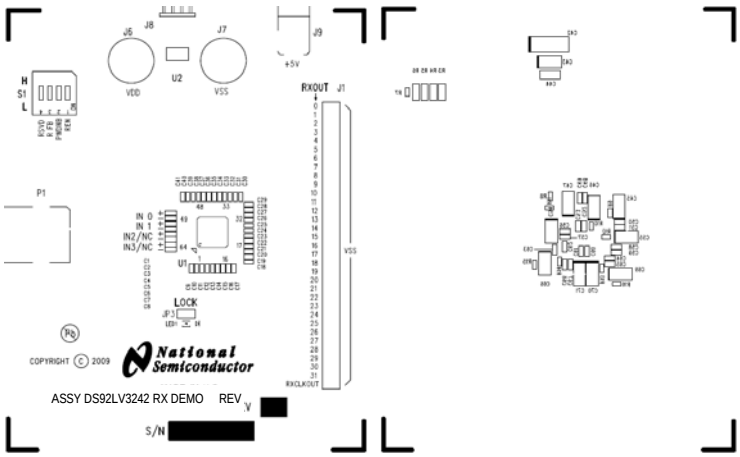
PRIMARY COMPONENT SIDE – LAYER 1 GROUND PLANE (VSS) – LAYER 2 POWER PLANE (VDD) – LAYER 3



SECONDARY COMP SIDE – LAYER 4 PRIMARY COMP SIDE – SOLDER MASK (LAYER 1) SECONDARY COMP SIDE – SOLDER MASK (LAYER 4)

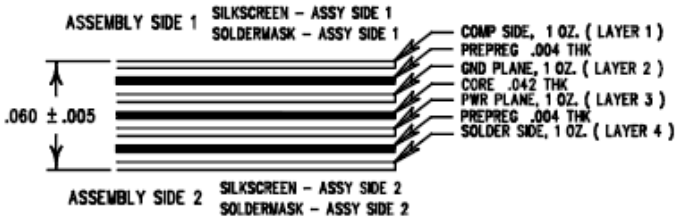


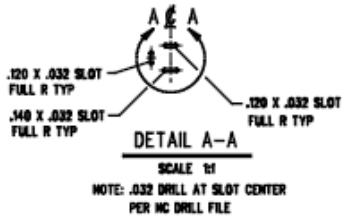
PRIMARY COMP SIDE – SOLDER PASTE (LAYER 1) SECONDARY COMP SIDE – SOLDER PASTE (LAYER 4)



PRIMARY COMP SIDE – SILKSCREEN (LAYER 1) SILKSCREEN COMP SIDE – SILKSCREEN (LAYER 4)

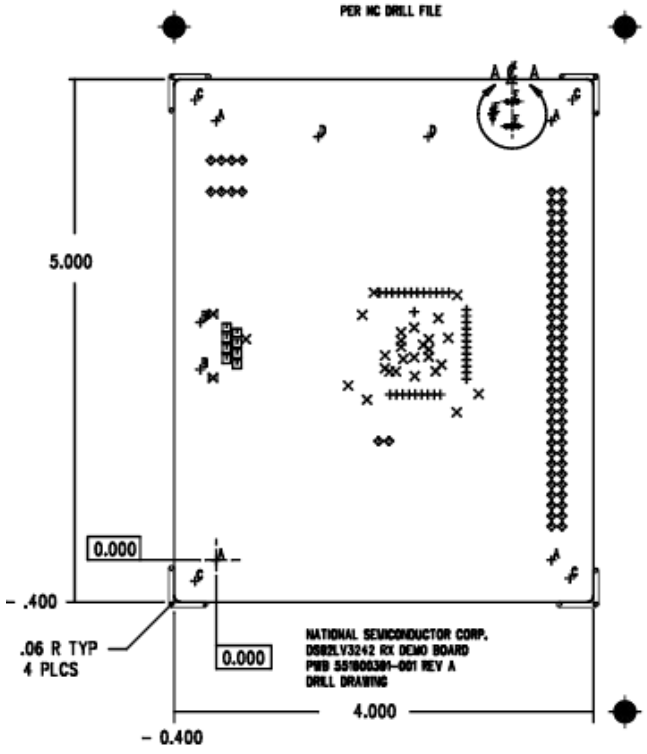
Deserializer (Rx) PCB Stackup:





THRU HOLE SLOT – SEE DETAIL A–A

HOLE CHART				
CODE	SIZE	QTY	PLATED	TOL
+	0.006	34	YES	± .003
×	0.014	27	YES	± .003
□	0.035	8	YES	± .003
◇	0.043	76	YES	± .003
⧖	0.062	2	YES	± .002
⋈	0.128	2	YES	± .003
A	0.125	4	NO	+ .003 – .000
B	0.156	4	YES	± .004
C	0.265	2	YES	± .005
D	0.032	3	YES	± .004



NOTES: UNLESS OTHERWISE SPECIFIED

1. PRIMARY COMPONENT SIDE IS SHOWN.
2. HOLES MARKED " A " ARE TOOLING HOLES, UNPLATED, AND SHALL BE "ONCE" DRILLED.
3. FABRICATE USING MASTER FILM 551600391–001 REV A. USE GERBER FILE B577BOA.PHO FOR BOARD ROUTE.
4. ACCEPTABILITY SHALL BE BASED ON IPC–A–600, CLASS 2
5. MATERIAL: BASE MATERIAL IS ISOLA IS410 OR EQUIVALENT. COLOR GREEN, 0.060 +/–.005 INCH NOM. THICKNESS COPPER CLADDING SHALL BE 1 OZ.
6. PLATING: ALL HOLES AND CONDUCTIVE SURFACES SHALL BE PLATED WITH A MIN. OF .001 INCH COPPER. SURFACE PLATING TO BE ELECTROLESS NICKEL .000150" / IMMERSION GOLD .000030" (ENIG).
7. FABRICATION TOLERANCES: END PRODUCT CONDUCTOR WIDTHS AND LAND DIAMETERS SHALL NOT VARY MORE THAN .002 INCH FROM THE 1:1 DIMENSIONS OF THE MASTER PATTERN. THE CONDUCTIVE PATTERN SHALL BE POSITIONED SO THAT THE LOCATION OF ANY LAND SHALL BE WITHIN .002 INCH DIAMETER TO THE TRUE POSITION OF THE HOLE IT CIRCUMSCRIBES THE MINIMUM ANNULAR RING SHALL BE .002 INCH. BOW AND TWIST SHALL NOT EXCEED .07 INCH PER INCH.
8. SOLDERMASK BOTH SIDES PER IPC–SM–840, TYPE A, CLASS B. COLOR–GREEN. THERE SHALL BE NO SOLDERMASK ON ANY LAND.
9. SILKSCREEN THE LEGEND ON BOTH SIDES USING NON CONDUCTIVE EPOXY INK, COLOR–WHITE. THERE SHALL BE NO INK ON ANY LAND.
10. THE .005 TRACES (LAYER 1) TO BE 50 OHM SINGLE ENDED IMPEDANCE THE .0044 TRACES (LAYER 1) TO BE 100 OHM DIFFERENTIAL IMPEDANCE, AND THE DIELECTRIC REFERENCED IN BOARD STACK DETAIL IS SUGESTED. HOWEVER, TRACE WIDTHS AND OR DIELECTRIC THICKNESS MAY BE MICRO–MODIFIED IN ORDER TO FABRICATE BOARDS TO THE REQUIRED IMPEDANCE NOMINALS TO A TOLERANCE OF +/– 10%.
11. THE PCB SHALL BE E.U. ROHS COMPLIANT.

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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
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