C187EVK01 User's Guide

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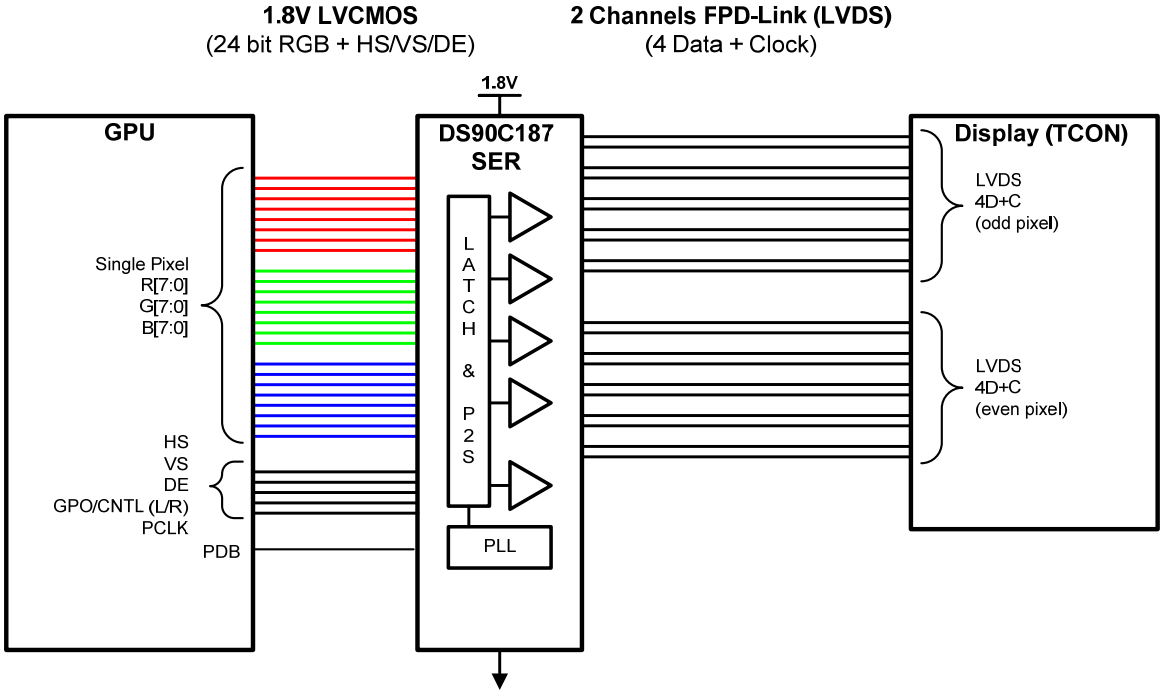
1. Introduction

The Texas Instruments C187EVK01 evaluation module (EVM) helps designers evaluate the performance of the DS90C187 Low Power 1.8V Dual Pixel FPD-Link (LVDS) Serializer. The device operates off of a single 1.8V supply and supports input pixel clocks from 50 MHz to 185 MHz (Single In Dual Out) or 25 MHz to 105 MHz (Single/Dual In Single/Dual Out). The typical application, Single In Dual Out, is shown below.



This EVM contains one Low Power 1.8V Dual Pixel FPD-Link (LVDS) Serializer (See Table 1).

Table 1: Device and Package Information

SERIALIZER	IC	PACKAGE
U1	DS90C187LF	LFA92A

2. Setup

This section describes the jumpers and connectors on the EVK as well and how to properly connect, set up and use the C187EVK01.

2.1. Input/Output Connector Description

JP1 – MODE1 is to be used in combination with JP2 (MODE0) to configure the DS90C187. Refer to Table 2.

JP2 – MODE0 is to be used in combination with JP1 (MODE1) to configure the DS90C187. Refer to Table 2.

Table 2: Device Configuration

MODE1	MODE1	Configuration
0	0	SISO – Single Pixel In Single Pixel Out
0	1	SIDO – Single Pixel In Dual Pixel Out
1	0	DIDO – Dual Pixel In Dual Pixel Out
1	1	**Reserved**

JP3 – RFB is the jumper that selects the clock edge that the input LVCMOS data will be sampled on. If RFB is logic HIGH, the input data is latched on the RISING EDGE of the pixel clock. If RFB is set to logic LOW, the input data is latched on the FALLING EDGE of the pixel clock.

Falling Edge Data Strobe **Rising Edge Data Strobe**

Figure 1: RFB Clock Strobe Settings

JP4 – PDB is the jumper used to enable the Serializer. Power Down Bar (PDB) set to logic HIGH enables the device, while connecting this jumper to logic LOW will disable the device.

JP5 – 18B is the jumper used to enable a power saving mode for 18-bit color applications. When this jumper is set to logic LOW, all data inputs will be sampled, serialized and driven out through the LVDS drivers to support 24-bit color applications or 28-bit generic data buses. If this jumper is set to logic HIGH, the device will enter a power saving mode that will power down the circuitry that feeds the 4th data LVDS driver and also the 8th data LVDS driver for dual pixel output configurations. In dual pixel outputs configurations the 4th data LVDS driver, OA_3+/-, and 8th data LVDS driver, OB_3+/- will be TRI-STATE®.

JP6 – VODSEL is the jumper that controls the differential output voltage. When VODSEL is set to logic HIGH, the output launch amplitude of the LVDS drivers will be set to have a larger output swing. If this jumper is set to logic LOW, then the LVDS drivers will be configured to have a power saving smaller output swing.

JP7 – LVDSSWAP is reserved for future use and should be tied LOW.

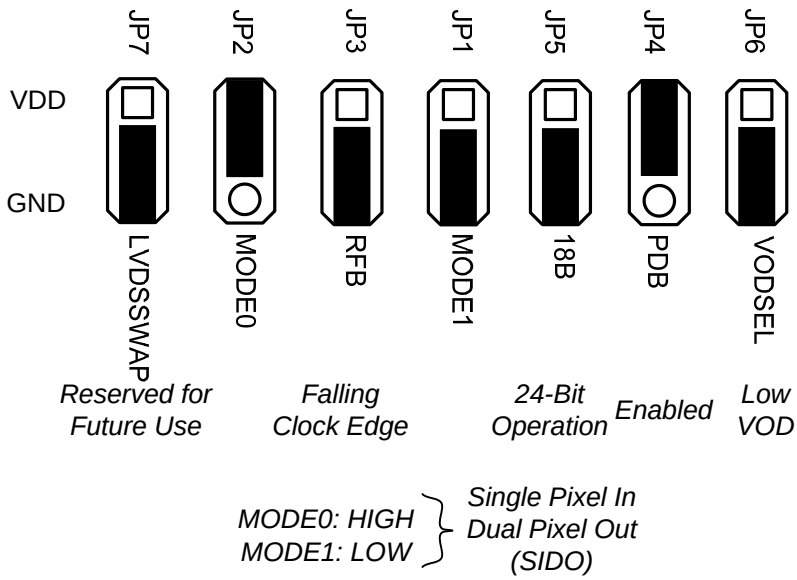


Figure 2: Default Jumper Settings

J3, J4 – LVDS OUTPUTS are brought out to two 2 x10 bank of header pins. Outputs for channel A are brought out to J3 and outputs for channel B are brought out to J4. Note that each LVDS output is separated from adjacent LVDS signals by one ground pin. By default, 100 ohm termination resistors are soldered onto the EVM to allow for easy measuring and probing of the LVDS signals. **If a cable is connected to J3 and/or J4, these termination resistors (R57, R58, R62, R63, R64 and/or R65, R66, R67, R68, R69) must be removed or the differential voltage swing will be reduced.**

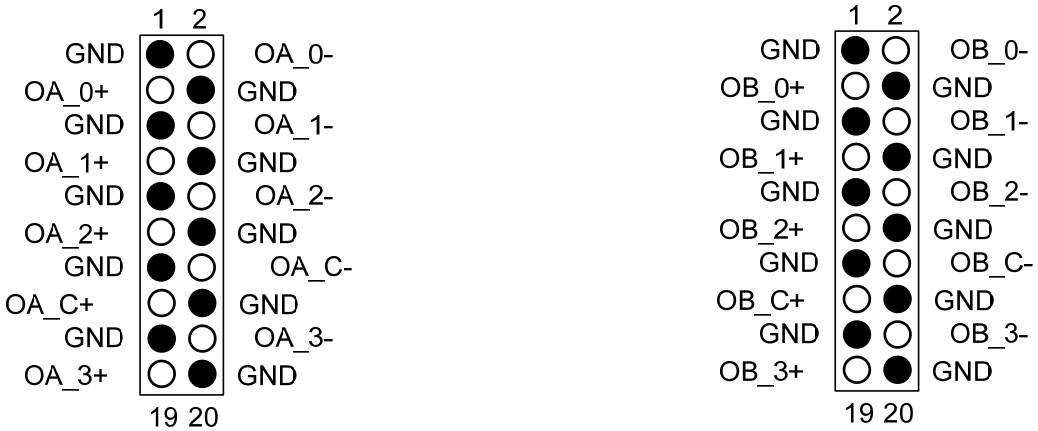


Figure 3: LVDS Output Connections (OA-J3 and OB-J4)

J5, J6 – LVCMOS INPUTS for channel A are connected to the 2 x 30 bank of header pins, J5. LVCMOS inputs for channel B are connected to the 2 x 28 bank of header pins, J6. Note that each LVCMOS signal is paired with a ground signal. When attaching external test equipment or other hardware to this board it is important that there be sufficient ground connections to ensure good signal integrity for the input clock and data waveforms. 50 ohm terminations are provided for each LVCMOS input by default. On a normal PCB these types of terminations are not needed. These resistors are provided by default to improve signal quality for long trace lengths during evaluation.

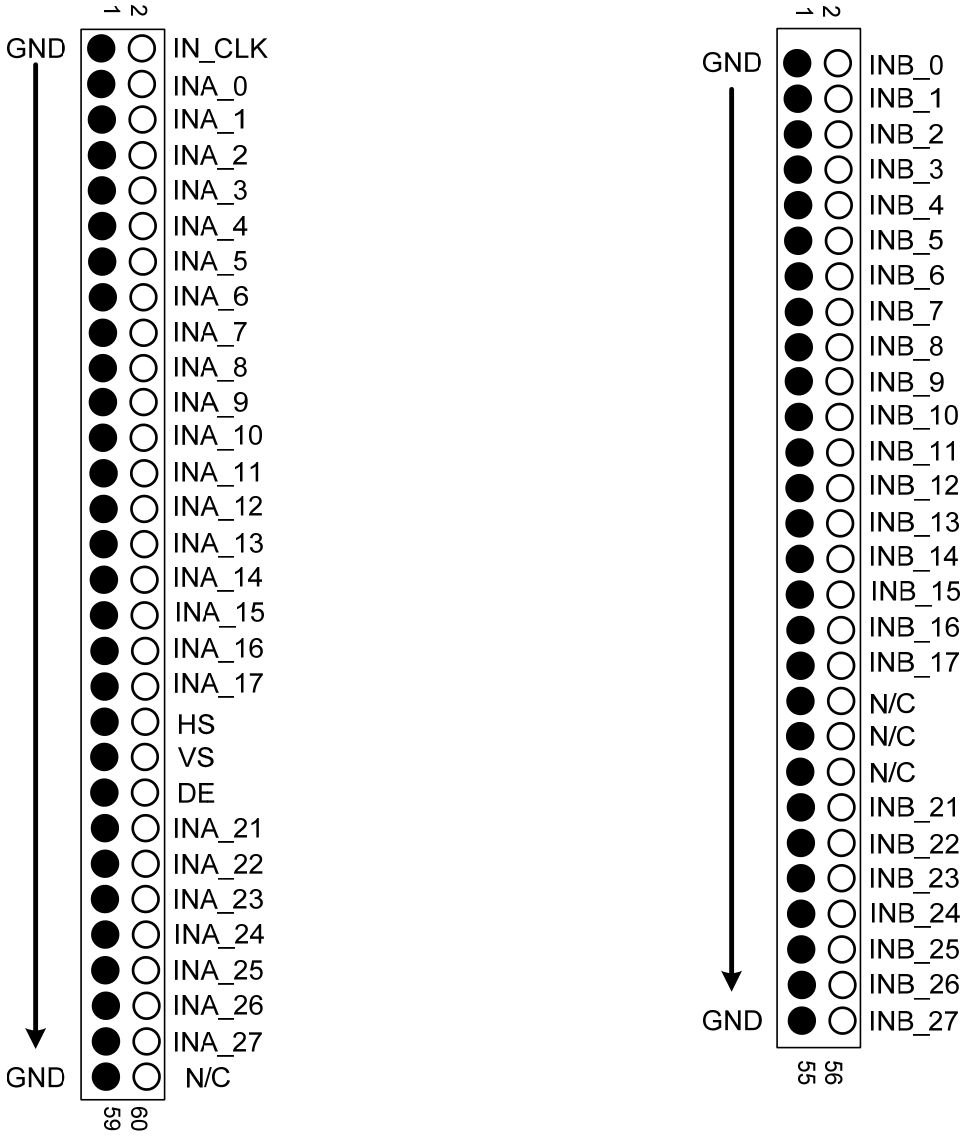


Figure 4: LVCMOS Input Connections (INA-J5 and INB-J6)

J1 – VDD is the terminal where 1.8V power should be applied.

J2 – GND is the terminal where ground should be applied.

2.2. System Setup

The input power jack (J1) should receive a voltage within the range of 1.71 V to 1.89 V referenced to ground which should be applied at J2, with JP4 set to LOW. Once, power has been applied to the board, JP4 (PDB pin) can be set to logic HIGH. After setting the PDB pin to HIGH, 1.8V clock and data can be transmitted to the EVM. **If a cable is connected to J3 and/or J4, the termination resistors (R57, R58, R62, R63, R64 and/or R65, R66, R67, R68, R69) should be removed.**

2.3. Operation

For proper operation of the DS90C187, JP1, JP2, JP3, JP4, JP5, JP6 and JP7 should be properly configured by using shorting blocks (jumpers); see Figure 3.

JP1 and JP2 set to the desired device mode (SISO, SIDO or DIDO)
JP3 to LOW for falling clock edge strobe or HIGH for rising clock edge strobe
JP4 to HIGH, after power on
JP5 to LOW for 24-bit color (28-bit data bus) or to HIGH for 18-bit color (21-bit data bus)
JP6 to LOW for reduced VOD swing or HIGH for large VOD swing
JP7 to LOW

After applying power and setting JP4 to HIGH, clock and data can be sent to the DS90C187. When the clock signal is detected, the DS90C187 will power on and begin to transmit serialized LVDS data.

3. Board Layout

Figure 5, Figure 6 and Figure 7 show the board layout for the C187EVK01 printed circuit board. The EVM offers jumpers to configure and power on/off the DS90C187. 50 ohm shunt terminations are populated by default. 100 ohm differential termination resistors are populated by default to allow for easy probing of the LVDS outputs at J3 and J4.

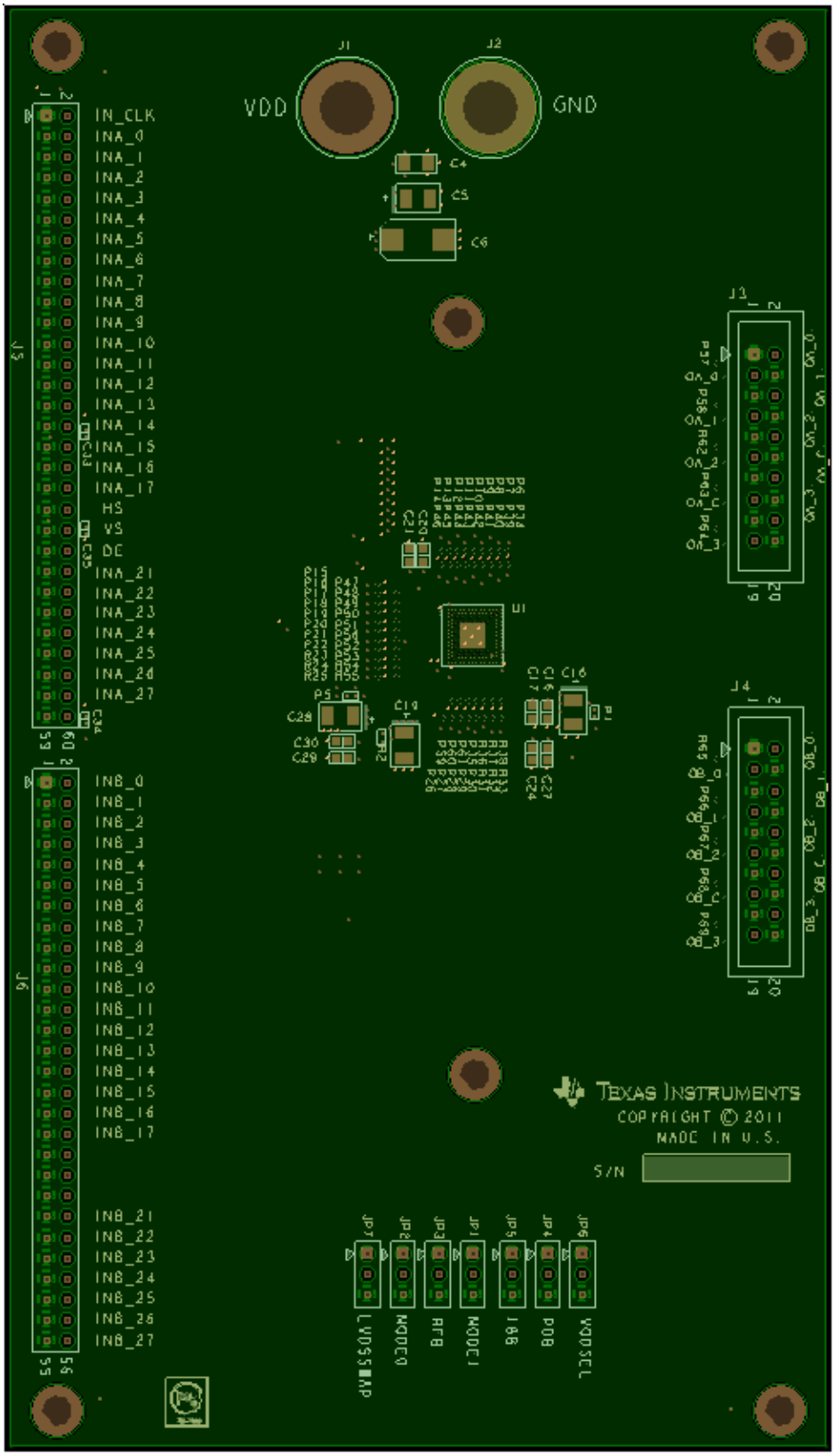


Figure 5: Top Assembly Layer

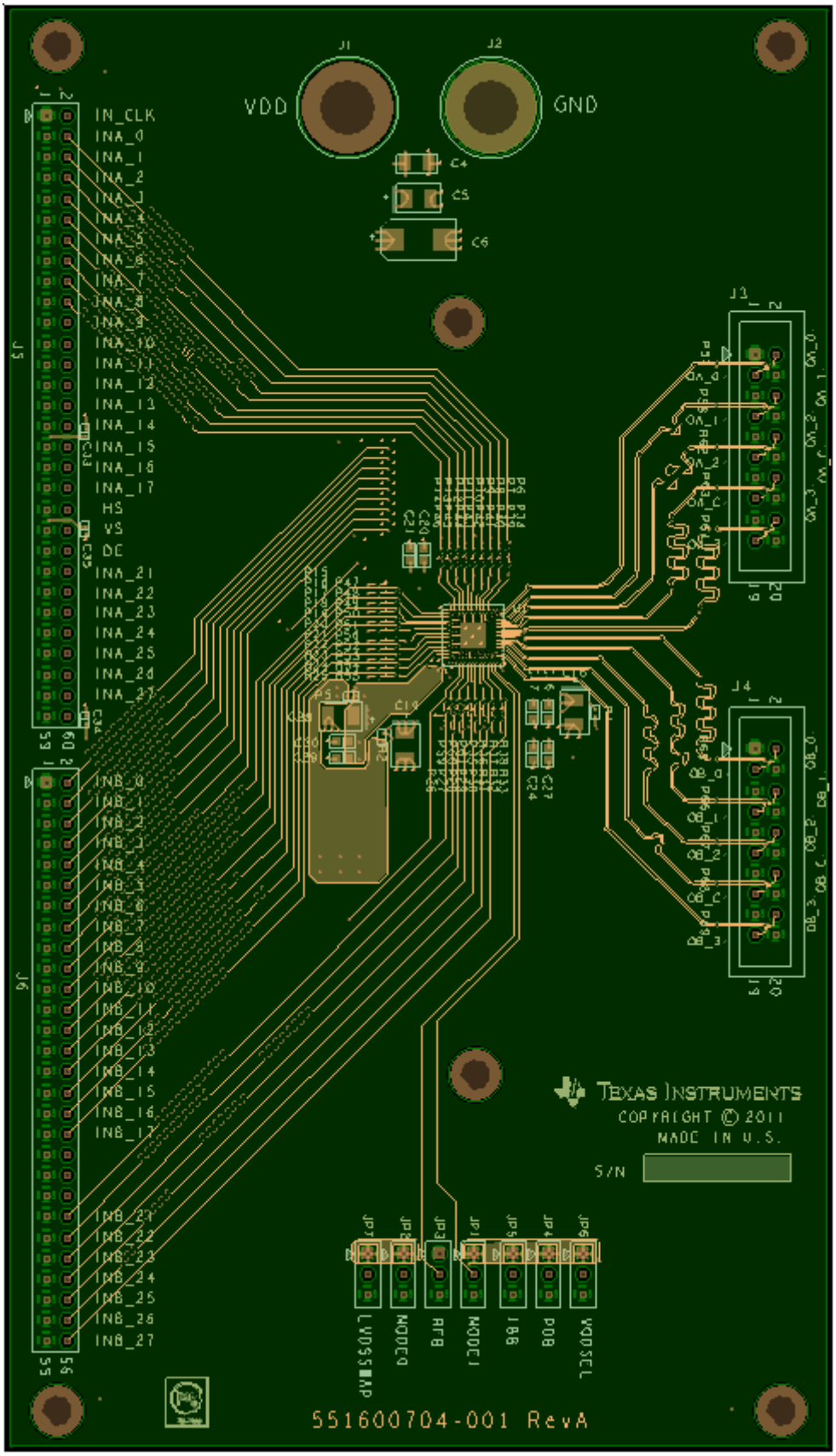


Figure 6: Top Layer Routing

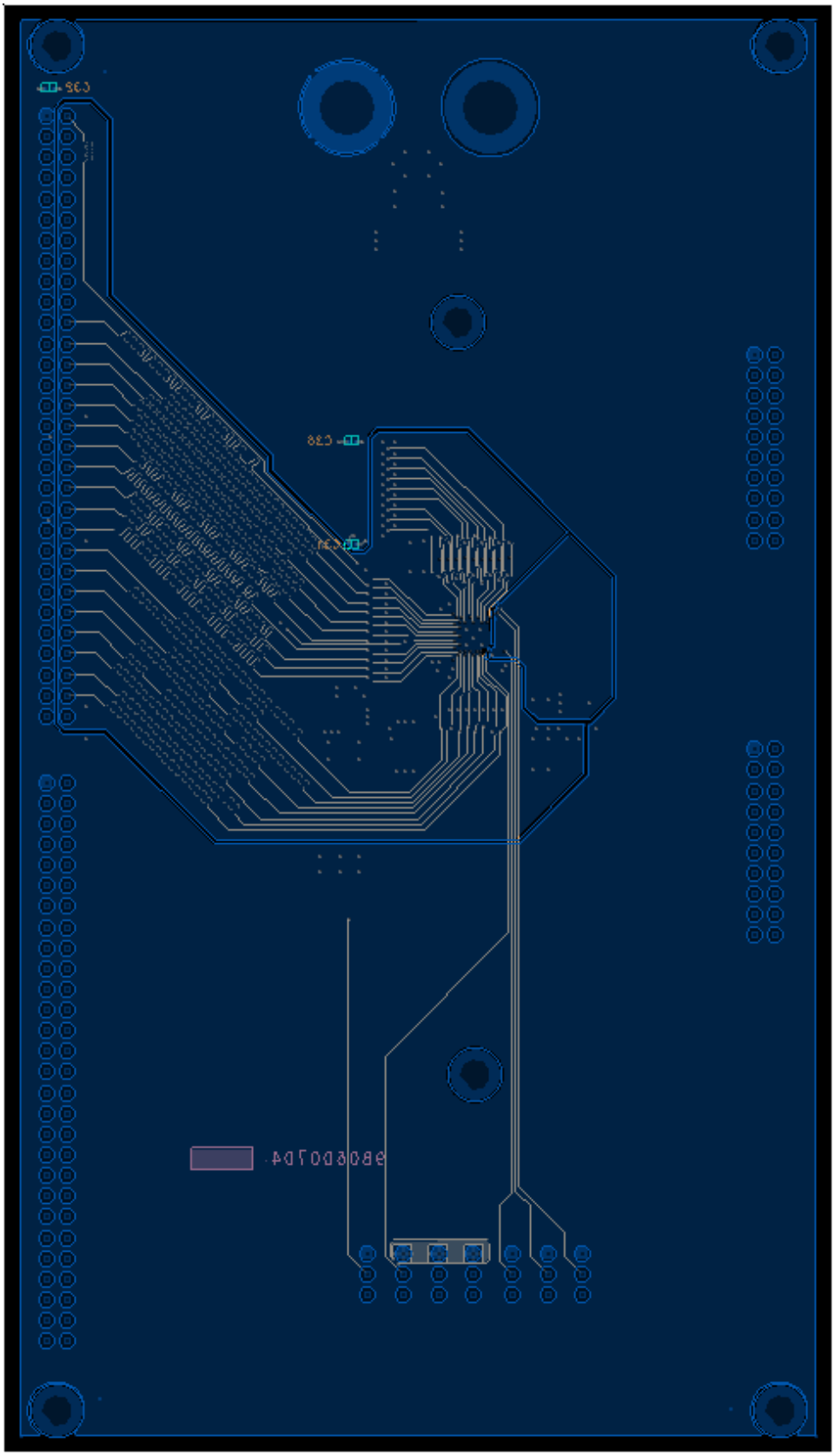


Figure 7: Bottom Layer Routing

4. Schematic

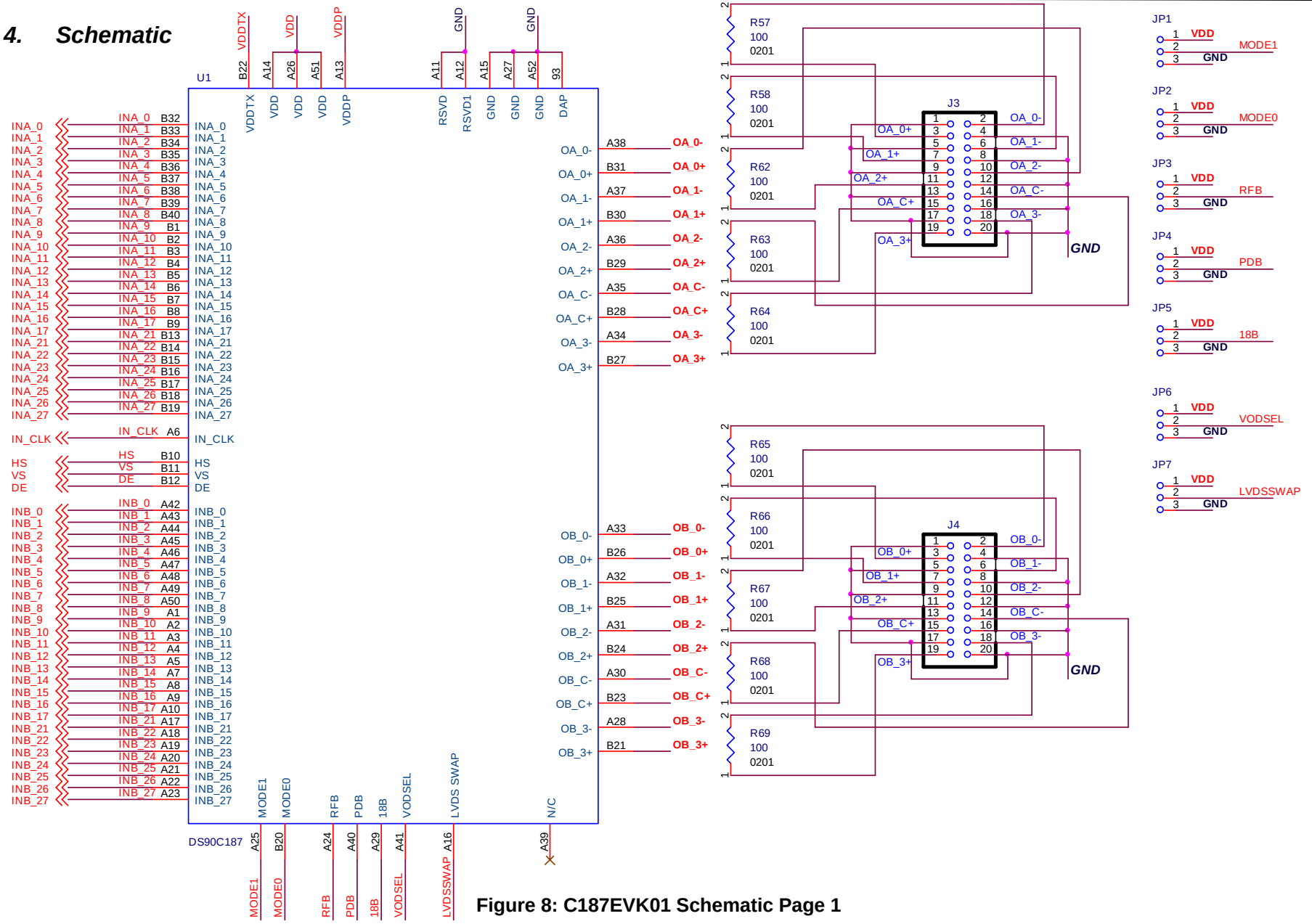


Figure 8: C187EVK01 Schematic Page 1

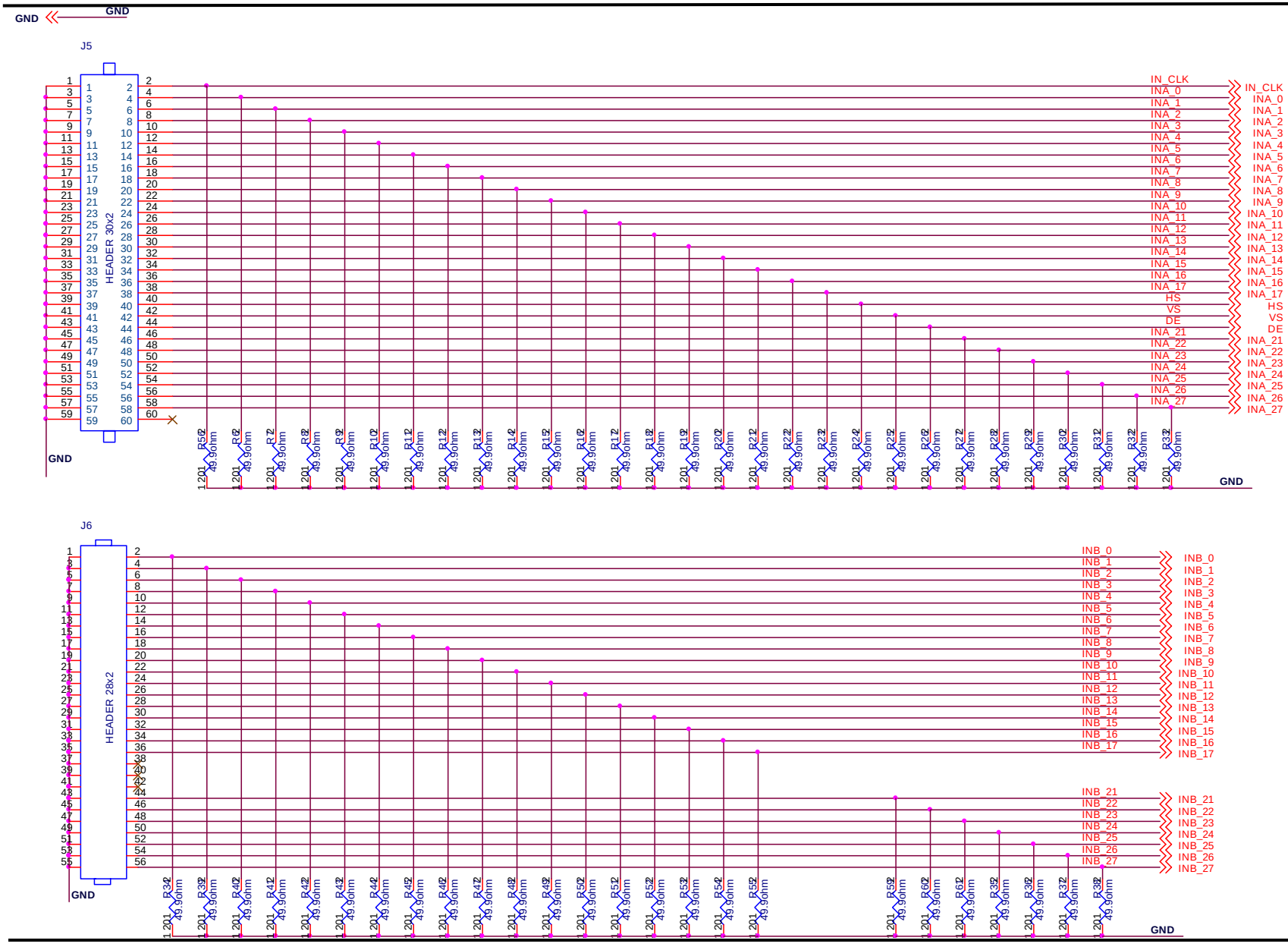

GND
GND
J5
HEADER 30x2
IN_CLK
INA_0
INA_1
INA_2
INA_3
INA_4
INA_5
INA_6
INA_7
INA_8
INA_9
INA_10
INA_11
INA_12
INA_13
INA_14
INA_15
INA_16
INA_17
HS
VS
DE
INA_21
INA_22
INA_23
INA_24
INA_25
INA_26
INA_27
GND
J6
HEADER 28x2
INB_0
INB_1
INB_2
INB_3
INB_4
INB_5
INB_6
INB_7
INB_8
INB_9
INB_10
INB_11
INB_12
INB_13
INB_14
INB_15
INB_16
INB_17
INB_21
INB_22
INB_23
INB_24
INB_25
INB_26
INB_27
GND

Figure 9: C187EVK01 Schematic Page 2

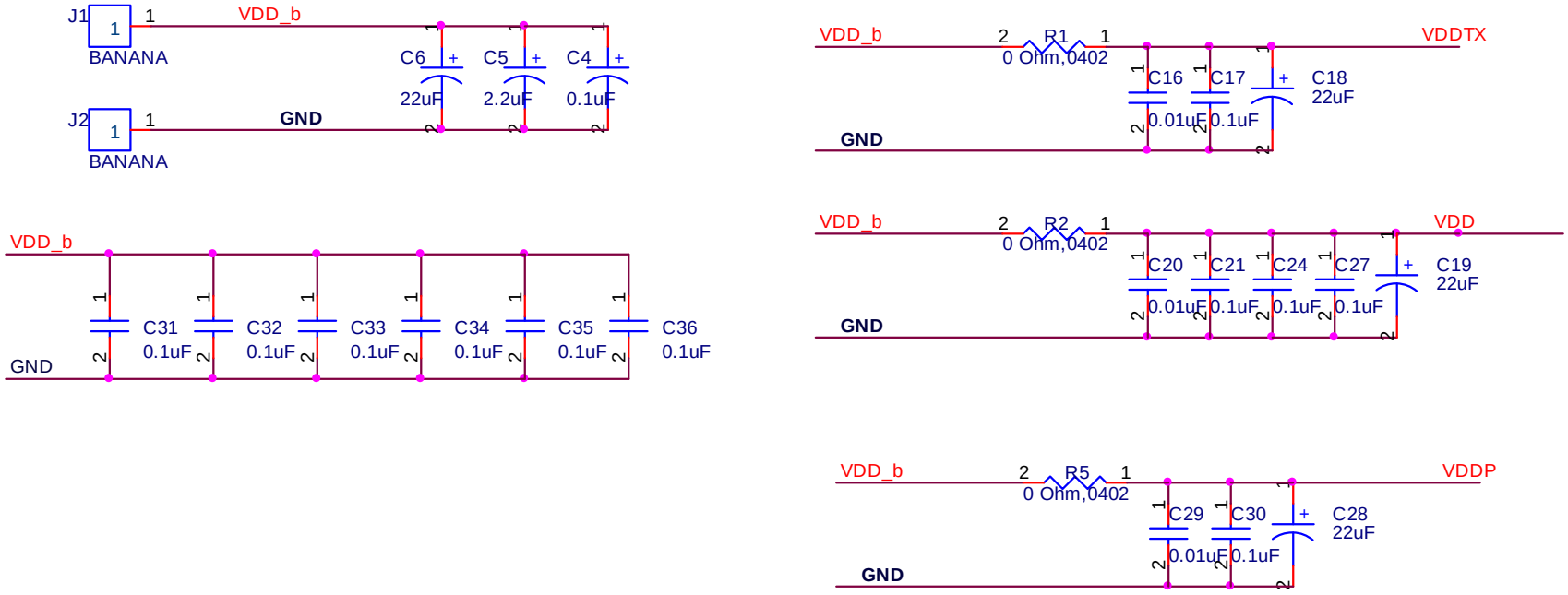


Figure 10: C187EVK01 Schematic Page

Table 3: C187EVK01 Bill of Materials

Quantity	Reference	Part	Vendor	Part Number
1	C4	0.1uF	KEMET	C1206C104K5RACTU
1	C5	2.2uF	KEMET	T491B225K020AT
1	C6	22uF	nichicon	F931E226MNC
3	C16,C20,C29	0.01uF	KEMET	C0603C103K1RACTU
5	C17,C21,C24,C27,C30	0.1uF	Panasonic	ECJ-1VB1E104K
3	C18,C19,C28	22uF	Kemet	T494B226M016AT
6	C31,C32,C33,C34,C35,C36	0.1uF	Murata	GCM155R71C104KA55D
7	JP1,JP2,JP3,JP4,JP5,JP6,JP7	3-Pin Header	AMP/Tyco	87224-3
2	J1,J2	BANANA	Johnson	108-0740-001
2	J3,J4	2X10-Pin Header	3M	N2520-6002RB
1	J5	HEADER 30x2	AMP/Tyco	3-87215-0
1	J6	HEADER 28x2	AMP/TYCO	3-87215-0
3	R1,R2,R5	0 Ohm,0402	Panasonic	ERJ-2GEJ0R00X
54	R6,R7,R8,R9,R10,R11,R12,R13,R14,R15,R16,R17,R18,R19,R20,R21,R22,R23,R24,R25,R26,R27,R28,R29,R30,R31,R32,R33,R34,R35,R36,R37,R38,R39,R40,R41,R42,R43,R44,R45,R46,R47,R48,R49,R50,R51,R52,R53,R54,R55,R56,R59,R60,R61	49.9 ohm	Panasonic	ERJ-1GEF49R9C
10	R57,R58,R62,R63,R64,R65,R66,R67,R68,R69	100 ohm	Susumu	RR0306P-101-D
1	U1	DS90C187	Texas Instruments	DS90C187LF

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It is important to operate this EVM within the input voltage range of -0.3 V to 48 V and the output voltage range of 0.9 V to 18 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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